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4ch White LED Driver with Buck-Boost (40 LED Maximum)

BD81A44MUV-M / BD81A44EFV-M

General Description

BD81A44MUV-M/EFV-M is a white LED driver with the capability of withstanding high input voltage (35V Max). This driver has 4ch constant-current drivers integrated in 1-chip, where each channel can draw up to 120mA (Max), which is also suitable for high illumination LED drive. Furthermore, a buck-boost current mode DC/DC controller is also integrated to achieve stable operation during power voltage fluctuation. Light modulation (10,000:1 @100Hz dimming function) is possible by PWM input.

Features

- Integrated Buck-Boost current mode DC/DC controller
- Integrated 4ch current driver for LED drive
- 10,000:1 PWM dimming @100Hz
- External switching frequency synchronization
- Built-In protection function (UVLO, OVP, OCP, SCP)
- LED abnormality detection function (Open/Short)
- Integrated V_{OUT} discharge function (Buck-Boost or Buck structure limitation)
- AEC-Q100 Qualified *(Note 1)*

(Note 1) Grade1

Application

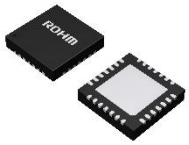
For Display audio, CID, Cluster, HUD
Small and Medium type LCD Panels for Automotive use.

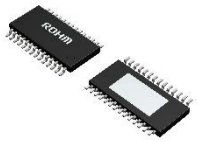
Key Specifications

- Operating Input Voltage Range: 4.5 to 35 V
- Output LED Current Accuracy: ±3.0%@50mA
- DC/DC Oscillation Frequency: 200 to 2200kHz
- Operating Temperature Range: -40 to +125℃
- LED Maximum Output Current: 120mA/ch
- PWM min pulse width: 1.0us

Package(s) W(Typ) x D(Typ) x H(Max)

VQFN28SV5050 (BD81A44MUV-M)	HTSSOP-B28 (BD81A44EFV-M)
W(Typ) × D(Typ) × H(Max)	W(Typ) × D(Typ) × H(Max)
5.0mm × 5.0mm ×1.0mm	9.7mm × 6.4mm × 1.0mm





Typical Application Circuit

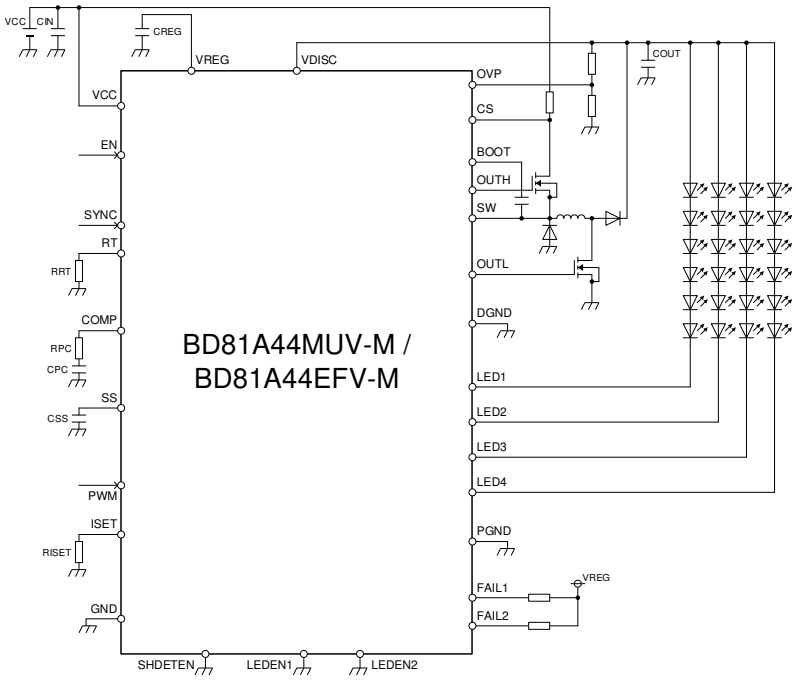
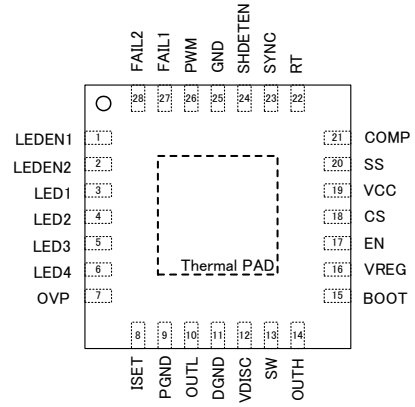


Figure 1. Buck-Boost Application Circuit

○Product structure：Silicon monolithic integrated circuit
○This product has no designed protection against radioactive rays

Pin Description

VQFN28SV5050 (Top view)



HTSSOP-B28 (Top view)

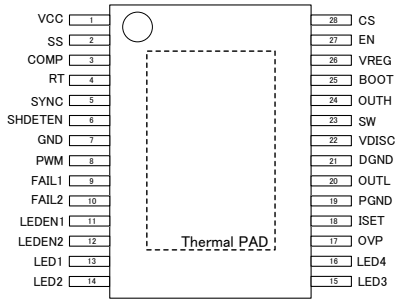


Figure 2. Pin Configuration

Pin Configuration

VQFN28 SV5050	HTSSOP -B28	Terminal Name	Function
1	11	LEDEN1	LED output pin enable terminal 1
2	12	LEDEN2	LED output pin enable terminal 2
3	13	LED1	LED output terminal 1
4	14	LED2	LED output terminal 2
5	15	LED3	LED output terminal 3
6	16	LED4	LED output terminal 4
7	17	OVP	Over-voltage detection terminal
8	18	ISET	LED output current setting terminal
9	19	PGND	LED output GND terminal
10	20	OUTL	Low side FET gate terminal
11	21	DGND	DC/DC output GND terminal
12	22	VDISC	Output voltage discharge terminal
13	23	SW	High side FET source terminal
14	24	OUTH	High side FET gate terminal
15	25	BOOT	High side FET driver power supply terminal
16	26	VREG	Internal constant voltage
17	27	EN	Enable terminal
18	28	CS	DC/DC current sense terminal
19	1	VCC	Input power supply terminal
20	2	SS	“Soft Start” Capacitor connection
21	3	COMP	ERR AMP output
22	4	RT	Oscillation Frequency-setting resistor input
23	5	SYNC	External synchronization input terminal
24	6	SHDETEN	Short detection enable signal
25	7	GND	Small signal GND terminal
26	8	PWM	PWM light modulation input terminal
27	9	FAIL1	“Failure” signal output terminal
28	10	FAIL2	LED open/short detection output signal
-	-	Thermal PAD	Back side thermal PAD (Please connect to GND)

Block Diagram

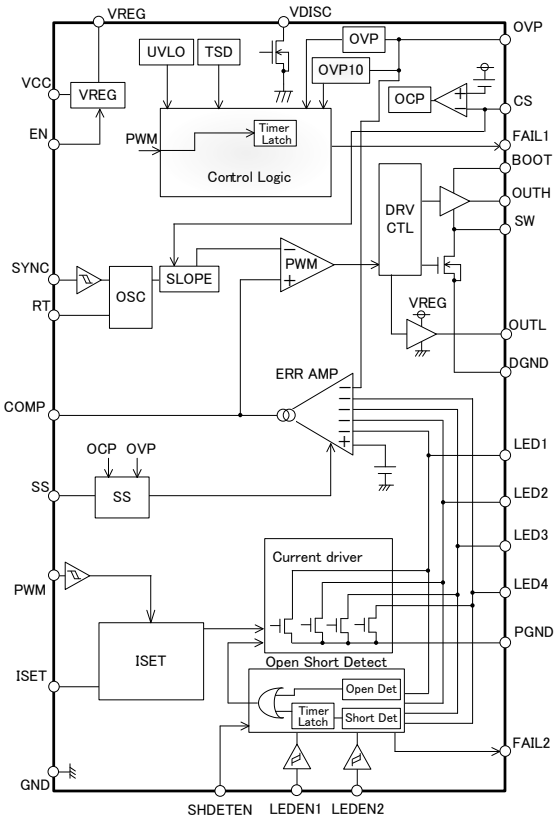


Figure 3. Internal Block Diagram

Description of Blocks

1. Voltage Reference (V_{REG})

5V (Typ) is generated from the V_{CC} Input Voltage (when at EN=High). This voltage (V_{REG}) is used as power supply of internal circuit and when fixing the pins outside of the IC at a high voltage, as well. The UVLO protection is integrated in V_{REG}. The circuit starts to operate at V_{CC}≧4.0V (Typ) and V_{REG}=3.5V (Typ) and stops when at V_{CC}≦3.5V (Typ) or V_{REG}≦2.0V (Typ). For release/cancellation condition and detection condition, please refer to Table 2 on page 11. Connect a ceramic capacitor (C_{REG}) to VREG terminal for phase compensation. Creg range is 1.0uF to 4.7uF and recommend value is 2.2uF. If the C_{REG} is not connected, the operation of circuit will be notably unstable.

2. Constant Current Driver

Table1. LED Control Logic

LEDEN1	LEDEN2	LED1	LED2	LED3	LED4
L	L	ON	ON	ON	ON
H	L	ON	ON	ON	OFF
L	H	ON	ON	OFF	OFF
H	H	ON	OFF	OFF	OFF

If less than four constant-current drivers are used, please make the LED1~4 terminal ‘open’ while the output ‘OFF’ by LEDEN1 and LEDEN2 terminal. The truth table for these pins is shown above. If the unused constant-current driver output will be set open without the process of LEDEN1,2 terminals, the ‘open detection’ will be activated. The LEDEN1, 2 terminals is pulled down internally in the IC and it is low at ‘open’ condition. They should be connected to VREG terminal or fixed to logic HIGH when in use.

(1) Output Current Setting (RISET)

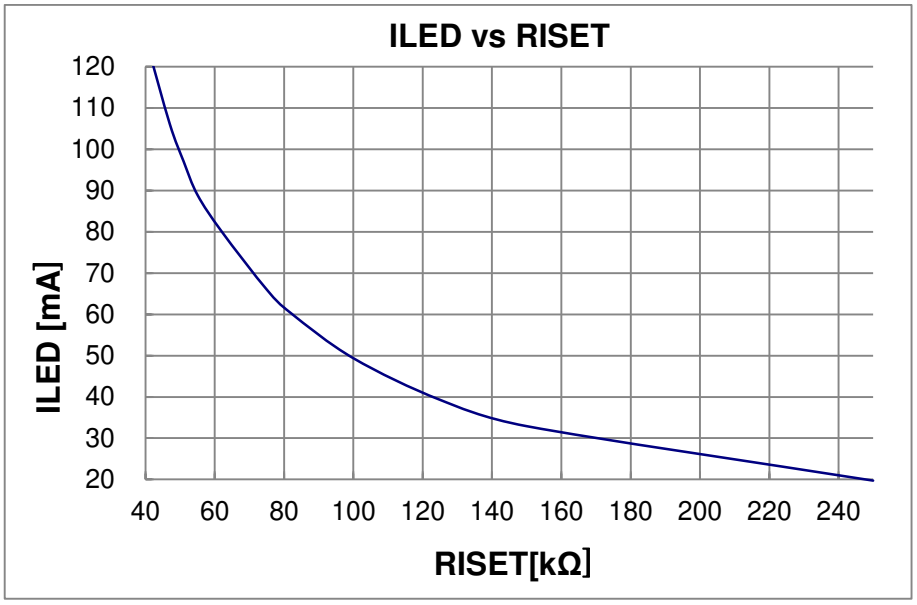


Figure 4. ILED vs RISET

The Output Current ILED can be obtained by the following equation:

$$ILED[mA] = (1.0V/RISET[k\Omega]) \times 5000$$

RISET operating range is 41kohm to 250kohm. It can not change the RISET value in the operation.
This IC has ISET-GND short protection that protect LED element from over current when ISET and GND is short. If the RISET value is under 4.7kohm, the IC detects ISET-GND short and LED current becomes off.

<Caution of LED current setting>
If the output current I_{LED} is set to >100mA/ch, the stability of LED current within specified operating temperature range will decrease. LED current supply value will depends on the amount of ripple in output voltage (VOUT). The figure below shows the temperature and the possible LED current maximum value settings, please adjust the ripple voltage in such a way that the LED current value setting will fall within the range as shown on the graph below. (ΔVOUT : Output Ripple Voltage) Please refer P.22, there is the detail information of VOUT ripple voltage.

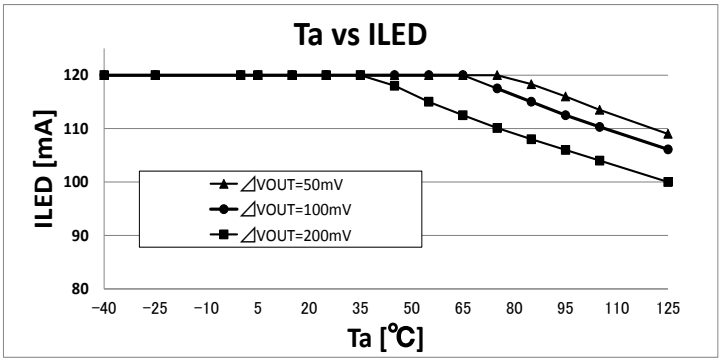


Figure 5. Temperature (Ta) vs Output LED Current (ILED)

(2) PWM Intensity Control

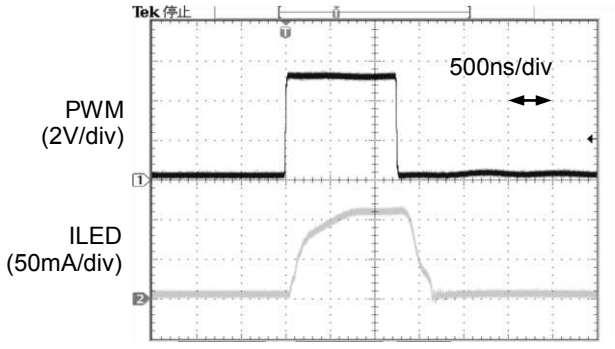


Figure 6. PWM=150Hz, Duty=0.02%, I_{LED} Waveform

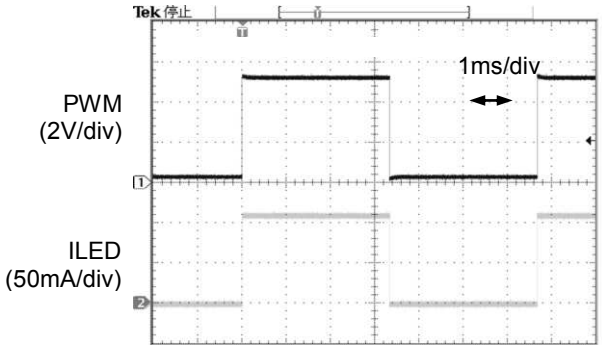


Figure 7. PWM=150Hz, Duty=50.0%, I_{LED} Waveform

The current driver ON/OFF is controlled by PWM terminal. The duty ratio of PWM terminal becomes duty ratio of I_{LED}. If don't use PWM dimming, please set the PWM terminal to HIGH. Output light intensity is greatest at 100% input

3. Buck-Boost DC/DC Controller

(1) Number of LED in Series Connection

In this IC, the output voltage of the DC/DC converter (VOUT) is controlled by LED cathode voltage (LED1–4 terminal voltage) becomes 1.0V (Typ). When two or more LED are operating at the same time, the LED terminal voltage that connects the highest LED Vf row is held at 1.0V (Typ). Then the voltages of other LED terminal will increased only LED VF tolerance. Please decide LED VF tolerance by using the description as shown below:

LED series number x LED VF tolerance voltage < Short Detection Voltage 4.2V (Min) − LED Control Voltage 1.1V (Max)

(2) Over Voltage Protection (OVP)

The output of the DC/DC converter (VOUT) should be connected to the OVP pin via voltage divider. If OVP terminal voltage is over 2.0V (Typ), Over Voltage Protection (OVP) is active and stop the DCDC switching. In determining an appropriate trigger voltage for OVP function, consider the total number of LEDs in series and the Maximum variation in VF. When OVP terminal voltage drops to 1.94V (Typ) after OVP operation, the OVP will be released. If ROVP1 is GND side resistance, ROVP2 is output voltage side resistance and output voltage is VOUT, OVP will occur at below equation.

$$VOUT[V] \geq \{(ROVP1[k\Omega] + ROVP2[k\Omega])/ROVP1[k\Omega]\} \times 2.0[V]$$

OVP will engage when V_{OUT} >32V if ROVP1=22kΩ and ROVP2=330kΩ.

(3) Buck-Boost DC/DC Converter Oscillation Frequency (FOSC)

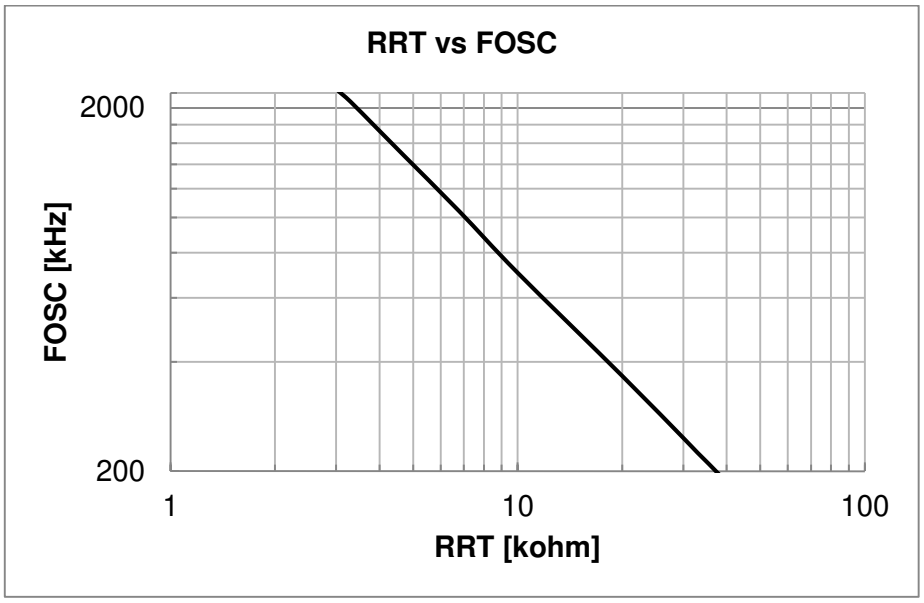


Figure 8. RRT vs FOSC

DCDC oscillation frequency can be set via a resistor connected to the RT pin. This resistor determines the charge/discharge current to the internal capacitor, thereby changing the oscillation frequency. Please set the resistance of RRT using the above data and below equation.

$$Fosc[kHz] = (81 \times 10^2 / RRT[k\Omega]) \times a$$

Where:
81×10^2 is the constant value in IC (+/-10%)
α is the adjustment factor
(RRT : α = 41kΩ: 1.01, 27kΩ: 1.00, 18kΩ: 0.99, 10 kΩ: 0.98, 4.7kΩ: 0.97, 3.9kΩ: 0.96)

A resistor in the range of 3.6 kΩ to 41 kΩ is recommended. Settings that deviate from the frequency range shown above may cause switching to stop, and proper operation cannot be guaranteed.

(4) External Synchronization Oscillation Frequency (FSYNC)
If the clock signal input to SYNC terminal, the internal oscillation frequency can be synchronized externally.

Do not switch from external to internal oscillation if the DC/DC converter is active.
The clock input to SYNC terminal is valid only in rising edge.
As for the external input frequency, the input of the internal oscillation frequency ± 20% decided in RT terminal resistance is recommended.

(5) Soft Start Function (SS)
The soft-start (SS) function can limits the start up current and output rise-time slowly if the capacitor connected to SS Terminal. It is available for prevention of output voltage overshoot and inrush current. If you don't use soft-start function, please set SS terminal open. For the calculation of SS time, please refer to the formula on page 19.

(6) Max Duty
If this IC operates by DCDC switching Max Duty, it would not output expect voltage and LED current decrease or LED current OFF by SCP. Please set load condition and external parts for DCDC switching Duty does not reach Max Duty.

4. Protect Function

Table 2. The detect condition of each protect function and the operation during detection

Protect Function	Detect Condition		Operation During Detection
	[Detection]	[Release/ Cancellation]	
UVLO	V_{CC}<3.5V or VREG<2.0V	VCC >4.0V and VREG>3.5V	All Blocks Shuts down (Except for VREG)
TSD	Tj>175°C	Tj<150°C	All Blocks Shuts down (Except for VREG)
OVP	$VOVP_P$>2.0V	V_{OVP}<1.94V	DCDC switching OFF
OCP	$V_{CS} \leqq V_{CC}$-0.2V	V_{CS}>V_{CC}-0.2V	DCDC switching OFF
SCP	One of the LED1-4 is under 0.3V or VOVP<0.57V (100ms delay @300kHz)	EN Reset or UVLO Reset	After SCP delay time, all block Latch Off (Except for VREG)
LED Open Protection	VLED<0.3V and VOVP>2.0V	EN Reset or UVLO Reset	Only the detected channel latches OFF
LED Short Protection	VLED>4.5V (100ms delay @300kHz)	EN Reset or UVLO Reset	After LED Short delay time, only the detected channel latch OFF

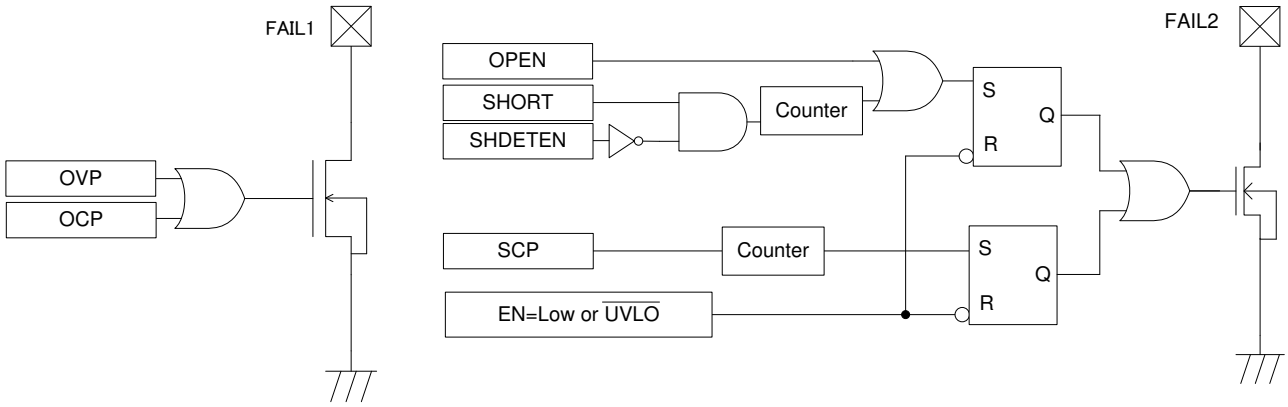


Figure 9. Protection Flag Output Block Diagram

The operating status of the protection is propagated to FAIL1 and FAIL2 terminals (open-drain outputs). FAIL1 becomes low when OVP or OCP protection is detected, whereas FAIL2 becomes low when SCP, LED open or LED short is detected. If the FAIL terminal will not be used as flag output, please make the FAIL terminal open or connect it to GND. But if the FAIL terminal will be used as a flag output, it is recommended to pull-up the FAIL1, 2 terminals to VREG terminal. The recommended value of pull-up resistance is 100kΩ.

(1) Under-Voltage Lock Out (UVLO)
The UVLO shuts down all the circuits except VREG when VCC<3.5V (Typ) or VREG <2.0V (Typ). And UVLO is released by Vcc>4.0V(Typ) and VREG>3.5V(Typ).

(2) Thermal Shut Down (TSD)
The TSD shuts down all the circuits except VREG when the Tj reaches 175°C (Typ), and releases when the Tj becomes below 150°C (Typ).

(3) Over-Voltage Protection (OVP)
The output voltage of DC/DC is detected from the OVP terminal voltage, and the over-voltage protection will activate if the OVP terminal voltage becomes greater than 2.0V (Typ). When OVP is activated, the switching operation of the DC/DC turns off. And OVP terminal becomes less than 1.94V (Typ), OVP is released and the switching operation of the DC/DC turns on.

(4) Over-Current Protection (OCP)
The OCP detects the coil current by monitoring the voltage of the high-side resistor, and activates when the CS voltage becomes less than V_{CC}-0.2V (Typ).
When the OCP is activated, the switching operation of the DC/DC turns off. And CS voltage becomes over than Vcc-0.2V (typ), OCP is released and the switching operation of the DC/DC turns on.

(5) Short Circuit Protection (SCP)
When the LED terminal voltage becomes less than 0.3V (Typ) or OVP terminal becomes less than 0.57V (typ), the built-in counter operation will start and the latch will activate at oscillation frequency in 32770 count. In case of fosc=300kHz, the count time is approximately 100ms. If the LED terminal voltage becomes over 0.3V or OVP terminal becomes over 1.0V (typ) before 32770 count, the counter resets and SCP is not detected.

(6) LED Open Detection
When the LED terminal voltage is below 0.3V (Typ) and OVP terminal voltage more than 2.0V (Typ) simultaneously, LED open is detected and latches off the open channel.

(7) LED Short Detection Circuit
If the LED terminal voltage becomes more than 4.5V (Typ), the built-in counter operation will start and the latch will activate at oscillation frequency in 32770 count. In case of fosc=300kHz, the count time is approximately 100ms. During PWM dimming, the LED Short Detect operation is carried out only when PWM=High. If the LED terminal voltage becomes less than 4.5V (Typ) before 32770 count, the counter resets and LED Short is not detected.
When LED Short Detect function will not be used, SHDETEN terminal should be connected to VREG before starting. When LED Short Detect function is used, the SHDETEN terminal should be connected to GND. In addition, It cannot change SHDETEN voltage (High or Low) during normal operation.

(8) PWM Low Latch Off Circuit
After the EN is ON, the low interval of PWM input is counted by built-in counter. The clock frequency of counter is the fosc Frequency, which is determined by RRT, and stops the operation of circuits except VREG at 32768 counts.
In case of fosc=300kHz, the count time is approximately 100ms.

(9) Output Voltage Discharge Circuit (VDISC function)

When EN restart with Vout charge remaining, there is the possibility of LED flicker. Therefore restarting DC/DC must be operated after discharging Vout. If using only pull-down resistance as setting OVP for discharge, it takes a lot time for discharging Vout. Therefore this product has functionality of circuit for Vout discharge. Vout discharge function is available for BuckBoost or Buck application. It is need to connect Vout and VDISC terminal and use VDISC function. When VDISC terminal is connected to Vout, the output can be discharged when DCDC circuit becomes OFF (with EN changing high to low or detection of protect).

The discharge time Tdisc is expressed in the following equations.

$$Tdisc[s] = \frac{3 \times Vout[V] \times Cout[F]}{4 \times IDISC[A]}$$

Where:
Tdisc : DC/DC Output Discharge Time
COUT : DC/DC Output Capacity
Vout : DC/DC Output Voltage
IDISC : Discharge current

Please confirm IDISC value that 25% of Vout voltage from following graph and input above equation. For example, when using Vout=20V, please use IDISC value of Vout=5V (approximately 76mA). It will take Tdisc time for Vout discharge. Please set EN=Low time over than Tdisc for prevent LED flicker.
This Tdisc value is reference data. Please verifying by actual measurements.

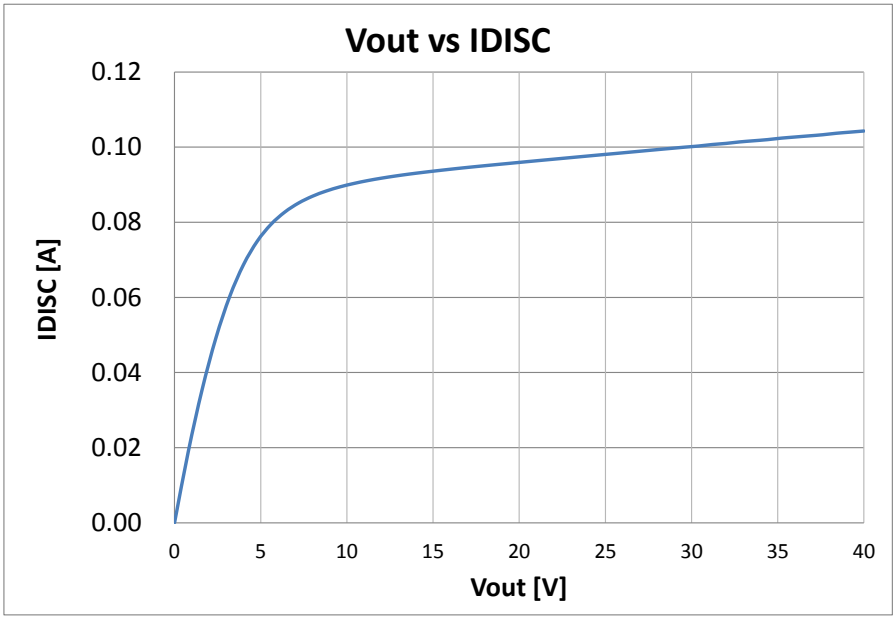


Figure.10 Vout vs IDISC

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	40	V
BOOT, OUTH Pin Voltage	V_{BOOT}, V_{OUTH}	45	V
SW, CS Pin Voltage	V_{SW}, V_{CS}	40	V
BOOT-SW Pin Voltage	$V_{BOOT-SW}$	7	V
LED1 to 4, VDISC Pin Voltage	$V_{LED1,2,3,4}$, V_{VDISC}	40	V
PWM, SYNC, EN pin Voltage	V_{PWM}, V_{SYNC}, V_{EN}	-0.3 to +7	V
VREG, OVP, FAIL1, FAIL2, SS, RT pin Voltage	V_{VREG}, V_{OVP}, V_{FAIL1}, V_{FAIL2}, V_{SS}, V_{RT}	-0.3 to +7 < VCC	V
LEDEN1, LEDEN2, ISET, OUTL, COMP, SHDETEN pin Voltage	V_{LEDEN1}, V_{LEDEN2}, V_{ISET} V_{OUTL}, V_{COMP}, $V_{SHDETEN}$	-0.3 to +7 < VREG	V
Junction Temperature Range	Tj	-40 to +150	℃
Storage Temperature Range	Tstg	-55～+150	℃
LED Maximum Output Current	I_{LED}	120 *(Note 1)*	mA

(Note 1) Current level per channel. Please set LED current that does not over Junction Temperature Range (Tj) maximum.

Recommended Operating Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage *(Note 2)*	V_{CC}	4.5	35	V
Operating Temp Range	Topr	-40	+125	℃
DC/DC Oscillation Frequency Range	F_{OSC}	200	2200	kHz
External Synchronization Frequency Range *(Note 3) (Note 4)*	F_{SYNC}	200	2200	kHz
External Synchronization Pulse Duty Range	F_{SDUTY}	40	60	%

(Note2) It is near Vcc terminal voltage. Please be careful the voltage drop by Vcc line impedance.
(Note3) If don't use an external synchronization frequency, please make the SYNC open or connect to GND.
(Note4) If using an external synchronization frequency, don't change to internal oscillation in the middle of process.

Recommended Parts Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
VREG Capacitor	CREG	1.0	4.7	μF
LED Current setting Resistance	RISET	41	250	kΩ
DC/DC Oscillation Frequency setting Resistance	RRT	3.6	41	kΩ
Soft Start setting Capacitor	CSS	0.047	0.47	μF

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN28SV5050				
Junction to Ambient	θ_{JA}	128.5	31.5	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	12	9	°C/W
HTSSOP-B28				
Junction to Ambient	θ_{JA}	107.0	25.1	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	6	3	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air)
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 4)*Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(NOTE 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers..

Electrical Characteristics (V_{CC}=12V, Ta = -40°C to +125°C *Unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Normal	Max		
Circuit Current	I_{CC}	-	-	10	mA	EN=High, SYNC=High, RT=OPEN PWM=Low, ISET=OPEN,C_{IN}=10µF
Standby Current	I_{ST}	-	-	10	µA	EN=Low, VDISC=OPEN
[VREG]						
Reference Voltage	V_{REG}	4.5	5.0	5.5	V	I_{REG}=-5mA, C_{REG}=2.2µF
[OUTH]						
OUTH High Side ON-Resistor	R_{ONHH}	1.5	3.5	7.0	Ω	IOUTH=-10mA
OUTH Low Side ON-Resistor	R_{ONHL}	0.8	2.5	5.5	Ω	IOUTH=10mA
OCP Detection Voltage	V_{OLIMIT}	VCC-0.22	VCC-0.2	VCC-0.18	V	
[OUTL]						
OUTL High Side ON-Resistor	R_{ONLH}	1.5	3.5	10.0	Ω	IOUTL=-10mA
OUTL Low Side ON-Resistor	R_{ONLL}	0.8	2.5	5.5	Ω	IOUTL=10mA
[SW]						
SW Low Side ON-Resistor	R_{ON_SW}	4.0	10.0	25.0	Ω	ISW=10mA
[Error AMP]						
LED Control Voltage	V_{LED}	0.9	1.0	1.1	V	
COMP Sink Current	$I_{COMPSINK}$	35	80	145	µA	VLED=2V, VCOMP=1V
COMP Source Current	$I_{COMPSOURCE}$	-145	-80	-35	µA	VLED=0.5V, VCOMP=1V
[Oscillator]						
Oscillation Frequency 1	fosc1	285	300	315	kHz	RT=27kΩ
Oscillation Frequency 2	fosc2	1800	2000	2200	kHz	RT=3.9kΩ
[OVP]						
OVP Detection Voltage	V_{OVP1}	1.9	2.0	2.1	V	VOVP=Sweep up
OVP Hysteresis Width	$V_{OVPHYS1}$	0.02	0.06	0.10	V	VOVP=Sweep down

Electrical Characteristics (V_{CC}=12V, Ta = -40°C to +125°C *Unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Normal	Max		
[UVLO]						
UVLO Detection Voltage	V_{UVLO}	3.2	3.5	3.8	V	VCC : Sweep down
UVLO Hysteresis Width	V_{UHYS}	0.25	0.5	0.75	V	VCC : Sweep up,VREG>3.5V
[LED Output]						
LED Current Relative Dispersion	I_{LED1}	-3	-	+3	%	ILED=50mA, Ta=25℃ ΔILED1=(ILED/ILED_AVG-1)×100
		-5	-	+5	%	ILED=50mA, Ta=-40℃～125℃ ΔILED1=(ILED/ILED_AVG-1)×100
LED Current Absolute Dispersion	I_{LED2}	-3	-	+3	%	ILED=50mA, Ta=25℃ ΔILED2=(ILED/50mA-1)×100
		-5	-	+5	%	ILED=50mA, Ta=-40℃～125℃ ΔILED2=(ILED/50mA-1)×100
ISET Voltage	V_{ISET}	0.9	1.0	1.1	V	RISET=100kΩ
PWM Minimum Pulse Width	T_{MIN}	1	-	-	μs	FPWM=100Hz～20kHz, ILED=20mA～100mA
PWM Frequency	f_{PWM}	0.1	-	20	kHz	
[Protection Circuit]						
LED Open Detection Voltage	V_{OPEN}	0.2	0.3	0.4	V	VLED1,2,3,4= Sweep down
LED Short Detection Voltage	V_{SHORT}	4.2	4.5	4.8	V	VLED1,2,3,4= Sweep up
LED Short Detection Latch OFF Delay Time	t_{SHORT}	70	100	130	ms	RRT=27kΩ
SCP Latch OFF Delay Time	t_{SCP}	70	100	130	ms	RRT=27kΩ
PWM Latch OFF Delay Time	t_{PWM}	70	100	130	ms	RRT=27kΩ
ISET-GND Short Protection impedance	$R_{ISETPROT}$	-	-	4.7	kΩ	
[Logic Input]						
Input High Voltage	V_{INH}	2.1	-	VREG	V	EN, SYNC, SHDETEN, PWM, LEDEN1, LEDEN2
Input Low Voltage	V_{INL}	GND	-	0.8	V	EN, SYNC, SHDETEN, PWM, LEDEN1, LEDEN2
Input Current	I_{IN}	15	50	100	μA	VIN=5V(EN,SYNC, SHDETEN PWM, LEDEN1, LEDEN2,)
[FAIL Output (Open Drain)]						
FAIL Low Voltage	V_{OL}	-	0.1	0.2	V	IOL=0.1mA

Typical Performance Curves

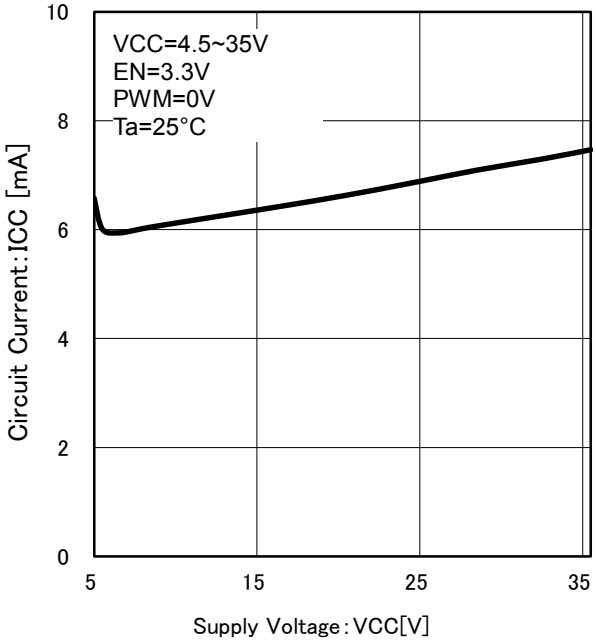


Figure 11. Circuit Current vs Supply Voltage

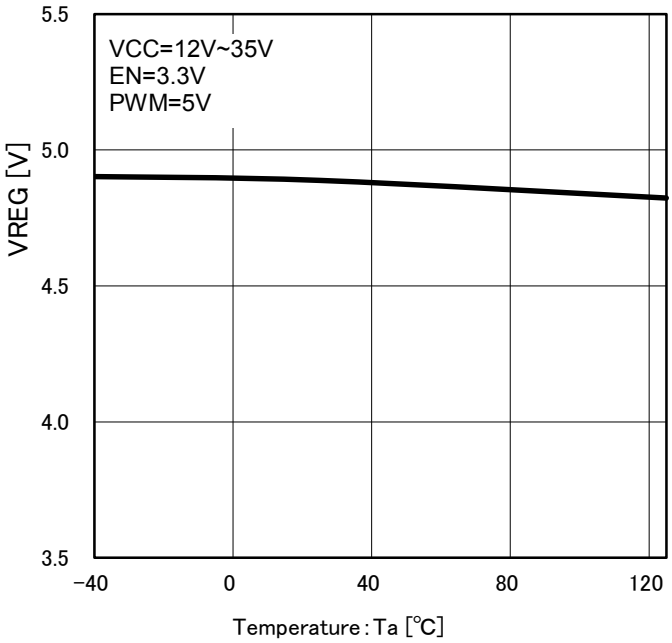


Figure 12. VREG vs Temperature

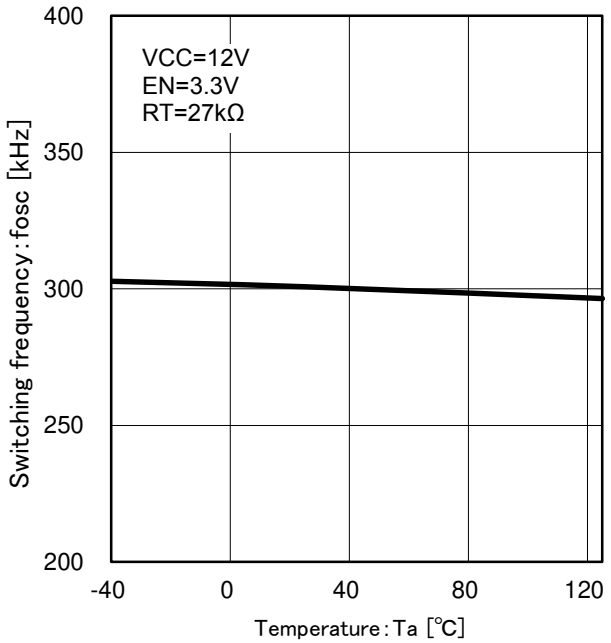


Figure 13. Switching Frequency vs Temperature (@ 300 kHz)

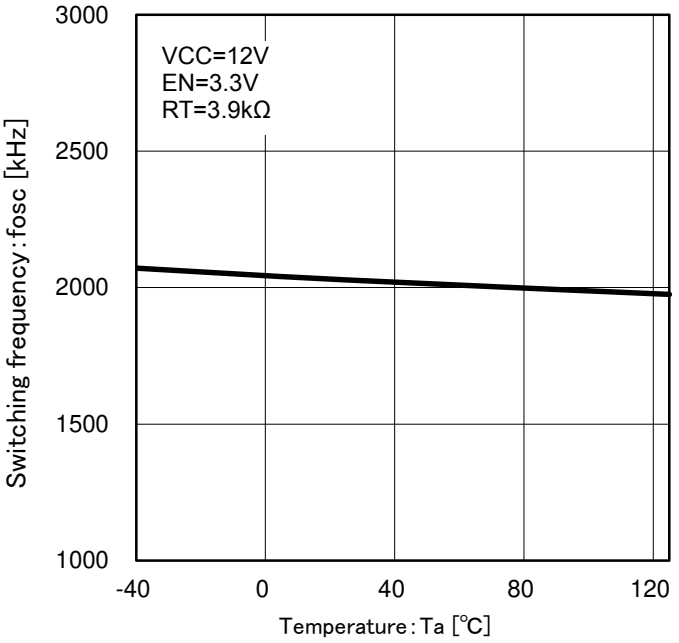


Figure 14. Switching Frequency vs Temperature (@ 2000 kHz)

Typical Performance Curves – continued

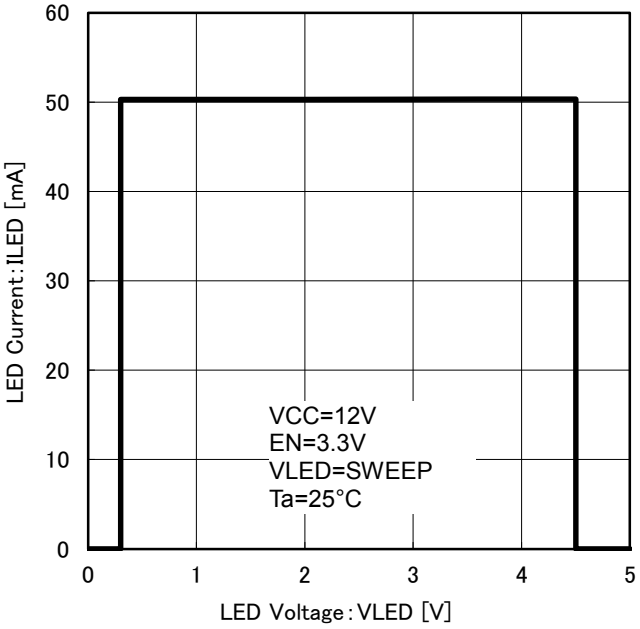


Figure 15. LED Current vs LED Voltage

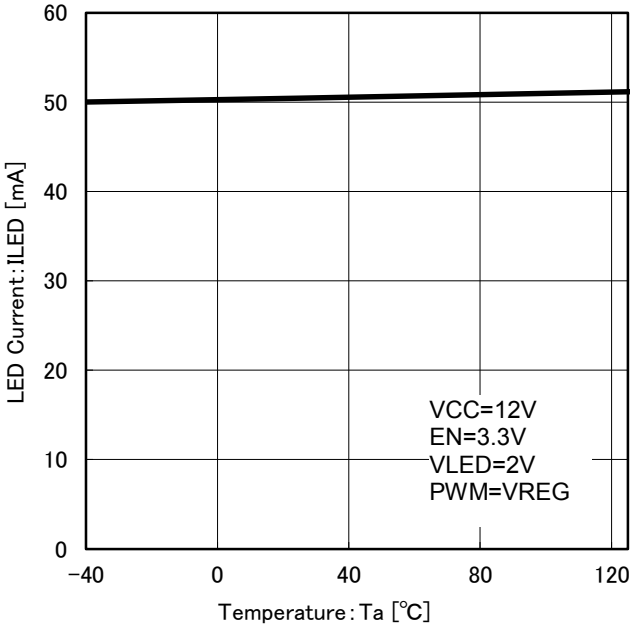


Figure 16. LED Current vs Temperature

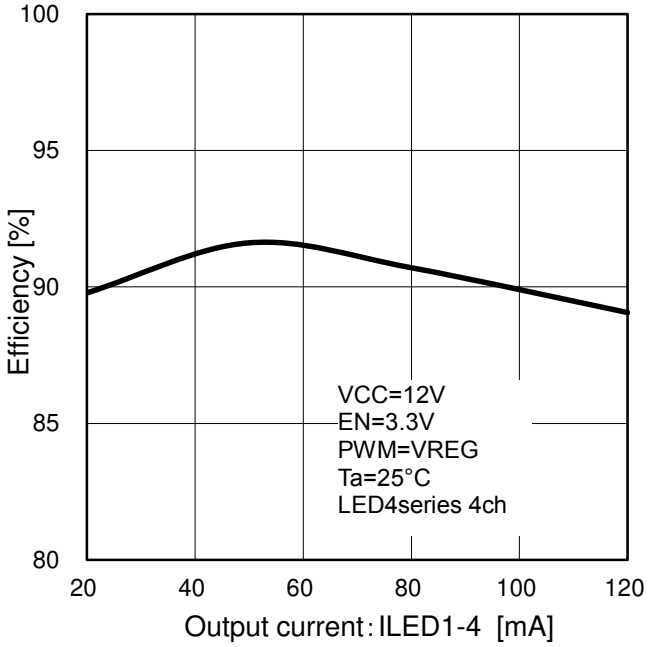


Figure 17. Efficiency vs Output Current
(Buck-Boost Application)

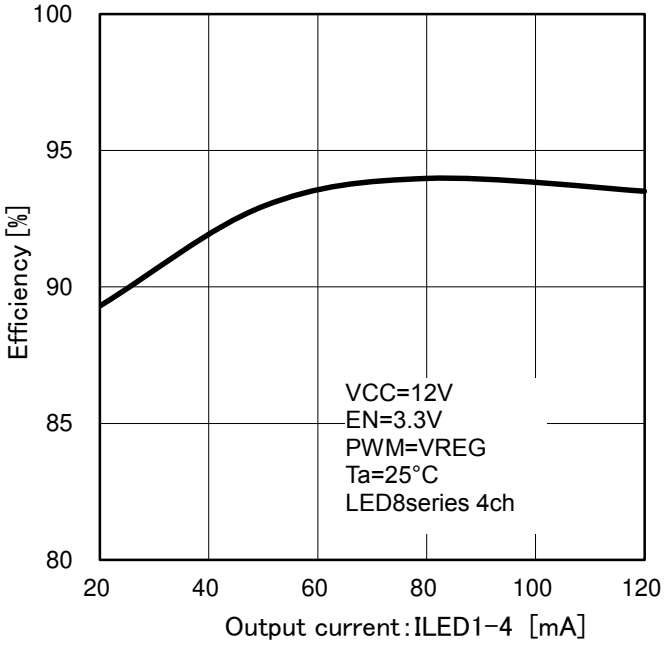


Figure 18. Efficiency vs Output Current
(Boost Application)

Timing Chart (Start up and Protection)

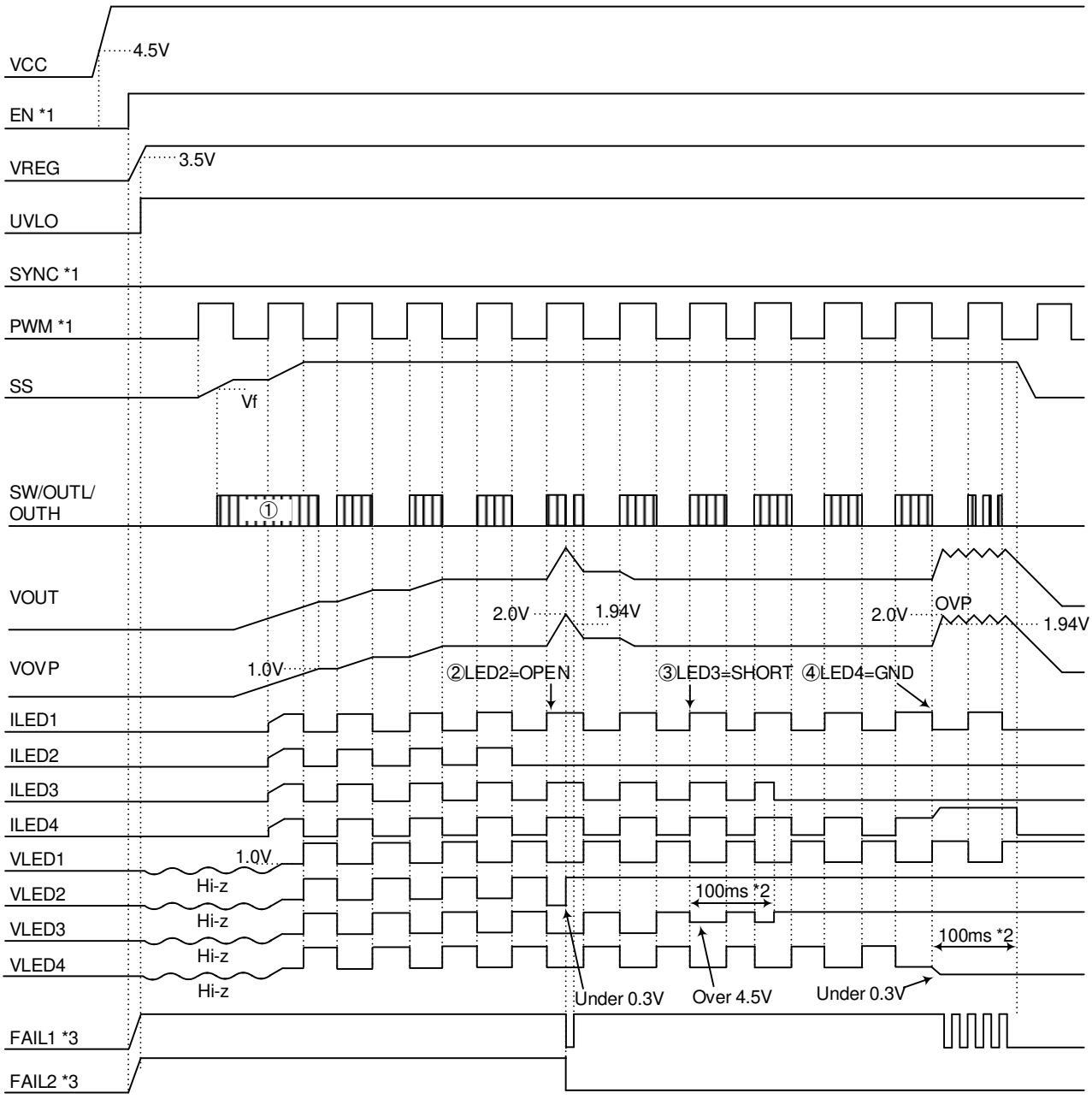


Figure 19. Startup and Protect function timing chart

*1 Vcc, EN, PWM, SYNC are input sequence free.
*2 The count time of 32770clk × 1/F_{OSC}. In case of fosc=300kHz, the count time is approximately 100ms.
*3 Above timing chart is the case of pulling up FAIL1 and FAIL2 terminal to VREG.

1. When VOVP less than 1.0V, regardless of PWM input, the DC/DC switching operation will be active (Pre-Boost function). And if VOVP reaches 1.0V, the Pre-Boost is finished.
2. When VLED2 less than 0.3V and VOVP more than 2.0V, LED Open Protect is active and LED2 is turned OFF. Then FAIL2 becomes Low.
3. If The condition of VLED3 more than 4.5V passes 100ms (@fosc=300kHz), LED3 is turned OFF. Then FAIL2 becomes Low.
4. When VLED4 short to GND, increase the Vout voltage. Then VOVP rises over 2.0V, FAIL1 becomes Low. If OVP occur, DCDC switching is OFF and decrease Vout voltage, then OVP repeats ON/OFF. And DCDC switching and LED current of each CH is OFF after approximately 100ms. (In case of fosc=300kHz).

Timing Chart (Start up and Restart)

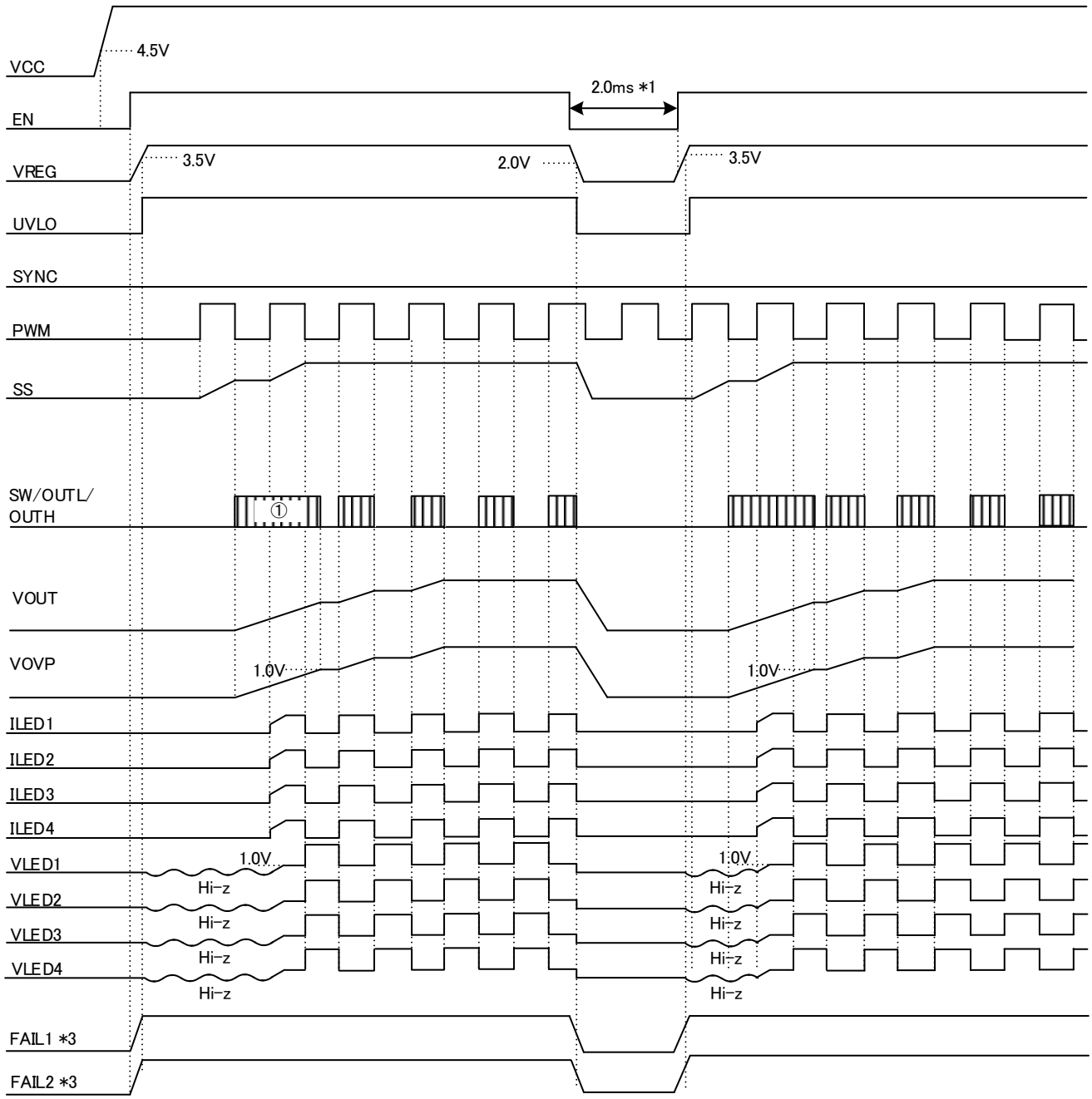


Figure 20. Start up and EN restart timing chart

*1 EN Low term when EN restart needs more 2.0ms

*2 Please restart after Vout voltage discharged. Vout discharge function (P.8) or external discharge switch is available. If EN restart with Vout voltage remaining, there is possibility of LED flash.

Application Examples

When using as Boost DC/DC converter

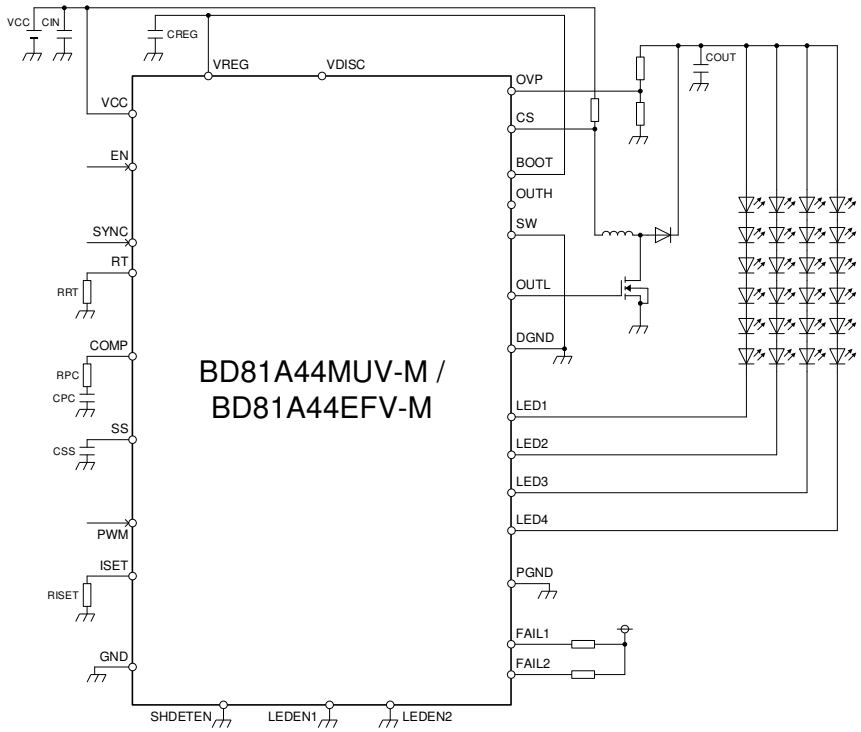


Figure 21. Boost application circuit

Note: When using as boost DC/DC converter, if the V_{OUT} and LED terminal are shorted, the over-current from VIN cannot be prevented. To prevent overcurrent, carry out measure such as inserting fuse in between V_{CC} and RCS.

When using as Buck DC/DC Converter

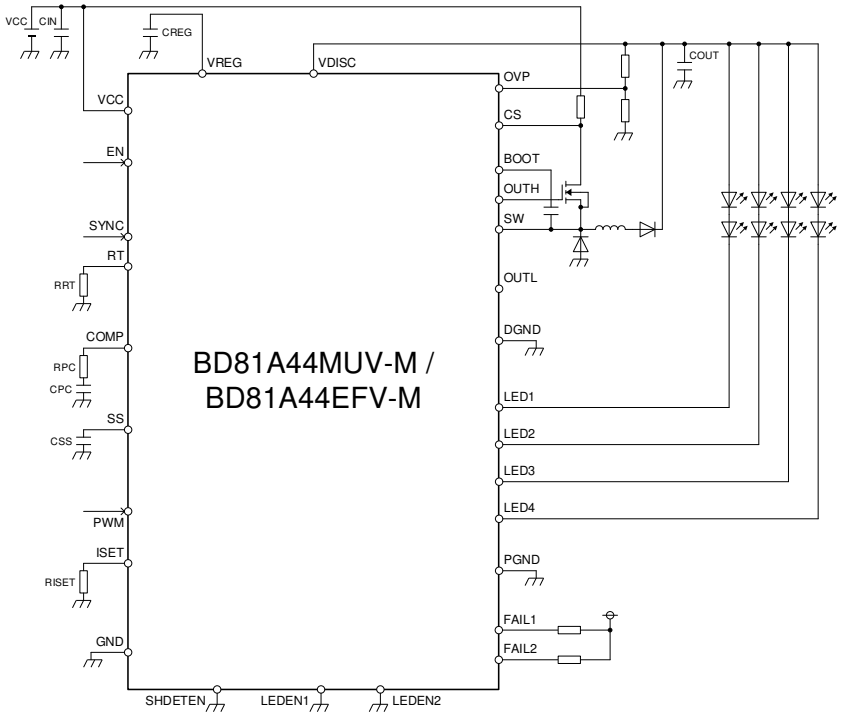


Figure 22. Buck application circuit

PCB Application Circuit

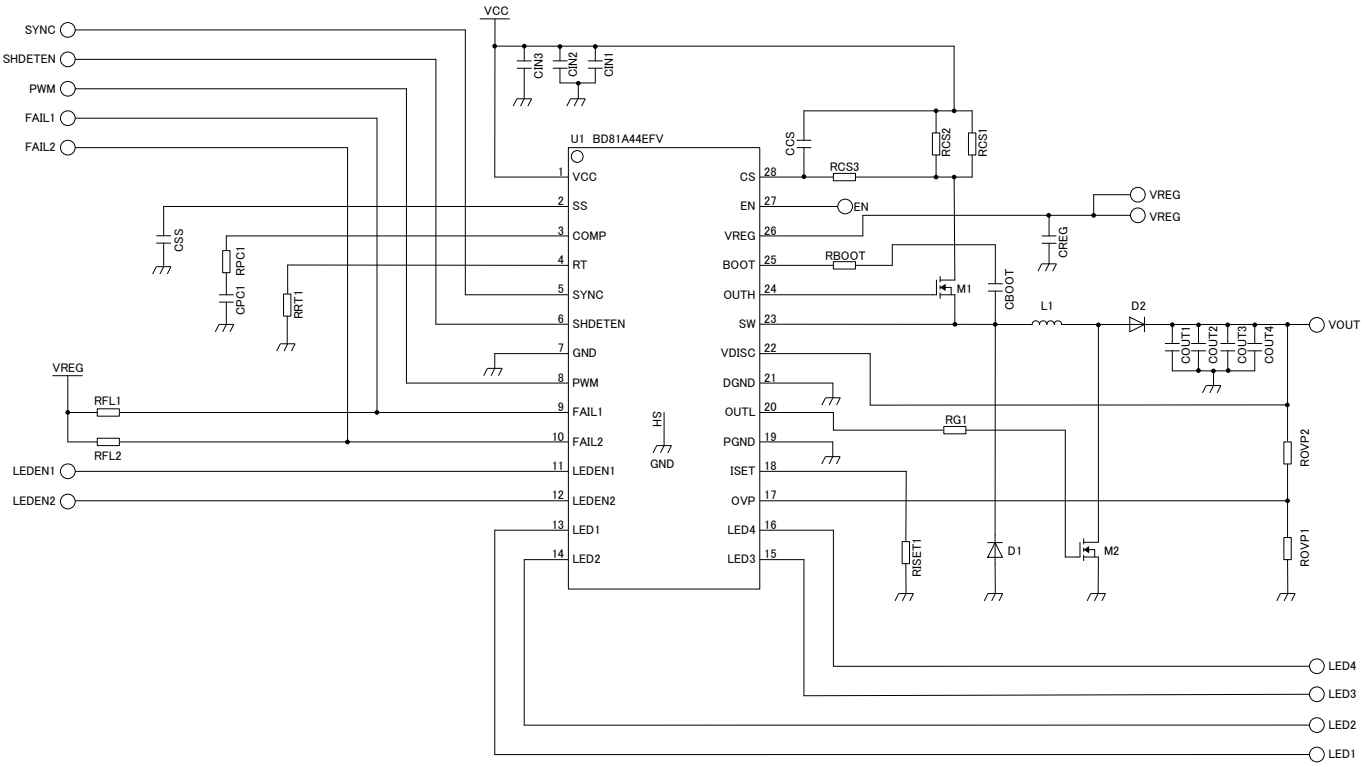


Figure 23. PCB Application Circuit

- Please arrange RRT resistor closest to RT pin and do not attach capacitor.
- Please arrange RISET resistor closest to ISET pin and do not attach capacitor.
- Please attach the decoupling capacitor of CIN and CREG to IC pin as close as possible.
- Because there is possibility that big current may flow into DGND and PGND, please make the impedance low.
- In pins of ISET, RT and COMP, please pay attention so that noise will not get in.
- Since PWM, OUTH, OUTL, SW, SYNC and LED 1-4 are switching, please pay attention so that it will not affect the surrounding pattern.
- There is a heat dissipation PAD at the back of package. Please solder the board for the heat dissipation PAD.
- Please set the gate resistor of step-down FET (M1) to 0Ω. If resistor is connected, M1 OFF timing is delayed in M1 parasitic capacity and gate resistor, and the penetrating current flows to the internal transistor of M1 and SW. OCP may be detected by penetrating current.
- To reduce noise, please consider the board layout in the shortest MIN impedance for Boost loop (D2→COUT→DGND→M2→D2) and Buck loop (VCC→RCS→M1→D1→DGND→GND→CIN→VCC).
- The ringing of Low side FET is decreased by RG1, but if RG1 value is increased, there is concern about a decrease of efficiency. Please evaluate to determine the proper value of RG1 to be used.

.

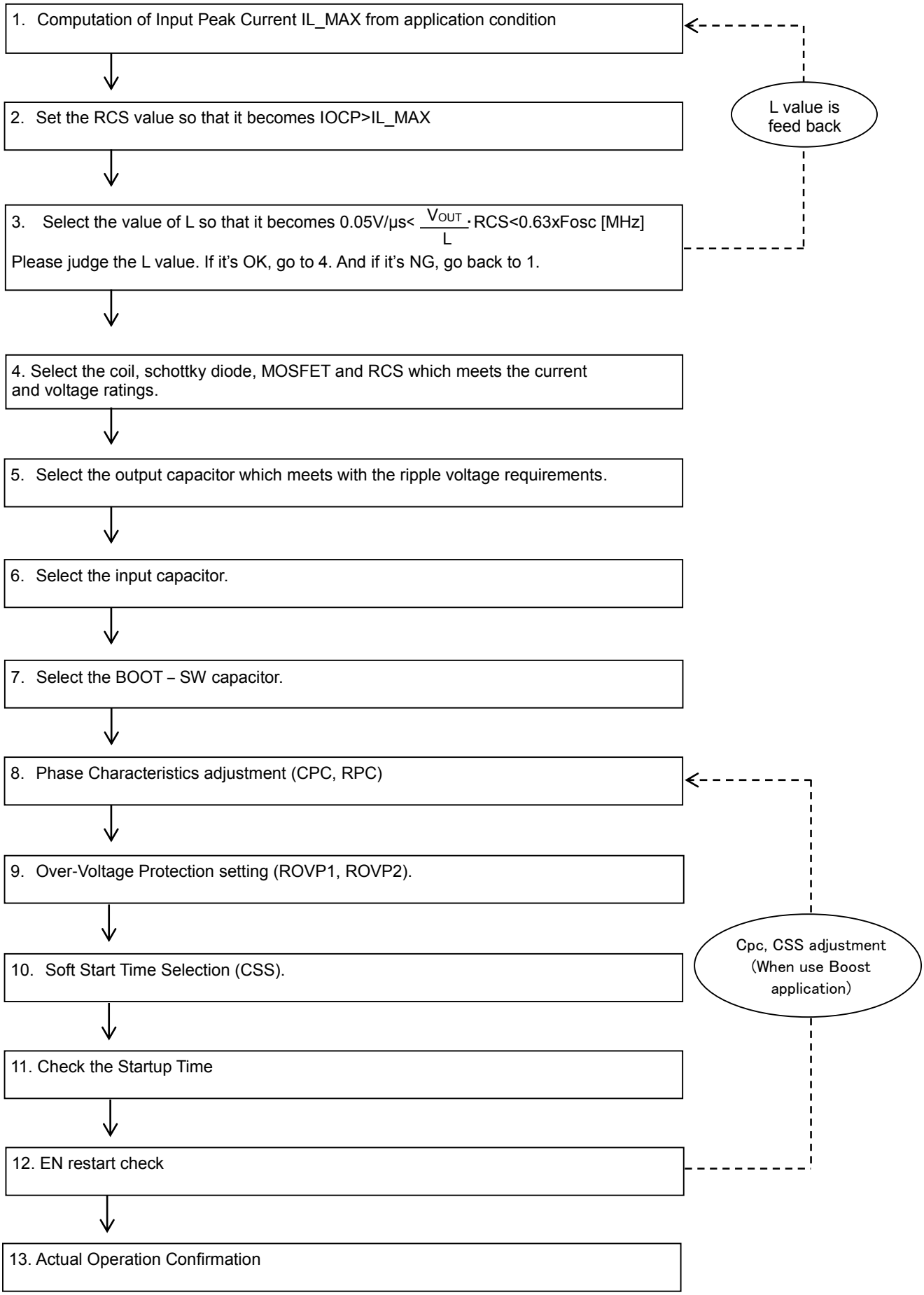
PCB Board External Components List（Buck Boost application）

serial No.	component name	component value	product name	Manufacturer
1	CIN1	10μF	GCM32EC71H106KA01	murata
2	CIN2	―	―	―
3	CIN3	―	―	―
4	RCS1	100mΩ	MCR100 Sieries	Rohm
5	RCS2	100mΩ	MCR100 Sieries	Rohm
6	RCS3	Short	―	―
7	CCS	―	―	―
8	CSS	0.1μF	GCM15R71H104KE37	murata
9	CPC1	0.01μF	GCM15R71H104KE37	murata
10	RPC1	5.1kΩ	MCR03 Series	Rohm
11	RRT1	27kΩ	MCR03 Series	Rohm
12	RFL1	100kΩ	MCR03 Series	Rohm
13	RFL2	100kΩ	MCR03 Series	Rohm
14	CREG	2.2μF	GCM188C71A225KE01	murata
15	CBOOT	0.1μF	GCM155R71H104KE37	murata
16	RBOOT	Short	―	―
17	L1	22μH	SLF12565T-220M3R5-PF	TDK
18	M1	―	RSS070N05	Rohm
19	M2	―	RSS070N05	Rohm
20	D1	―	RB050L-40	Rohm
21	D2	―	RB050L-40	Rohm
22	COUT1	10μF	GCM32EC71H106KA01	murata
23	COUT2	10μF	GCM32EC71H106KA01	murata
24	COUT3	10μF	GCM32EC71H106KA01	murata
25	COUT4	10μF	GCM32EC71H106KA01	murata
26	ROVP1	30kΩ	MCR03 Series	Rohm
27	ROVP2	360kΩ	MCR03 Series	Rohm
28	RISET1	100kΩ	MCR03 Series	Rohm
29	RG1	0Ω	―	―

* Above components should be changed by load or conditions.

Selection of Components Externally Connected

Follow the steps as shown below for selecting the external components.



1. Input Peak Current IL_Max Computation

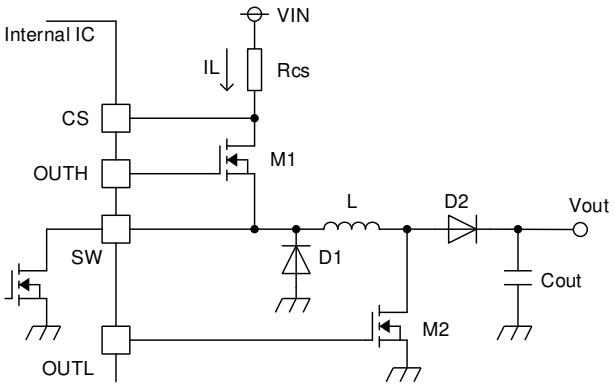


Figure 24. Output Application Circuit Diagram (In case of Buck-Boost application)

(1) Max Output Voltage (Vout_Max) Computation

Consider the VF variation and number of LED connection in series for Vout_Max derivation

$$Vout\_Max = (V_F + \Delta V_F) \times N + 1.1V$$

Vout_Max [V] : Max Output Voltage
VF[V] : LED VF Voltage
ΔVF[V] : LED VF Voltage Variation
N : LED series number

(P) Max Output Current I_{OUT_MAX} Computation

$$Iout\_Max = ILED \times 1.05 \times M$$

Iout_Max[A] : Max Input Peak Current
ILED[A] : Output Current per Channel
M : LED parallel number

(P) Max Input Peak Current I_{L_MAX} Computation

$$IL\_Max = IL\_AVG + 1 / 2\Delta IL$$

IL_Max[A] : Max Input Peak Current
IL_AVG[A] : Max Input Average Current
Δ IL[A] : Input Current Amplification

(In case of Boost application)

$$IL\_AVG = Vout\_Max \times Iout\_Max / (\eta \times VCC)$$

$$\Delta I_L = \frac{VCC}{L} \times \frac{1}{Fosc} \times \frac{Vout\_Max - VCC}{Vout\_Max}$$

(In case of Buck-Boost application)

$$IL\_AVG = (VCC + Vout\_Max) \times Iout\_Max / (\eta \times VCC)$$

$$\Delta I_L = \frac{VCC}{L} \times \frac{1}{Fosc} \times \frac{Vout\_Max}{VCC + Vout\_Max}$$

(In case of Buck application)

$$IL\_AVG = Iout\_Max / \eta$$

$$\Delta I_L = \frac{Vout}{L} \times \frac{1}{Fosc} \times \frac{VCC - Vout\_Max}{VCC}$$

VCC[V] : Input Voltage
Fosc[Hz] : Switching Frequency
η : Efficiency
L[H] : Coil Value

The worst case for VIN is Minimum, so the Minimum value should be applied in the equation.
The current-mode Type of DC/DC convertor is adopted for BD81A34MUV-M/EFV-M, which is optimized with the use of the recommended L value in the design stage. This recommendation is based upon the efficiency as well as the stability. The L values outside this recommended range may cause irregular switching waveform and hence deteriorate stable operation. N (efficiency) becomes almost 80%.

2. Setting of Over-Current Protection (IOCP) Value

$$IOCP[A] = Vocp\_Min[V](= 0.18V) \div Rcs[\Omega] > IL\_Max[A]$$

RCS should be selected by above equation.

3. Selection of the inductor
In order to achieve stable operation of the current mode DC/DC converter, we recommend selecting the L value in the range indicated below.

$$0.05[V/\mu s] < \frac{Vout[V] \times Rcs[\Omega]}{L[\mu H]} < 0.63 \times Fosc[MHz]$$

Since there is almost ±30% variation in the value of coil L, keep enough margin and set.
The smaller $\frac{Vout[V] \times Rcs[\Omega]}{L[\mu H]}$ allows stability improvement but slows down the response time.

If the condition of VCC is under 5V, please satisfy below equation when selecting the coil.

$$L[\mu H] < \frac{12 \times VCC[V] \times VCC[V] \times \eta}{Vout[V] \times ILED[A] \times Fosc[MHz]}$$

The coil outside of above equations may cause Low LED brightness.

4. Selection of Coil L, Diode D1, D2, MOSFET M1, RCS and COUT

	Current Rating	Voltage Rating	Heat Loss
Coil L	> IL_Max	—	—
Diode D1	> IOCP	> VCC_Max	—
Diode D2	> IOCP	> Vovp_Max	—
MOSFET M1	> IOCP	> VCC_Max	—
MOSFET M2	> IOCP	> Vovp_Max	—
R_{CS}	—	—	> $Iocp^2 \times Rcs$
C_{OUT}	—	>Vovp_Max	—

Please consider external parts deviation and make the setting with enough margin.
In order to achieve fast switching, choose the MOSFET's with the smaller gate-capacitance.

5. Selection of Output Capacitor
Select the output capacitor COUT based on the requirement of the ripple voltage Voutpp.

$$Voutpp[V] = \frac{20 \times ILED[A]}{Fosc[Hz] \times Cout[F] \times \eta} + \Delta I_L[A] \times R_{ESR}[\Omega]$$

Actually, VOUT ripple voltage is sensitive to PCB layout and external components characteristics. Therefore, when designing for mass-production, stability should be thoroughly investigated and confirmed in the actual physical design. Available Cout max value is 500uF.

6. Selection of Input Capacitor
We recommend an input capacitor greater than 10μF with the small ESR ceramic capacitor. The input capacitor outside of our recommendation may cause large ripple voltage at the input and hence lead to malfunction.

7. Selection of BOOT – SW capacitor
When using the BuckBoost application or Buck application, please input BOOT – SW capacitor 0.1uF.

8. Phase Characteristics adjustment

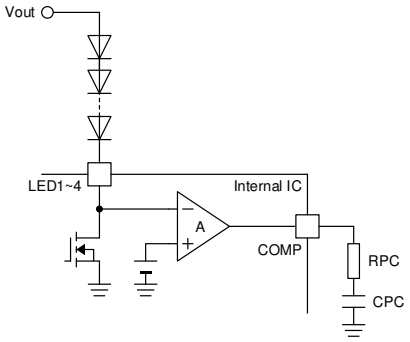


Figure 25. COMP terminal Application Circuit Diagram

About Application Stability Condition
The stability in LED voltage feedback system is achieved when the following conditions are met.
(1) The phase delay when gain is 1(0dB) is below 150°C (or simply, phase margin >30°C).
(2) The frequency (Unity Gain Frequency) when gain is 1(0dB) is <1/10 of switching frequency.

One way to assure stability based on phase margin adjustment is setting the Phase-lead fz close to switching frequency. In addition, the Phase-lag fp1 shall be decided based on COUT and Output impedance RL.
Respective formula shall be as follows.

Phase-lead $fz[Hz] = \frac{1}{2\pi Rpc[\Omega]Cpc[F]}$

Phase-lag $fp1[Hz] = \frac{1}{2\pi R_L[\Omega]Cout[F]}$ (Note) The output impedance calculated from $R_L = \frac{VOUT}{IOUT}$

Good stability would be obtained when the fz is set between 1kHz～10kHz.

It is important to keep in Mind that these are very loose guidelines, and adjustments may have to be made to ensure stability in the actual circuitry. It is also important to note that stability characteristics can change greatly depending on factors such as substrate layout and load conditions. Therefore, when designing for mass-production, stability should be thoroughly investigated and confirmed in the actual physical design.

9. Setting of Over Voltage Protection(OVP)
Over voltage protection (OVP) is set from the external resistance ROVP1 and ROVP2.
The setting described below will be important in the either boost, buck, buck-boost applications.

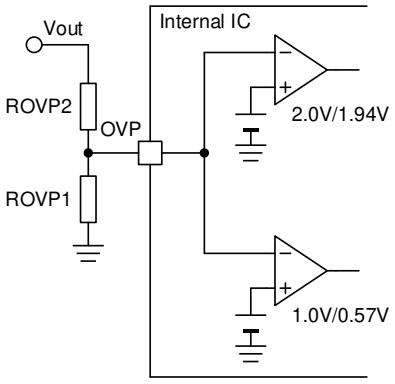


Figure 26. OVP Application Circuit

The OVP terminal detects the over voltage when at >2.0V (Typ) and stops the DC/DC switching. In addition, it detects the open condition when OVP terminal is at >2.0V (Typ) and LED1 to 4 pin voltage is at <0.3V (Typ), and the circuit is latched to OFF (Please refer to page 11, Protect Function). In preventing error in detection of OPEN, it is necessary that the resistor divide voltage of the maximum value of output voltage shall be less than the MIN value of OPEN detection voltage. Please set the ROVP1 and ROVP2 is such a way the formula shown below can be met.

$$Vout(Max)[V] \times \{ROVP1[\Omega]/(ROVP1[\Omega] + ROVP2[\Omega])\} < VOVPopen(Min)[V] \quad \cdots(1)$$

Vout : DC/DC Output Voltage VOVPopen : OVP Pin Open Detection Voltage

Sample 1: When V_F=3.2V±0.3V LED is used in 8series

$$Vout(Max)[V] = 1.1V(LED\ \ control\ \ voltage\ \ Max) + (3.2V + 0.3V) \times 8 = 29.1V$$

Open Detection OVP Pin Voltage $VOVPopen\ \ (Min) = 1.9V$

If ROVP1=20kΩ, please set by ROVP2 > 286.3kΩ from (1)

Sample 2: VF=3.2V±0.3V LED is used in 3series

$$Vout(Max)[V] = 1.1V(LED\ \ control\ \ voltage\ \ Max) + (3.2V + 0.3V) \times 3 = 11.6V$$

Open Detection OVP Pin Voltage $VOVPopen\ \ (Min) = 1.9V$

If ROVP1=20kΩ, please set by ROVP2 > 102.21kΩ from (1).

10. Setting of Soft Start time

The soft start circuit minimizes the coil current at the input and overshoot at the output voltage during the start-up condition. A capacitance in the range of 0.047 to 0.47μF is recommended. A capacitance of less than 0.047μF may cause overshoot at the output voltage. However, a capacitance greater than 0.47μF may cause massive reverse current through the parasitic elements when power supply is OFF and may damage the IC.

Soft start time TSS (Typ) is below.

$$TSS[s] = CSS[\mu F] \times 3.3[V] \,/\, 5[\mu A]$$ CSS: The capacitance at SS terminal

11. Check the Start up time

If the PWM duty at start up is small, the start up time is longer. If you want to setup the Startup Time shorter, small CPC value is available, but it needs phase margin check. Below data is PWM duty vs Startup Time of representative two conditions.

Condition 1 (Boost, below figure left side)
Vcc = 12V, Vout = 30V (assumed LED 8 series), RRT = 27kΩ (Fosc = 300kHz), CPC=0.01μF, RPC=5.1kΩ, CSS = 0.1μF, ROVP1 = 20kΩ, ROVP2 = 360kΩ

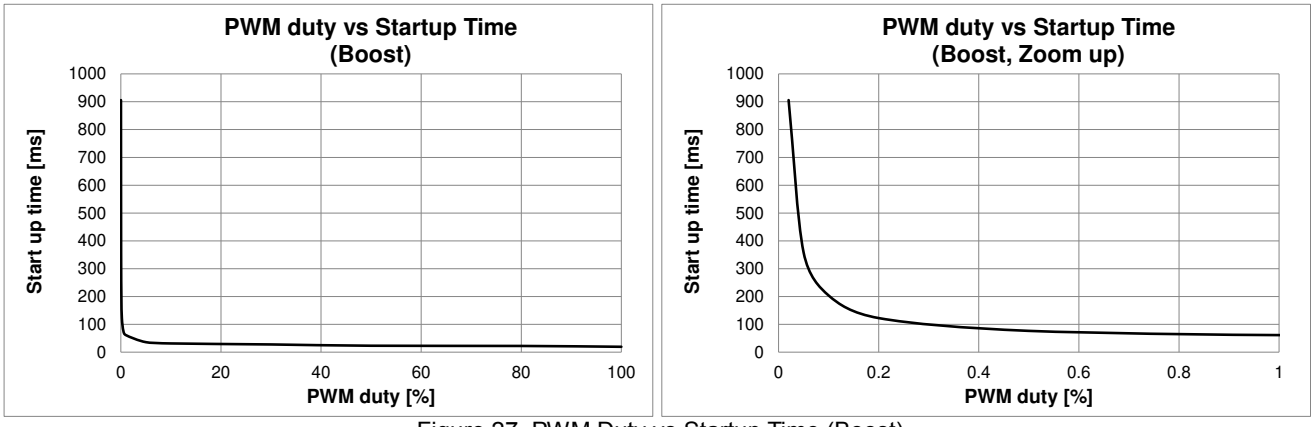


Figure 27. PWM Duty vs Startup Time (Boost)

Condition 2 (BuckBoost, below figure right side)
Vcc = 12V, Vout = 20V (assumed LED 5 series), RRT = 27kΩ (Fosc = 300kHz), CPC=0.01μF, RPC=5.1kΩ, CSS = 0.1μF, ROVP1 = 30kΩ, ROVP2 = 360kΩ

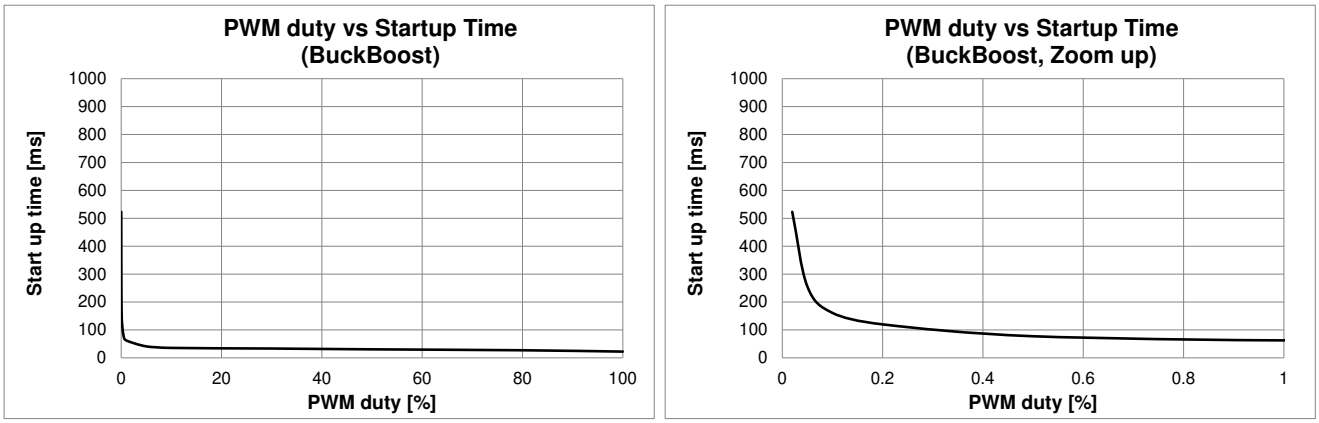


Figure 28. PWM Duty vs Startup Time (BuckBoost)

Above data is only reference data. Actual Startup Time depends on layout pattern, parts value and part characteristics, Please verify your design by the actual measurements.

12. EN restart check

EN restart when Vout voltage is remain, it possible to detect SCP. Please set the condition according to applications.

When use the BuckBoost or Buck application.

Please connect Vout and VDISC terminal and set EN=Low time refer to the below equation.

$$Tdisc[s] = \frac{3 \times Vout[V] \times Cout[F]}{4 \times IDISC[A]} < EN\ \ Low\ \ Time\ \ [s]$$

Regarding Tdisc details, please refer P.8.

When use the Boost application.

Please adjust CSS and Cpc value according to below. If Cpc value is changed, phase margin will changed, and if CSS value is changed, start up time is changed. Please verifying by actual measurements.

$$T1[s] = \left(\frac{0.4 + 2.7 \times n - VCC[V]}{0.4 + 2.7 \times n} \times \frac{1}{Fosc[kHz] \times RRT[kHz] \times 138\mu} + 1.56\right) \times Cpc[\mu F] / (0.46 \times Duty[\%])$$

$$T2[s] = CSS[\mu F] \times 0.61 + 29.8 / Fosc[kHz]$$

Please adjust CSS and Cpc value with $T1[s] < T2[s]$

n : LEDseries number
VCC[V] : Power supply
Fosc[kHz] : DCDC Frequency
RRT[kΩ] : RT resistence
Cpc[μF] : COMP capacitor
Duty[%] : PWM Duty
CSS[μF] : SS capacitor

Ex.) n=7, Vcc=7V, Fosc=300kHz, RRT=27kΩ, Cpc=0.01μF, CSS=0.1μF, PWM Duty = 1%

$$T1[s] = \left(\frac{0.4 + 2.7 \times 7 - 7}{0.4 + 2.7 \times 7} \times \frac{1}{300 \times 27 \times 138\mu} + 1.56\right) \times 0.01 / (0.46 \times 1) = 46.3ms$$

$$T2[s] = 0.1 \times 0.61 + \frac{29.8}{300} = 160.3ms$$

$T1[s] < T2[s]$ This condition is OK.

13. Verification of the operation by taking measurements

The overall characteristics may change based on load current, input voltage, output voltage, inductance, load capacitance, switching frequency, and PCB layout. We strongly recommend verifying your design by the actual measurements.