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LED Drivers for Automotive Light

BD8381AEFV-M

General Description

BD8381AEFV-M is a white LED driver with the capability of withstanding high input voltage (50V MAX). It has also an integrated current-mode, buck-boost DC/DC controller to achieve stable operation against high input voltage and to remove the constraint of the number of LEDs in series connection.

The LED brightness is controlled by either linear or PWM signal and is also possible to be controlled even without using a microcomputer, but instead, by means of the built-in PWM brightness signal generation circuit.

Features

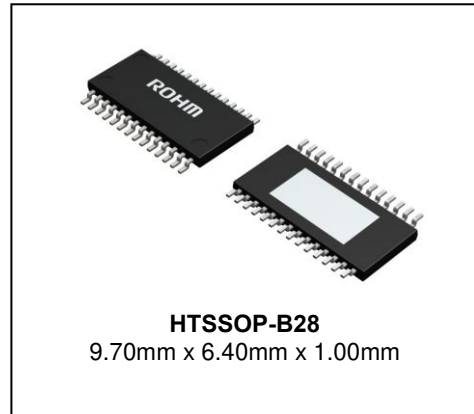
- Integrated buck-boost current-mode DC/DC controller
- Built-in CR timer for PWM brightness
- PWM linear brightness
- Built-in protection functions (UVLO, OVP, TSD, OCP, SCP)
- LED error status detection function (OPEN/SHORT)

Key Specifications

- Input Supply Voltage Range: 5.0V to 30V
- Operating Temperature Range: -40°C to +125°C

Package

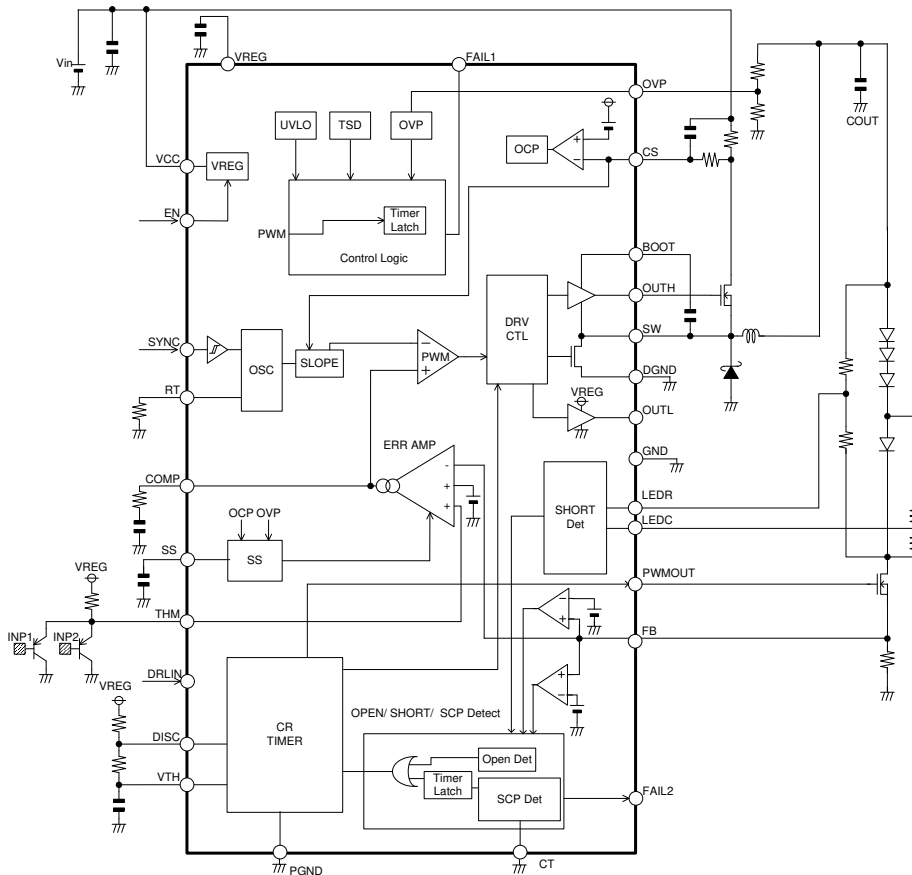
W(Typ) x D(Typ) x H(Max)



Applications

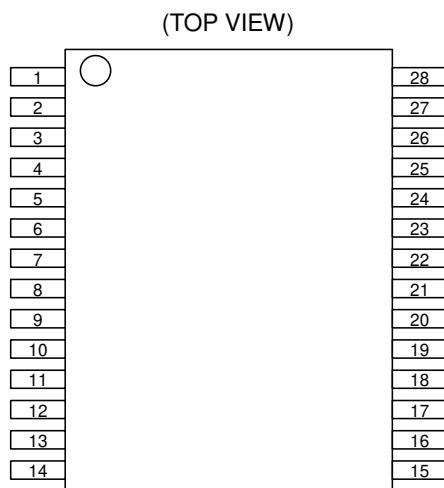
Headlight and Daytime Running Light etc.

Typical Application Circuit and Block Diagram



○Product structure: Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration



Pin Descriptions

Pin	Symbol	Function
1	COMP	Error amplifier output
2	SS	Soft start setting input
3	VCC	Input power supply
4	EN	Enable input
5	RT	Oscillation frequency-setting resistance input
6	SYNC	External synchronization signal input
7	GND	Small-signal GND
8	THM	Thermally sensitive resistor connection pin
9	FB	ERRAMP FB signal input pin
10	DISC	CR Timer discharge pin
11	VTH	CR Timer threshold pin
12	DRLIN	DRL switch pin (Pulse output setting pin)
13	FAIL1	Failure signal output
14	FAIL2	LED open/short detection signal output
15	OVP	Over-voltage detection input
16	LEDC	LED short detection pin (LED detection side)
17	LEDR	LED short detection pin (Resistor detection side)
18	N.C.	-
19	PGND	PWM brightness source pin
20	PWMOUT	PWM brightness signal output pin
21	CT	GND short protection timer setting pin
22	OUTL	Low-side external FET Gate Drive out put
23	DGND	Low-side FET driver source pin
24	SW	High-side FET Source pin
25	OUTH	High-side external FET Gate Drive out put
26	CS	DC/DC output current detection pin
27	BOOT	High-side FET driver source pin
28	VREG	Internal reference voltage output

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V _{CC}	50	V
Boot Voltage	V _{BOOT}	55	V
SW,CS,OUTH Voltage	V _{SW} , V _{CS} , V _{OUTH}	50	V
BOOT-SW Voltage	V _{BOOT-SW}	7	V
V _{REG} , V _{OVP} , V _{OUTL} , V _{FAIL1} , V _{FAIL2} , V _{THM} , V _{SS} , V _{COMP} , V _{RT} , V _{SYNC} , V _{EN} , V _{DISC} , V _{VTH} , V _{FB} , V _{LEDR} , V _{LEDC} , V _{DRLIN} , V _{PWMOUT} , V _{CT} Voltage		-0.3 to +7 < V _{CC}	V
Power Consumption	P _d	1.45 ^(Note 1)	W
Operating Temperature Range	T _{opr}	-40 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Junction Temperature	T _{jmax}	150	°C

(Note 1) IC mounted on glass epoxy board measuring 70mm x 70mm x 1.6mm, power dissipated at a rate of 11.60mW/°C at temperatures above 25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings..

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V _{CC}	5.0 to 30	V
Oscillating Frequency Range	f _{osc}	100 to 600	kHz
External Synchronization Frequency Range (Note 2) (Note 3)	f _{SYNC}	f _{osc} to 600	kHz
External Synchronization Pulse Duty Range	f _{SDUTY}	40 to 60	%

(Note 2) Connect SYNC to GND or OPEN when not using external frequency synchronization.

(Note 3) Do not switch between internal and external synchronization when an external synchronization signal is input to the device.

Electrical Characteristics (Unless otherwise specified, $V_{CC}=12V$ $T_a=25^{\circ}C$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I_{CC}	-	4.5	7.0	mA	EN=Hi, SYNC=Hi, RT=OPEN, $C_{IN}=10\mu F$
Standby Current	I_{STBY}	-	0	8	μA	EN=Low
[VREG Block (VREG)]						
Reference Voltage	V_{REG}	4.5	5.0	5.5	V	$I_{REG}=-5mA$, $C_{REG}=10\mu F$
[OUTH Block]						
OUTH High-Side ON-Resistance	R_{ONHH}	1.5	3.5	7.0	Ω	$I_{ON}=-10mA$
OUTH Low-Side ON-Resistance	R_{ONHL}	1.0	2.5	5.0	Ω	$I_{ON}=10mA$
Over-Current Protection Operating Voltage	V_{OLIMIT}	$V_{CC}-0.68$	$V_{CC}-0.60$	$V_{CC}-0.52$	V	
SS Charge Current	I_{SS}	3	5	7	μA	$V_{SS}=0V$
[OUTL Block]						
OUTL High-Side ON-Resistance	R_{ONLH}	2.0	4.0	8.0	Ω	$I_{ON}=-10mA$
OUTL Low -Side ON-Resistance	R_{ONLL}	1.0	2.5	5.0	Ω	$I_{ON}=10mA$
[SW Block]						
SW Low -Side ON-Resistance	R_{ONSW}	2.0	4.5	9.0	Ω	$I_{ONSW}=10mA$
[PWMOUT Block]						
PWMOUT High-Side ON-Resistance	R_{ONPWMH}	2.0	4.0	8.0	Ω	$I_{ONPWMH}=-10mA$
PWMOUT Low-Side ON-Resistance	R_{ONPWML}	1.0	2.5	5.0	Ω	$I_{ONPWML}=10mA$
[Error Amplifier Block]						
Reference Voltage1	V_{REF1}	0.194	0.200	0.206	V	FB-COMP Short, $1M\Omega/250k\Omega$
Reference Voltage2	V_{REF2}	0.190	0.200	0.210	V	FB-COMP Short, $1M\Omega/250k\Omega$ $T_a=-40^{\circ}C$ to $+125^{\circ}C$
The Amount of Change of VREF by Temperature	dV_{REF2}	-0.090	-0.045	-0.003	mV/ $^{\circ}C$	
COMP Sink Current	$I_{COMPSINK}$	50	75	100	μA	$V_{FB}=0.4V$, $V_{COMP}=1V$
COMP Source Current	$I_{COMPSOURCE}$	-100	-75	-50	μA	$V_{FB}=0V$, $V_{COMP}=1V$
Max Duty Output	D_{max}	83	90	-	%	$f_{OSC}=300kHz$
[Oscillator Block]						
Oscillating Frequency	f_{OSC}	285	300	315	KHz	$R_{RT}=200k\Omega$
[OVP Block]						
Over-Voltage Detection Reference Voltage	V_{OVP}	1.9	2.0	2.1	V	V_{OVP} =Sweep up
OVP Hysteresis Width	V_{OHYS}	0.45	0.55	0.65	V	V_{OVP} = Sweep down
[UVLO Block]						
UVLO Voltage	V_{UVLO}	4.0	4.35	4.7	V	V_{CC} = Sweep down
UVLO Hysteresis Width	V_{UHYS}	50	150	250	mV	V_{CC} = Sweep up
[PWM Generation Circuit Block]						
VTH Threshold Voltage	V_{TH1}	3	$2/3V_{REG}$	3.7	V	
VTH Threshold Voltage	V_{TH2}	1	$1/3V_{REG}$	2	V	
PWM Minimum ON Width	t_{PWMON}	25	-	-	μs	
LED OPEN Detection Function	V_{OPEN}	30	50	70	mV	
LED SHORT Detection Function	V_{SHORT}	100	200	400	mV	$V_{SHORT} \geq V_{LEDR} - V_{LEDC} $
LED GND Short Protection Timer	t_{SHORT}	100	150	200	ms	$C_{CT}=0.1\mu F$
[Logic Inputs]						
Input HIGH Voltage	V_{INH}	3.0	-	-	V	
Input LOW Voltage	V_{INL}	GND	-	1.0	V	
Input Current 1	I_{IN}	20	35	50	μA	$V_{IN}=5V$ (SYNC/DRLIN)
Input Current 2	I_{EN}	15	30	45	μA	$V_{EN}=5V$ (EN)
[FAIL Output (Open Drain)]						
Fail LOW Voltage	V_{OL}	-	0.1	0.2	V	$I_{OL}=0.1mA$

Typical Performance Curves
 (Unless otherwise specified, Ta=25°C)

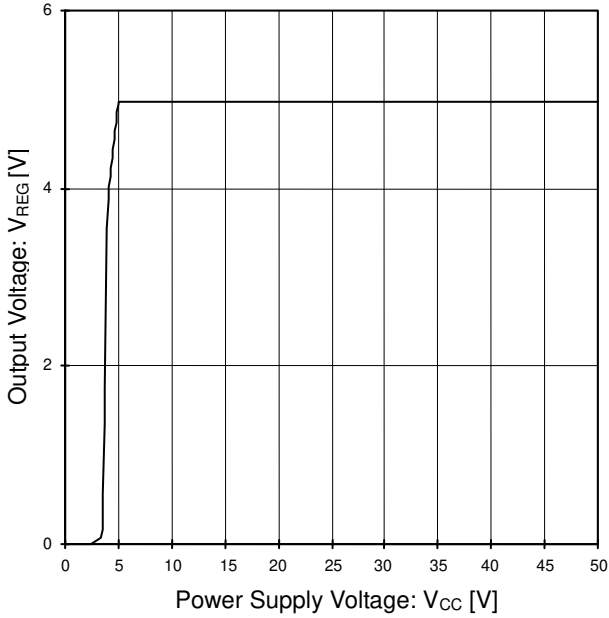


Figure 1. Output Voltage vs Power Supply Voltage (VREG Voltage Characteristic)

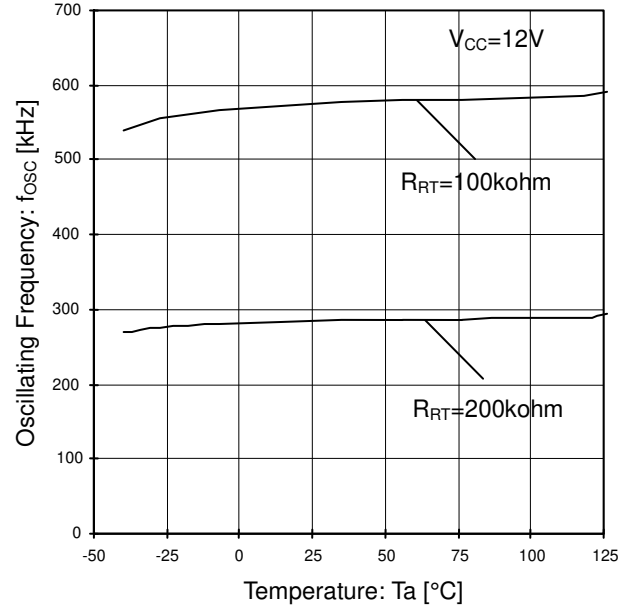


Figure 2. Oscillating Frequency vs Temperature (fOSC Temperature Characteristic)

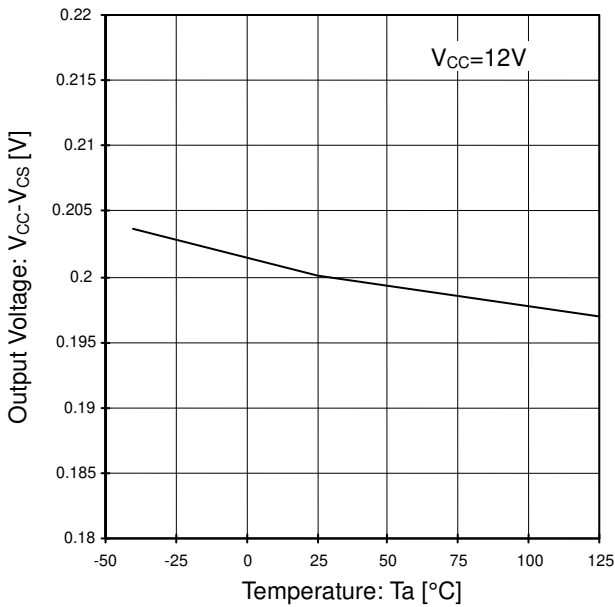


Figure 3. Output Voltage vs Temperature (Standard Voltage Temperature Characteristic)

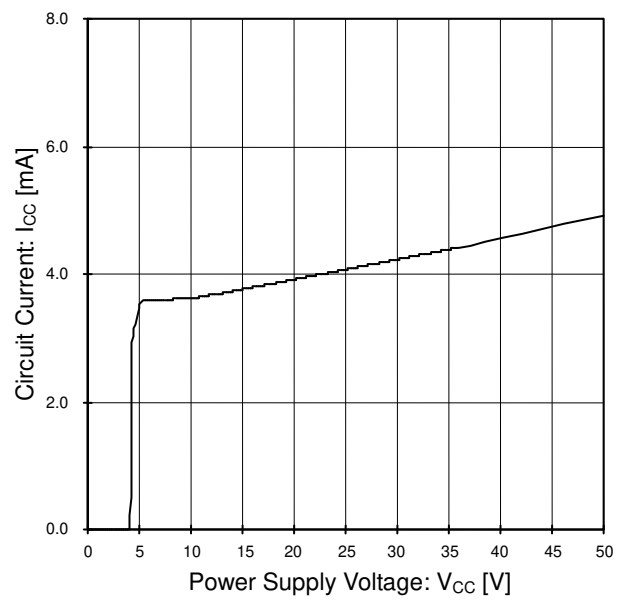


Figure 4. Circuit Current vs Power Supply Voltage

Typical Performance Curves – continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$)

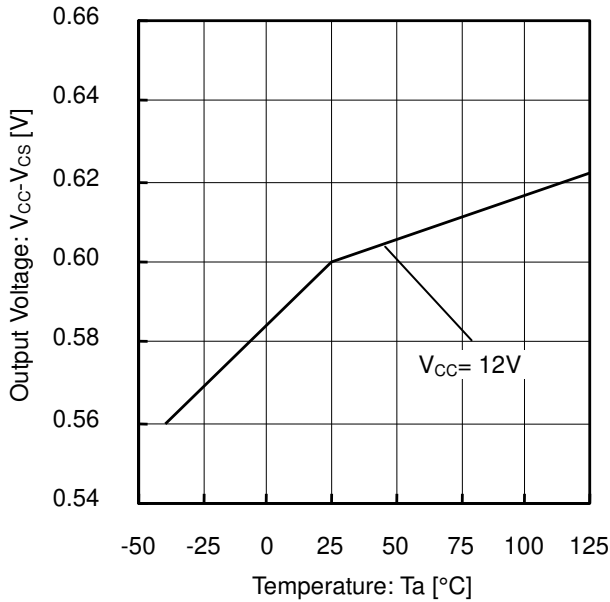


Figure 5. Output Voltage vs Temperature (Overcurrent Detection Voltage Temperature Characteristic)

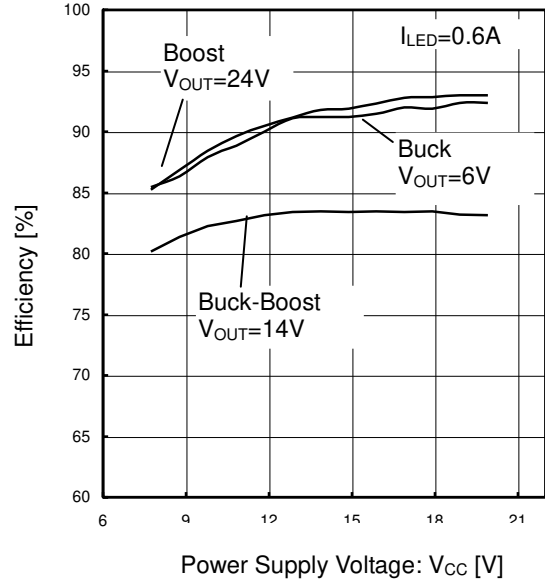


Figure 6. Efficiency vs Power Supply Voltage (Input Voltage Dependence)

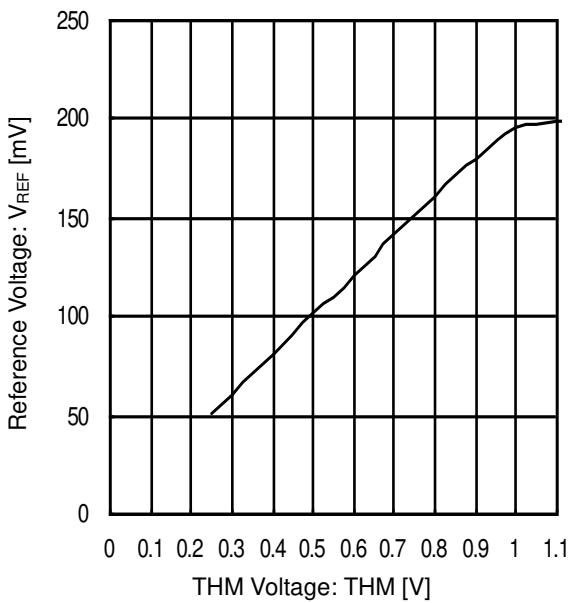


Figure 7. Reference Voltage vs THM Voltage (THM Gain)

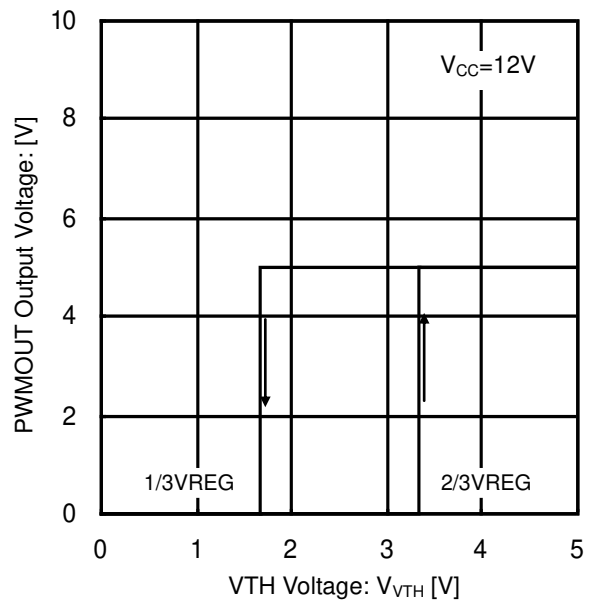


Figure 8. PWMOUT Output Voltage vs VTH Threshold Voltage

Typical Performance Curves – continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$)

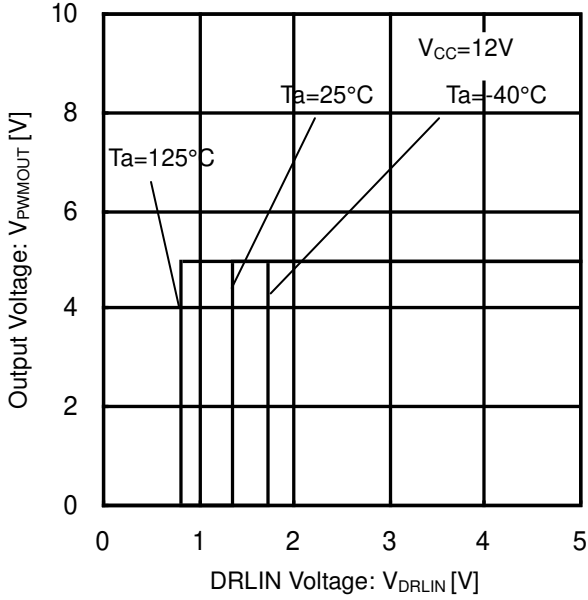


Figure 9. Output Voltage vs DRLIN Threshold Voltage

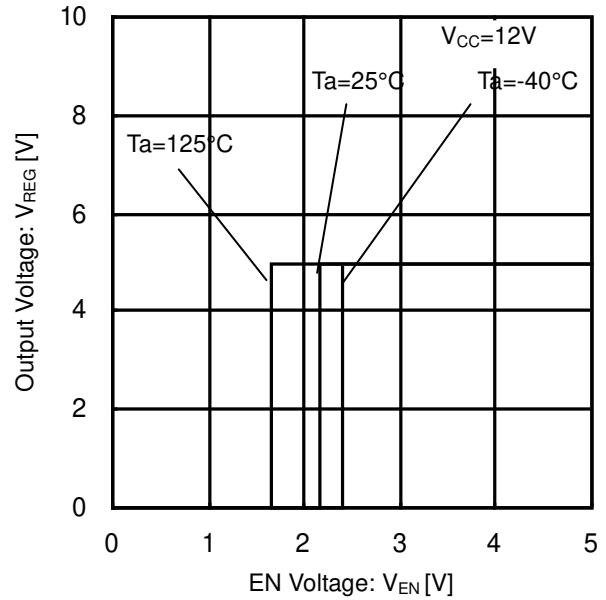


Figure 10. Output Voltage vs EN Threshold Voltage (DRLIN=VREG)

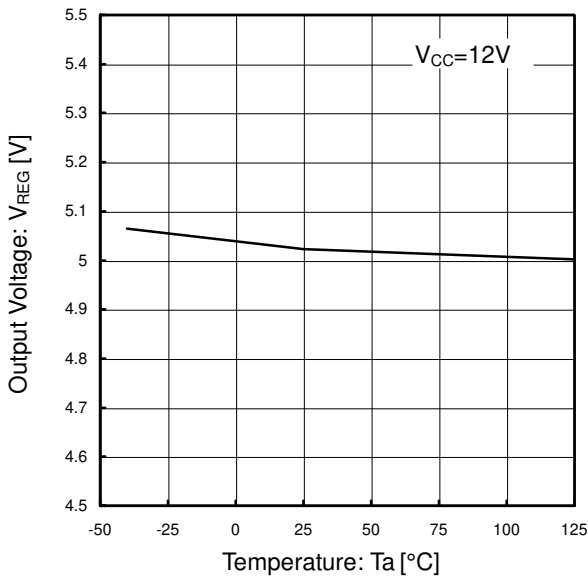


Figure 11. Output Voltage vs Temperature (VREG Voltage Temperature Characteristic)

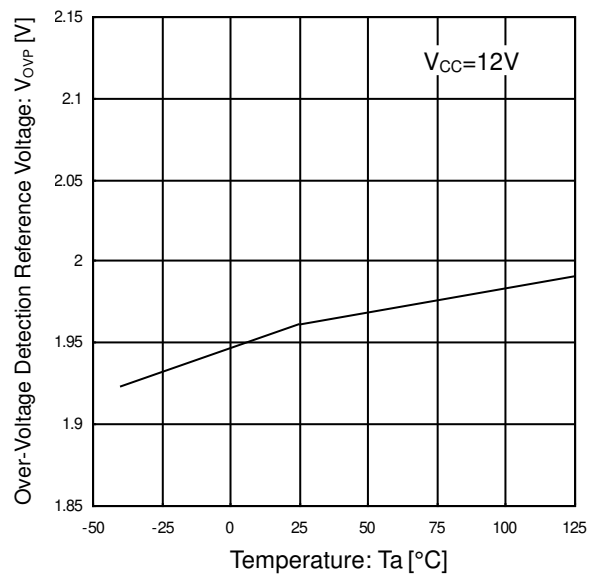


Figure 12. Over-Voltage Detection Reference Voltage vs Temperature (OVP Voltage Temperature Characteristic)

Typical Performance Curves – continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$)

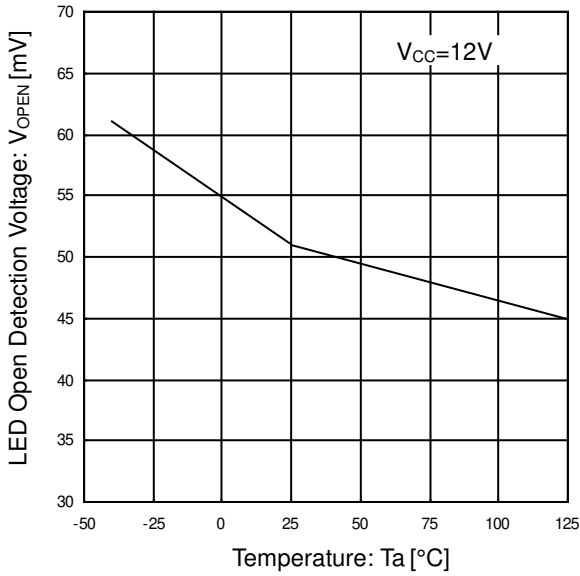


Figure 13. LED Open Detection Voltage vs Temperature

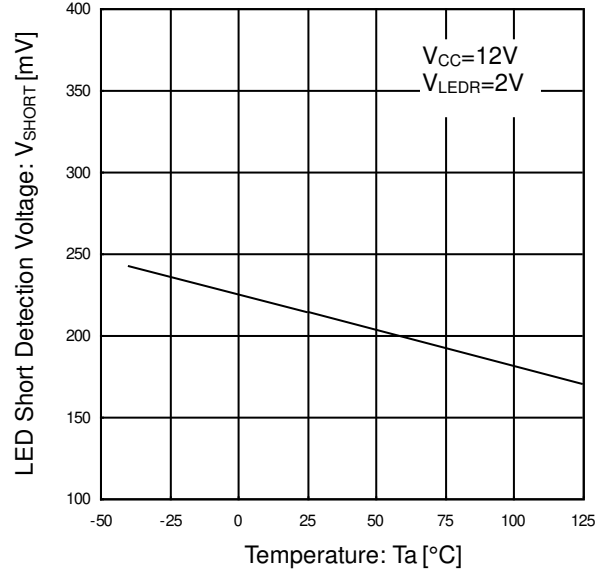


Figure 14. LED Short Detection Voltage vs Temperature

Application Information

1. Application Circuit

Application Circuit 1

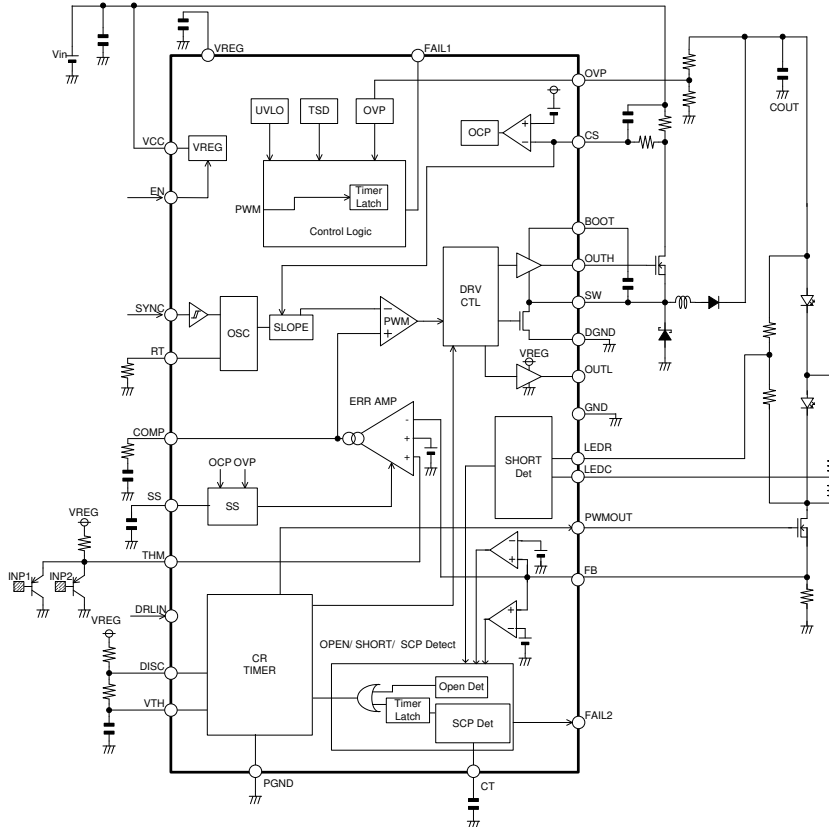


Figure 15

Buck application composition (It is INP1, INP2 and two input selector function and EN connected direct to VCC)

Application Circuit 2

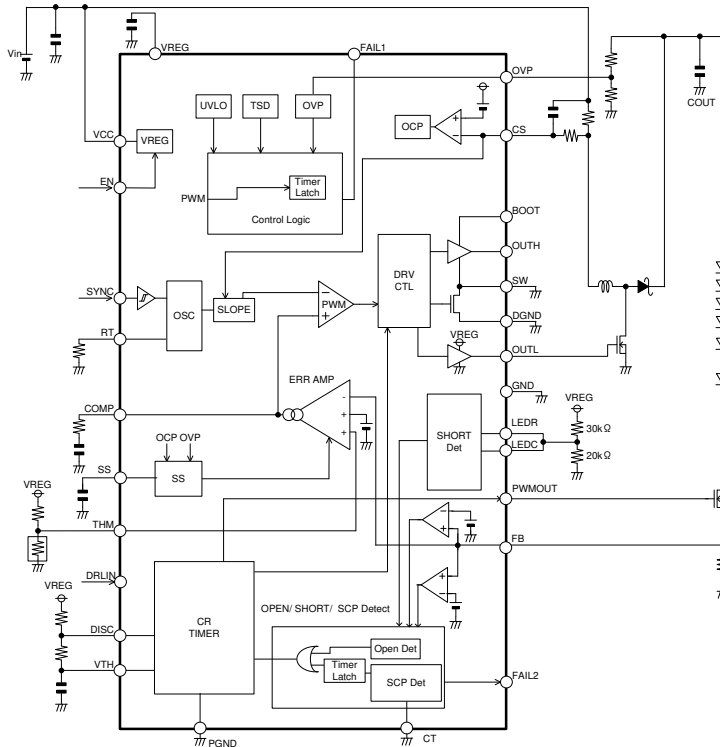


Figure 16

Boost application composition (When invalidating short detection and EN is inputted by a voltage divider)

2. Reference PCB Setting

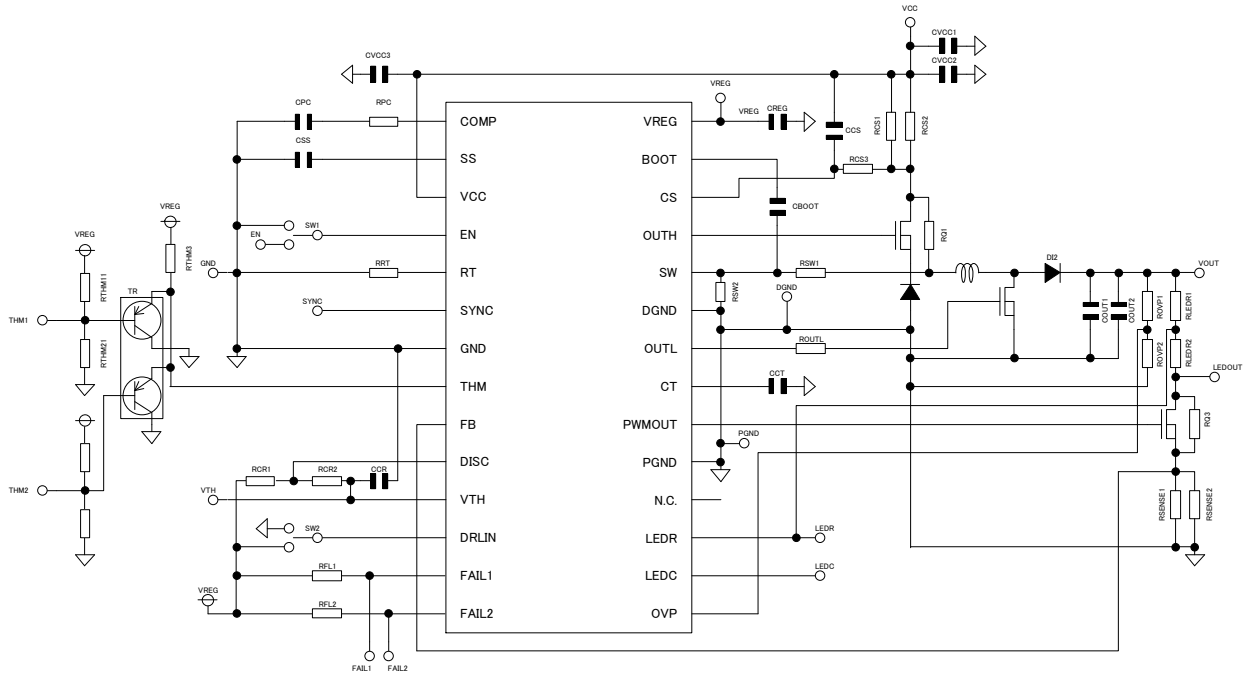


Figure 17

V_{CC}=8V to 16V, V_{OUT}=16V, I_{LED}=1A, f_{OSC}=300kHz, PWM dummign25%, PWM Frequency 130Hz

No.	Component Name	Component Value	Product Name	No.	Component Name	Component Value	Product Name
1	CVCC1	10μF	GCM32ER71E106KA42	23	CCS	N.M	-
2	CVCC2	10μF	GCM32ER71E106KA42	24	CBOOT	0.1μF	GCM188R11H104KA42
3	CVCC3	0.1μF	GRM31CB31E104KA75B	25	Q1	RSS070N05	-
4	CPC	0.1μF	GCM188R11H104KA42	26	DI1	RB050L-40	-
5	RPC	820Ω	MCR03 Series	27	RSW1	0Ω	-
6	CSS	0.1μF	GCM188R11H104KA42	28	RSW2	N.M	-
7	RRT	200kΩ	MCR03 Series	29	RQ1	N.M	-
8	RTHM11	100kΩ	MCR03 Series	30	L	10μH	SLF12575T100M5R4-H
9	RTHM12	100kΩ	MCR03 Series	31	ROUTL	0Ω	MCR03
10	RTHM21	100kΩ	MCR03 Series	32	Q2	RSS070N05	-
11	RTHM22	100kΩ	MCR03 Series	33	DI2	RF201L2S	-
12	RTHM3	0Ω	-	34	COUT1	10μF	GCM32ER71E106KA42
13	TR	-	-	35	COUT2	10μF	GCM32ER71E106KA42
14	RCR1	30kΩ	MCR03 Series	36	CCT	0.1μF	GCM188R11H104KA42
15	RCR2	10kΩ	MCR03 Series	37	ROVP1	270kΩ	MCR03
16	CCR	0.22μF	GCM21BR11H224KA01	38	ROVP2	30kΩ	MCR03
17	FRL1	100kΩ	MCR03 Series	39	RLED1	90kΩ	MCR03
18	FRL2	100kΩ	MCR03 Series	39	RLED2	30kΩ	MCR03
19	CREG	10μF	GCM32ER71E106KA42	40	Q3	RSS070N0	-
20	RCS1	110mΩ	MCR100JZHFSR110	41	RQ3	N.M	-
21	RCS2	N.M	-	42	RSENSE1	200mΩ	MCR100JZHFSR510
22	RCS3	0Ω	-	43	RSENSE2	N.M	-

(Note)

- When no PWM dimming, DI2 should be a schottky diode instead of a Fast Recovery diode to improve efficiency. When dimming with External PWM signal, DISC should be pulled up to VREG with 10KΩ, then input PWM signal to VTH. (when no PWM dimming, remove Q3 and replace R_{Q3}=0Ω and short to DS)
- Efficiency improvement is possible by making DI2 a schottky Diode. However, since high temperature leakage current is large and output voltage ripple is large as well, LED may flicker when PWM dimming ratio is very low. So it is recommended to use a Fast recovery Diode.
- Values of the capacitors can be smaller than the amount that was selected by the DC bias characteristics of the capacitor when using ceramic capacitors.
- For EMI reduction, please insert resistance to ROUTL and RBOOT. It is recommended to be below 20Ω.
- The output voltage ripple is larger in Boost application than in Buck application. Hence, it is recommended to use at least 100μF output capacitor.

3. 5V Voltage Reference (VREG)

5V (Typ) is generated from the VCC input voltage when the enable pin is set high. This voltage is used to power internal circuitry, as well as the voltage source for device pins that need to be fixed to a logical HIGH. UVLO protection is integrated into the VREG pin. The voltage regulation circuitry operates uninterrupted for output voltages higher than 4.5 V (Typ), but if output voltage drops to 4.3 V (Typ) or lower, UVLO engages and turns the IC off. Connect a capacitor ($C_{REG} = 10\mu\text{F}$ Typ) to the VREG terminal for phase compensation. Operation may become unstable if C_{REG} is not connected.

4. LED Current Setting and Control Method.

(1) Method of setting the LED current

The LED current can be calculated by the following formula.

$\text{THM} \geq 1.0\text{V} \rightarrow I_{LED} = 0.2\text{V(Typ)} / R_{SET}$

$\text{THM} < 1.0\text{V} \rightarrow I_{LED} = V_{THM} / (\text{GAIN} \times R_{SET})$

(GAIN : the gain of internal AMP 5(Typ))

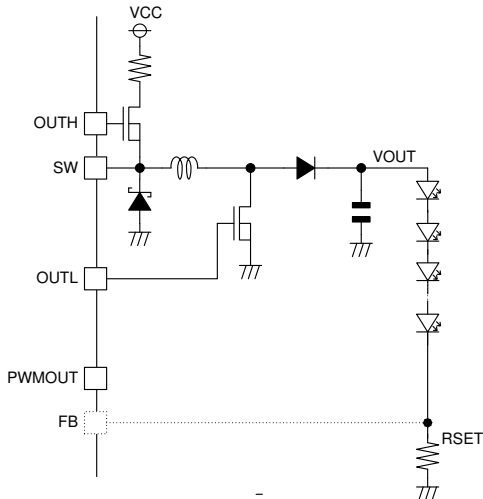


Figure 18. LED current setting block diagram

LED Current : I_{LED}
 THM terminal voltage : V_{THM}
 Resistance of LED current setting : R_{SET}

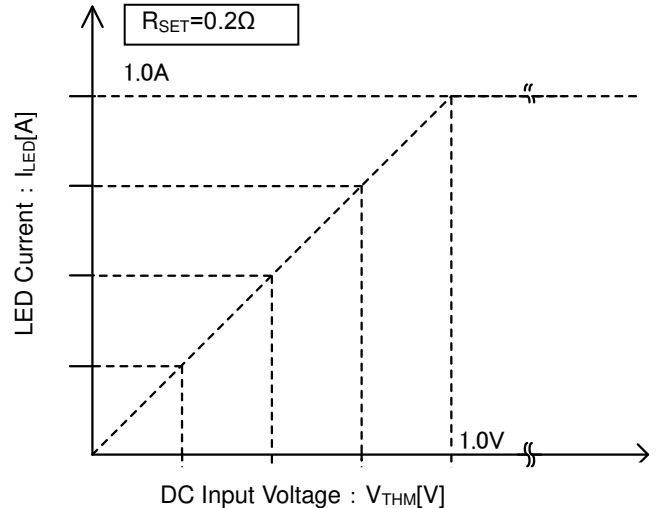
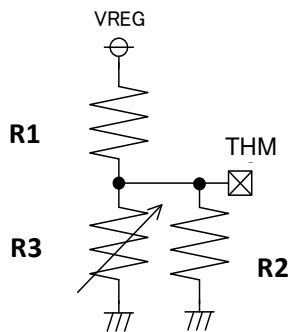


Figure 19. The LED current derating by THM terminal

(2) Linear dimming function

LED current can be controlled linearly by using the THM terminal which is commonly used as a derating function. For example, THM terminal is used when suppressing the degradation at high temperature of the LED (Figure 20) and controlling the excessive current to the external components under the conditions likely to occur in the power supply voltage fluctuations in the idling stop function. V_{THM} input range is recommended $V_{THM} \geq 0.4\text{V}$.



product	value	unit
VREG	5	V
R1	20	kΩ
R2	47	kΩ
R3	47	kΩ

R3:NTCG104BF473F

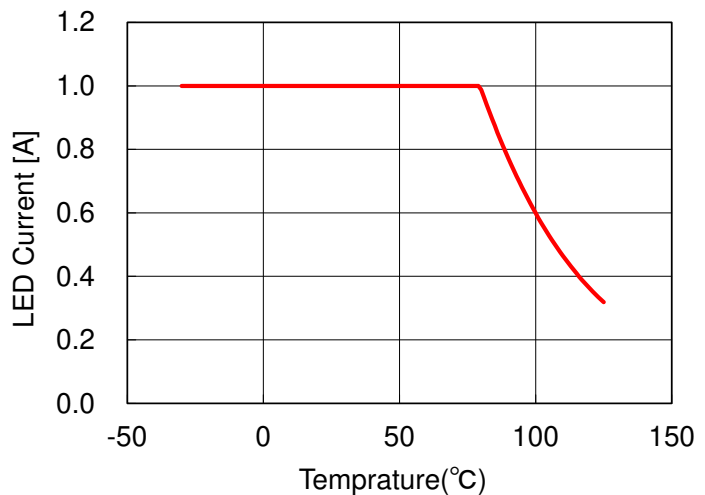
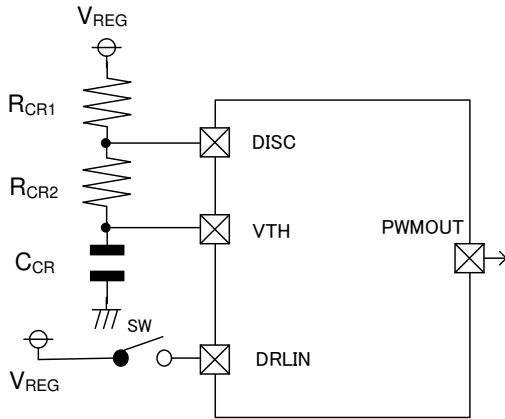


Figure 20. The derating use case with thermistor resistor.

5. Setting of CR Timer Dimming

It is possible to set the PWM frequency (f_{PWM}) and the PWM on Duty (DON) with the external resistor and capacitor by using the built-in CR timer function. This function can be used to set the Dimming range from 2% up to 45% and the frequency range from 100Hz up to 20kHz. When a Hi voltage is applied at DRLIN terminal, 100% On-Duty is outputted at the PWMOUT terminal and at the LED current, independent of the PWM signal and the CR Timer. The minimum PWM pulse width is 25 μ s.



PWMOUT

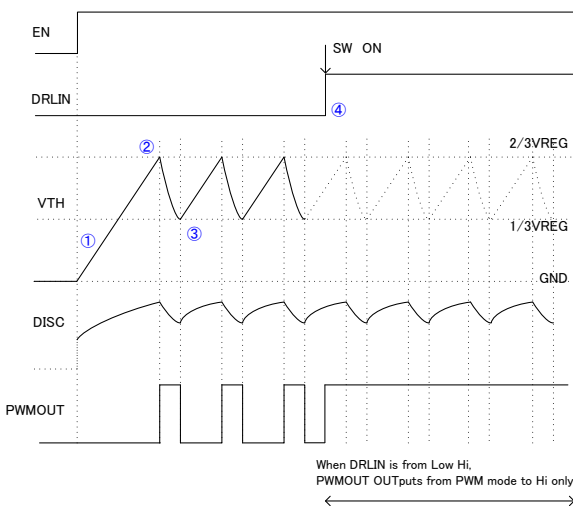
DON

PWM Frequency (f_{PWM})

$$f_{PWM} = \frac{1.44}{(R_{CR1} + 2 \times R_{CR2}) C_{CR}}$$

PWM on Duty (DON)

$$DON = \frac{R_{CR2}}{(R_{CR1} + 2 \times R_{CR2})} \times 100$$



- ① Turning on EN, VTH voltage is increased and C_{CR} starts charging.
- ②,③ C_{CR} is discharged in the DISC to 1/3VREG, when VTH voltage reaches 2/3VREG.
- ④ PWMOUT is Hi when the DRLIN is Hi.

Figure 21. The setting of PWM dimming using CR Timer and Timing chart

Synchronization of the PWM dimming signal with an external signal is possible by inputting the external signal at the VTH terminal. The Hi voltage of the external signal can be more than 3.7V and the Low voltage can be less than 1.0V.

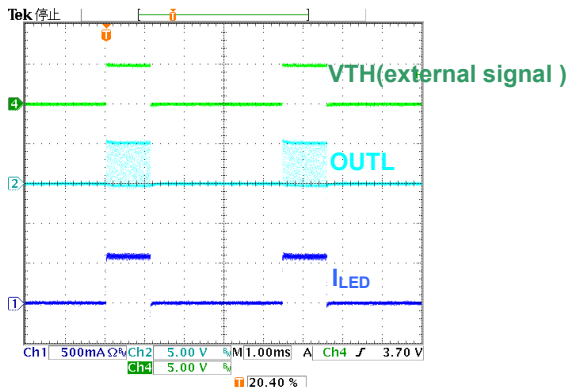


Figure 22. The waveform of PWM dimming in synchronization with an external signal

6. Relationship between PWM dimming and SCP protection

If the PWM ON-Time is short, even if it is an internal or an external PWM dimming, it will cause the rise time of the output voltage to be delayed and there is likely to have a false detection of the SCP. Figure 23 and Figure 24 indicates the relation between SCP and PWM dummng. Detail explanation of SCP is described in P.16.

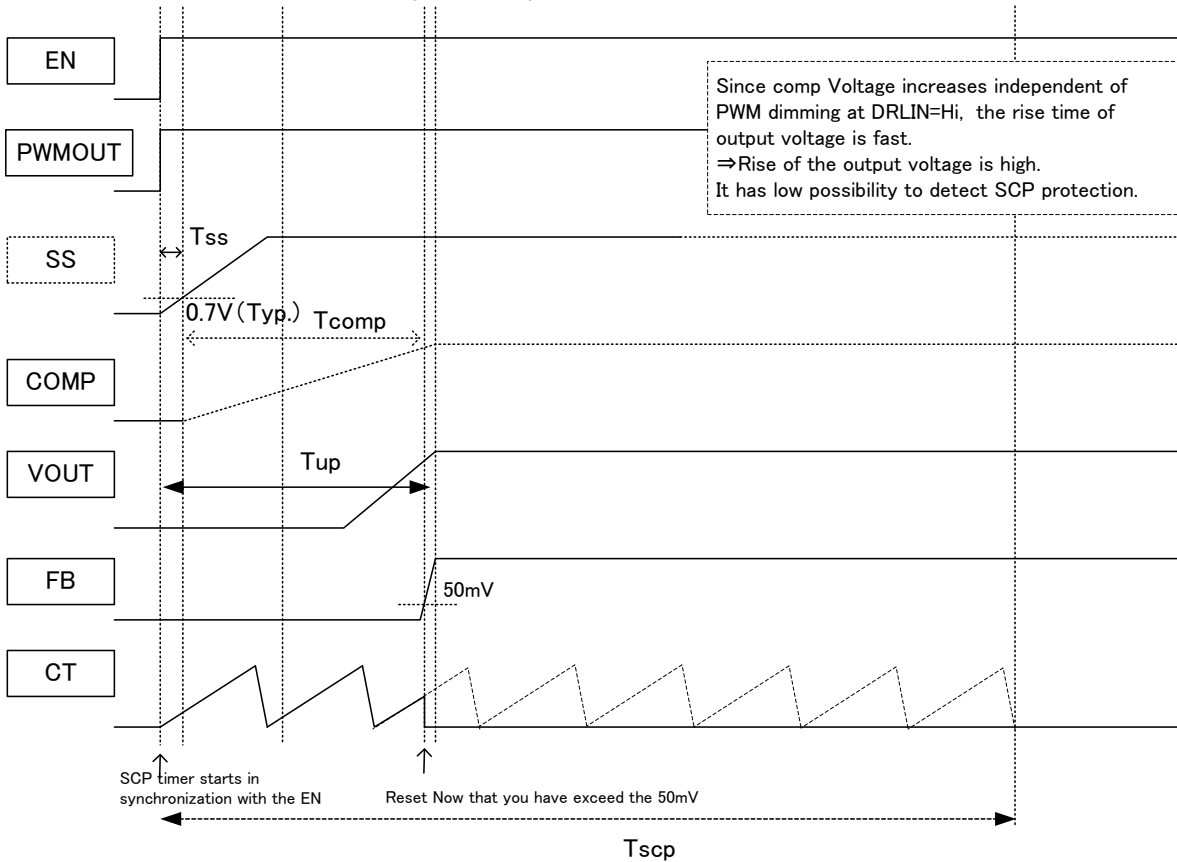


Figure 23. The relation of the output voltage rise time and SCP protection (not at PWM 100% dimming)

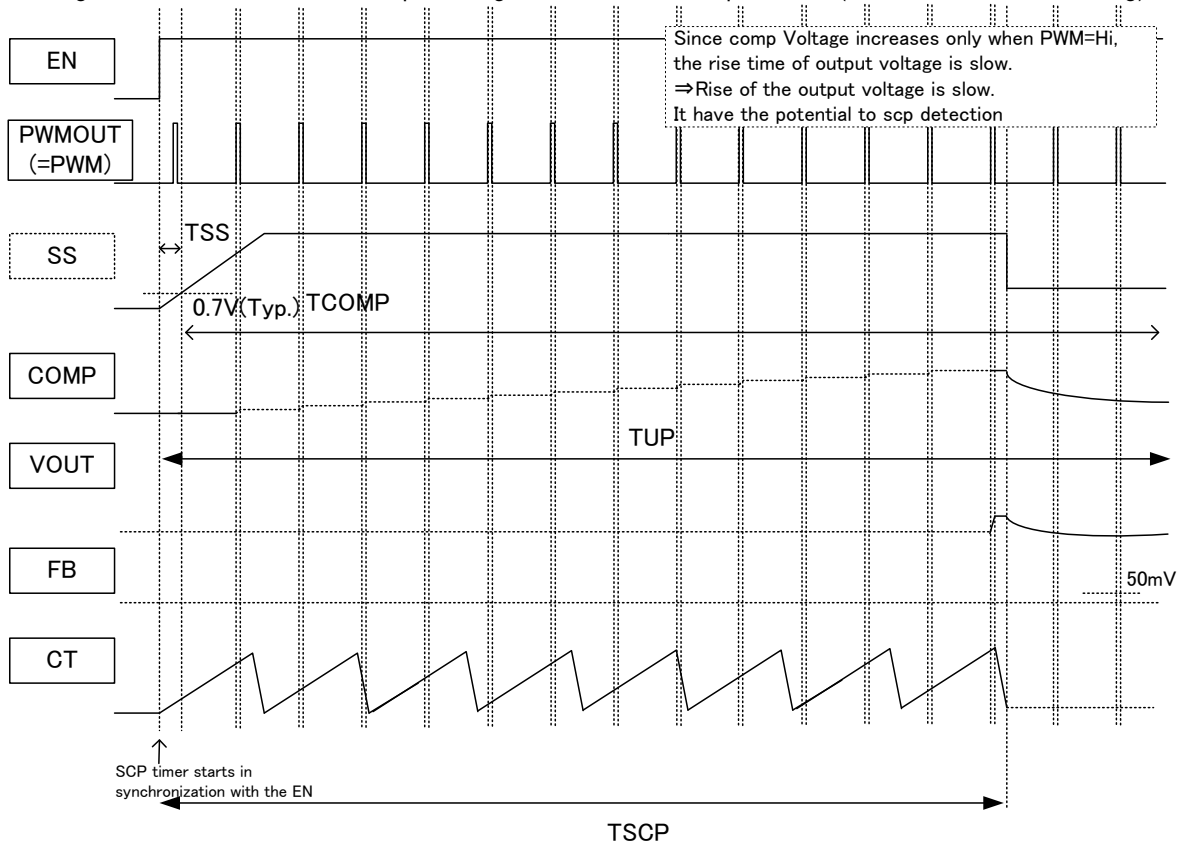


Figure 24. The relation of the output voltage rise time and SCP protection (at PWM dimming)

The rise time of the output voltage at PWM dimming is calculated as follows. The COMP voltage starts to increase when PWM=Hi and the switching output of the DC/DC circuit depends on the C_{PC} capacitor connected at the COMP terminal. It also affects the soft start time during start-up to prevent the rush current. (Refer to P.15 for more details.)

Based on the above explanation, the time (t_{UP}) it takes for the output voltage to reach the steady state level is calculated as follows.

$$t_{UP} = t_{SS} + t_{COMP}$$

$$t_{SS} = \frac{V_{SWST}[V] \times C_{SS}[\mu F]}{I_{SS}[\mu A]}$$

$$t_{COMP} = \frac{V_{SWMAX}[V] \times C_{PC}[\mu F]}{I_{COMPSOURCE}[\mu A]} \times \frac{1}{DON}$$

Rise Time of COMP voltage : t_{COMP}
 COMP source current : $I_{COMPSOURCE}$
 Capacitor of COMP : C_{PC}
 Soft start time : t_{SS}
 SS Charged current : I_{SS}
 Capacitor of SS : C_{SS}
 PWM Dimming rate : DON
 Soft start release voltage 0.85V (Max) : t_{SWST}
 MaxDuty output voltage 2.0V (Max) : V_{SWMAX}

During the rise time of the output voltage which is calculated above, SCP detection starts the timer operation which is synchronized with EN. If the PWM dimming ratio is low and the rise time of output voltage is delayed, there is a possibility for a false detection of SCP.

Ex)

The condition that
 $I_{COMPSOURCE}=75\mu A, C_{PC}=0.1\mu F, I_{SS}=5\mu A, C_{SS}=0.1\mu F,$
 $DON=5\%$ are $t_{SS}=17ms, t_{COMP}=53.3ms.$
 So, t_{UP} is about 60ms

From the above, when using the PWM dimming, it must establish the below relationship. (t_{SCP} indicates the SCP mask time. It indicates P.16 in detail.)

$$t_{UP} < t_{SCP}$$

As a reference, it is recommended that $1.2 \times t_{UP} < t_{SCP}$.

There is a need to reduce C_{PC} or C_{SS} in order to achieve fast rise time. If the C_{SS} is decreased, the overshoot of the output voltage increases as the inrush current increases. On the other hand, if the C_{PC} is decreased, the phase margin becomes unstable due to the failure to start at the right timing when the recommended range of $1.2 \times t_{UP} < t_{SCP}$ is not met. Also, always confirm that, CT terminal is connected to GND. The power supply voltage VCC after applying a PWM signal input, please input always earlier than the EN control signal when used in external input PWM as stated in P.19.

7. DC/DC controller

(1) Over-voltage protection circuit (OVP)

The output of the DCDC converter should be connected to the OVP pin via a voltage divider. In determining the appropriate trigger voltage of the OVP block, consider the total number of LEDs in series and the maximum V_F variation. The OVP terminal voltage, V_{OVP} is recommended to be in the range of $1.2V < V_{OVP} < 1.4V$ during normal operation. If V_{OVP} is not at the normal operating range, it is possible to detect LED open protection. And the role of the OVP function is for the protection of the half-short mode of FB terminal short ($V_{FB} \approx 0.1V$).

(2) DC/DC converter oscillation frequency (f_{osc})

The regulator's internal triangular wave oscillation frequency can be set via a resistor connected to the RT pin (pin 5). This resistor determines the charge/discharge current to the internal capacitor, thereby changing the oscillation frequency. Refer to the following theoretical formula when setting RT:

$$f_{osc} = \frac{60 \times 10^6}{R_{RT}[\Omega]} \times \alpha \text{ [kHz]}$$

60×10^6 (V/A/S) is a constant ($\pm 5\%$) determined by the internal circuitry, and α is a correction factor that varies in relation to RT: (RT: $\alpha = 100k\Omega: 1.0, 150k\Omega: 0.99, 200k\Omega: 0.98, 280k\Omega: 0.97$)

A resistor in the range of $100k\Omega$ to $280k\Omega$ is recommended. Settings that deviate from the frequency range shown below may cause switching to stop, causing the device operation to be unstable.

Please consider the parasitic capacitance of RT terminal at PCB board design. It must be less than $50pF$.

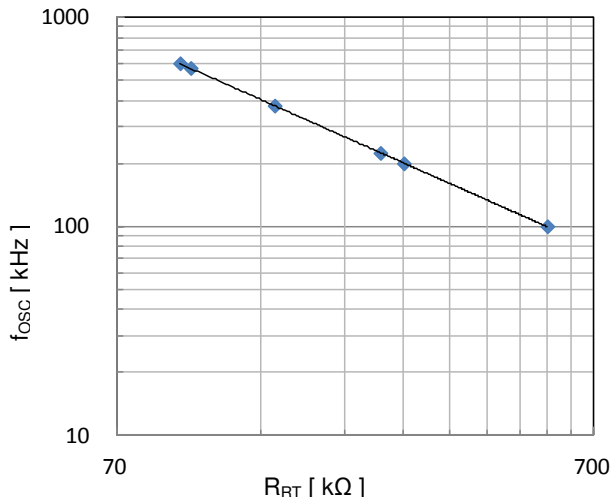


Figure 25. f_{osc} vs R_{RT}

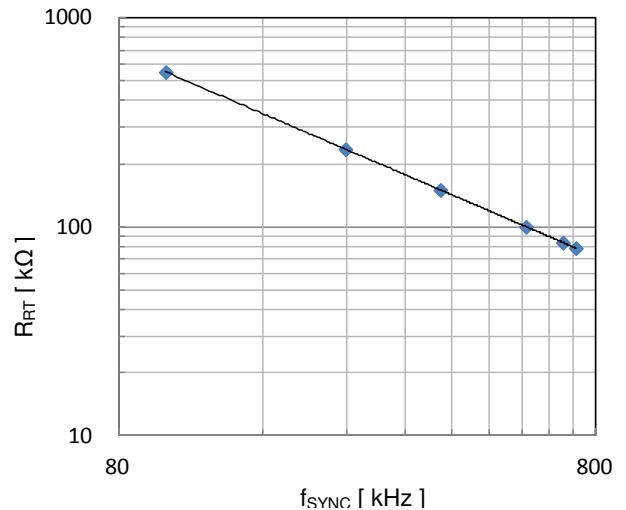


Figure 26. R_{RT} vs f_{SYNC}

(3) External DC/DC converter oscillation frequency synchronization (f_{sync})

Please do not switch from external to internal oscillation of the DC/DC converter if an external synchronization signal is present on the SYNC pin. When the signal on the SYNC terminal is switched from high to low, a delay of about $30 \mu s$ (typ) occurs before the internal oscillation circuit starts to operate (only the rising edge of the input clock signal on the SYNC terminal is recognized). Consider that; if the external sync is already running and is switched to internal synchronization from external synchronization. It may cause the output voltage overshoot and erroneous open detection may occur.

In addition, whenever an external synchronization is used, please set the R_{RT} such that the external synchronization frequency is $f_{sync} < f_{osc} \times 1.2$.

(4) Soft Start Function

The soft-start (SS) limits the current and slows the rise-time of the output voltage during the start-up, and hence leads to the prevention of the overshoot of the output voltage and the inrush current. The SS voltage is Low when the OCP and the OVP is detected. Switching is stopped and operation is resumed.

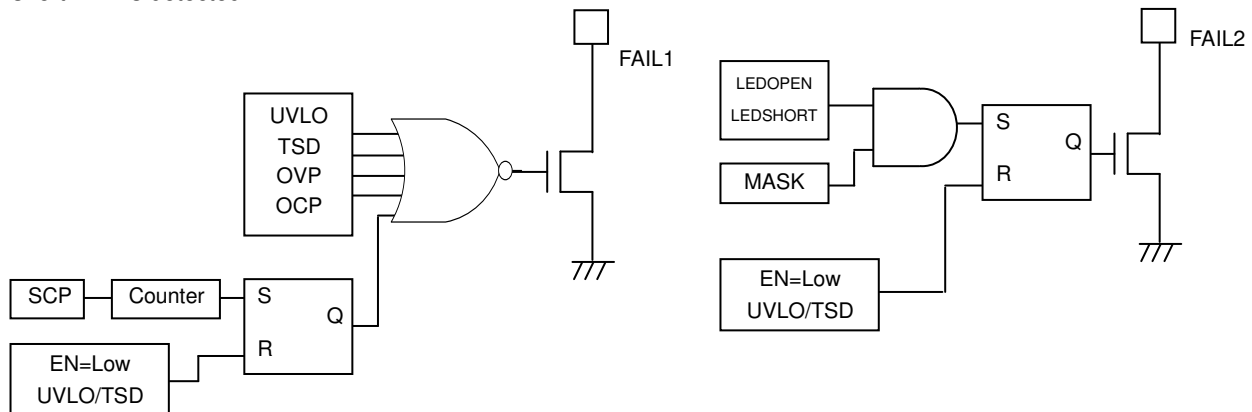
t_{SS} (soft-start time) is calculated using the formula below. Please refer to P.23 for more detailed application of the setting method.

$$t_{SS} = \frac{V_{SWST}[V] \times C_{SS}[\mu F]}{I_{SS}[\mu A]}$$

Soft start time: t_{SS}
 Soft start charge current $5\mu A$ (Typ): I_{SS}
 Capacitor of SS: C_{SS}
 Soft start release voltage $0.85V$ (Max): V_{SWST}

(5) Self-diagnostic functions

The operating status of the built-in protection circuit is propagated to FAIL1 and FAIL2 pins (open-drain outputs). FAIL1 becomes low when UVLO, TSD, OVP, OCP, or SCP protection is engaged, whereas FAIL2 becomes low when open or short LED is detected.

**(6) Operation of the Protection Circuit****(a) Under-Voltage Lock Out (UVLO)**

The UVLO shuts down all the circuits except for VREG when $V_{CC} \leq 4.3V$ (TYP).

(b) Thermal Shut Down (TSD)

The TSD shuts down all the circuits except for REG when the T_j reaches $175^\circ C$ (TYP), and releases when the T_j becomes below $150^\circ C$ (TYP).

(c) Over Current Protection (OCP)

The OCP detects the current through the power-FET by monitoring the voltage of the high-side resistor and activates when the CS voltage becomes less than $V_{CC}-0.6V$ (TYP). When the OCP is activated, the external capacitor of the SS pin will discharge and the switching operation of the DCDC turns off.

(d) Over Voltage Protection (OVP)

The output voltage of the DCDC is detected with the OVP-pin voltage and the protection activates when the OVP-pin voltage becomes greater than $2.0V$ (TYP). When the OVP is activated, the external capacitor of the SS pin will discharge and the switching operation of the DCDC turns off.

(7) Short Circuit Protection (SCP) (Following Figure 36 in P.21)

SCP is independent from PWM dimming. When the FB-pin voltage becomes less than $0.05V$ (TYP), the internal counter starts operating and latches off the circuit approximately after 150ms (when $C_{CT} = 0.1\mu F$). If the FB-pin voltage becomes over $0.05V$ before 150ms, then the counter resets. When the LED anode (i.e. DCDC output voltage) is shorted to ground, the LED current turns off and the FB-pin voltage becomes low. Furthermore, the LED current also turns off when the LED cathode is shorted to ground. Hence in summary, the SCP works in both cases when the LED anode and the LED cathode is being shorted.

SCP mask timer (t_{SCP}) can be calculated using the following expression.

$$t_{SCP} = \frac{C_{CT}[\mu F] \times V_{CT}[V]}{I_{CT}[\mu A]} \times 8count$$

SCP mask timer : t_{SCP} CT charge current $5\mu A$ (Typ) : I_{CT} Capacitor of CT : C_{CT} CT terminal Voltage $0.8V$ (Typ) : V_{CT}

The need for SCP varies depending on the application. The OCP is detected and limited by High side SW, when the output is shorted to GND in the Buck / Buck-Boost application. Since the current continues to flow continuously, set the SCP timer to stop after an error is detected. On the other hand, the current path can not be cut off and large current continues to flow in the Boost application because there is no High side SW in Buck / Buck-Boost application. Therefore, please mask the SCP function in boost application. (CT terminal short to GND)

(8) LED Open Detection(Following Figure 34 in P.20)

When the FB-pin voltage $< 50mV$ (TYP) as well as OVP-pin voltage $\geq 1.7V$ (TYP) operates in these ranges, the device detects LED open and latches off that particular channel.

(9) LED Short Detection(Following Figure 35 in P.20)

Less brightness of the light source will be produced whenever one LED is shorted somewhere within the load. If the guaranteed luminance of the light source is required, detection of the failure in the circuit must be performed. LED short detection is activated whenever one of the LEDs in the circuit, is shorted. In case of a short circuit, problem of LED short detection is informed. When one of the LEDs used is shorted somewhere in the circuit, $|LEDR-LEDC| \geq 0.2$ (TYP), the internal counter starts operating, and approximately after 100ms (when $f_{OSC} = 300$ kHz) the operation latches off. With the PWM brightness control, the detection operation only proceeds when PWM=Hi. If the condition of the detection operation is released before 100ms (when $f_{OSC} = 300$ kHz), then the internal counter resets.

$$t_{SHORT} = 1 / f_{OSC} \times 32770 / DON$$

LED short timer : t_{SHORT}
 DC/DC oscillator frequency : f_{OSC}
 PWM dimming ratio : DON

There is a possibility that the LED short detection malfunctions when the difference of V_F is large. Therefore, please adjust external resistance connected for V_F . It is recommended to be 1V-3V of the input voltage range of LEDR and LEDC.

(Note) The counter frequency is the DCDC switching frequency determined by the RT. The latch proceeds at the count of 32770.

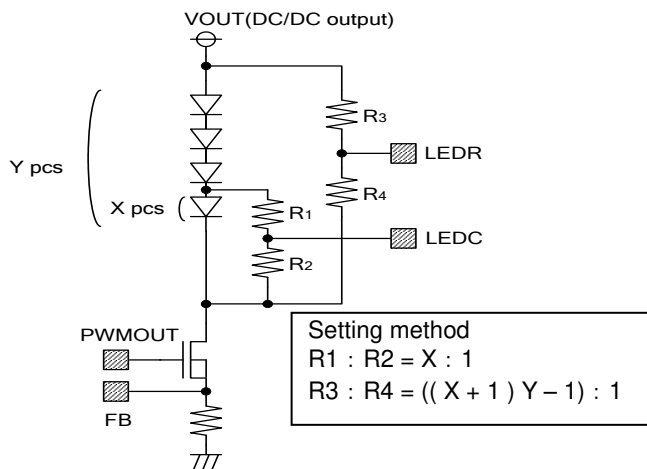


Figure 27. High luminance LED (multichip) when using Y piece

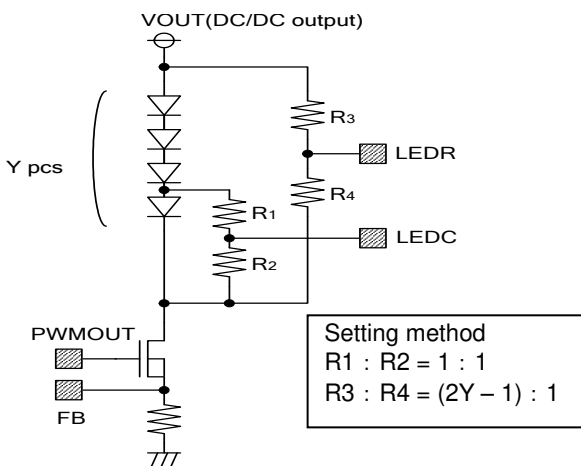


Figure 28. When using the single chip (White LED)

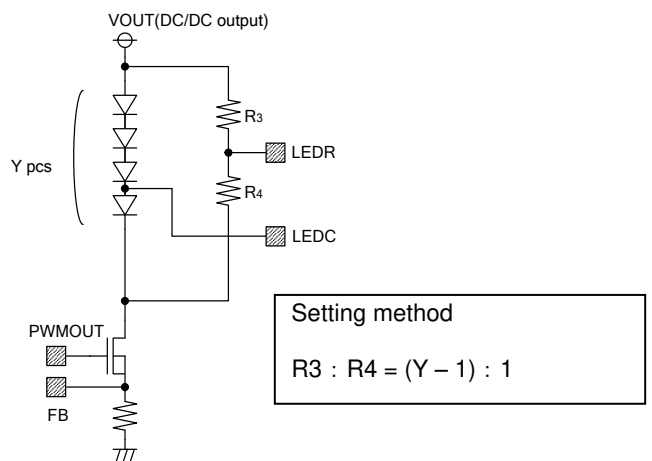


Figure 29. When using the Low V_F LED as Red LED

8. Error all condition

Protection	Detecting Condition		Operation after detect
	[Detect]	[Release]	
UVLO	$V_{CC} < 4.35V$	$V_{CC} > 4.5V$	All blocks (but except VREG) shut down
TSD	$T_j > 175^{\circ}C$	$T_j < 150^{\circ}C$	All blocks (but except VREG) shut down
OVP	$V_{OVP} > 2.0V$	$V_{OVP} < 1.45V$	SS discharged
OCP	$V_{CS} \leq V_{CC} - 0.6V$	$V_{CS} > V_{CC} - 0.6V$	SS discharged
SCP	$V_{FB} < 0.05V$ (150ms delay when $C_{CT} = 0.1\mu F$)	EN or UVLO	Counter starts and then latches off all blocks (but except REG)
LED open	$V_{FB} < 0.05V$ & $V_{OVP} > 1.7V$	EN or UVLO	Counter starts and then latches off all blocks (but except REG)
LED short	$I_{VLEDR} - V_{LEDCI} \geq 0.2V$ (100ms delay when $f_{OSC} = 300kHz$)	EN or UVLO	Counter starts and then latches off all blocks (but except REG)

9. Effectiveness of the protection of each application

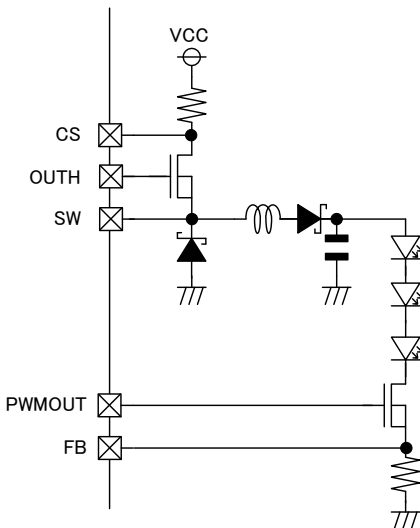


Figure 30. Buck Application

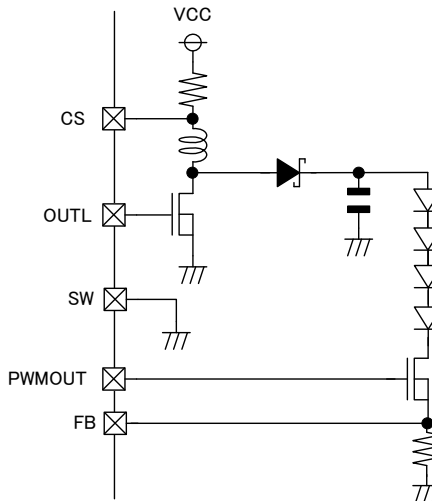


Figure 31. Boost Application

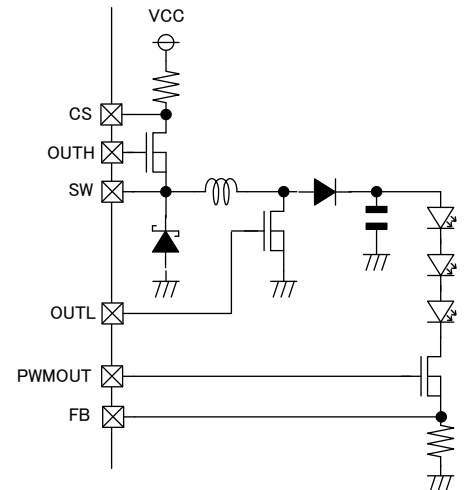


Figure 32. Buck-Boost Application

PROTECTION	DC/DC Application		
	Buck	Boost	Buck-Boost
UVLO	✓	✓	✓
OCP	✓	✓	✓
OVP	✓	✓	✓
DC/DC Output short GND detection	✓	Note1	✓
LED short detection	✓	✓	✓
LED Open detection	✓	✓	✓
LED Anode/Casode short detection	Note2	Note2	Note2

Note1 : When the DC/DC output is shorted to GND using Boost application, there is a possibility of high current flow which lead to the destruction of the external components. For the reduction of current in the external components, CT terminal is connected to GND.

Note2 : LED doesn't light when LED is shorted between anode and cathode. Under shorting LED, when using Buck/Buck-Boost application, may cause the large current not to flow while when using Boost application, there is a large current flowing from VCC to GND.

10. Power supply turning on sequence

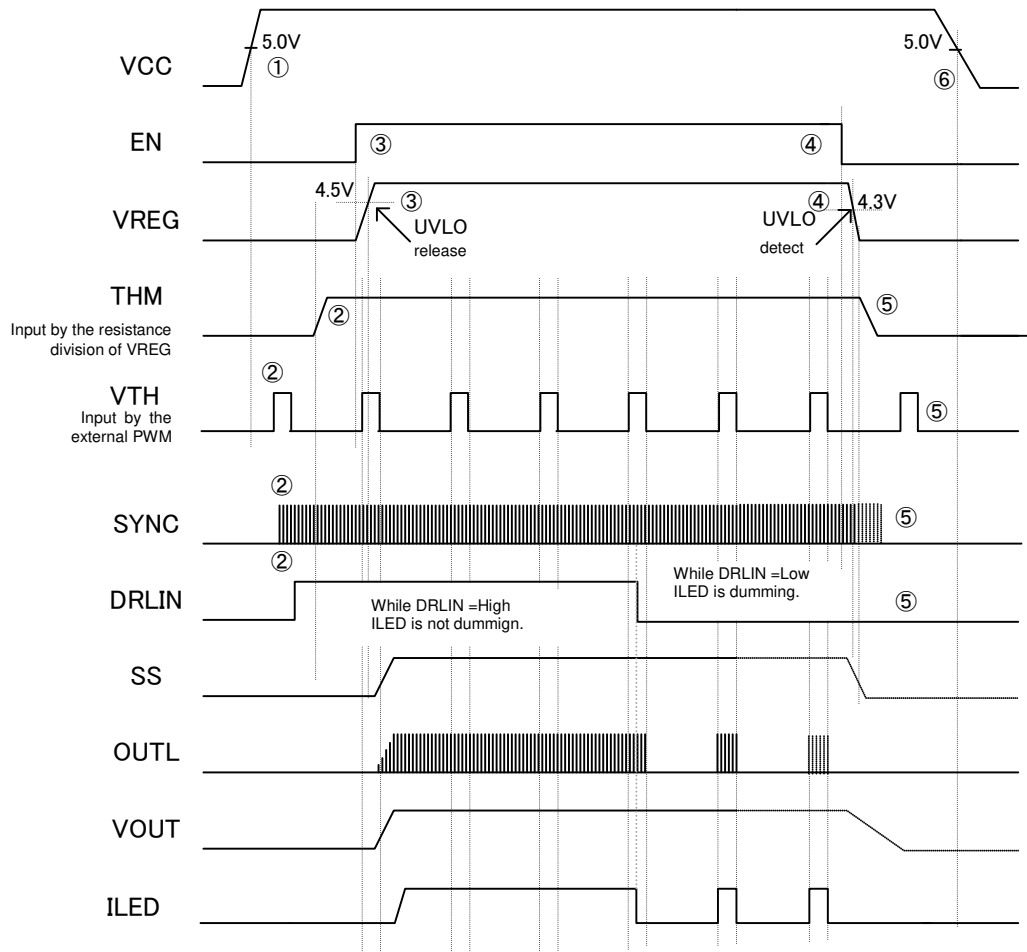


Figure 33

Power supply turning on sequence

- ① After becoming $V_{CC} > 5V$, the input of the other signals is possible.
- ② Before EN inputs, please fix VTH, THM, DRLIN, SYNC terminal voltage. An input order is not related.
- ③ VREG rises simultaneously with the input of EN, UVLO protection releases and switching starts.
- ④ VREG falls simultaneously with EN=Off.
- ⑤ Please stop input signal of VTH, THM, DRLIN, SYNC terminal voltage. An input order is not related.
- ⑥ VCC is OFF.

Note: It leads to the destruction of IC and external parts because it doesn't error output according to an external constant of adjacent pin 24pin SW terminal, 25pin OUTH terminal, 26pin CS terminal and 27pin BOOT terminal.

11. Operation in error circumstances of LED

(1) LED open detection

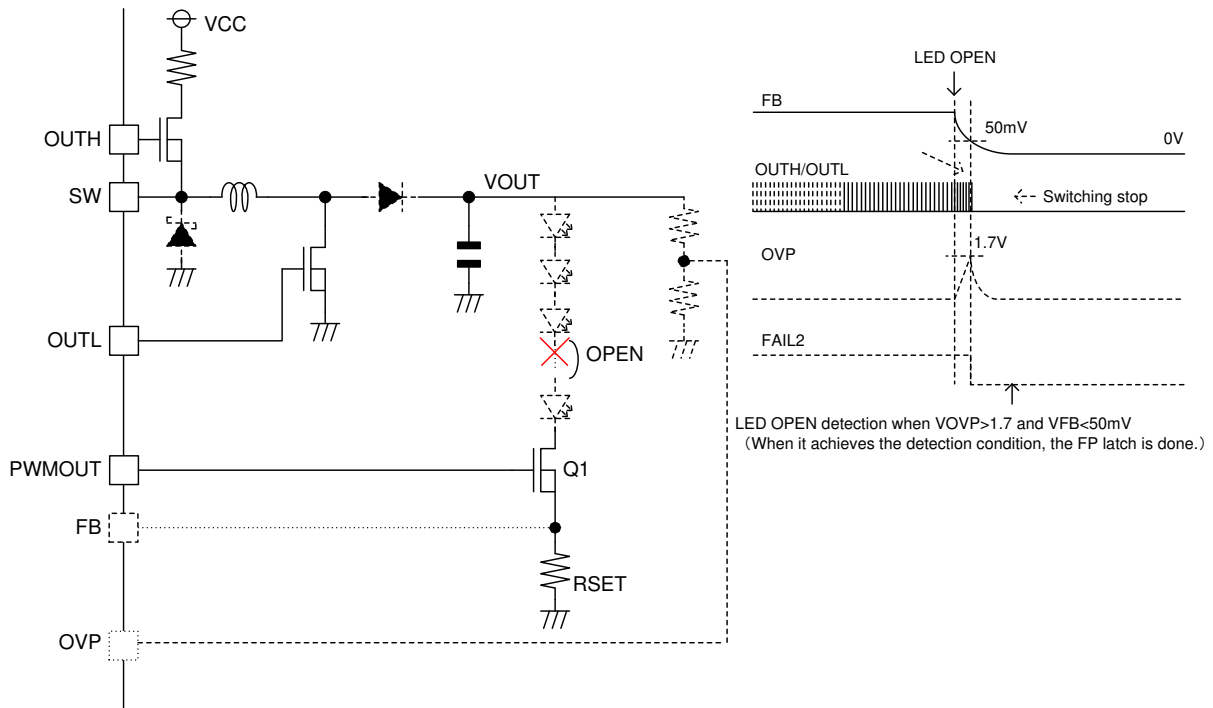


Figure 34

(2) LED short detection

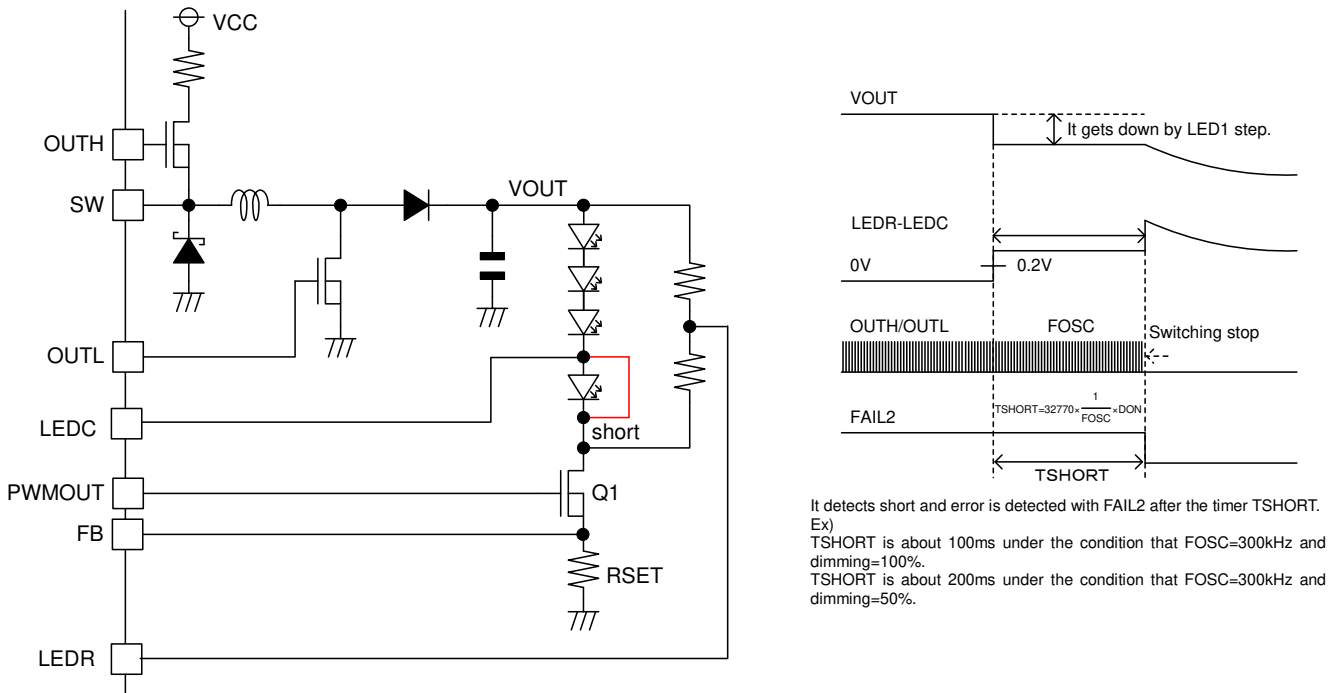


Figure 35

(3) LED anode short to GND detection

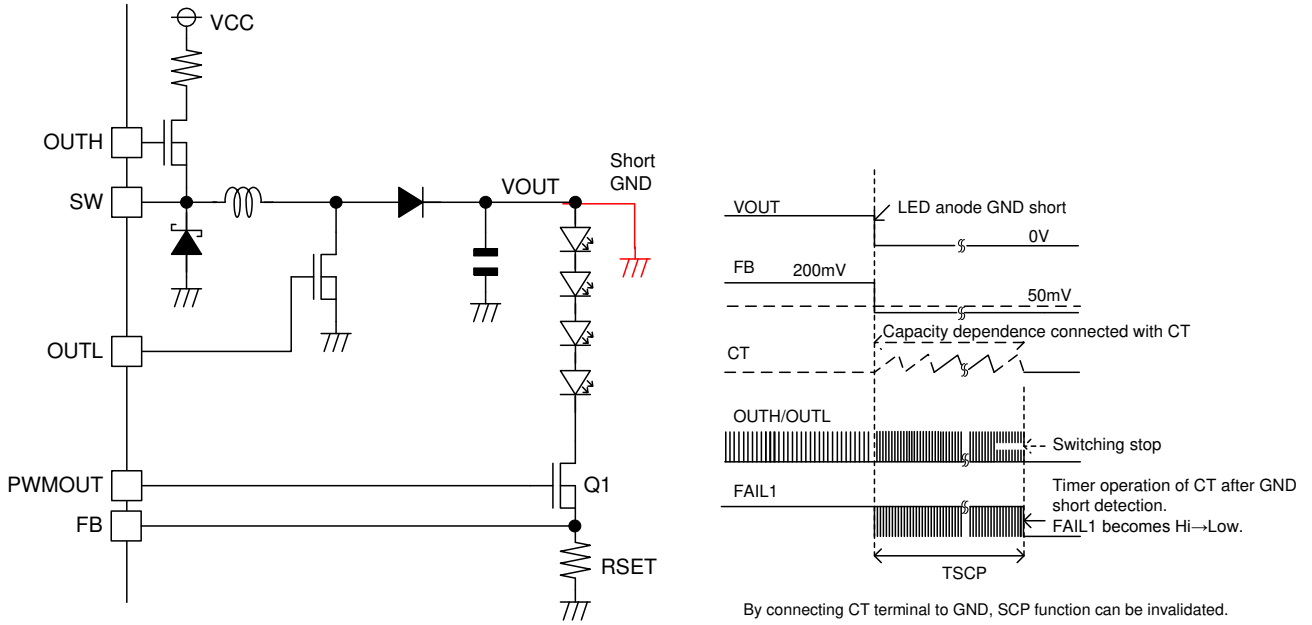
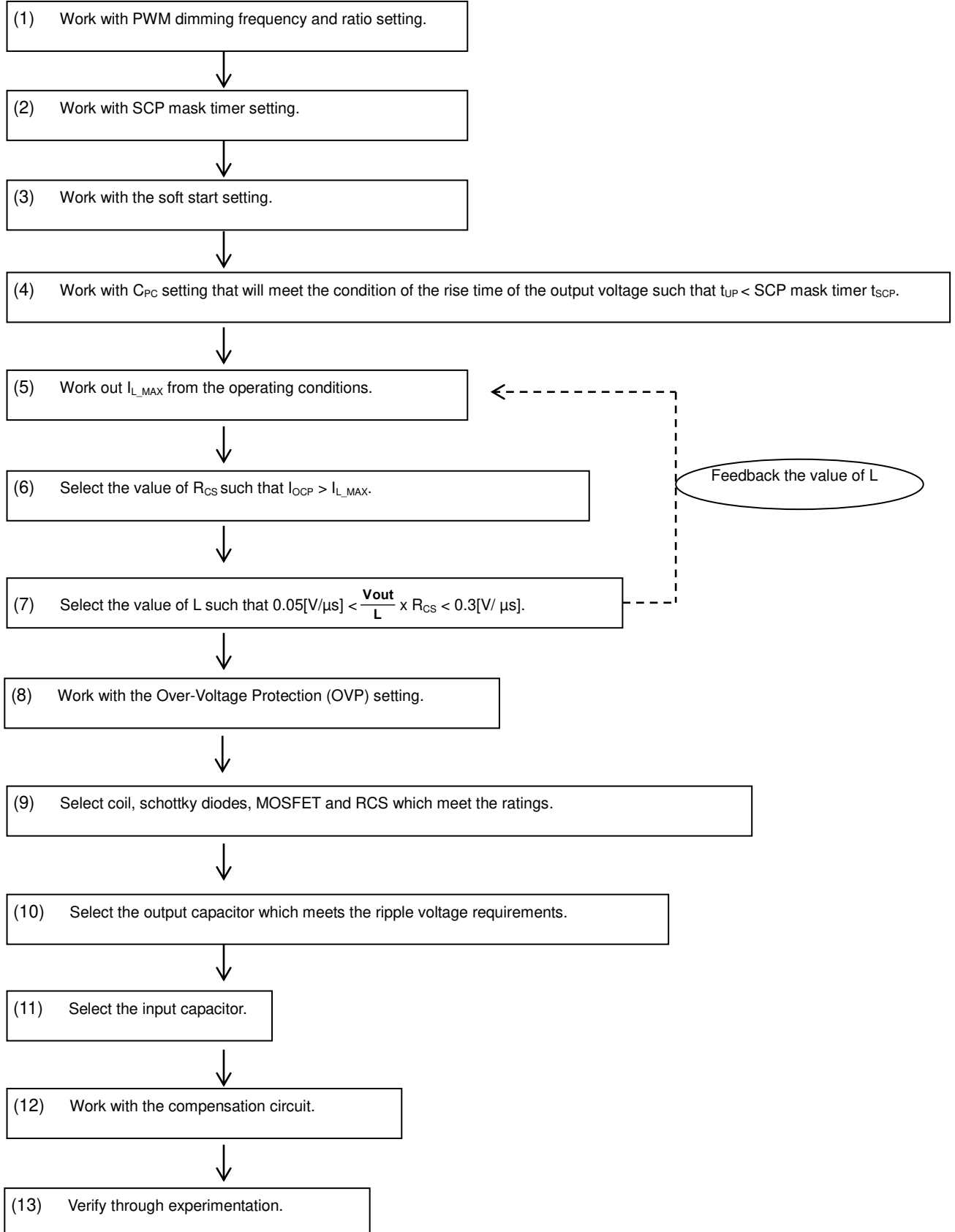


Figure 36

Note: When GND short-circuits by the DC/DC output by Boost application, high current flows and may lead to the destruction of external parts. The boost application does not enable the GND short protection of the DC/DC output.

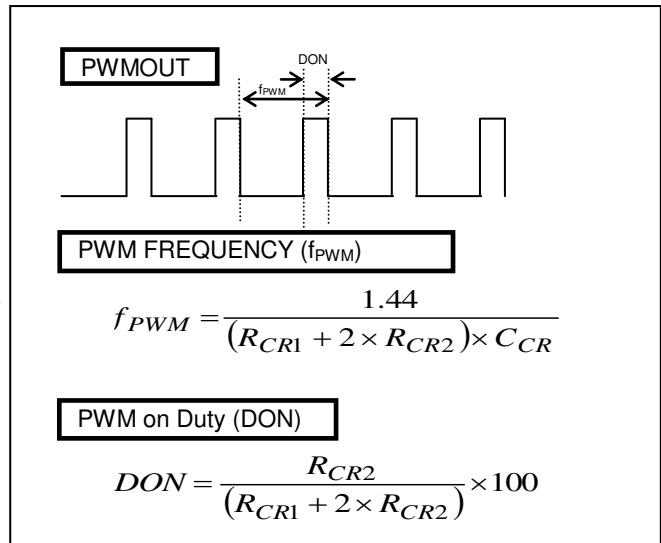
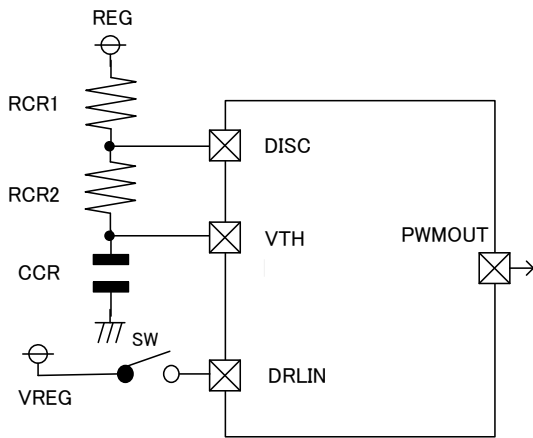
12. Procedure for external components selection

Follow the steps as shown below in selecting the external components



(1) PWM dimming frequency and ratio setting

It is possible to set the PWM frequency (f_{PWM}) and the PWM on Duty (DON) in the external resistor and capacitor using the built-in CR timer function.



(2) SCP mask timer setting

SCP mask timer (t_{SCP}) is determined by the CT terminal capacitor which is calculated using the following expression.

$$t_{SCP} = \frac{C_{CT}[\mu F] \times V_{CT}[V]}{I_{CT}[\mu A]} \times 8count$$

SCP mask timer : t_{SCP}
CT charge current $5\mu A$ (Typ) : I_{CT}
Capacitor of CT : C_{CT}
CT terminal Voltage $0.8V$ (Typ) : V_{CT}

In the P.14, when LED number is large or PWM dimming ratio is low, it may not satisfy the relational formula which has been described in P.14. Please connect CT terminal to GND in case the relational formula is not satisfied.

(3) Setting of the soft-start

The soft-start allows the coil current as well as the overshoot of the output voltage at the start-up to be minimized. For the capacitance, it is recommended to be in the range of $0.001\mu F \sim 0.1\mu F$. If the capacitance is less than $0.001\mu F$, it may cause an overshoot on the output voltage while if the capacitance is greater than $0.1\mu F$, it may cause massive reverse current through the parasitic elements of the IC and may damage the whole device.

$$t_{SS} = \frac{V_{SWST}[V] \times C_{SS}[\mu F]}{I_{SS}[\mu A]}$$

(4) C_{PC} setting that meets the condition of the rise time of the output voltage such that t_{UP} < SCP mask timer t_{SCP}

The rise time of the output voltage (t_{UP}) can be calculated using the following formula.

$$t_{UP} = t_{SS} + t_{COMP}$$

$$t_{COMP} = \frac{V_{SWMAX}[V] \times C_{PC}[\mu F]}{I_{COMPSOURCE}[\mu A]} \times \frac{1}{DON}$$

Rise Time of the COMP voltage : t _{COMP} COMP source current : I _{COMPSOURCE} Capacitor of COMP : C _{PC} PWM Dimming rate : DON MaxDuty output voltage 2.0V (Max) : V _{SWMAX}

Please adjust C_{PC} and C_{CT} to satisfy the following relationship.

$$t_{UP} < t_{SCP}$$

For a guide, it is recommended that $1.2 \times t_{UP} < t_{SCP}$.

If the above formula is not satisfied, failure in the activation of the SCP may occur regardless of which application. So it is important to connect CT terminal to GND to prevent the false detection of SCP protection circuit.

(5) I_{L_MAX} from the operating conditions.**(a) Calculation of the maximum output voltage (V_{OUT})**

To calculate the V_{OUT}, it is necessary to take into account the V_F variation and the number of LEDs connected in series connection.

$$V_{OUT} = (V_F + \Delta V_F) \times N + V_{REF} + R_{PWMON} \times I_{OUT}$$

(b) Calculation of the output current I_{LED}

$$I_{LED} = \frac{V_{REF}}{R_{SET}}$$

(c) Calculation of the input peak current I_{L_MAX}**Buck-Boost**

$$I_{L_MAX} = I_{L_AVG} + 1/2 \Delta I_L$$

$$I_{L_AVG} = (V_{CC} + V_{OUT}) \times I_{LED} / (\eta \times V_{CC})$$

$$\Delta I_L = \frac{V_{CC}}{L} \times \frac{1}{f_{OSC}} \times \frac{V_{OUT}}{V_{CC} + V_{OUT}}$$

V _F of LED : V _F V _F distribution : ΔV _F Series of LED : N DC/DC feedback Ref voltage 0.2V (Typ) : V _{REF} ON Resistance of PWM dimming : R _{PWMON} LED current : I _{LED} PWM dimming ratio : DON Resistance of LED current setting : R _{SET} Coil max current : I _{L_MAX} Coil average current : I _{L_AVG} Ripple current : ΔI _L Power supply voltage : V _{CC} Output voltage : V _{OUT} Efficiency : η DC/DC Frequency : f _{OSC}

Boost

$$I_{L_MAX} = I_{L_AVG} + 1/2 \Delta I_L$$

$$I_{L_AVG} = V_{OUT} \times I_{LED} / (\eta \times V_{CC})$$

$$\Delta I_L = \frac{V_{CC}}{L} \times \frac{V_{OUT} - V_{CC}}{V_{OUT}} \times \frac{1}{f_{OSC}}$$

Buck

$$I_{L_MAX} = I_{L_AVG} + 1/2 \Delta I_L$$

$$I_{L_AVG} = I_{LED}$$

$$\Delta I_L = \frac{V_{OUT}}{L} \times \frac{V_{CC} - V_{OUT}}{V_{OUT}} \times \frac{1}{f_{OSC}}$$

- The worst case scenario for V_{CC} is when it is at the minimum, and thus the minimum value should be applied in the equation.
- The L value of 6.8μH to 33μH is recommended. The current-mode type of DC/DC conversion is adopted for BD8381AEFV-M, which is optimized with the use of the recommended L value in the design stage. This recommendation is based upon the efficiency as well as the stability. The L values outside this recommended range may cause irregular switching waveform and hence deteriorate stable operation.
- η (Efficiency) is approximately 80% in Buck-Boost application and approximately 90% in Buck / Boost application.

(6) The setting of over-current protection

Choose R_{CS} using the formula $V_{OCP_MIN} (= 0.52V) / R_{CS} > I_{L_MAX}$. When investigating the margin, please note that the L value may vary by approximately ±30%. And $I_{OCP_MAX} = V_{OCP_MAX} (0.68V) \div R_{CS}$.

(7) The selection of the L

In order to achieve stable operation of the current-mode DC/DC converter, we recommend selecting the L value in the ranges indicated below:

Buck/Buck-Boost

$$0.05 [V / \mu s] < \frac{V_{OUT} \times R_{CS}}{L} < 0.3 [V / \mu s]$$

Boost

$$0.05 [V / \mu s] < \frac{(V_{OUT} - V_{CC}) \times R_{CS}}{L} < 0.3 [V / \mu s]$$

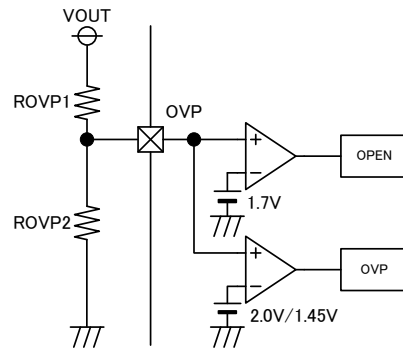
Stability will be greatly increased by reducing the calculated value but there is also a possibility that the response will be lowered.

(8) The setting of OVP voltage

It is recommended that OVP terminal voltage is set from 1.2V to 1.4V. When $V_{OVP} < 1.2V$, it is necessary that the external components are in high voltage ratings.. When $V_{OVP} > 1.4V$, there is a possibility that LED open protection may malfunction and by determining R_{OVP1} and R_{OVP2} , V_{OUT_MAX} can be calculated using the following formula.

$$V_{OUT_OVPMAX} = \frac{R_{OVP1} [k\Omega] + R_{OVP2} [k\Omega]}{R_{OVP2} [k\Omega]} \times V_{OVP}$$

Output voltage at OVP detection : V_{OUT_OVPMAX}
 OVP resistance : R_{OVP1}, R_{OVP2}
 OVP detection voltage 2.1V (MAX) : V_{OVP}



$$1.2V < \frac{V_{OUT}}{R_{OVP1} + R_{OVP2}} \times R_{OVP} < 1.4V$$

Figure 37. The circuit of OVP terminal