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Battery Charger IC Series

Boost DC/DC Charger With Input Current Limiter

BD8664GW BD8665GW BD8668GW

General Description

BD8664GW, BD8665GW and BD8668GW are lithium-ion battery charger IC's, suitable for charging 2S batteries from a 5V source, such as a USB port with DC/DC boost topology.

Features

- CP/CV Charging
- Charge-On/ Off control available with EN pin
- Integrated Input Detection (VBUSOK)
- Integrated Power Good
- Boost Switching Topology
- Low Ron integrated MOSFET
- Output Short Circuit Protection
- 0.4mm pitch Chip Scale Package (UCSP75M2)

Applications

DVC, DSC, MID and other Lithium battery-powered portable devices

Key Specifications

- Input Current Accuracy ±2%(BD8664GW)
  ±3%(BD8665GW/BD8668GW)
- Charging Voltage Accuracy ±0.5%
- Selectable Input Current
  100mA/500mA/900mA/1500mA (max)
- Charging frequency 1MHz (typ)
- Input Standby Current 71μA(typ)
- battery leakage current while charging is off 0μA(typ)

Package

W(Typ) x D(Typ) x H(Max)

UCSP75M2 2.20mm x 2.20mm x 0.85mm

Line Up

Charge Voltage	Package	Pin number	Orderable Part Number
8.30V	USCP75M2	20	BD8664GW
8.40V			BD8665GW
		25	BD8668GW

Typical Application Circuit

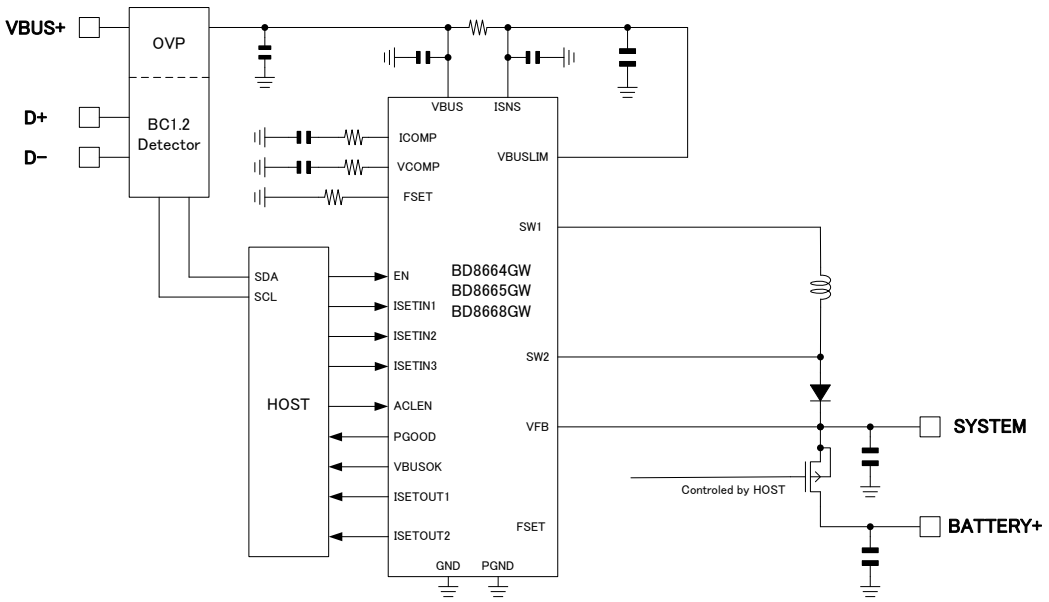


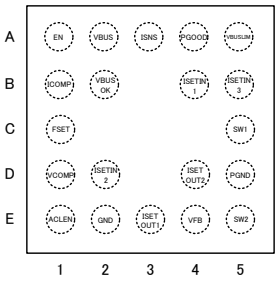
Figure 1. Typical Application

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

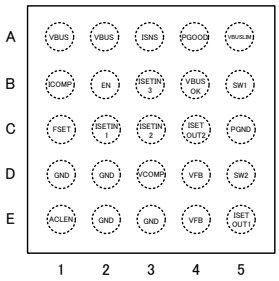
Contents

Pin Configuration (TOP VIEW)

BD8664GW / BD8665GW



BD8668GW



Pin Description

BD8664GW / BD8665GW

No.	Name	I/O	Description
A1	EN	I	Charging ON/OFF
A2	VBUS	I	Power input
A3	ISNS	I	Current sensing
A4	PGOOD	O	Power GOOD output
A5	VBUSLIM	O	VBUS current limiter output
B1	ICOMP	O	Pin for phase compensation of constant current
B2	VBUSOK	O	VBUSOK output
B3	-	-	-
B4	ISETIN1	I	Current setting pin1
B5	ISETIN3	I	Current setting pin3
C1	FSET	I	Frequency setting pin
C2	-	-	-
C3	-	-	-
C4	-	-	-
C5	SW1	O	Inductor connection pin1
D1	VCOMP	O	Pin for phase compensation of constant current connection
D2	ISETIN2	I	Current setting pin2
D3	-	-	-
D4	ISETOUT2	O	Current setting output2
D5	PGND	I	Power GND(0.0V)
E1	ACLEN	I	Automatic current ON/OFF selection pin
E2	GND	I	GND(0.0V)
E3	ISETOUT1	O	Current setting output 1
E4	VFB	I	Feedback pin of CV charging voltage
E5	SW2	O	Inductor connection pin2

No upper ESD protection diodes are connected to ISETIN1, ISETIN2, ISETIN3, and EN.

Pin Description – continued

BD8668GW

No.	Name	I/O	Description
A1	VBUS	I	Power input
A2	VBUS	I	Power input
A3	ISNS	I	Current sensing
A4	PGOOD	O	Power GOOD output
A5	VBUSLIM	O	VBUS current limiter output
B1	ICOMP	O	Pin for phase compensation of constant current
B2	EN	I	Charging ON/OFF
B3	ISETIN3	I	Current setting pin3
B4	VBUSOK	O	VBUSOK output
B5	SW1	O	Inductor connection pin1
C1	FSET	I	Frequency setting pin
C2	ISETIN1	I	Current setting pin1
C3	ISETIN2	I	Current setting pin2
C4	ISETOUT2	O	Current setting output2
C5	PGND	I	Power GND (0.0V)
D1	GND	I	GND (0.0V)
D2	GND	I	GND (0.0V)
D3	VCOMP	O	Pin for phase compensation of constant current connection
D4	VFB	I	Feedback pin of CV charging voltage
D5	SW2	O	Inductor connection pin2
E1	ACLEN	I	Automatic current ON/OFF selection pin
E2	GND	I	GND (0.0V)
E3	GND	I	GND (0.0V)
E4	VFB	I	Feedback pin of CV charging voltage
E5	ISETOUT1	O	Current setting output 1

No upper ESD protection diodes are connected to ISETIN1, ISETIN2, ISETIN3, and EN.

Block Diagram

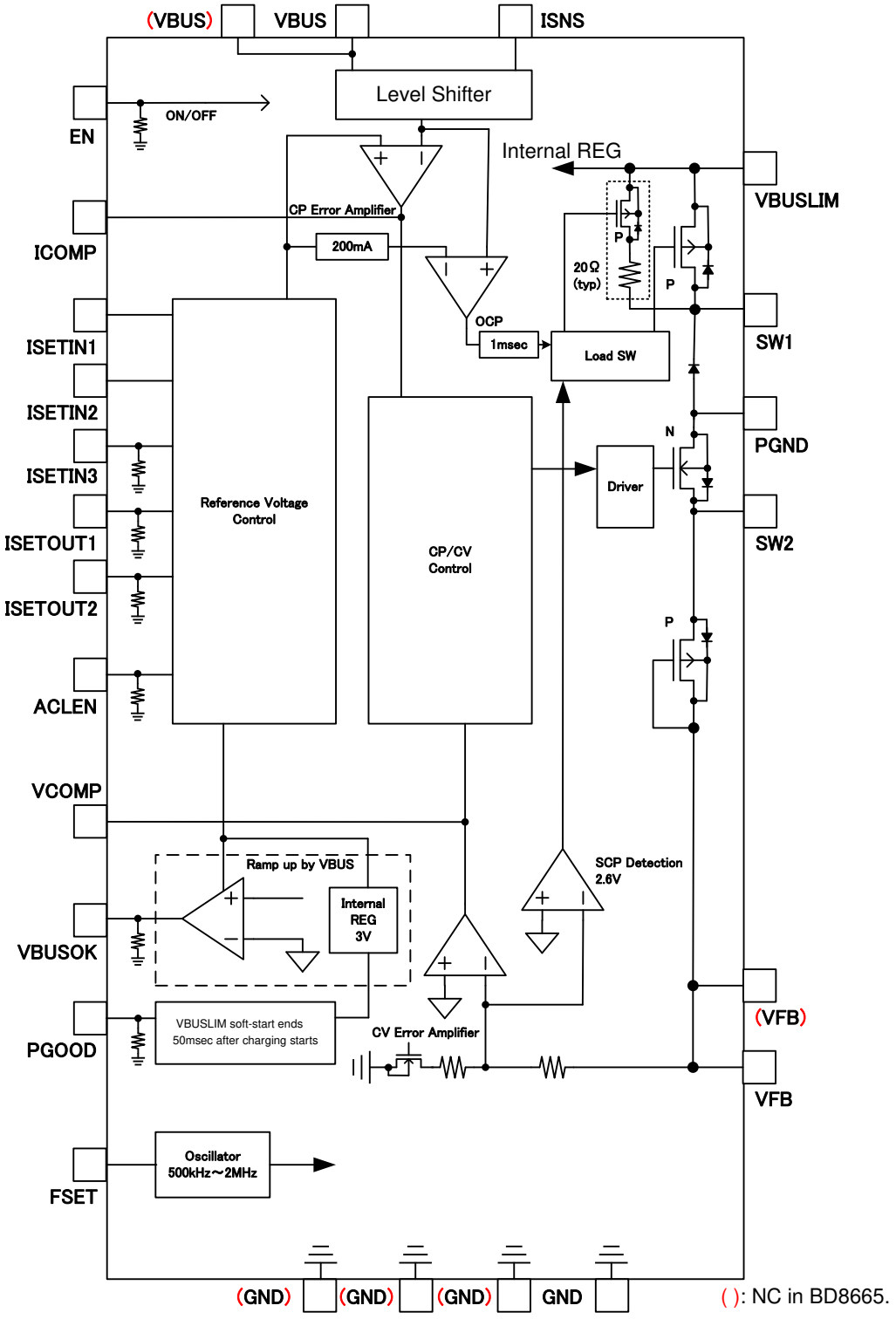


Figure 2. Block Diagram

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Range	Unit
VBUS Voltage	V_{VBUS}	-0.3 to +7.0	V
VBUSLIM Voltage	$V_{VBUSLIM}$	-0.3 to VBUS+0.3 (Note 3)	V
VFB Voltage	V_{VFB}	-0.3 to +13.0	V
SW1 Voltage	V_{SW1}	-0.3 to VBUSLIM+0.3 (Note 4)	V
SW2 Voltage	V_{SW2}	-0.3 to VFB+0.3	V
Terminal Voltage 1 (Note 1)	V_{INOUT1}	-0.3 to VBUS+0.3 (Note 3)	V
Terminal Voltage 2 (Note 2)	V_{INOUT2}	-0.3 to +6.0	V
Voltage Between Terminals (Note 5)	V_{INOUT3}	-0.3 to +0.3	V
Maximum Power Dissipation (Note 6)	Pd	1.00	W
Operating Temperature	Topr	-30 to +85	°C
Storage Temperature	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	+150	°C

(Note 1) ISNS, FSET, VBUSOK, PGOOD, VCOMP, ICOMP, ISETOUT1, ISETOUT2
(Note 2) ACLEN, EN, ISETIN1, ISETIN2, ISETIN3
(Note 3) 7.0V against GND
(Note 4) 7.0V against PGND
(Note 5) GND-PGND, VBUS-ISNS
(Note 6) When mounted on 54mm x 62mm PCB. Pd decreases by 8mW per 1°C when Ta is 25°C or higher.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-30 to +85°C)

Item	Symbol	Value			Unit	Part No.
		Min	Typ	Max		
VBUS Voltage	V_{VBUS}	4.1	5.0	5.5	V	-
VFB Voltage	V_{VFB}	0.0	8.4	10.0	V	BD8665GW/BD8668GW
			8.3			BD8664GW

Electrical Characteristics

(Unless otherwise specified, V_{VBUS}=5.0V V_{VFB}=7.4V $V_{ISETIN1,2,3}$=0V GND=PGND=0V Ta=25°C)

Item	Symbol	Value			Unit	Conditions
		Min	Typ	Max		
VBUS Stand-by Current	I_{VBUS1}	-	71	142	μA	V_{EN}= 0.0V, Only VBUSOK is ON
VBUS Operational Current	I_{VBUS2}	-	2	5	mA	No Switching
Battery Stand-by Current	I_{BATT1}	-1	0	+1	μA	V_{EN}= 0.0V
Battery Operational Current	I_{BATT2}	-	60	120	μA	No Switching
Frequency 1	F_{OSC1}	0.9	1.0	1.1	MHz	R_{FSET}= 47kΩ
Frequency 2	F_{OSC2}	(1.8)	2.0	(2.2)	MHz	R_{FSET}= 22kΩ
FSET Output Voltage	V_{FSET}	-	0.6	-	V	
<Constant Voltage Control Block>						
Constant Voltage Charging Accuracy	V_{CV2}	8.258	8.300	8.342	V	±0.5%, BD8664GW
	V_{CV2}	8.358	8.400	8.442	V	±0.5%, BD8665GW/BD8668GW
< VBUSLIM Current Control Block>						
VBUSLIM Current Accuracy (VBUS-ISNS Voltage)	$I_{VBUSLIM1}$	6.0	8.0	10.0	mV	$V_{ISETIN1}$ = 0.0V, $V_{ISETIN2}$ = 0.0V
	$I_{VBUSLIM2}$	47.0	48.5	50.0	mV	$V_{ISETIN1}$ = 0.0V, $V_{ISETIN2}$ = 3.3V
	$I_{VBUSLIM3}$	85.2	87.0	88.8	mV	$V_{ISETIN1}$ = 3.3V, $V_{ISETIN2}$ = 0.0V BD8664GW, ±2%
		84.0		90.0	mV	$V_{ISETIN1}$ = 3.3V, $V_{ISETIN2}$ = 0.0V BD8665GW/BD8668GW, ±3%
	$I_{VBUSLIM4}$	142.1	145.0	147.9	mV	$V_{ISETIN1}$ = 3.3V, $V_{ISETIN2}$ = 3.3V BD8664GW, ±2%
		140.0		150.0	mV	$V_{ISETIN1}$ = 3.3V, $V_{ISETIN2}$ = 3.3V BD8665GW/BD8668GW, ±3%
VBUSLIM Current Limiter Level (VBUS-ISNS Voltage)	$I_{VBUSOCP}$	(+15)	+20	(+30)	mV	Against The Current Set By V_{BUSLIM}
< PGOOD Block>						
PGOOD H Voltage	V_{PGOODH}	2.94	3.00	3.06	V	±2%
PGOOD L Voltage	V_{PGOODL}	-	0.0	-	V	
<VBUSOK Pin >						
VBUS Threshold 1	$V_{VBUSOKTH1}$	3.9	4.0	4.1	V	V_{BUS} = L to H
VBUS Threshold 2	$V_{VBUSOKTH2}$	3.8	3.9	4.0	V	V_{BUS} = H to L
VBUSOK L->H Delay Time	$V_{VBUSOKDELAY}$	20	40	-	ms	
VBUSOK H Voltage	$V_{VBUSOKH}$	2.94	3.00	3.06	V	±2%
VBUSOK L Voltage	$V_{VBUSOKL}$	-	0.0	-	V	
<Comparator Block>						
VBUS UVLO Threshold	$V_{VBUSUVLOON}$	3.40	3.60	3.80	V	
VBUS UVLO Unlock Threshold Voltage	$V_{VBUSUVLOFF}$	3.50	3.70	3.90	V	
VFB Low Voltage Detection1	V_{VFBLV1}	-	2.4	-	V	VFB = H to L
VFB Low Voltage Detection2	V_{VFBLV2}	-	2.6	-	V	VFB = L to H
VFB Overvoltage Detection1	V_{VFBOV1}	8.5	9.0	9.5	V	VFB = H to L
VFB Overvoltage Detection2	V_{VFBOV2}	9.2	9.7	10.2	V	VFB = L to H
VBUS Current Automatic Selection Voltage 1	$V_{VBUSAUTOTH}$	3.9	4.0	4.1	V	VBUS = H to L
VBUS Current Automatic Selection Voltage 1	$V_{VBUSAUTOTH}$	4.0	4.1	4.2	V	VBUS = L to H
<Power MOSFET>						
VBUSLIM-SW1 PMOS Ron	R_{SW1A}	-	70	-	mΩ	I_{SW1} = -10mA
VBUSLIM-SW1small PMOS Ron	R_{SW1B}	-	20	-	Ω	I_{SW1} = -10mA
SW2-PGND NMOS Ron	R_{SW2}	-	60	-	mΩ	I_{SW2} = 10mA
SW2 Max Duty Width	$T_{SW2MAXDUTY}$	-	80	-	ns	R_{FSET}= 47kΩ
SW2 Min Duty Ratio	$T_{SW2MINDUTY}$	-	0	-	%	R_{FSET}= 47kΩ

Electrical Characteristics - continued

<Input/ Output>						
EN/ISETIN1,2,3/ACLEN L Voltage	V_{INL}	-	-	0.4	V	
EN/ISETIN1,2,3/ACLEN H Voltage	V_{INH}	2.5	-	5.5	V	
ISETIN1,2 Input Current	I_{INH}	-	0	-	μA	No Pull-Down, Open Is Not Allowed.
EN/ACLEN/ISETIN3 Pull-Down Resistor	R_{IN2}	300	500	700	kΩ	
ISETOUT1,2 L Voltage	V_{OUTL}	-	0.0	-	V	
ISETOUT1,2 H Voltage	V_{OUTH}	2.94	3.00	3.06	V	

This product has no designed protection against radioactive rays.
Pd is the maximum power. Please keep the current to meet power lower than the Pd.

Typical Performance Curves

(Unless otherwise specified, V_{VBUS}=5.0V V_{VFB}=7.4V $V_{ISETIN1,2,3}$=0V GND=PGND=0V Ta=25°C)

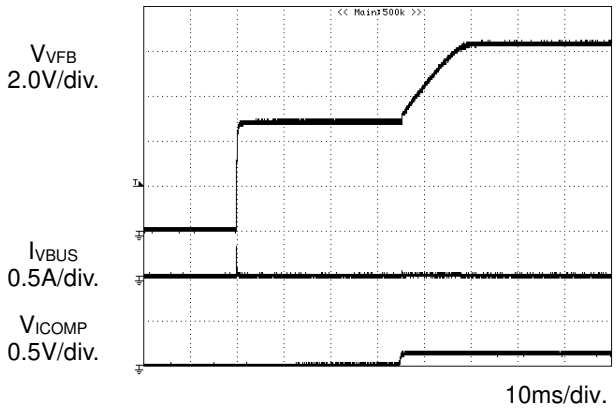


Figure 3. Feeding Mode Ramp-up (No Load)

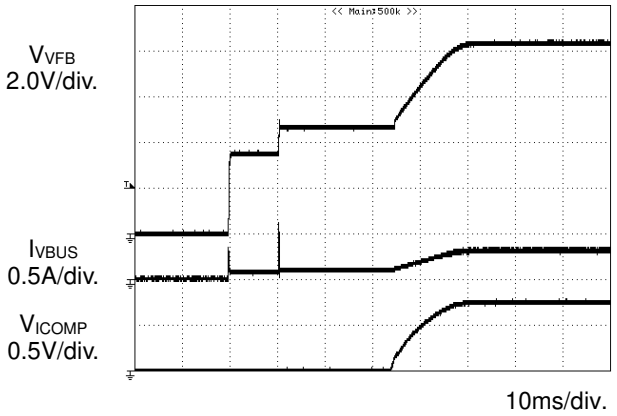


Figure 4. Feeding Mode Ramp-up (50Ω Load)

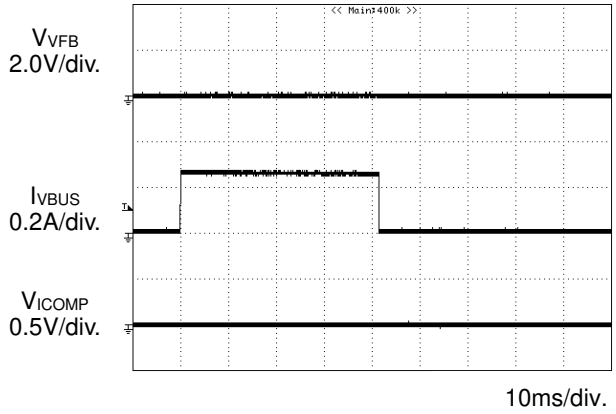


Figure 5. Start-up Waveform
(VFB is Shorten to Ground)

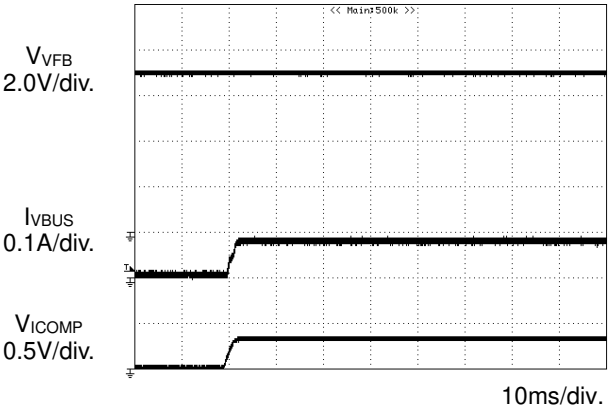


Figure 6. Charging Mode Start-up
(100mA mode)

Typical Performance Curves - continue

(Unless otherwise specified, V_{VBUS}=5.0V V_{VFB}=7.4V $V_{ISETIN1,2,3}$=0V GND=PGND=0V Ta=25°C)

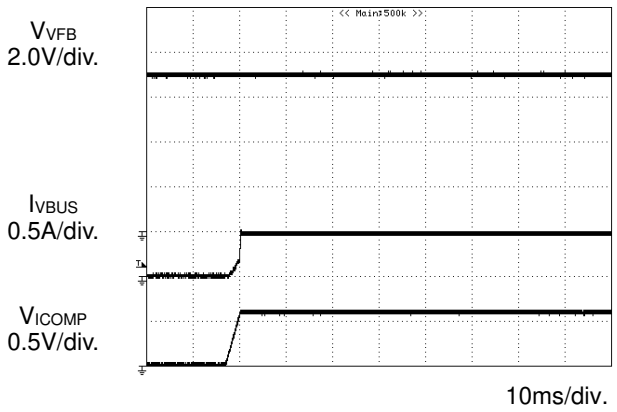


Figure 7. Charging Mode Start-up
(500mA Mode)

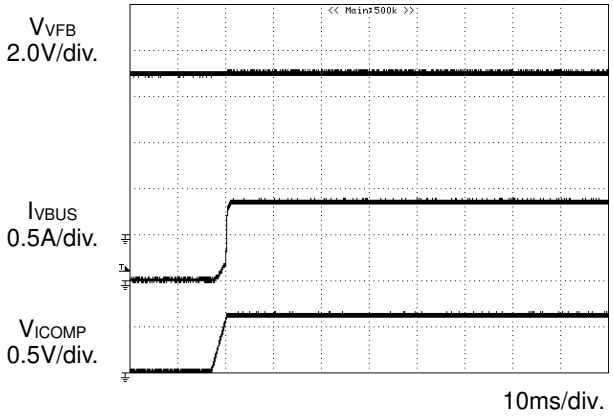


Figure 8. Charging Mode Start-up
(900mA Mode)

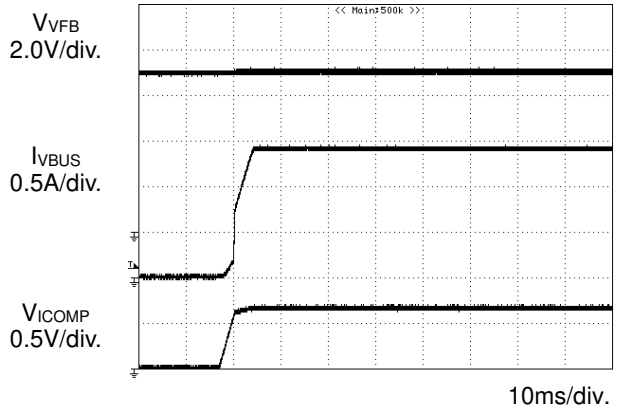


Figure 9. Charging Mode Start-up
(1500mA Mode)

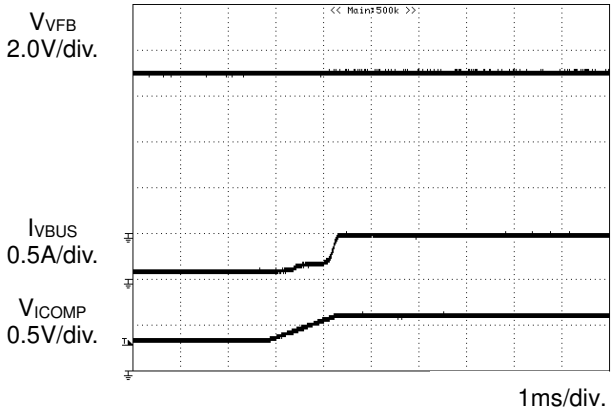


Figure 10. Changing Current
(100mA to 500mA)

Typical Performance Curves - continue

(Unless otherwise specified, V_{VBUS}=5.0V V_{VFB}=7.4V $V_{ISETIN1,2,3}$=0V GND=PGND=0V Ta=25°C)

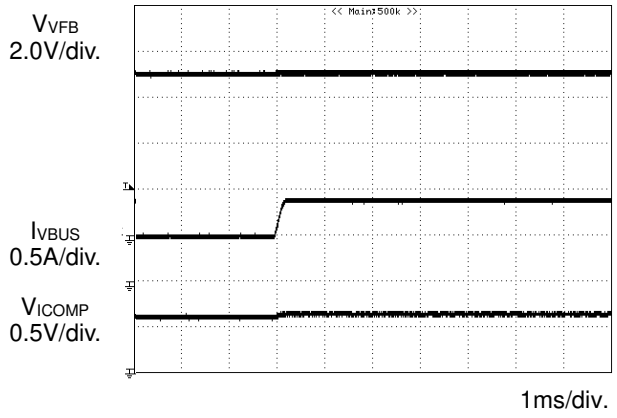


Figure 11. Changing Current
(500mA to 900mA)

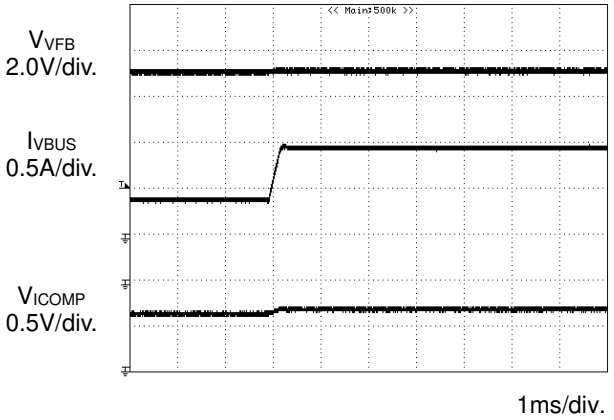


Figure 12. Changing Current
(900mA to 1500mA)

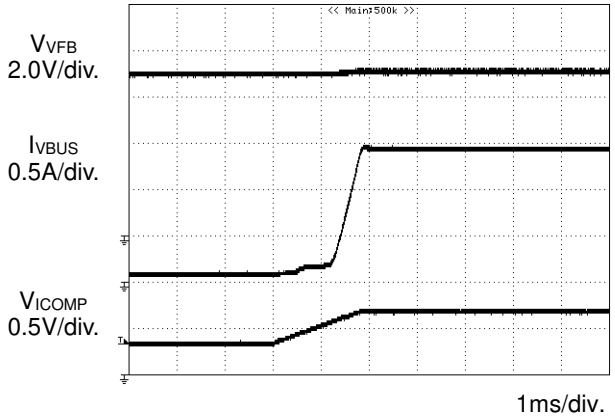


Figure 13. Changing Current
(100mA to 1500mA)

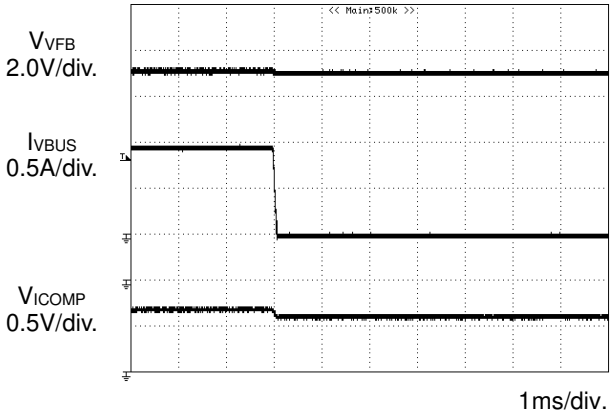


Figure 14. Changing Current
(1500mA to 500mA)

Typical Performance Curves - continue

(Unless otherwise specified, V_{VBUS}=5.0V V_{VFB}=7.4V $V_{ISETIN1,2,3}$=0V GND=PGND=0V Ta=25°C)

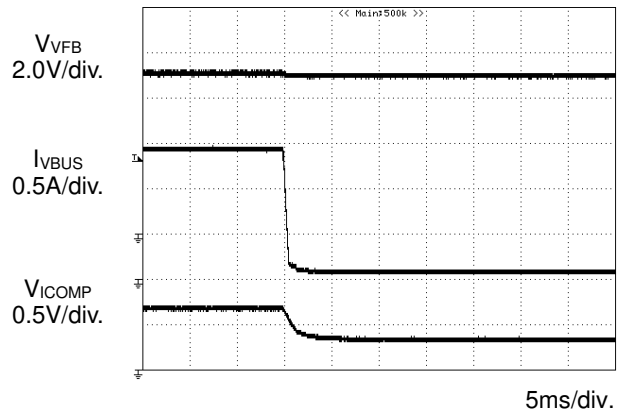


Figure 15. Changing Current
(1500mA to 100mA)

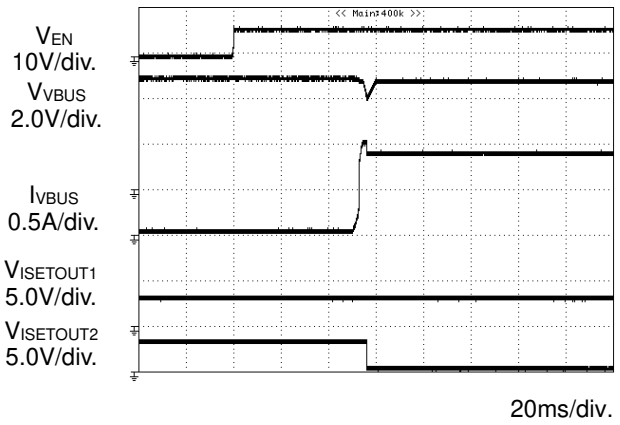


Figure 16. Automatically Changing Current
(1500mA to 900mA)

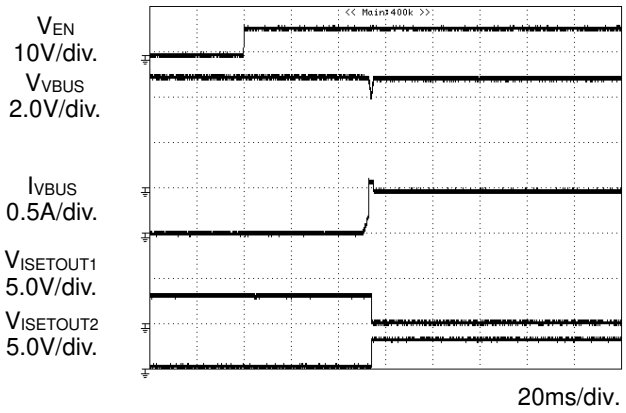


Figure 17. Automatically Changing Current
(900mA to 500mA)

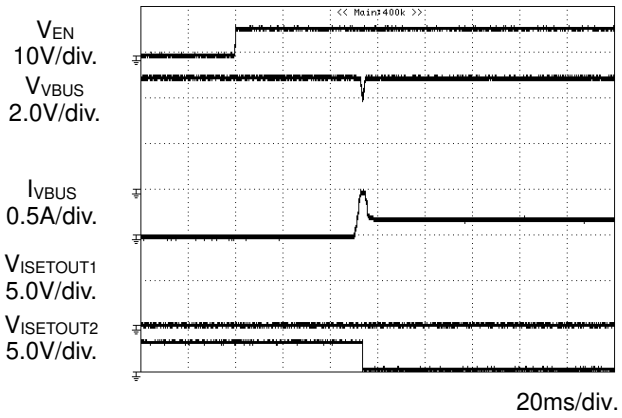


Figure 18. Automatically Changing Current
(500mA to 100mA)

Typical Performance Curves - continue

(Unless otherwise specified, V_{VBUS}=5.0V V_{VFB}=7.4V $V_{ISETIN1,2,3}$=0V GND=PGND=0V Ta=25°C)

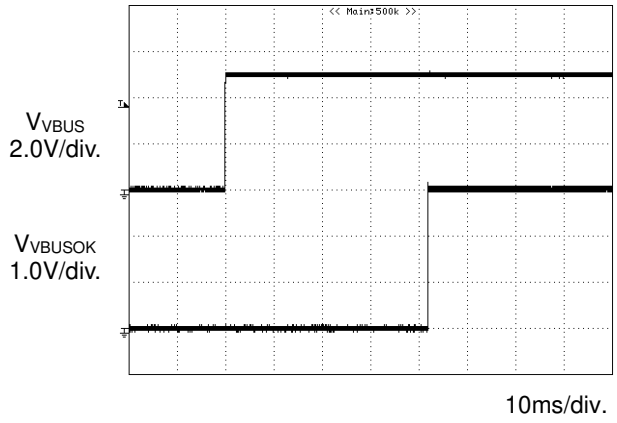


Figure 19. VBUSOK (L to H Delay Time)

Reference Data

(Unless otherwise specified, V_{VBUS}=5.0V V_{VFB}=7.4V $V_{ISETIN1,2,3}$=0V GND=PGND=0V Ta=25°C)

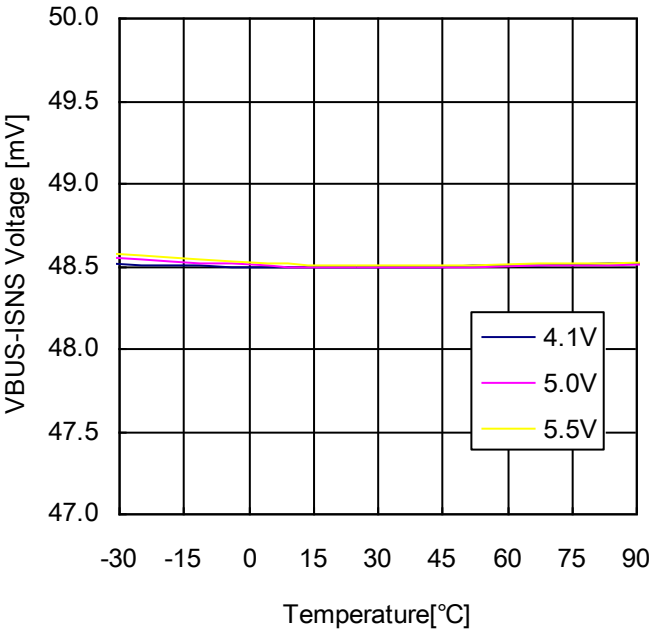


Figure 20. CV Voltage vs Temperature

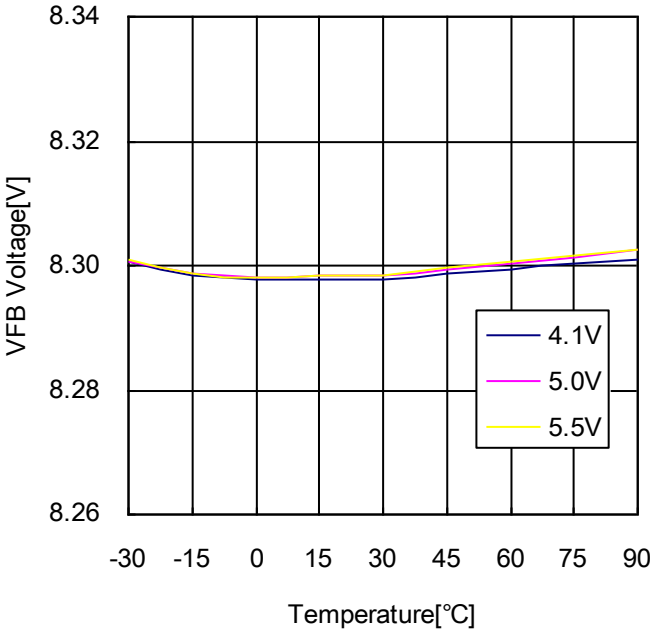


Figure 21. CV Voltage VBUS Voltage Dependency (BD8664GW)

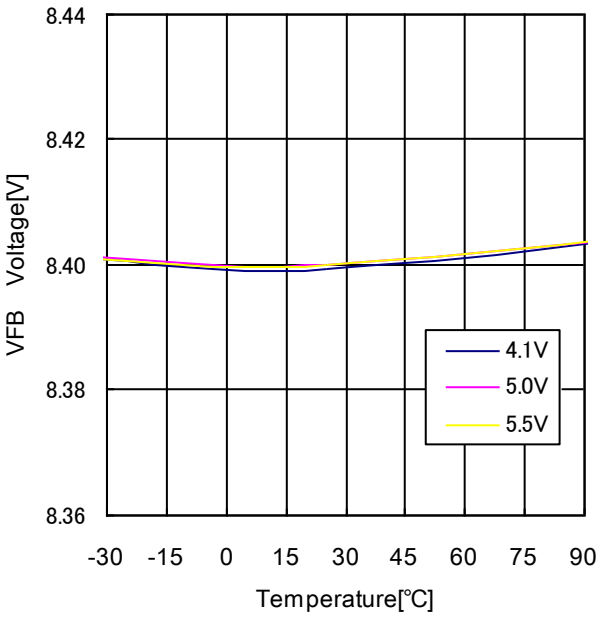


Figure 22. CV Voltage VBUS Voltage Dependency (BD8665GW/BD8668GW)

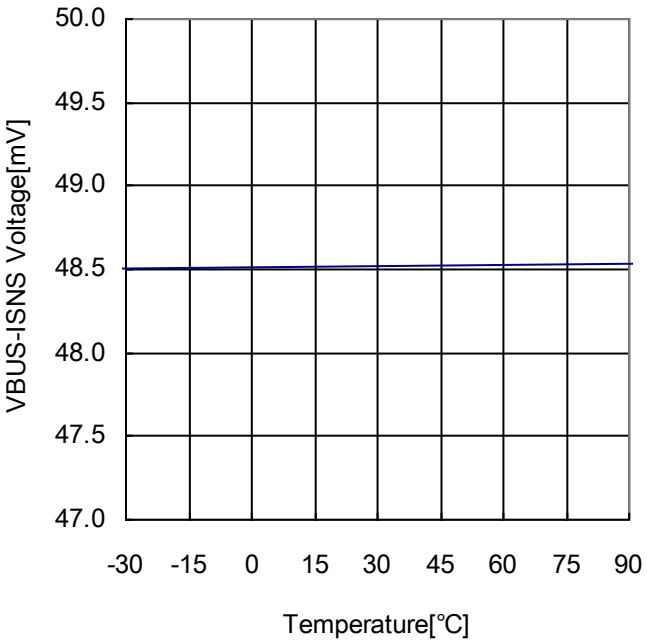


Figure 23. 500mA Mode CP Current Temperature Characteristic

Reference Data - continue

(Unless otherwise specified, V_{VBUS}=5.0V V_{VFB}=7.4V $V_{ISETIN1,2,3}$=0V GND=PGND=0V Ta=25°C)

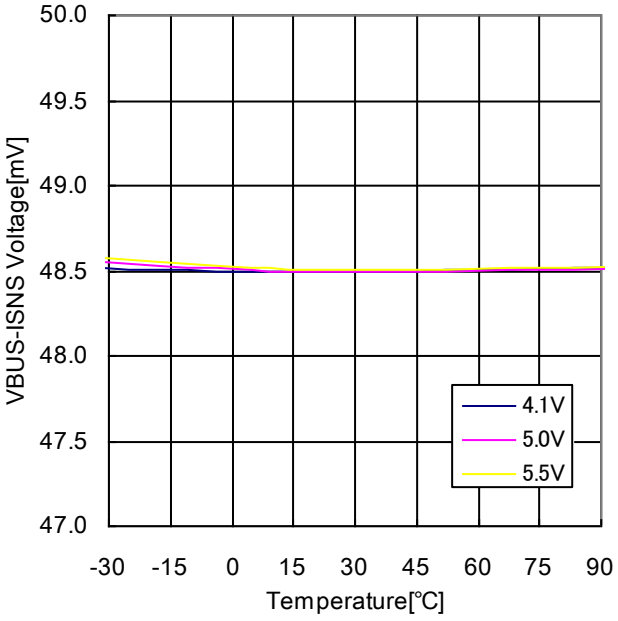


Figure 24. 500mA Mode CP Current VBUS Dependency

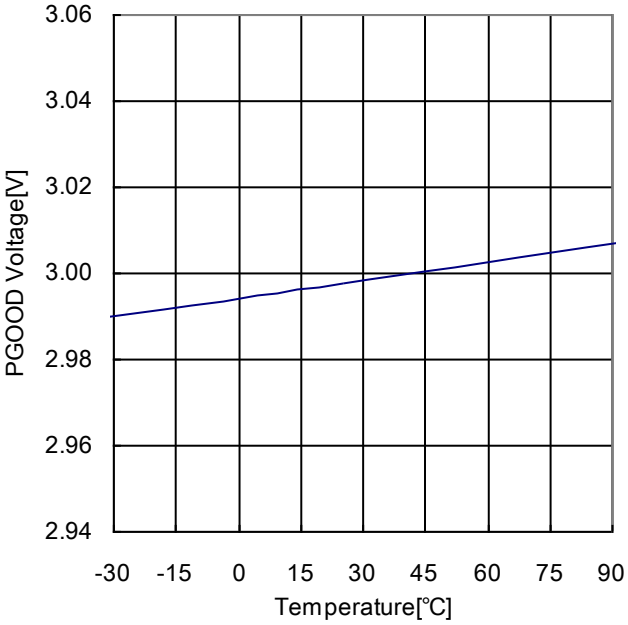


Figure 25. PGOOD Pin H Voltage Temperature Characteristic

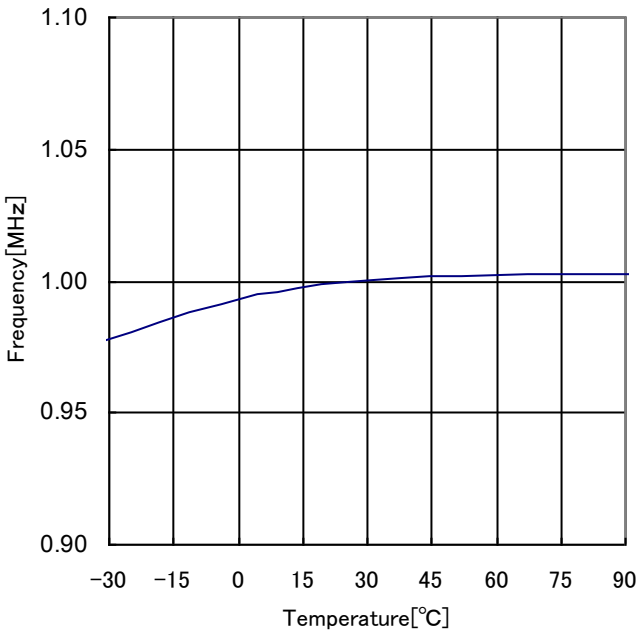


Figure 26. Frequency Temperature Characteristic

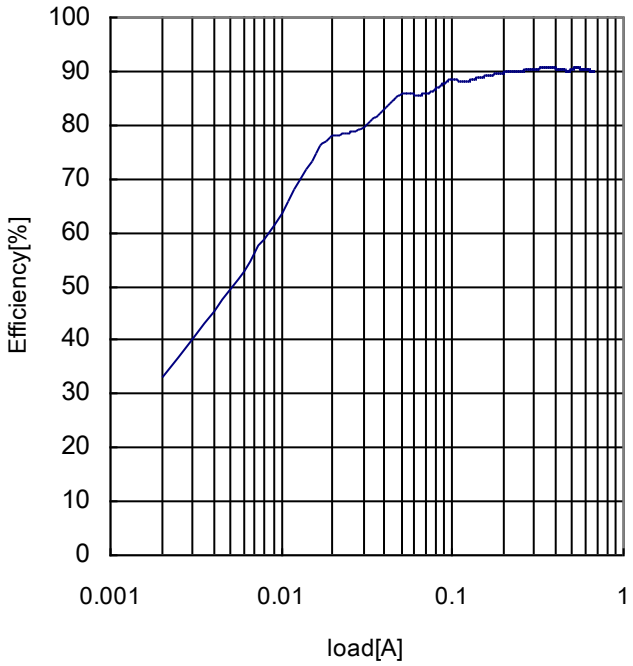


Figure 27. Efficiency 500mA Mode

Block Descriptions

1. VBUS Input Detection Comparator Output (VBUSOK)

VBUS voltage can set VBUSOK. 40ms after detecting that VBUS is higher than 4.0V (typ), VBUSOK turns H (3.0V [typ]). In case VBUS ramps down, and reaches 3.9V (typ), VBUSOK turns L without any delay. The function works independently from the condition of EN and thermal shut down.

VBUS	VBUSOK
< 3.9V (typ)	L 0.0V (typ)
>= 4.0V (typ)	H 3.0V (typ)

2. Charging ON/OFF (EN)

ON/OFF is controlled with the EN pin. When EN is L, the IC enters shutdown mode (or USB suspend mode), the battery leakage current is set to 0μA, and all other functions but VBUSOK turns off. EN pin is connected to a 500kΩ (typ) pull-down resistor.

3. USB Current Setting (ISETIN1,2,3)

ISET1	ISET2	ISET3	VBUS Input Current Settings
L	L	L	100mA (max)
L	L	H	500mA (max)
L	H	L	500mA (max)
L	H	H	500mA (max)
H	L	L	900mA (max)
H	L	H	900mA (max)
H	H	L	1500mA (max)
H	H	H	1500mA (max)

Note: Open is NOT allowed for ISETIN1,2 pins. No pull-down resistor is connected to ISETIN1, 2 pins. 500kΩ (typ) pull-down resistor is internally connected to ISETIN3.

4. VBUS Current Setting (ISETOUT1,2)

ISETOUT1	ISETOUT2	VBUS Current Settings
L	L	100mA (max)
L	H	500mA (max)
H	L	900mA (max)
H	H	1500mA (max)

Note: 500kΩ(typ) is connected internally to ISETOUT1,2. Even in the case VBUS=0V, the output stays stable.

5. Frequency Setting (FSET)

The PWM switching frequency can be set.

FSET	PWM
100kΩ	500kHz (typ)
47kΩ	1MHz (typ)
33kΩ	1.5MHz (typ)
22kΩ	2MHz (typ)

6. CV Control Soft-Start

If the system boots up with NO battery, CV control method suppresses the 8.3V (typ) in case of using BD8664GW and 8.4V (typ) in case of using BD8665GW/BD8668GW, on VFB pin, and enters “feeding mode”. In this mode, it will take 40ms (typ) for the VFB to reach 8.4V (typ).

7. Load Switch Function

A PMOS load switch is integrated between VBUSLIM and SW1. When EN=L, the load switch turns off. If a low battery is connected, charging can be stopped. The integrated load resistors are 20Ω (typ) and 70mΩ (typ). The higher resistance is connected during start-up. After 10ms (typ), the lower resistance is connected if no short circuit is detected by VFB pin.

8. OCP for Load Switch

Through a sense resistor between VBUS and ISNS, over-current can be detected while the load switch is on. If the over-current is constantly detected for more than 1ms, the load switch turns off and latches, and PGOOD is set L. To unlatch, the IC must be rebooted by switching EN to low, then back to high; or set VBUS to a voltage lower than UVLO, then back to the operating VBUS voltage.

9. Battery Low Voltage Detection (Output SCP)

If during start-up, the battery's voltage is lower than VFB voltage or the output is shorted to ground, the low-side load switch will never be turned on, and the high-side load switch will be on for 80ms (typ). But, if the high-side load switch is kept on for more than 80ms, the load switch is turned off. This function is off after the PGOOD is turned H.

10. Power Good (PGOOD)

The IC is enabled by EN pin. After CV, CP, and soft start, PGOOD condition changes its state from L to H. Inversely, during thermal shutdown, overvoltage battery and OCP, PGOOD is L.

11. Battery Overvoltage Detection

Due to the VBUS current limiter, overvoltage can occur at VFB terminal during CP charging. This can cause damage to devices that are connected to the IC. To prevent this, overvoltage protection is integrated. Once overvoltage is detected, SW2 becomes Hi-Z, the error amp output and soft start are reset to default, and PGOOD is set L. Once VFB voltage is at a safe level, the IC automatically restarts with soft start.

12. Auto VBUS Current Setting

Once VBUS voltage exceeds 4.1V (typ), the VBUS current set to ISET1 to 3 pins are automatically changed from 1500mA (max) to 900mA (max), from 900mA (max) to 500mA (max), and from 500mA (max) to 100mA (max), while VBUS is continuously monitored. If ISET1 to 3 are changed after the auto change is done, the initial current that has been set to ISET1 to 3 will be employed again.

Notes:

(1) If VBUS voltage remains lower than 4.1V and current is changed from 1500mA to 900mA, the current will not be changed to 500mA.
(2) ACLEN has a pull-up resistor. The pin is L if it is open and auto setting becomes active.
(3) It can be turned off by setting ACLEN to H.
(4) It starts to work after the lower resistance load is turned on. Until PGOOD is changed to H, the bus current value is determined only by ISETIN1 to 3 and will not to be changed by VFB low voltage function.

13. Feeding Mode and Charging Mode

Feeding Mode: If the system boots up with NO battery to the IC, CV control method suppresses 8.3V (typ) for BD8664GW and 8.4V (typ) for BD8665GW/BD8668GW on VFB pin. During the feeding mode, the constant voltage is done by the VFB pin.

Charging Mode: If the system boots up with a battery to the IC, CP/CV control method is employed. During charging mode, the CV/CP function is applied to the battery. The two modes, however, are not internally controllable by the IC. An application that applies constant output voltage with CV charging is called “feeding mode” and another application that charges with CV/ CP charging is called “charging mode” in this technical note.

Timing Chart/Application Information

1. VBUSOK/VBUS Threshold at Automatic Change Current Setting

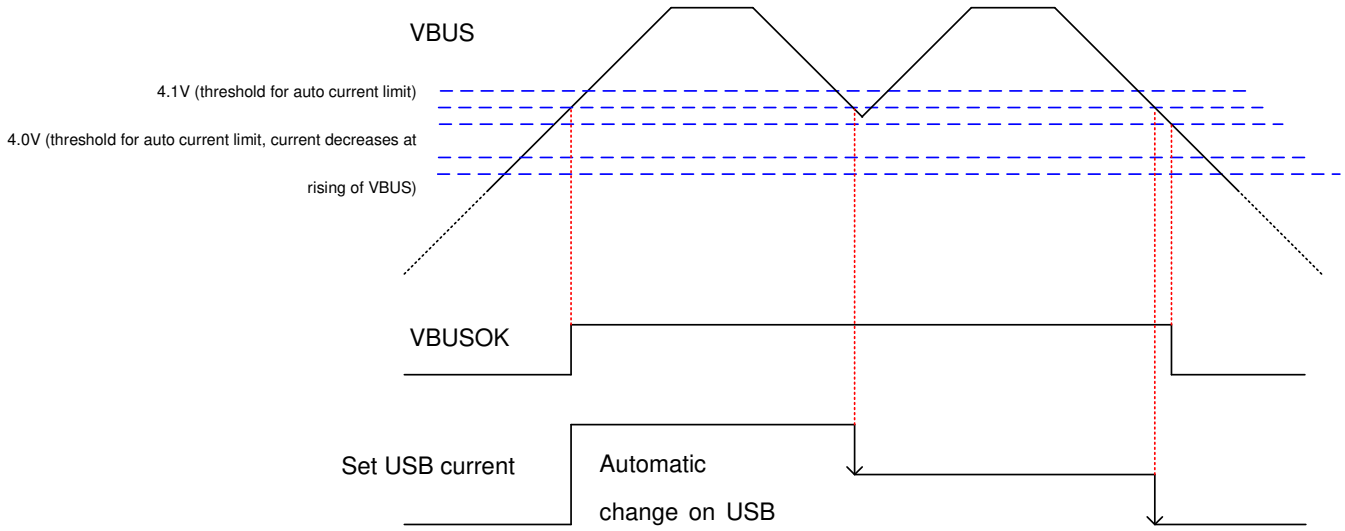


Figure 28. VBUSOK/VBUS Threshold at Automatic Change Current Setting waveform

1. Start-up Waveform at Feeding Mode (No Battery, Light Load)

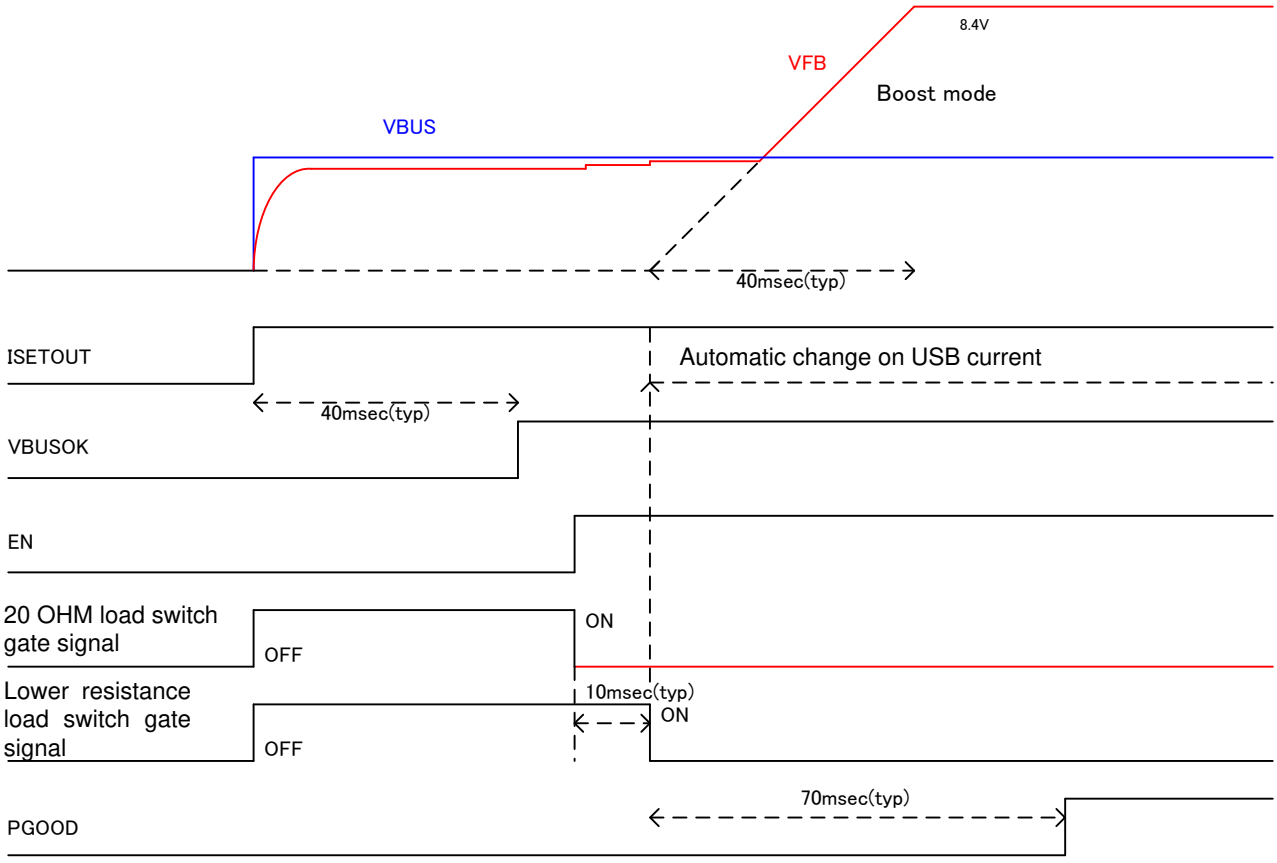


Figure 29. Start-up Waveform at Feeding Mode

2. Start-up Waveform at Feeding Mode (No Battery, 50Ω Load)

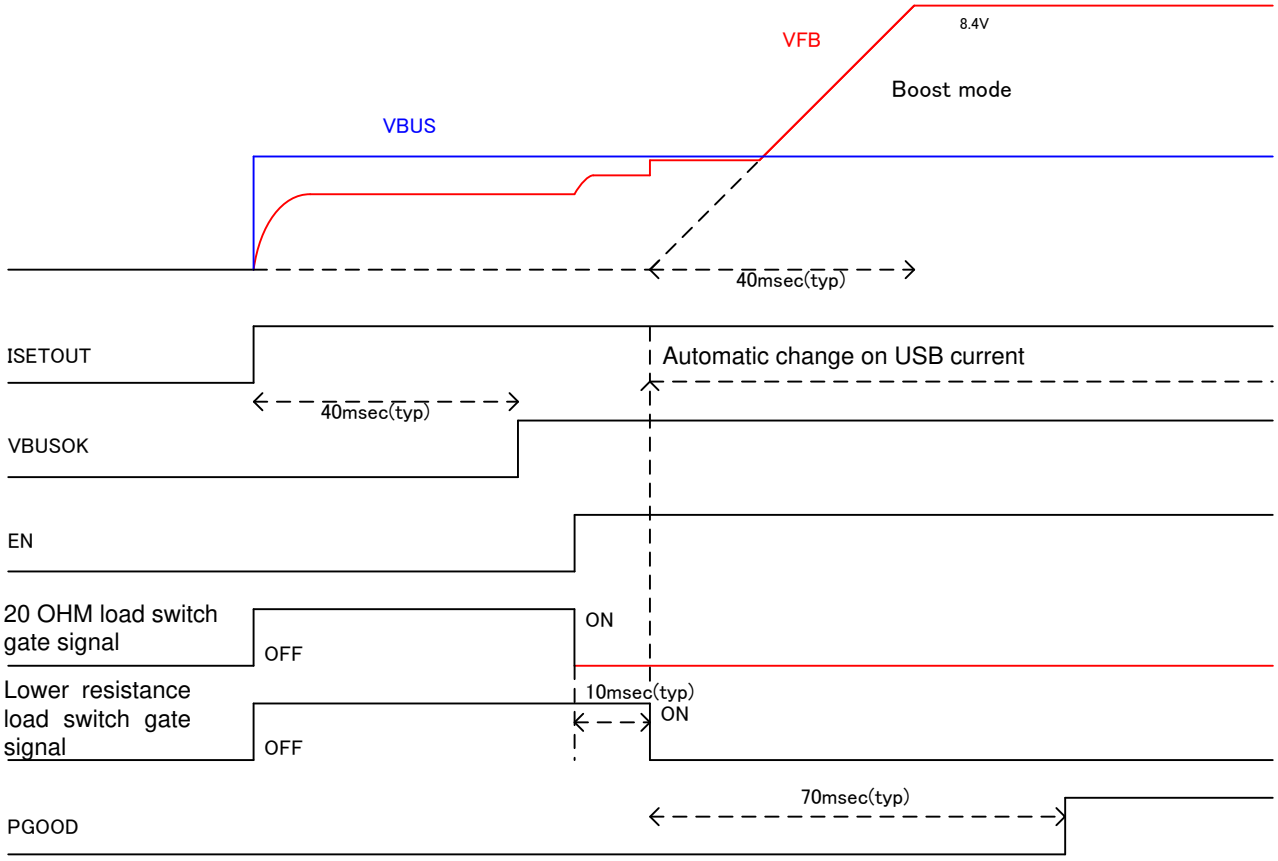


Figure 30. Start-up Waveform at Feeding Mode (No Battery, 50Ω Load)

3. Start-up Waveform at Feeding Mode(No battery, Heavy Load [Short to Ground])

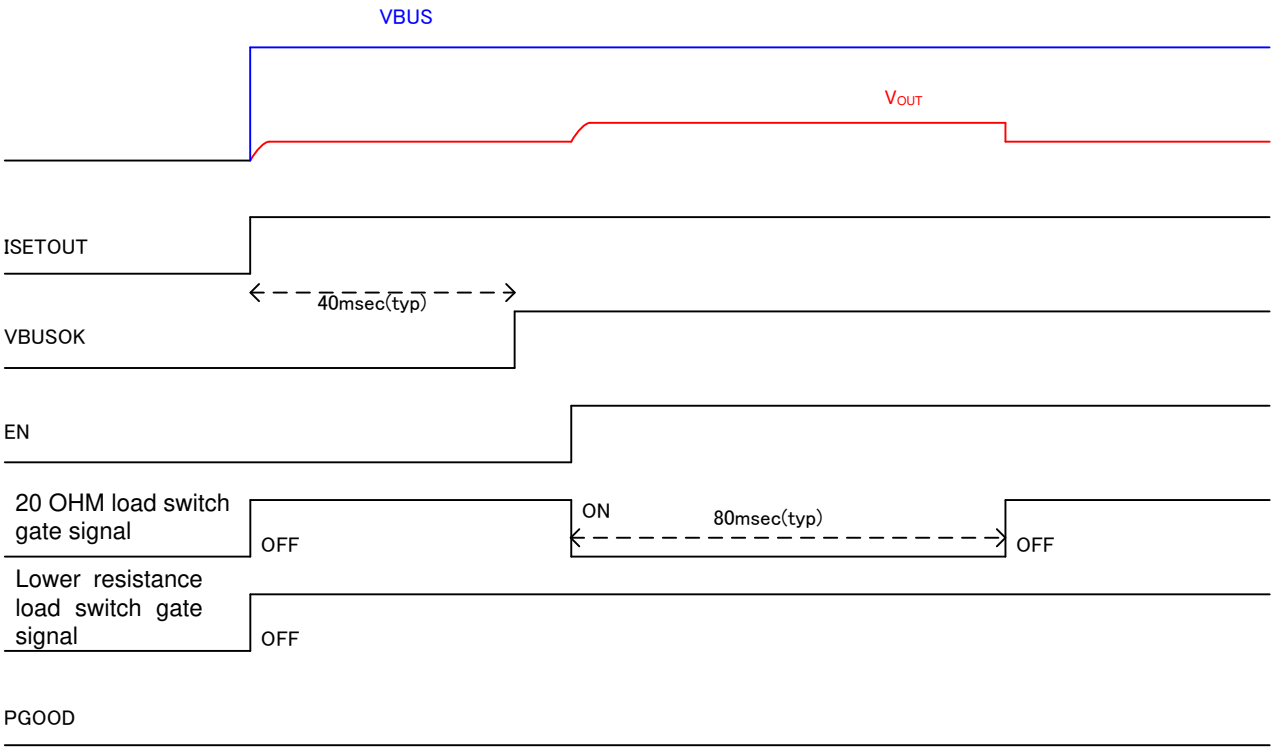


Figure 31. Start-up Waveform at Feeding Mode (No battery, Heavy Load [Short to Ground])

4. Voltage Waveform to PGOOD at Charging Mode (With Battery)

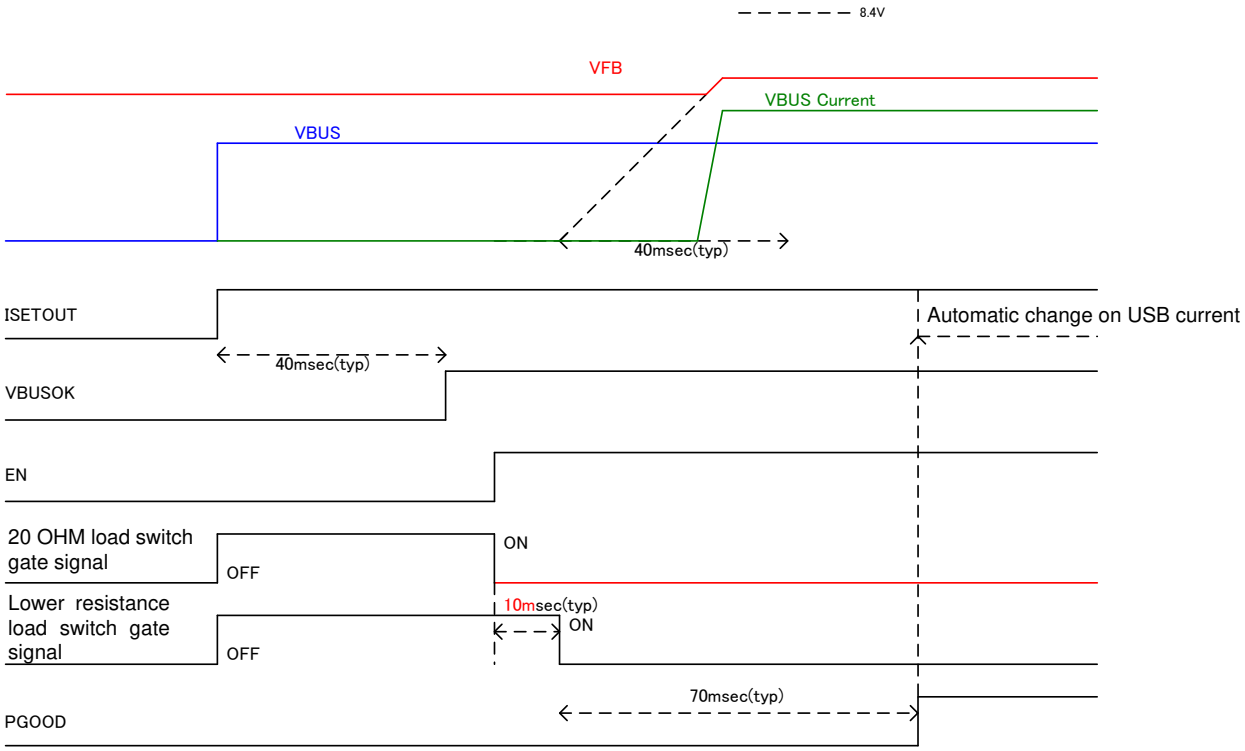


Figure 32. Voltage Waveform to PGOOD at Charging Mode (With Battery)

5. Operation from Feeding Mode to Charging Mode

During feeding mode, after the output started up with 8.3V(typ) for BD8664GW and 8.4V(typ) for BD8665GW/BD8668GW, if the battery has to be connected and the mode has to change to charging mode, set EN to L then H to enable CP charging. This turns PGOOD pin to L then H. Note that VBUS current may exceed the set value unless the EN is set L once.

6. Operation from Charging Mode To Feeding Mode

During charging mode, if the mode has to change to feeding mode, set the EN to L, detach the battery, then set EN to H again. This turns PGOOD pin to L, ramps up VFB to 8.3V (typ) for BD8664GW and 8.4V (typ) for BD8665GW/BD8668GW by feeding mode, and turns PGOOD to H, afterwards. Note that the overcurrent protection may occur unless the EN is set L like aforementioned VFB overvoltage detection waveform.

7. Battery Overvoltage Detection Waveform

During charging, if the battery is detached by a user, V_{OUT} will go higher as the mode changes to feeding mode. In this scenario, to prevent damage to devices connected to this IC, OVP is integrated. PGOOD has to be turned off to L when OVP is detected. Soft-start is again implemented when V_{OUT} goes low due to its output load.

In the application circuit example, note that the VFB node goes down to VBUS -1Vf, as determined by an external schottky diode.

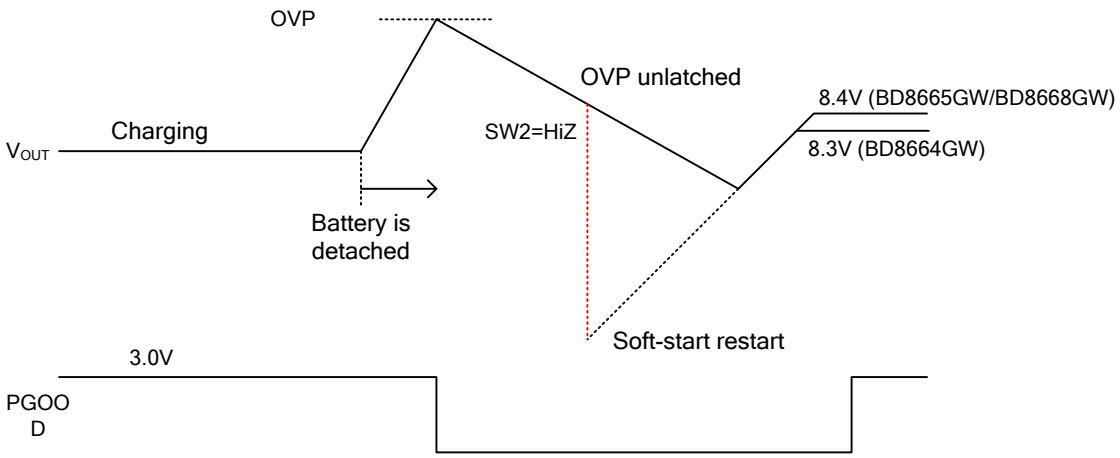


Figure 33. Battery Overvoltage Detection Waveform

8. Precaution on Voltage Application between Constant-Voltage Charging Voltage and OVP

When the voltage between constant-voltage charging voltage and OVP is applied to the VFB node, (e.g., An AC adapter is unplugged when the AC adapter voltage is applied to the VFB pin), the VFB terminal drops drastically, so avoid the above mentioned condition.

Application Components Selection

1. Frequency Setting (FSET) Resistor

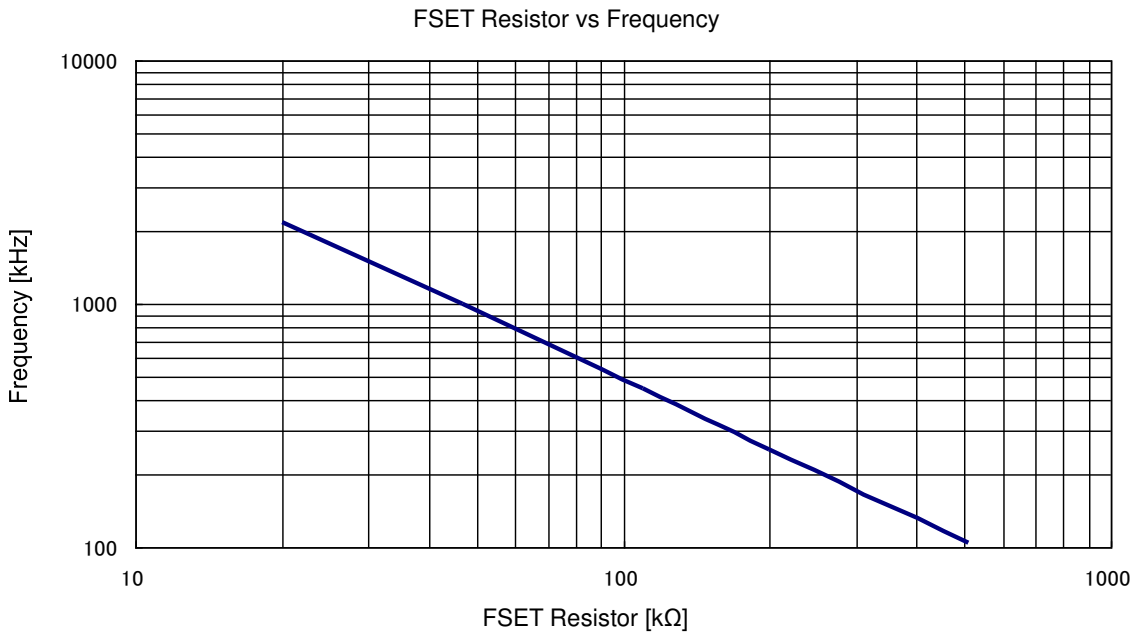


Figure 34.. Frequency Setting (F_{SET}) Resistor

2. Inductor Selection

Inductance for the boost switching affects its ripple current and ripple current at feeding mode. The ripple voltage is inversely proportional to the inductance and switching frequency so that the inductance must be higher if the frequency is lower. In other words, the inductance can be smaller if the frequency is higher. However, if the inductance changes, since the LC cutoff frequency changes, the phase compensation of ICOMP and VCOMP may have to be changed.

PWM	Inductance	Output Capacitance	ICOMP Time Constant	VCOMP Coefficient
1MHz(typ)	4.7μH	40μF	200Ω, 0.1μF serial	47kΩ, 0.1μF serial

※If the external coefficient is changed from the designated value above, check the open-loop gain phase carefully.

Example of Recommended Circuit

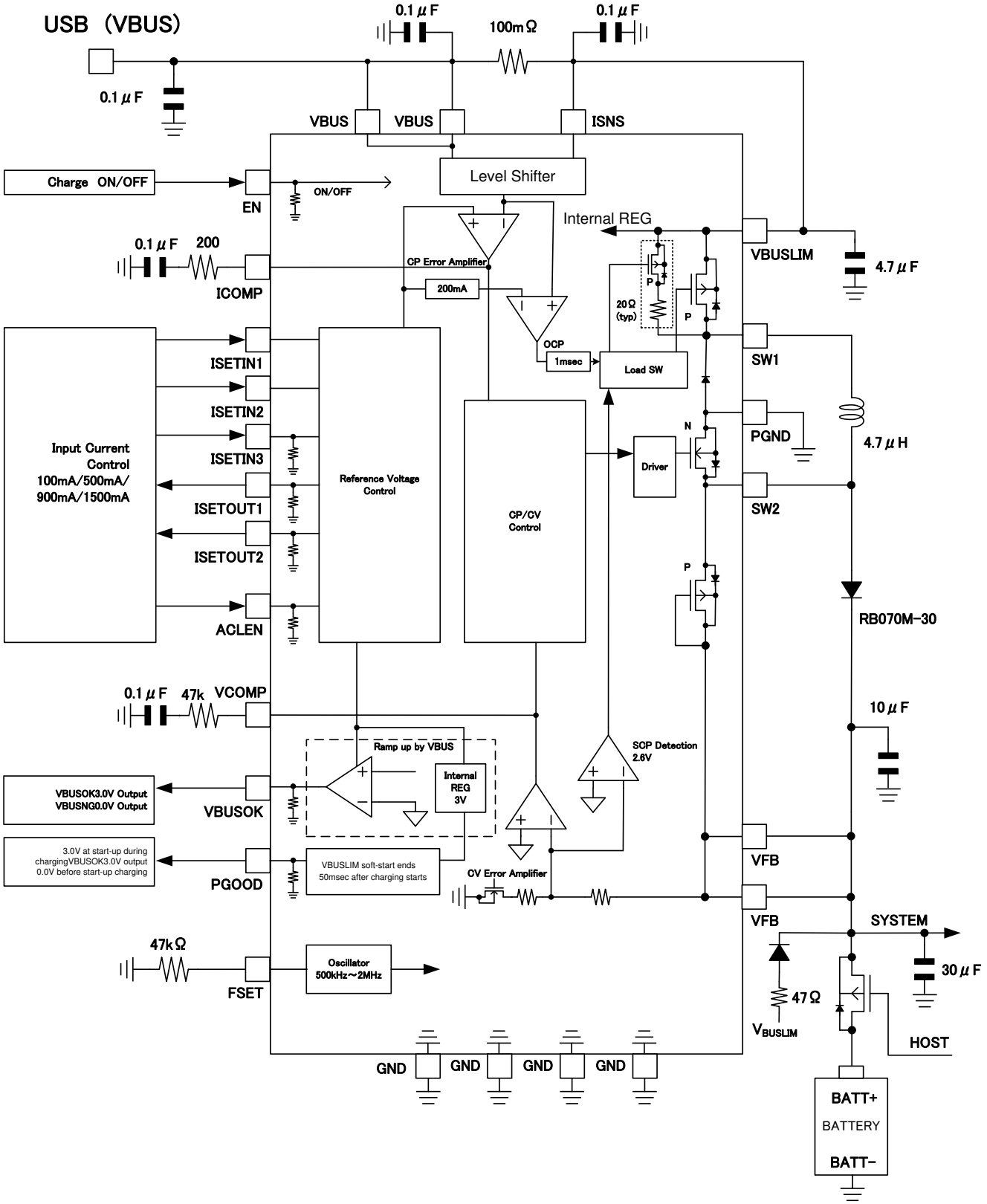
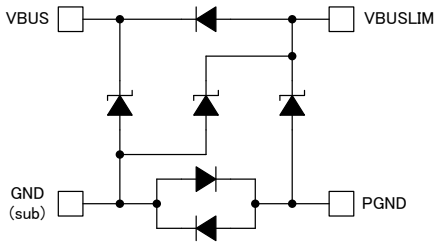
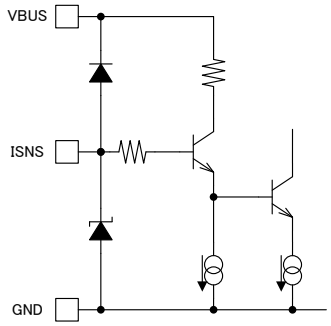
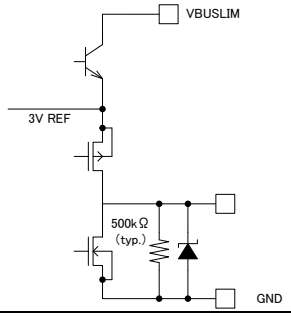
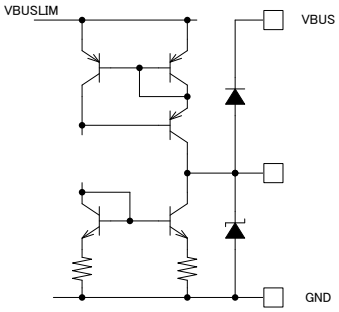
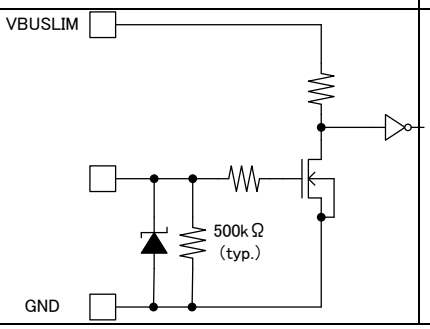
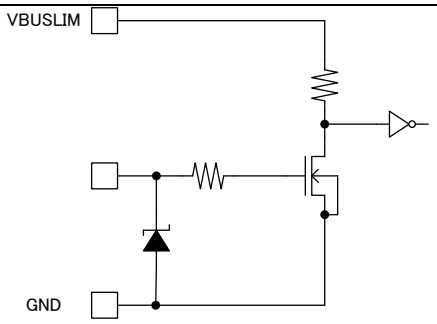
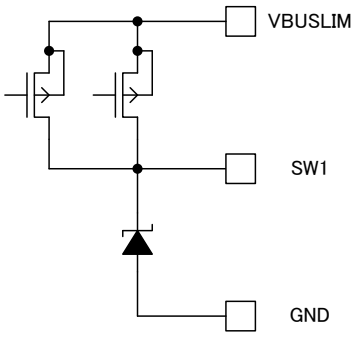
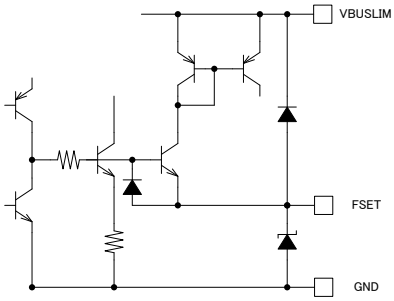
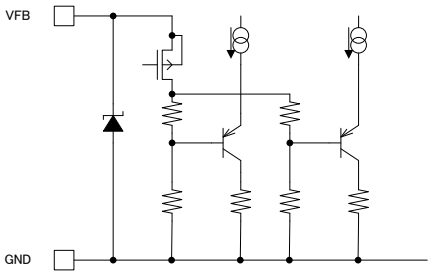
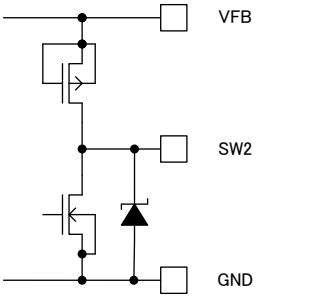


Figure 35. Example of Recommended Circuit

Input/Output Pin Immediate Circuit

Pin No. (BD8668GW)	Pin Name	Pin Immediate Circuit	Function
A1/A2	VBUS		USB power input
A5	VBUSLIM		USB current limiter
D1/D2 /E2/E3	GND		Ground
C5	PGND		Power Ground
A3	ISNS		Current detection amp input
A4 B4 C4 E5	PGOOD VBUSOK ISETOUT2 ISETOUT1		Logic output (with pull-down resistor)
B1 D3	ICOMP VCOMP		Error amp output
B2 E1 B3	EN ACLEN ISETIN3		Logic input (with pull-down resistor)

Input/Output Pin Immediate Circuit - continued

Pin No. (BD8668GW)	Pin Name	Pin Immediate Circuit	Function
C2 C3	ISETIN1 ISETIN2		Logic input (without pull-down resistor)
B5	SW1		Load switch output Inductor connection1
C1	FSET		Frequency setting resistor terminal
D4 E4	VFB VFB		CV charging voltage feed-back terminal
D5	SW2		Boost switching terminal Inductor connection 2

Thermal Reduction Characteristics

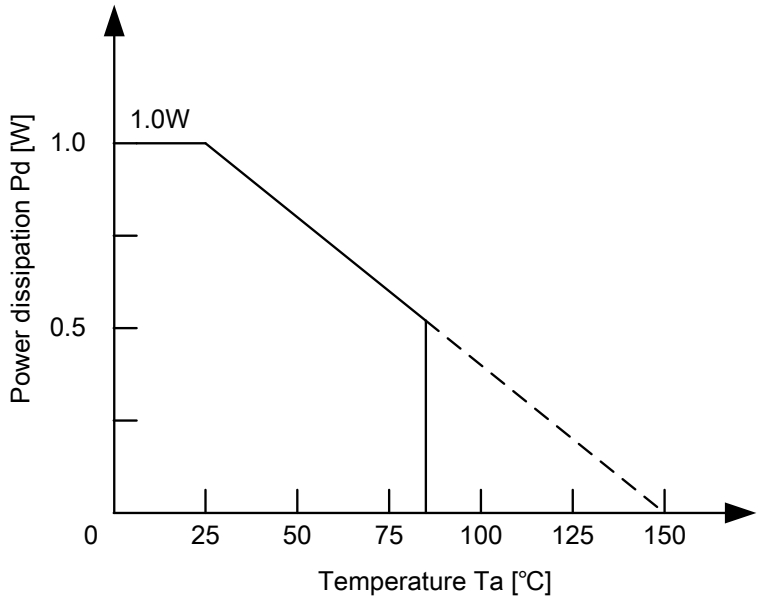


Figure 36.. Power Dissipation (Mounted on a 4-layer substrate board)