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IPD series for Automotive

8ch Low-side switch

BD8LA700EFV-C

Features

- Monolithic power IC that has a built-in control part (CMOS) and a power MOS FET on 1chip
- 8ch Low-side switch for driving resistive, inductive load
- 16bit Serial peripheral interface(SPI) for diagnostics and control
- Built-in Open Load Detection circuit in output-off state
- Built-in Over Current Protection circuit (OCP)
- Built-in Active Clamp circuit
- Built-in Thermal shutdown circuit (TSD)
- Low On resistance of $R_{ON}=700m\Omega$ ($V_{IN}=5V, T_j=25^\circ C, I_o=0.2A, Typ$)
- Surface mount HTSSOP-B24 Package
- AEC-Q100 Qualified (Note 1) Grade1

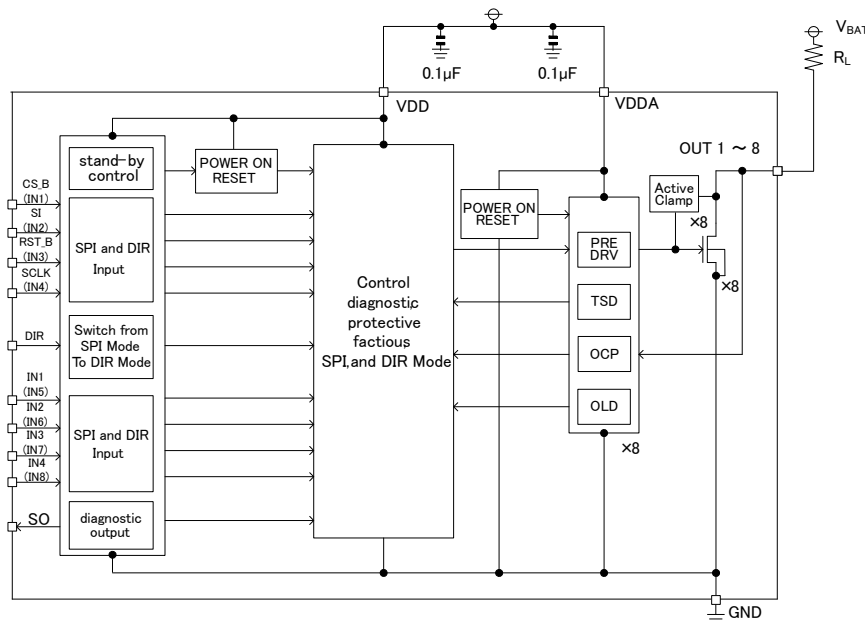
Overview

BD8LA700EFV is 8ch Low-Side switch for automotive and industrial equipment. It has a built-in, Open Load Detection circuit, Over Current Protection circuit, Active clamp circuit and Thermal Shutdown circuit.

Application

For driving resistive, inductive load

Basic Application Circuit (Recommendation)



Product Summary

Digital part Operating voltage	3.0V to 5.5V
Analog part Operating voltage	4.0V to 5.5V
On-state resistance (25°C, Typ)	700mΩ
Over current limit (Typ)	1.2A
Active clamp energy(25°C)	75mJ

Package

HTSSOP-B24

W(Typ) x D(Typ) x H(Max)
7.80mm x 7.60mm x 1.00mm



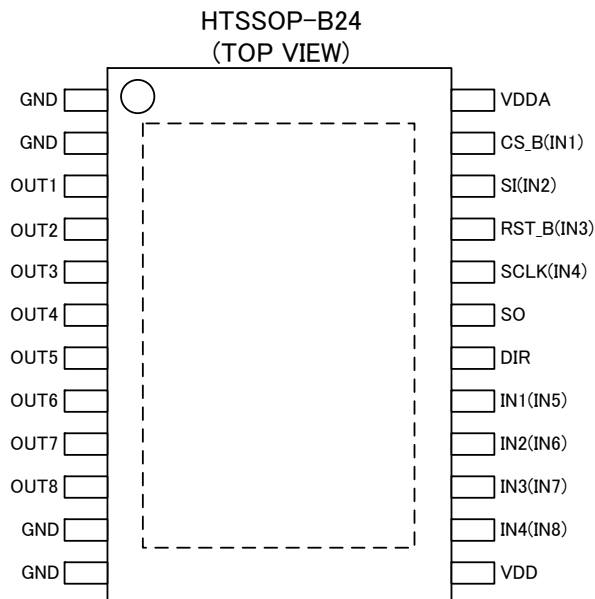
○Product configuration: Silicon monolithic integrated circuit ○The product is not designed for radiation resistance.

Pin Descriptions

Pin	Symbol	I/O ^(Note 1)		Function
1	GND	-		GND
2	GND	-		GND
3	OUT1	O		Channel 1 output
4	OUT2	O		Channel 2 output
5	OUT3	O		Channel 3 output
6	OUT4	O		Channel 4 output
7	OUT5	O		Channel 5 output
8	OUT6	O		Channel 6 output
9	OUT7	O		Channel 7 output
10	OUT8	O		Channel 8 output
11	GND	-		GND
12	GND	-		GND
13	VDD	-		Digital power supply
14	IN4(IN8)	I	PD	Control input for Channel 4 and 8 (DIR=L) / Control input for Channel 8 (DIR=H)
15	IN3(IN7)	I	PD	Control input for Channel 3 and 7 (DIR=L) / Control input for Channel 7 (DIR=H)
16	IN2(IN6)	I	PD	Control input for Channel 2 and 6 (DIR=L) / Control input for Channel 6 (DIR=H)
17	IN1(IN5)	I	PD	Control input for Channel 1 and 5 (DIR=L) / Control input for Channel 5 (DIR=H)
18	DIR	I	PD	SPI mode, DIR mode change input terminal
19	SO		O	Serial data output terminal
20	SCLK(IN4)	I	PD	Serial clock (DIR=L) / Control input for Channel 4 (DIR=H)
21	RST_B(IN3)	I	PD	Reset terminal (DIR=L) / Control input for Channel 3 (DIR=H)
22	SI(IN2)	I	PD	Serial data input (DIR=L) / Control input for Channel 2 (DIR=H)
23	CS_B(IN1)	I	PU/PD ^(Note 2)	SPI enable input (DIR=L) / Control input for Channel 1 (DIR=H)
24	VDDA	-		Analog power supply
FIN	FIN	-		Since it has connected with sub of IC, please connect the heat dissipation metal to external GND potential.

(Note 1) O : Output terminal, I : Input terminal
 PD : Pull Down terminal, PU : Pull Up terminal
 (Note 2) Pull Up at DIR=Low setting, Pull Down at DIR=High

Pin Configurations



Absolute Maximum Ratings

Item	Symbol	Limit values	Unit
Power supply voltage (Pin No:13,24)	V_{CC}	-0.3 to +7	V
Output voltage (Pin No:3 to 10)	$V_{DS1\sim 8}$	-0.3 to 45(Internally limited)	V
Output current (Pin No:3 to 10)	I_{Dn}	0.5(Internally limited) ^(Note 1)	A
Diagnostic output voltage (Pin No:19)	V_{SO}	-0.3 to +7	V
Input voltage(Pin No:14 to 18,20 to 23)	V_{IN}	-0.3 to +7	V
Junction temperature range	T_j	-40 to +150	°C
Storage temperature range	T_{stg}	-55 to +150	°C
Maximum junction temperature	T_{jmax}	150	°C
Active clamp energy (single pulse) ($T_{j(0)}=25^{\circ}C$)	E_{S1}	75 ^(Note 2)	mJ
Active clamp energy (single pulse) ($T_{j(0)}=150^{\circ}C$)	E_{S2}	25 ^(Note 3)	mJ
Active clamp energy (repetitive) ($T_{j(0)}=105^{\circ}C$)	E_{AR}	20 ^(Note 4)	mJ

(Note 1) However, never exceed T_{jmax} .

(Note 2) Max Active clamp energy at $T_{j(0)} = 25^{\circ}C$, using single non-repetitive pulse of 0.5A

(Note 3) Max Active clamp energy at $T_{j(0)} = 150^{\circ}C$, using single non-repetitive pulse of 0.5A. Not 100% tested.

(Note 4) Max Active clamp energy at $T_{j(0)} = 105^{\circ}C$, using repetitive pulse of 0.4A and cycles of 1M times. Not 100% tested.

Operating Voltage Ratings (-40°C ≤ T_j ≤ +150°C)

Item	Code	Limit values	Unit
Digital part Operating voltage	V_{DD}	3.0 to 5.5	V
Analog part Operating voltage	V_{DDA}	4.0 to 5.5	V

Electrical Characteristics (unless otherwise specified, $V_{DDA}=V_{DD}=5V$, $-40^{\circ}C \leq T_j \leq +150^{\circ}C$)

Item	Symbol	Limit values			Unit	Condition
		Min	Typ	Max		
[Power Supply Block]						
VDDA Standby current (All output on standby mode)	I_{DDAS}	-	0	20	μA	$V_{DDA}=V_{DD}=V_{CS_B}=5V$ $V_{RST_B}=0V$
VDD Standby current (All output on standby mode)	I_{DDS}	-	0	20	μA	$V_{DDA}=V_{DD}=V_{CS_B}=5V$ $V_{RST_B}=0V$
VDDA Operating current)	I_{DDA}	-	3.0	5.0	mA	$V_{DDA}=V_{DD}=5V$
VDD Operating current)	I_{DD}	-	0.5	1.0	mA	$V_{DDA}=V_{DD}=5V$
VDDA power on reset Threshold Voltage	V_{PORA}	-	-	4.0	V	
VDD power on reset Threshold Voltage	V_{POR}	-	-	2.7	V	
[Input PIN]						
L level input voltage	V_{INL}	0	-	$V_{DD} \times 0.2$	V	
H level input voltage	V_{INH}	$V_{DD} \times 0.7$	-	VDD	V	
Input Hysteresis	V_{HYS}	0.1	0.3	0.5	V	
L level input current 1 (RST_B,DIR,IN1 to IN4,SCLK,SI)	I_{INL1}	-10	0	10	μA	$V_{RST_B}, V_{DIR}, V_{IN1}$ to $V_{IN4}, V_{SCLK},$ $V_{SI}=0V$
L level input current 2(CS_B)	I_{INL2}	-100	-50	-25	μA	$V_{CS_B}=0V, V_{DIR}=0V$
L level input current 3(CS_B)	I_{INL3}	-10	0	10	μA	$V_{CS_B}=0V, V_{DIR}=5V$
H level input current 1 (RST_B,DIR,IN1 to IN4,SCLK,SI)	I_{INH1}	25	50	100	μA	$V_{RST_B}, V_{DIR}, V_{IN1}$ to $V_{IN4}, V_{SCLK},$ $V_{SI}=5V$
H level input current 2(CS_B)	I_{INH2}	-10	0	10	μA	$V_{CS_B}=5V, V_{DIR}=0V$
H level input current 3(CS_B)	I_{INH3}	25	50	100	μA	$V_{CS_B}=5V, V_{DIR}=5V$
[Power MOS Output]						
Output ON resistance	$R_{DS(ON)}$	-	0.70	0.87	Ω	$V_{DD}=V_{DDA}=5V, I_{Dn}^{(Note\ 1)}=0.2A,$ $T_j=25^{\circ}C$
		-	1.30	1.56	Ω	$V_{DD}=V_{DDA}=5V, I_{Dn}^{(note\ 1)}=0.2A,$ $T_j=150^{\circ}C$
Output leak current	$I_{L(OFF)}$	-	0	1	μA	$V_{DS}=30V, T_j=25^{\circ}C, V_{DIR}=0V$
		-	5	20	μA	$V_{DS}=30V, T_j=150^{\circ}C, V_{DIR}=0V$
Output leak current (Open load detected)	I_{OL}	15	40	90	μA	$V_{DS}=40V, V_{DIR}=5V$
Switching time	t_{ON}	-	30	50	μs	$V_{DD}=5V, V_{INn}^{(Note\ 1)}=0V/5V,$ $R_L=60\Omega, V_{BAT}=12V, V_{DIR}=5V$
	t_{OFF}	-	30	50	μs	$V_{DD}=5V, V_{INn}^{(Note\ 1)}=0V/5V,$ $R_L=60\Omega, V_{BAT}=12V, V_{DIR}=5V$
Slew rate on	dV/dt_{ON}	0.3	1.0	3.0	V/ μs	$V_{DD}=5V, V_{INn}^{(Note\ 1)}=0V/5V,$ $R_L=60\Omega, V_{BAT}=12V, V_{DIR}=5V,$ 80% to 20% of V_{BAT}
Slew rate off	$-dV/dt_{OFF}$	0.3	1.0	3.0	V/ μs	$V_{DD}=5V, V_{INn}^{(Note\ 1)}=0V/5V,$ $R_L=60\Omega, V_{BAT}=12V, V_{DIR}=5V,$ 20% to 80% of V_{BAT}
PWM Output range	f_{PWM}	-	-	5	kHz	$V_{DD}=5V, V_{INn}^{(Note\ 1)}=0V/5V,$ $R_L=60\Omega, V_{DIR}=5V, V_{BAT}=12V$
Output clamp voltage	V_{CL}	45	50	55	V	$I_{Dn}^{(Note\ 1)}=1mA$ (output off state)

(Note 1) "n" shows the channel number.

Electrical Characteristics (unless otherwise specified, $V_{DDA}=V_{DD}=5V$, $-40^{\circ}C \leq T_j \leq +150^{\circ}C$)

Item	Symbol	Limit values			Unit	Condition
		Min	Typ	Max		
[Serial Output]						
L level output voltage	V_{SOL}	-	0.3	0.6	V	$I_{SO}=1mA$
H level output voltage	V_{SOH}	$V_{DD}-0.6$	$V_{DD}-0.3$	-	V	$I_{SO}=-1mA$
Serial out output leak current	$I_{SO(OFF)}$	-5	0	5	μA	
[Protect circuit]						
Over current detection current	$I_{OCP(ON)}$	0.5	1.2	2.0	A	
Over current detection time	t_{OCP}	400	1000	2200	μs	
Open load release voltage	$V_{OLD(OFF)}$	1.2	2.5	3.5	V	
Open load detection voltage	$V_{OLD(ON)}$	1.0	2.0	3.0	V	$V_{INn}^{(Note\ 1)}=0V$, $V_{DIR}=5V$
Open load detection time	t_{OLD}	50	150	600	μs	
TSD detection temperature ^(Note 2)	T_{jd}	-	175	-	$^{\circ}C$	

(Note 1) "n" shows the channel number.
 (Note 2) Not 100% tested..

Definition

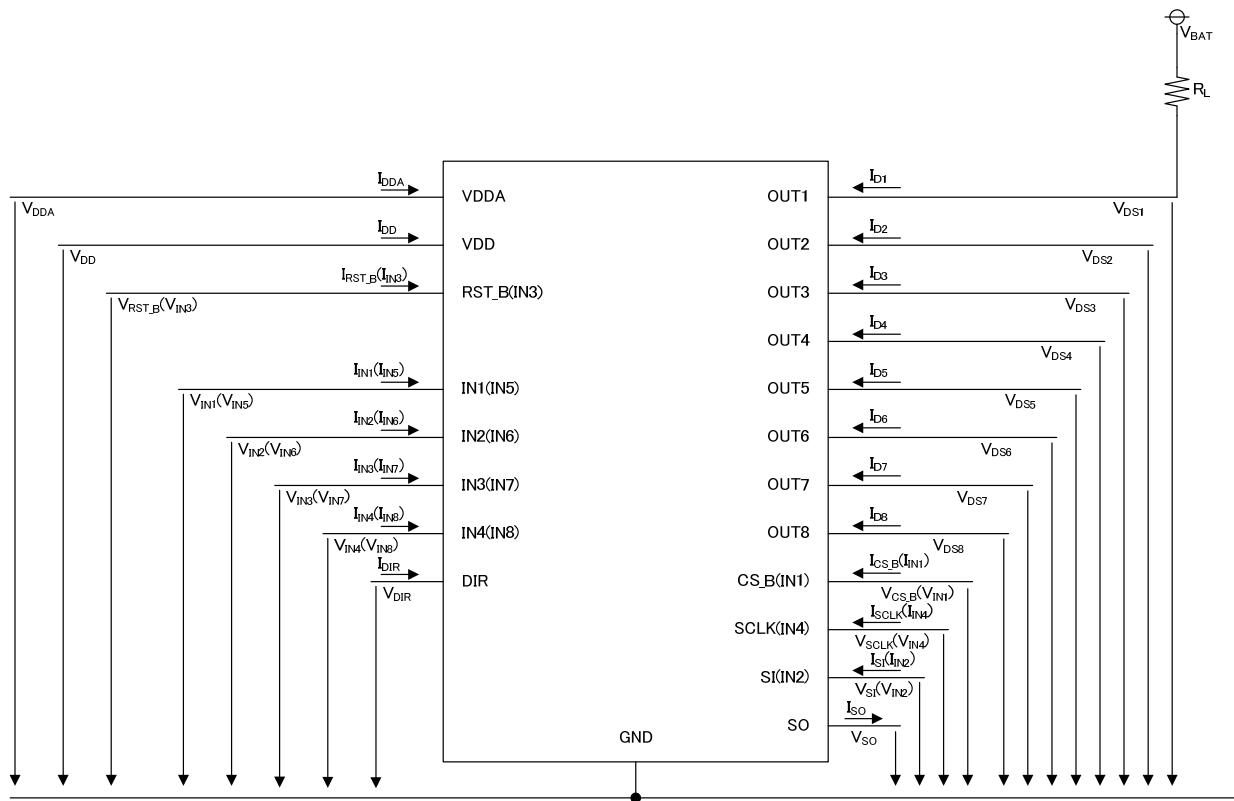


Figure 1. Definition

Measurement Circuit

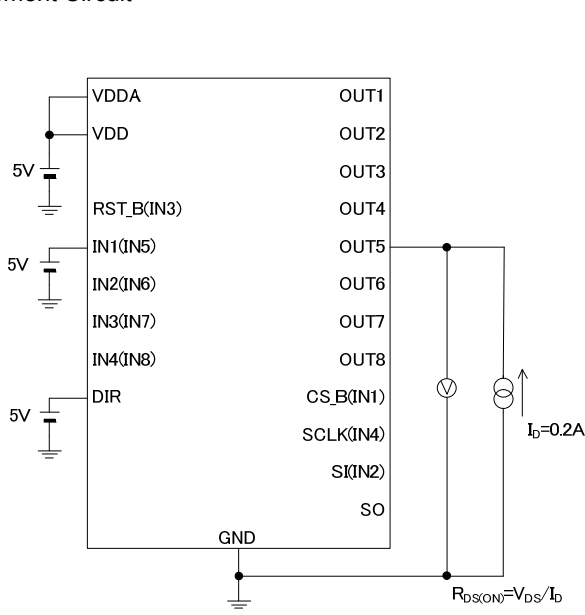


Figure 2. Output ON Resistance Measuring Circuit Diagram

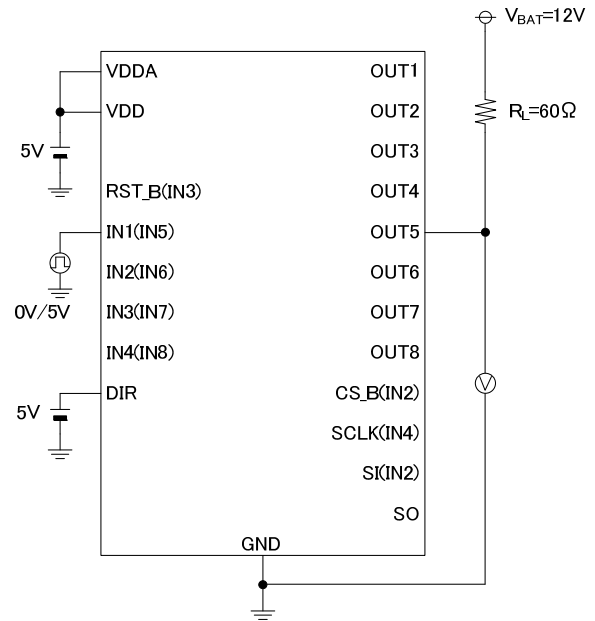


Figure 3. Switching Time Measuring Circuit Diagram

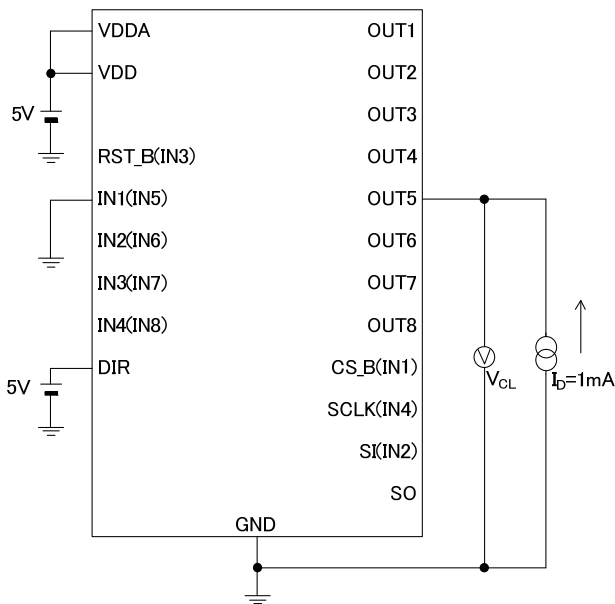


Figure 4. Output Clamp Voltage Measuring Circuit Diagram

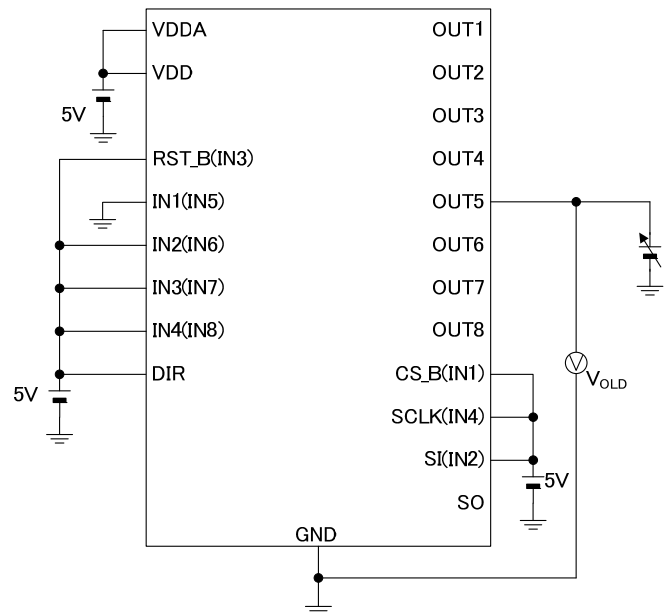


Figure 5. Open Detection Measuring Circuit Diagram

DIR(Direct)mode Diagnostic Output Truth Table

V _{IN}	TSD	OUTPUT		mode	V _{SO}	Output state
		V _{OUT}	I _{OUT}			
H	OFF	-	I _D < 0.5A	Normal	L	ON
			I _D ≥ 0.5 to 2.0A	Over current detection	H	OFF
	ON	-	-	Thermal shut down	H	OFF
L	-	V _{DS} > 3.0V	-	Normal	L	OFF
		V _{DS} ≤ 1.0 to 3.0V	-	Open load detection	H	OFF

Characteristic Data (Reference Data) ($V_{DD}=5V, V_{DDA}=5V, I_N=5V, T_J=25^{\circ}C$ unless otherwise is specified)

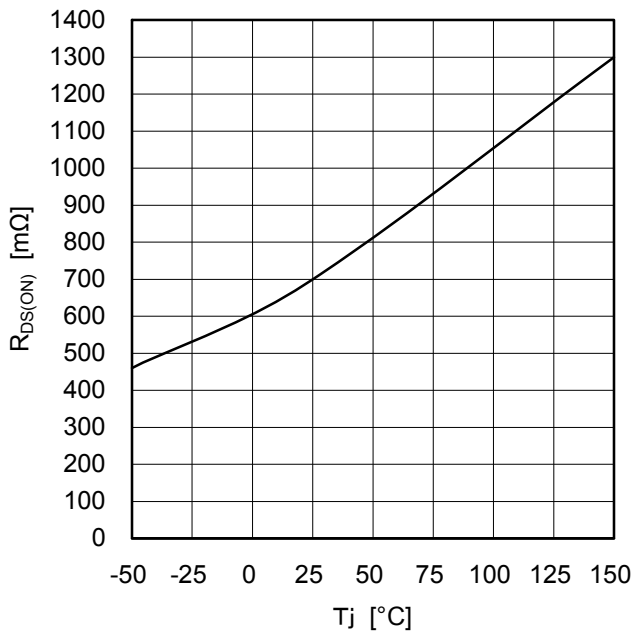


Figure 6. Output ON Resistance Characteristic [Temperature Characteristic]

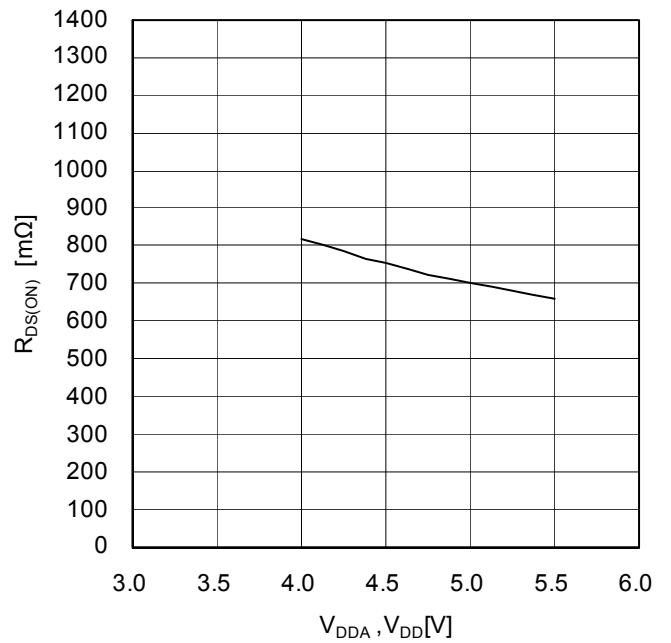


Figure 7. Output ON Resistance Characteristic [Source Voltage Characteristic]

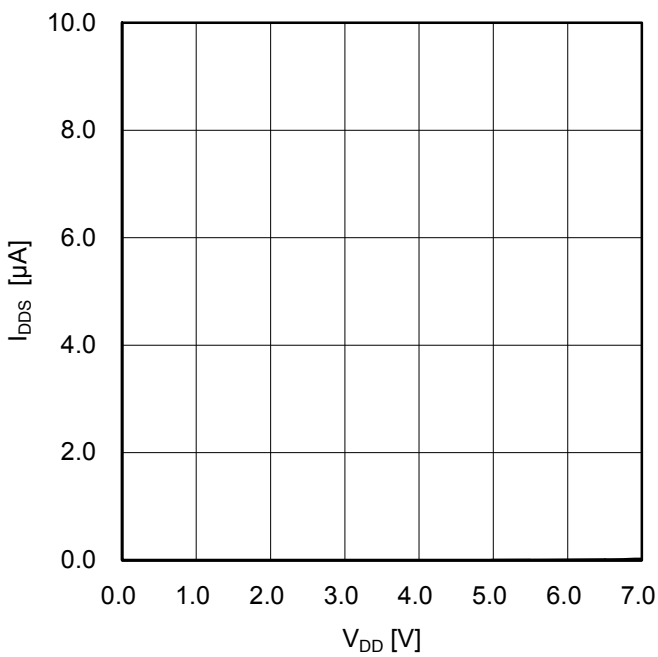


Figure 8. Standby Current Characteristic (VDD)

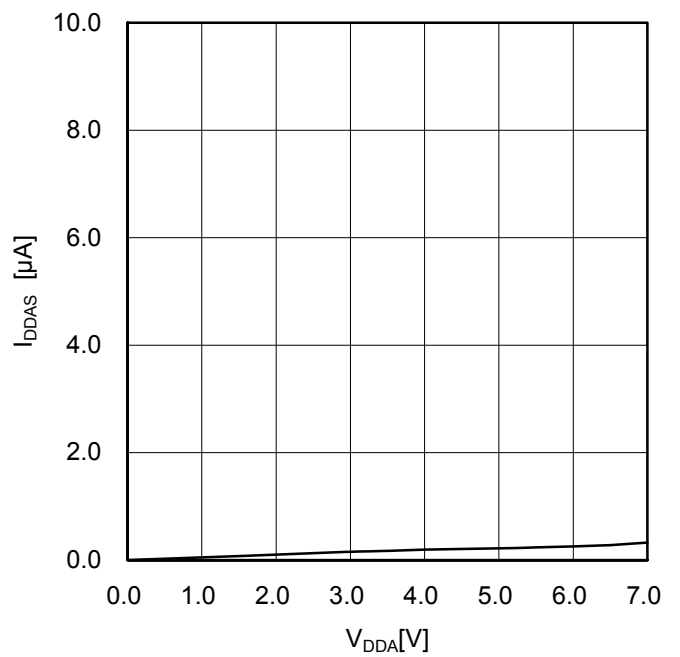


Figure 9. Standby Current Characteristic (VDDA)

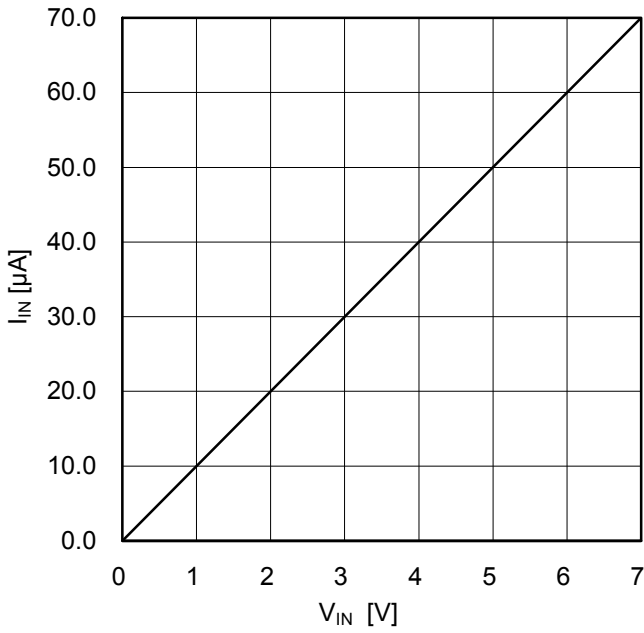


Figure 10. Input current Characteristic (IN1~4, DIR, SCLK, SI, RST_B, CS_B^(Note 1))

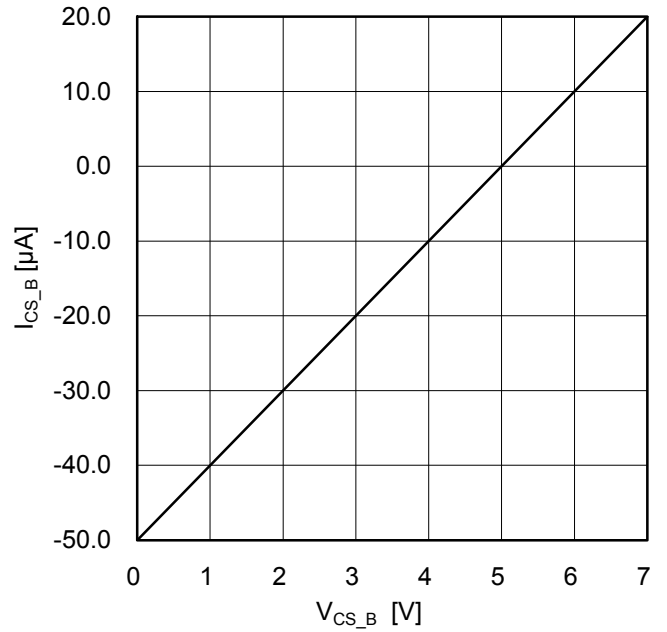


Figure 11. Input current Characteristic (CS_B)

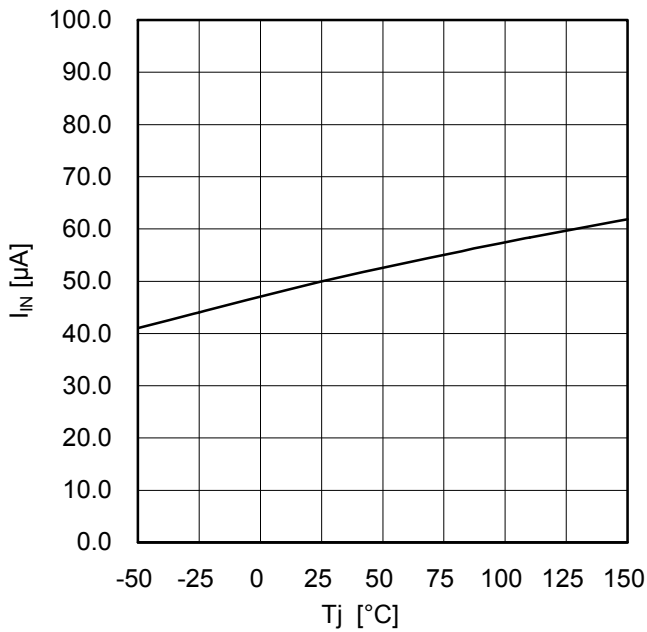


Figure 12. Input current Characteristic [Temperature Characteristic] (V_{IN1} to 4, V_{SCLK}, V_{SI}, V_{CS_B}^(Note 1), V_{RST_B}=5V) (Note 1)DIRMode

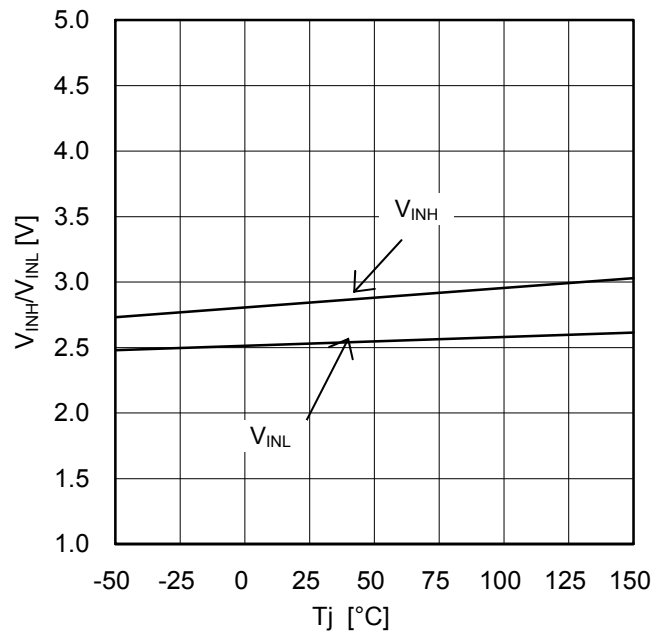


Figure 13. Input Voltage Threshold Characteristic [Temperature Characteristic]

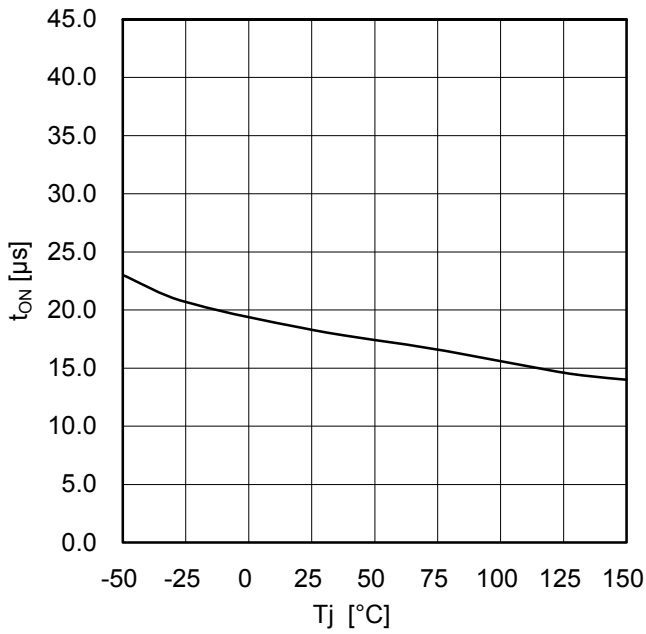


Figure 14. Switching Time (t_{ON}) [Temperature Characteristic]

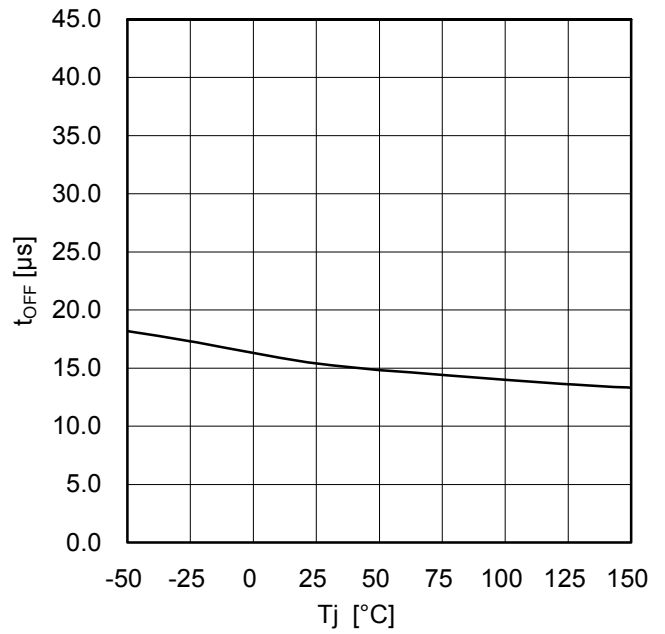


Figure 15. Switching Time (t_{OFF}) [Temperature Characteristic]

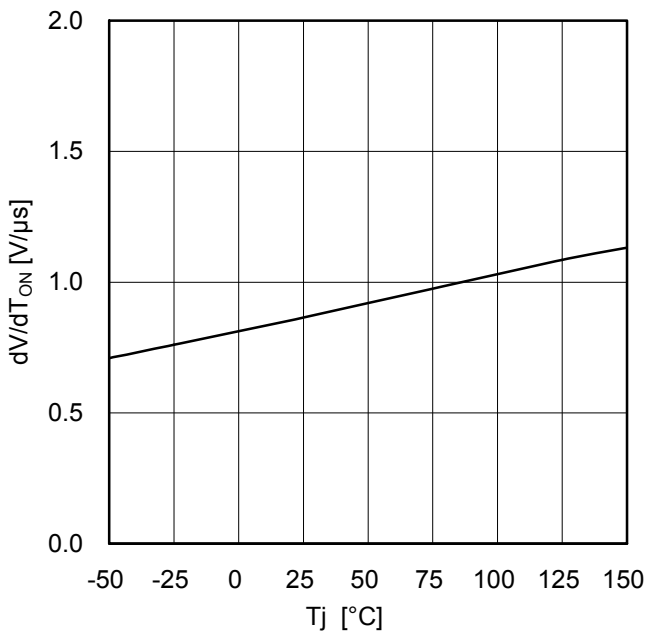


Figure 16. Slew Rate (at ON) [Temperature Characteristic]

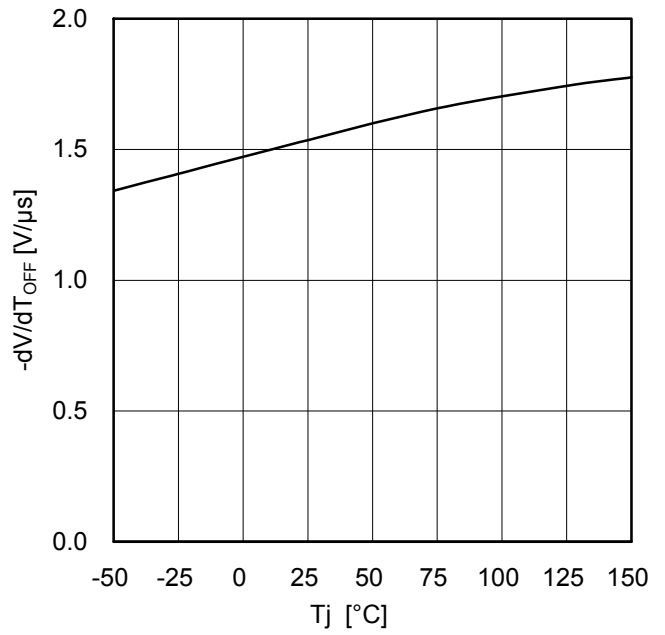


Figure 17. Slew Rate (at OFF) [Temperature Characteristic]

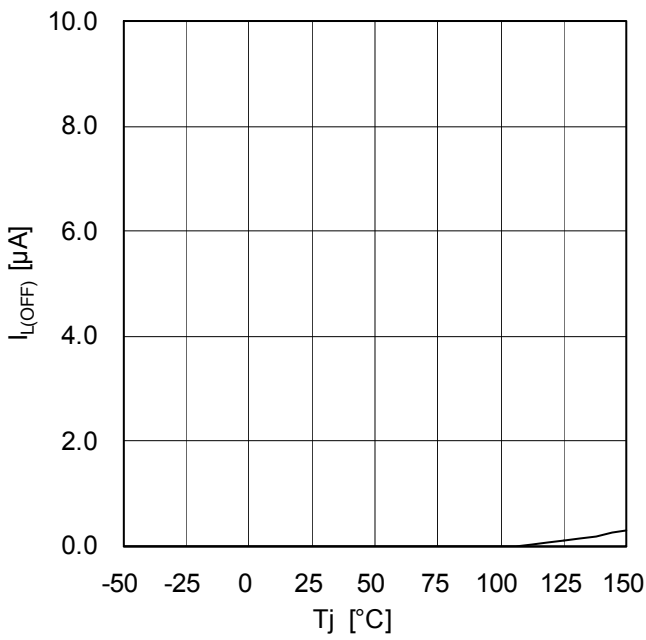


Figure 18. Output Leak Current [Temperature Characteristic]($V_{DS}=30V$)

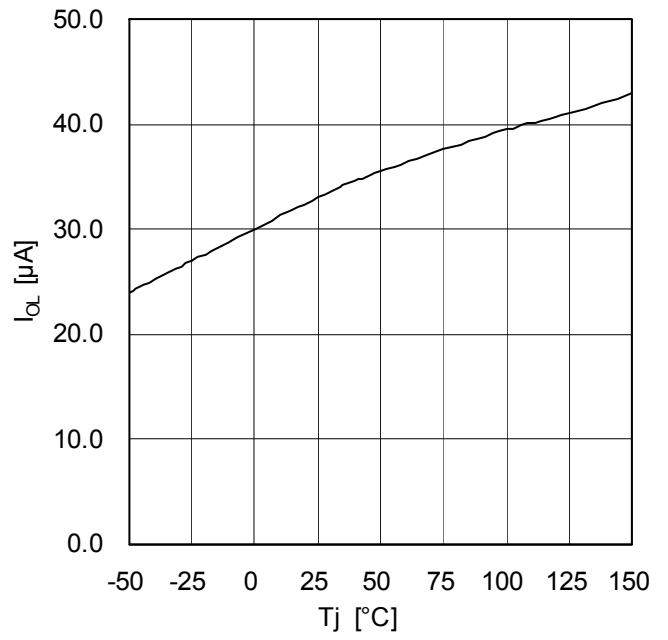


Figure 19. Output Leak Current (Open detect) [Temperature Characteristic]($V_{DS}=40V$)

Switching Time Measurement

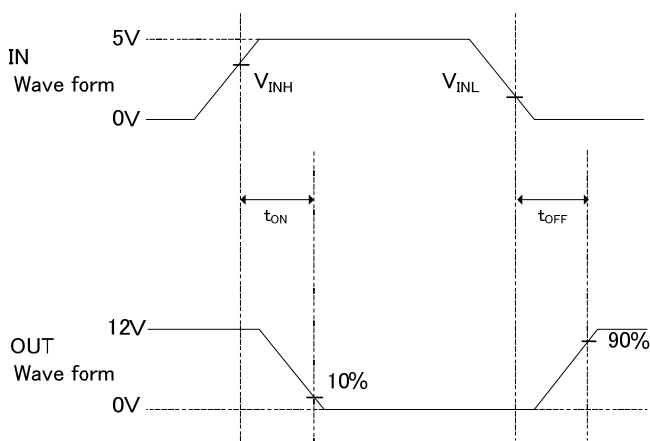


Figure 20. Switching Time

Timing Chart with Inductive Load

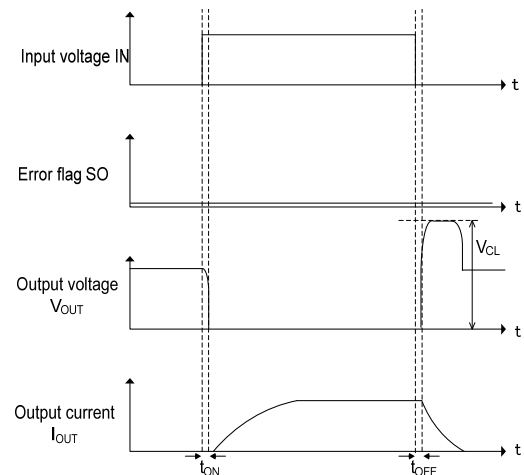


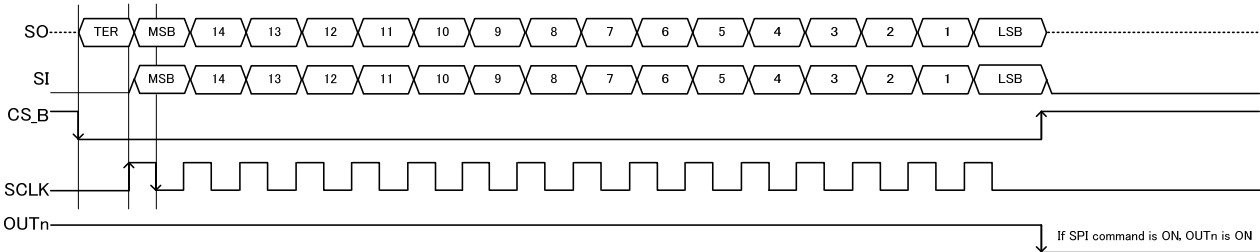
Figure 21. Timing Chart with inductive Load

I/O Equivalent Circuits

Pin	Symbol	I/O Equivalent Circuits
1,2, 11,12	GND	
3 to 10	OUT1 to OUT8	
13	VDD	
14 to 17 18 20 to 22	IN4(IN8), IN3(IN7), IN2(IN6), IN1(IN5), DIR, SCLK(IN4), RST_B(IN3), SI(IN2)	
19	SO	
23	CS_B	
24	VDDA	

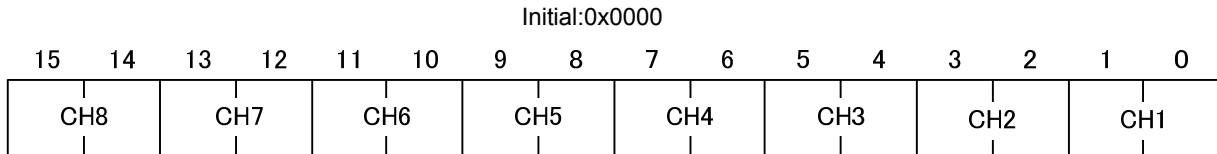
SPI mode

When CS_B=H,
 SO Terminal become Hi-Z
 When CS_B=L,
 Internal state (TSD, OCP, OLD) is latched at falling edge of CS_B, and output to SO at rising edge of SCLK.
 SI is taken in register at falling edge of SCLK.
 Output corresponding to each register input is controlled at rising edge of CS_B.



Definitions of SI and SO signals are shown below.

SI signals



Bits	CHn	States of output and protective circuits			
		Output	OCP	TSD	OLD
15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0	00	OFF	disable	disable	disable
	01	ON/OFF ^(Note 1)	enable/disable	enable/disable	disable/enable
	10	ON	enable	enable	disable
	11	OFF	disable	disable	enable

(Note 1) When INn=01, output is controlled by IN terminal.

Output controlled by each input is shown below.

Input	Controlled output
IN1(IN5)	OUT1
IN2(IN6)	OUT2
IN3(IN7)	OUT3
IN4(IN8)	OUT4
IN1(IN5)	OUT5
IN2(IN6)	OUT6
IN3(IN7)	OUT7
IN4(IN8)	OUT8

SO signals

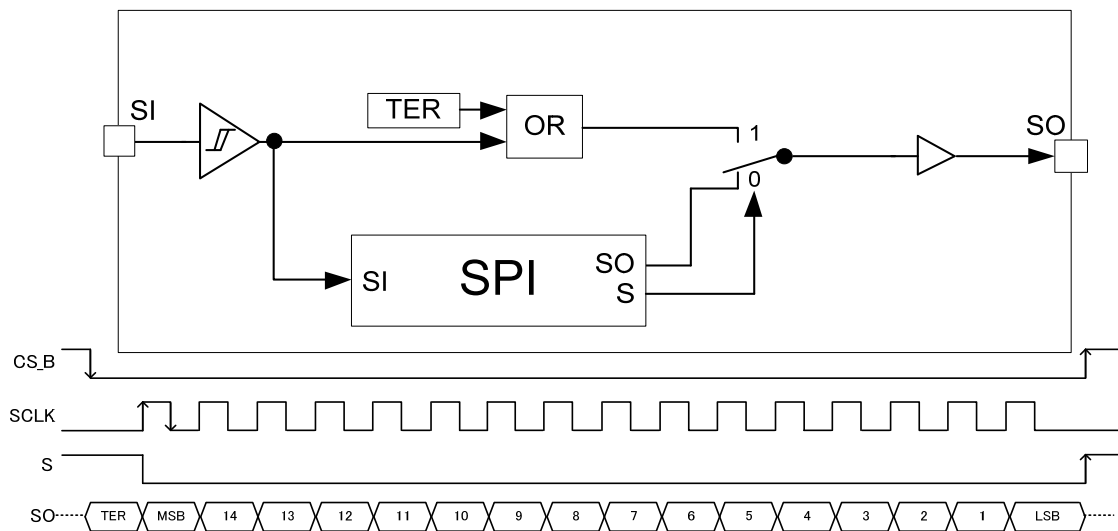
When CS_B=H,
SO Terminal become Hi-Z

When CS_B=L,
Explanation of each Bit is shown below.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TER	OL8	D8	OL7	D7	OL6	D6	OL5	D5	OL4	D4	OL3	D3	OL2	D2	OL1	D1
OUT8		OUT7		OUT6		OUT5		OUT4		OUT3		OUT2		OUT1		

Field	Bits	Data	STATE
TER	16 ^(Note 1)	0	Correspondence just after reset and normal operation
		1	Correspondence error of last time
OLn (n = 8 to 1)	15,13,11 9,7,5 3,1	0	Normal operation
		1	Load open
Dn (n = 8 to 1)	14,12 10,8,6 4,2,0	0	Normal operation
		1	OCD or TSD

(Note 1) TER bit outputs logical sums of TER signal and input signal of this device with SI signal in the interval from fall of CS_B to rise of SCLK as shown below.
Block diagram and timing chart are shown below.



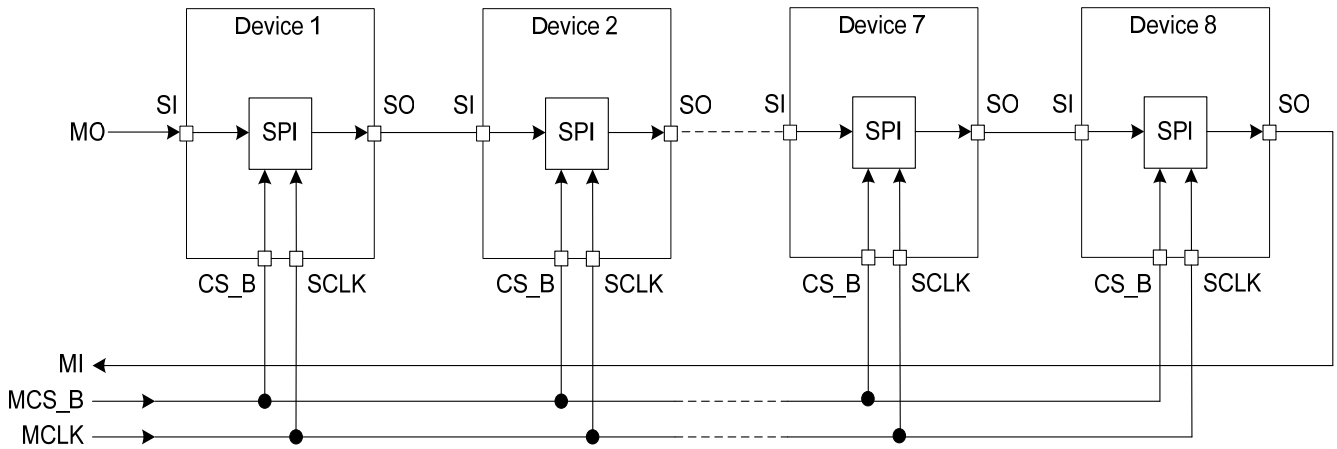
In order to select whether TER signal is output or SPI data output (OLn, Dn) signal is output, “S” signal is generated within IC and output is switched.

Seroal Daisy Chain

Plurality of devices can be connected as shown in the diagram below.

CS_B signal and SCLK signal connect common signal.

SI/SO line can connect SO of Device 1 to SI of Device 2 as shown in the diagram below.



Timing chart when 8 devices are connected is shown below.

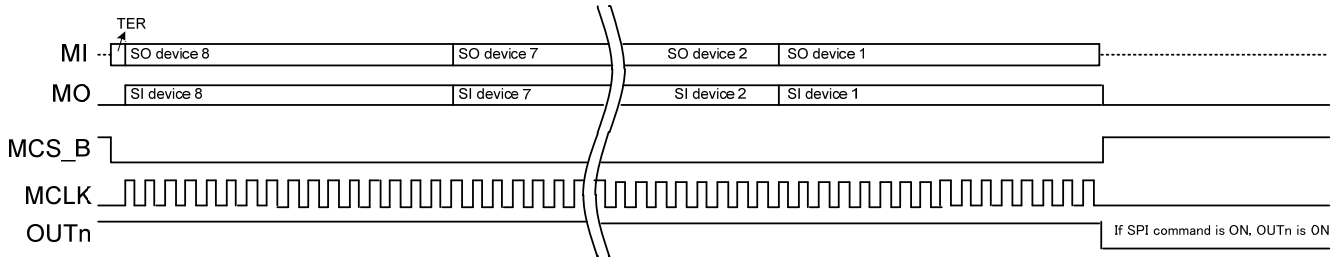
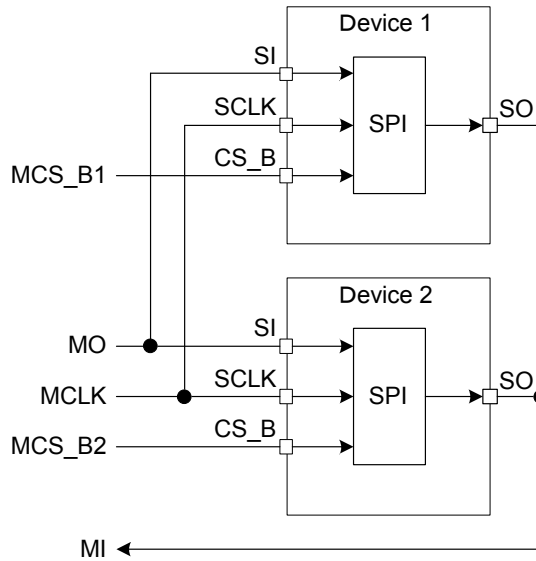


Figure 22. Timing chart when 8 devices are connected

Parallel Connection

Plurality of devices can be connected to parallel as shown in the diagram below.
 SI signal, SCLK signal and SO signal connect common signal.
 Each signal is necessary every each device for the CS_B signal.



Timing chart when 2 devices are connected is shown below.

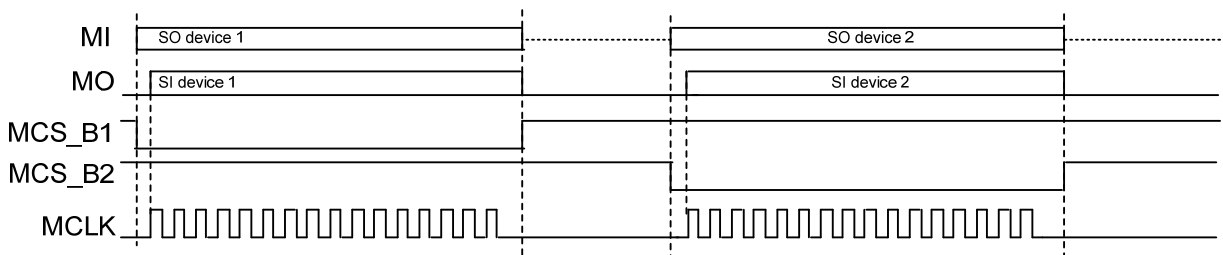


Figure 23. Timing chart when 2 devices are connected

SPI RST_B releasing sequence

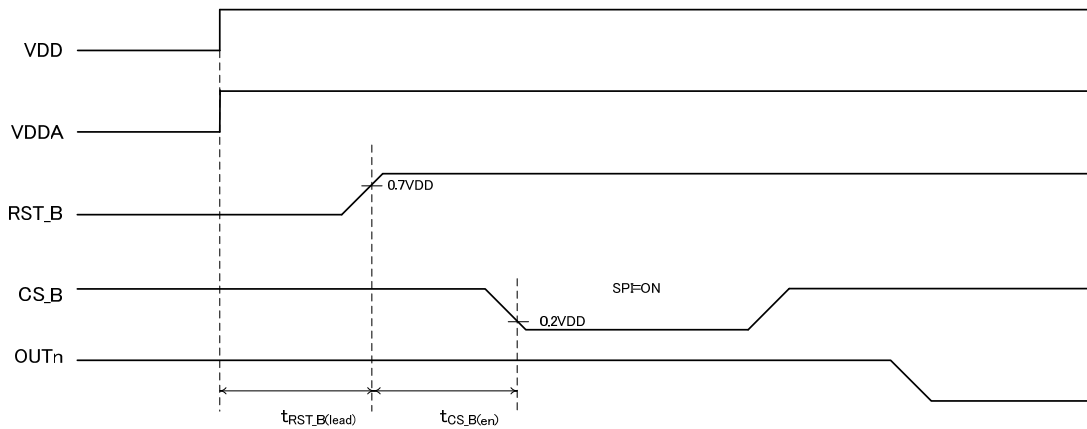


Figure 24. RST_B Releasing Sequence

Item	Symbol	Min	Typ	Max	Unit
RST_B lead time ^(Note 1) ^(Note 2)	t _{RST_B (lead)}	1	-	-	ms
CS_B enable time ^(Note 1)	t _{CS_B (en)}	10	-	-	μs

(Note 1) Not 100% tested

(Note 2) RST_B L time and H time must be over 10μs

SPI timing chart

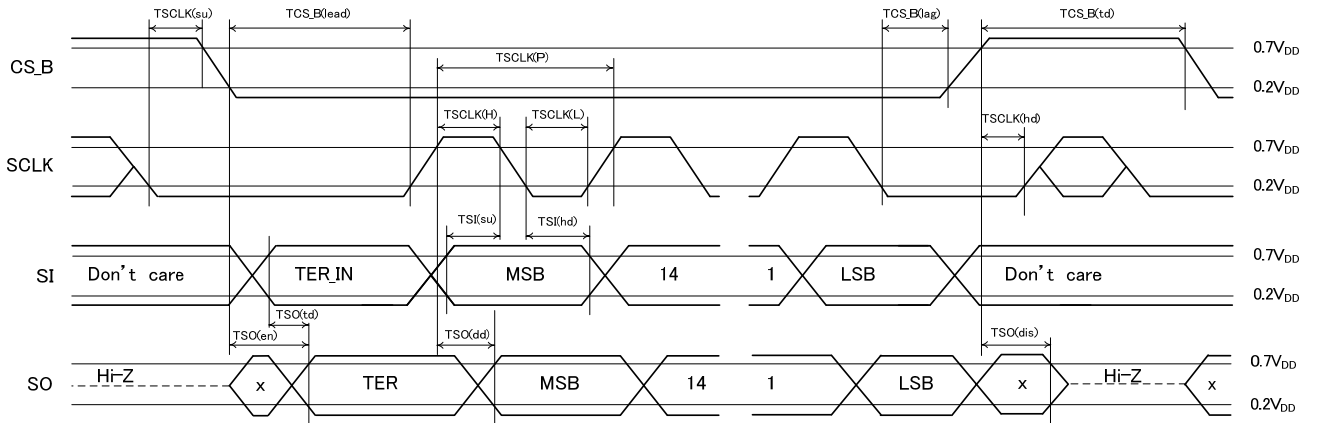


Figure 25. SPI Timing Chart

Item	Symbol	Min	Typ	Max	Unit
SCLK frequency	f _{SCLK}	0	—	5	MHz
SCLK cycle length	T _{SCLK(P)}	200	—	—	ns
SCLK high time	T _{SCLK(H)}	50	—	—	ns
SCLK low time	T _{SCLK(L)}	50	—	—	ns
SCLK setup time	T _{SCLK(su)}	50	—	—	ns
SCLK hold time	T _{SCLK(hd)}	50	—	—	ns
CS_B lead time	T _{C_S_B(lead)}	250	—	—	ns
CS_B lag time	T _{C_S_B(lag)}	250	—	—	ns
Transfer delay time	T _{C_S_B(td)}	250	—	—	ns
Data setup time	T _{SI(su)}	20	—	—	ns
Data hold time	T _{SI(hd)}	20	—	—	ns
SPI Output enable time ^(Note 1)	T _{SO(en)}	—	—	200	ns
SPI Output disable time ^(Note 1)	T _{SO(dis)}	—	—	250	ns
SPI Output Data delay time ^{(Note 1), (Note 2)}	T _{SO(dd)}	—	—	100	ns
ERR Output Through delay time ^(Note 1)	T _{SO(td)}	—	—	200	ns

(Note 1) Not 100% tested.

(Note 2) When SO terminal capacity=10pF, 3.0V ≤ V_{DD} ≤ 5.5V. Refer to Figure 25 and Figure 26.

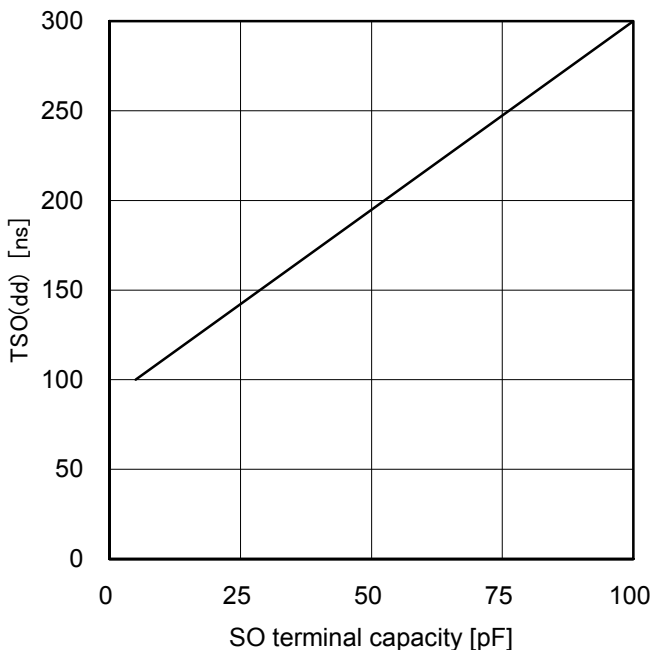


Figure 26. Max of SPI Output Data delay time (3.0V ≤ V_{DD} < 4.5V)

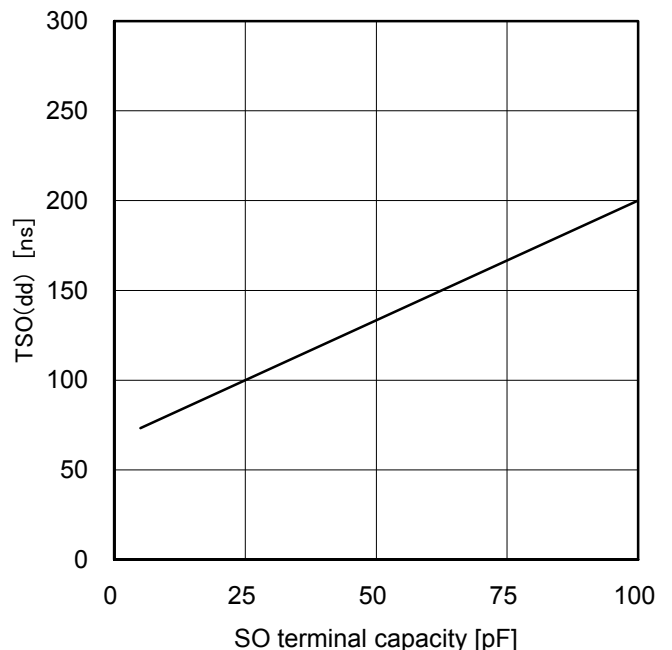


Figure 27. Max of SPI Output Data delay time (4.5V ≤ V_{DD} ≤ 5.5V)

DIR (direct) mode

Transition to direct mode is brought about by switching DIR terminal to High.
 Output controlled for each input is shown below.
 Further, SPI input and RST_B input are not accepted during direct mode.

Input Pin	Controlled Output
CS_B(IN1)	OUT1
SI(IN2)	OUT2
RST_B(IN3)	OUT3
SCLK(IN4)	OUT4
IN1(IN5)	OUT5
IN2(IN6)	OUT6
IN3(IN7)	OUT7
IN4(IN8)	OUT8

DIR (direct) mode timing chart (1)

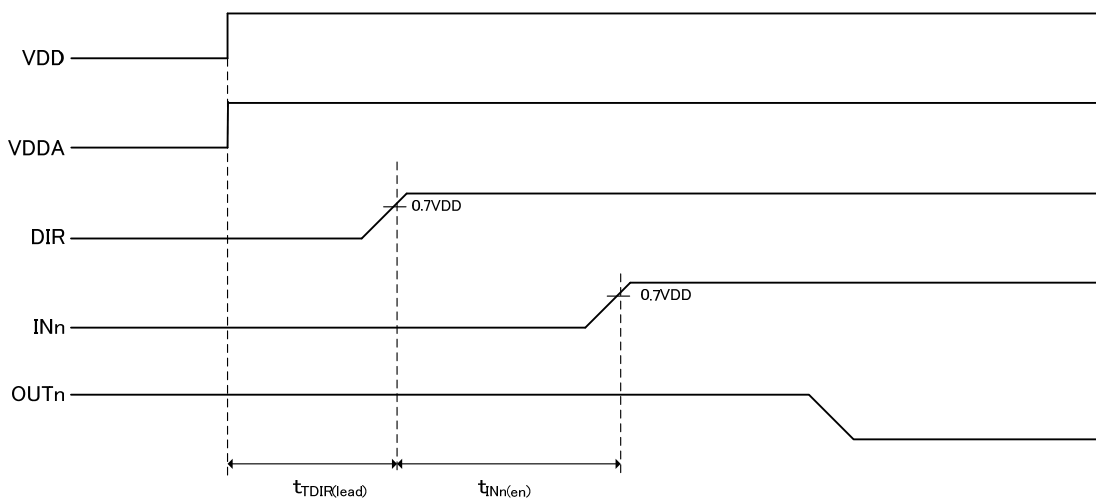


Figure 28. DIR Mode Timing Chart (1)

Item	Symbol	Min	Typ	Max	Unit
DIR lead time ^(Note 1)	$t_{DIR(lead)}$	1	-	-	ms
INn enable time ^(Note 1)	$t_{INn(en)}$	10	-	-	μs

(Note 1) Not 100% tested.

DIR (direct) mode timing chart (2)

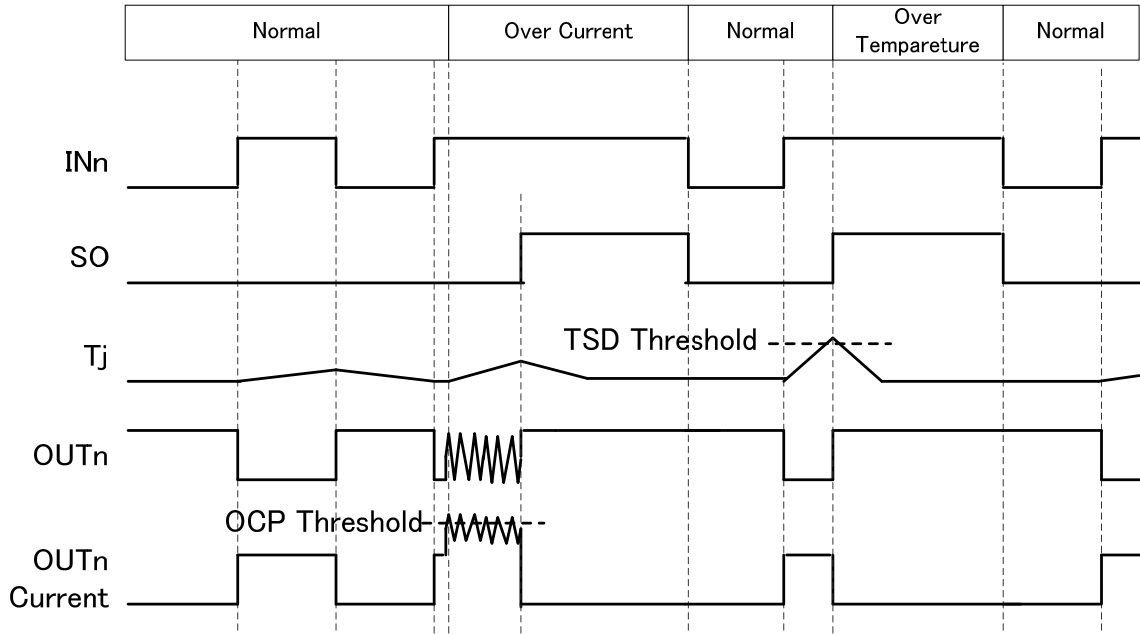


Figure 29. DIR Mode Timing Chart (2)

Direct mode operation current ($I_{DDA} + I_{DD}$) state transition

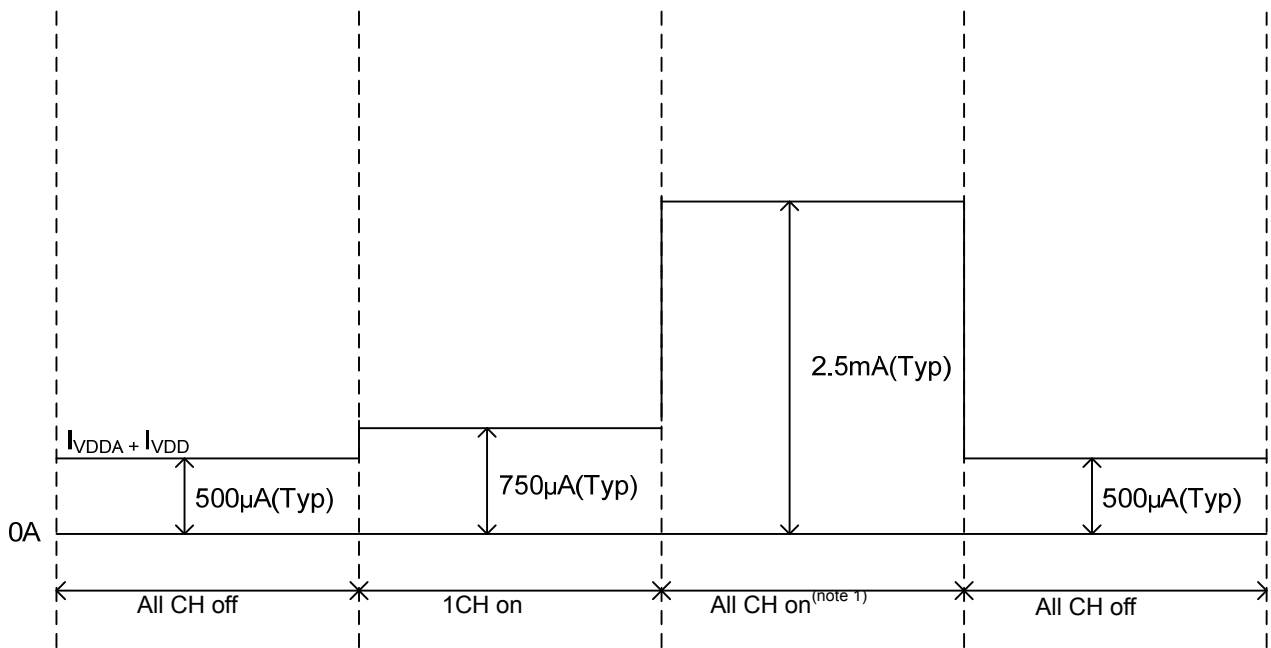


Figure 30. Operation Current State Transition Diagram

(Note 1) Sum of P.4 VDDA operation current (when all outputs are on) and VDD operation current (when all outputs are on).

Power source ON/OFF sequence

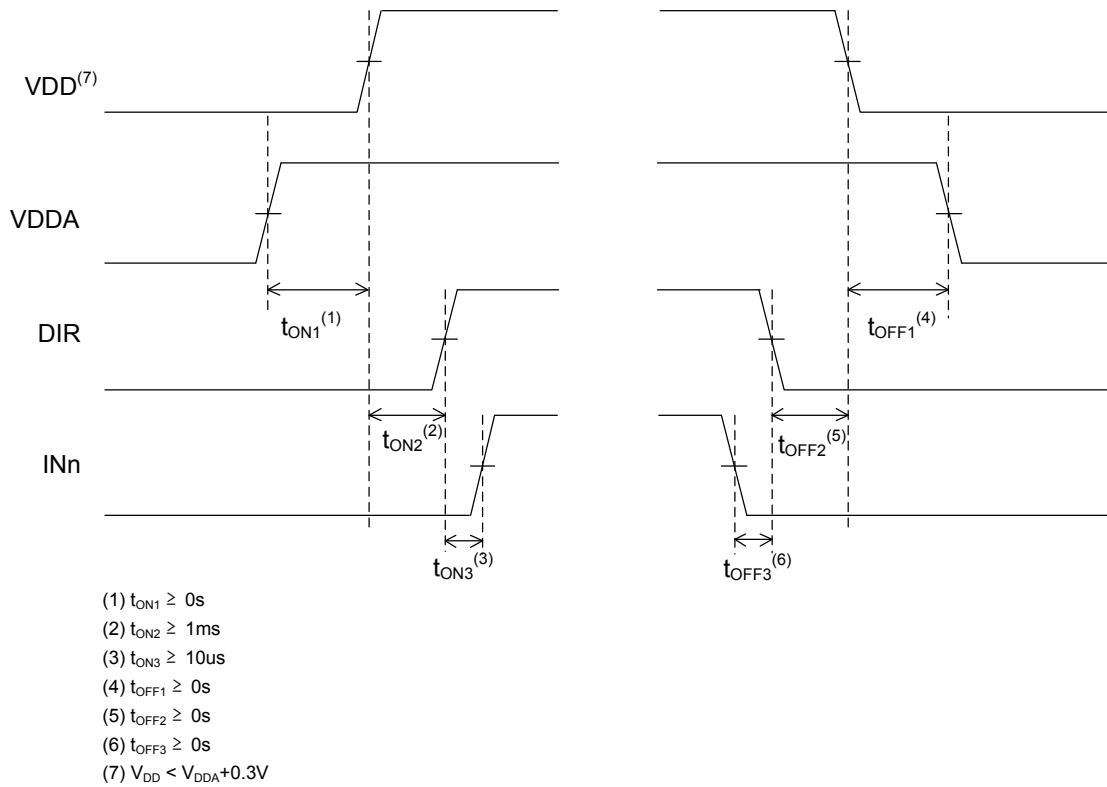


Figure 31. Power Source ON/OFF Sequence

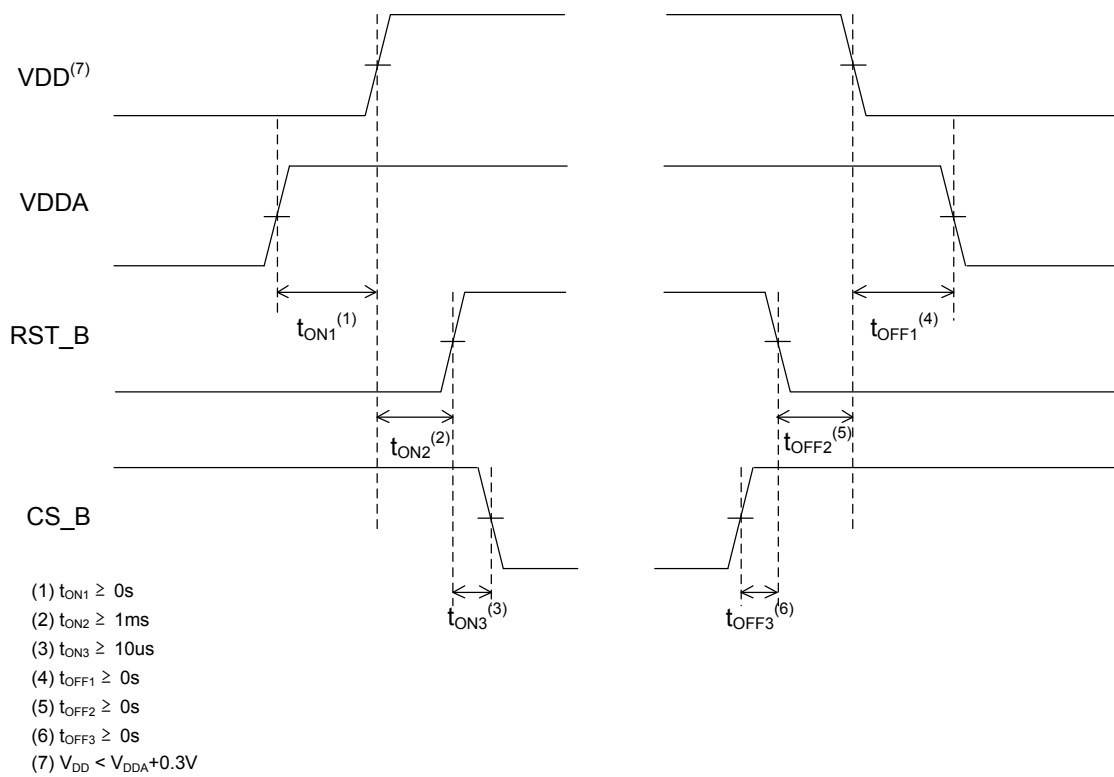


Figure 32. Power Source ON/OFF Sequence (SPI MODE)

Detection functions

① Overcurrent protection

When current of no less than 1.2A (Typ) is flown in output transistor of from OUT1 to OUT8 in 1000µs (Typ), the error flag is output. The error flag is released by OUTENn^(Note 1) becoming L^(Note 2).

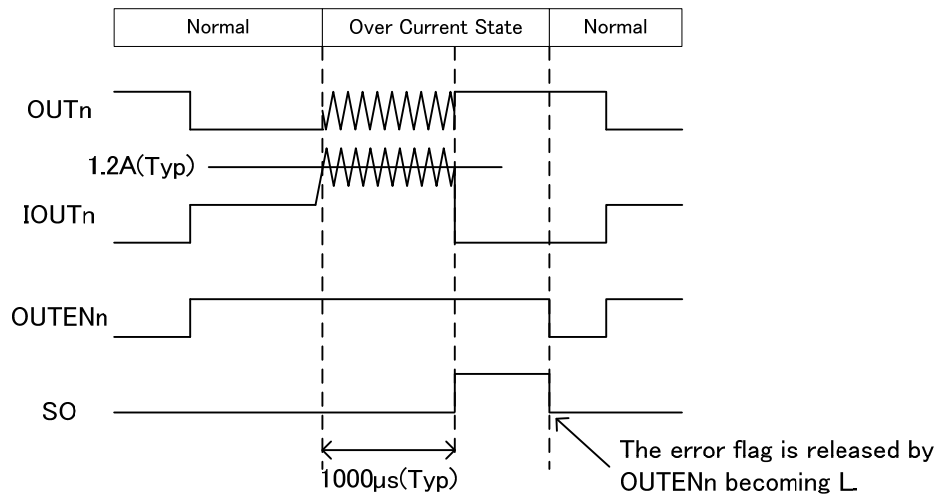


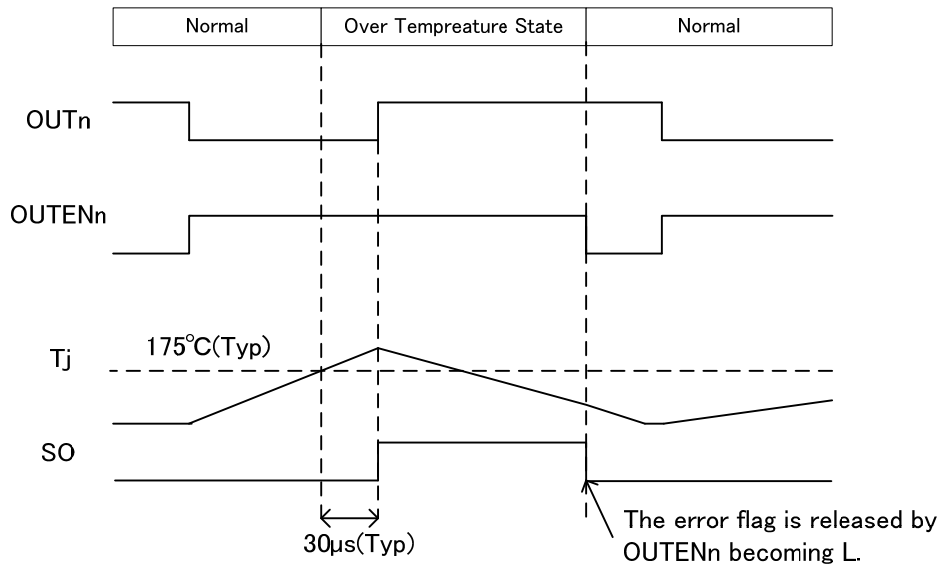
Figure 33. Overcurrent Protection Timing Chart

(Note 1) OUTENn shows the ON/OFF control signal of the OUT terminals. "n" shows the channel number.

(Note 2) The over current detection latch timer is cleared, and the error flag is not output when OUTENn become L before Over current detection time(Typ:1000µs Max: 2200µs).

② Overheat protection

When T_j of from OUT1 to OUT8 reaches 175°C (Typ) or above and it passes for $30\mu\text{s}$ (Typ), output is turned off.
The error flag is released by $\text{OUTENn}^{(\text{Note 1})}$ becoming L^(Note 2).



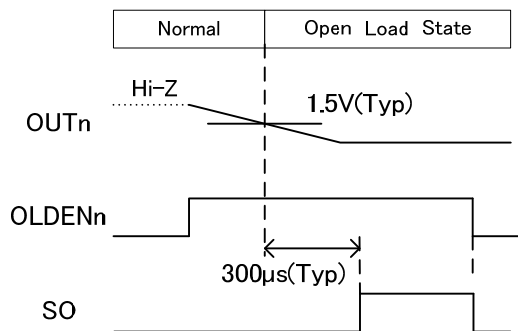
(Note 1) OUTENn shows the ON/OFF control signal of the OUT terminals. n shows the channel number.

(Note 2) The overheat detection latch timer is cleared, and the error flag is not output when OUTENn become L before Overheat detection time(Typ:30µs Max: 65µs).

Figure 34. Overheat Protection Timing Chart

③ Open detection

In case of enable at Open detection function^(Note 3), when output voltage of from OUT1 to OUT8 falls below 1.5V (Typ), open detection is detected and the error flag is output.



(Note 3) As for the DIR mode, $\text{OLDENn}=\text{H}$ (open detection function becomes effective) in $\text{OUTENn}=\text{L}$.

$40\mu\text{A}$ (Typ) is flown from OUT to GND because $60\text{k}\Omega$ (Typ) is connected between OUT and GND.

As for the SPI mode, Please refer to Page 13.

"n" shows the channel number.

Figure 35. Open Detection Protection Timing Chart

Thermal resistance ^(Note 1)

Item	Symbol	Typ	Unit	Condition
HTSSOP-B24				
Junction-Ambient thermal resistance	θ_{JA}	42	°C / W	1s ^(Note 2)
		30	°C / W	2s ^(Note 3)
		23	°C / W	2s2p ^(Note 4)
Junction-Package upper side ^(Note5) thermal characteristic parameter	Ψ_{JT}	4	°C / W	1s ^(Note 2)

- (Note 1) Based on JESD51 - 2A (Still-Air), in case of 8ch ON state
- (Note 2) Based on JESD51 - 3 FR4 114.3 mm x 76.2 mm x 1.57 mm 1 layer (1s)
(TOP Copper layer : ROHM original land pattern + wiring for measurement, copper thickness 2oz, copper area 600mm²)
- (Note 3) Based on JESD51 -5 FR4 114.3 mm x 76.2 mm x 1.60 mm 2 layer(2s)
(TOP Copper layer : ROHM original land pattern + wiring for measurement, Bottom Copper area : 74.2 mm x 74.2 mm, Copper thickness (Top and Bottom layers) 2oz)
- (Note 4) Based on JESD51 -5 / -7 FR4 114.3 mm x 76.2 mm x 1.60 mm 4 layers (2s2p)
(TOP Copper layer : ROHM original land pattern + wiring for measurement / 2nd, 3rd, Bottom layer Copper area : 74.2 mm x 74.2 mm, Copper thickness(Top and Bottom layers / Internal layers) 2oz / 1oz)
- (Note 5) T_T : The central temperature on the surface of molding is measured.

① PCB Layout 1s

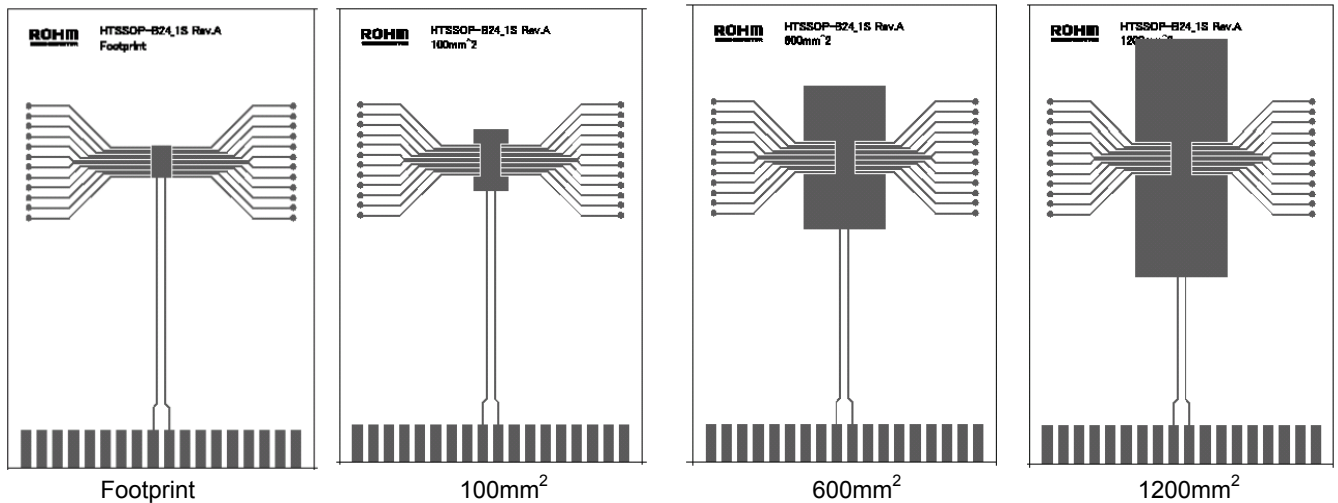


Figure 36. PCB Layout 1s

Dimension	Value
Board finish thickness	1.57 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu:2oz)
Heatsink copper area dimension	Footprint / 100mm ² / 600mm ² / 1200mm ²

② PCB Layout 2s

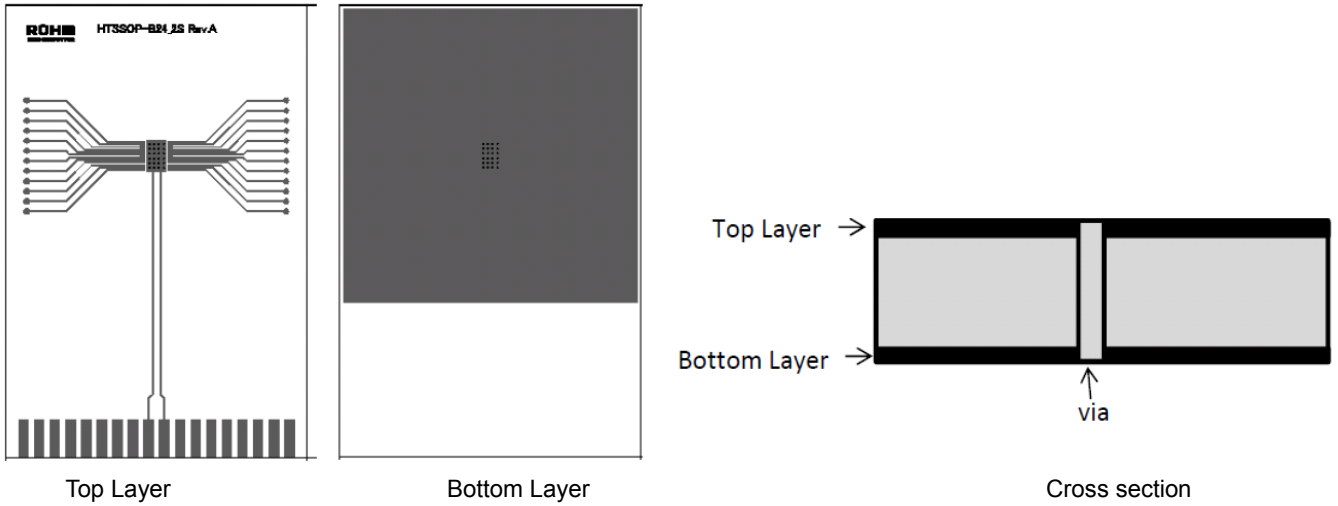


Figure 37. PCB Layout 2s

Dimension	Value
Board finish thickness	1.60 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu + Plating)
Therml vias separation / diameter	1.2mm / 0.3mm

③ PCB Layout 2s2p

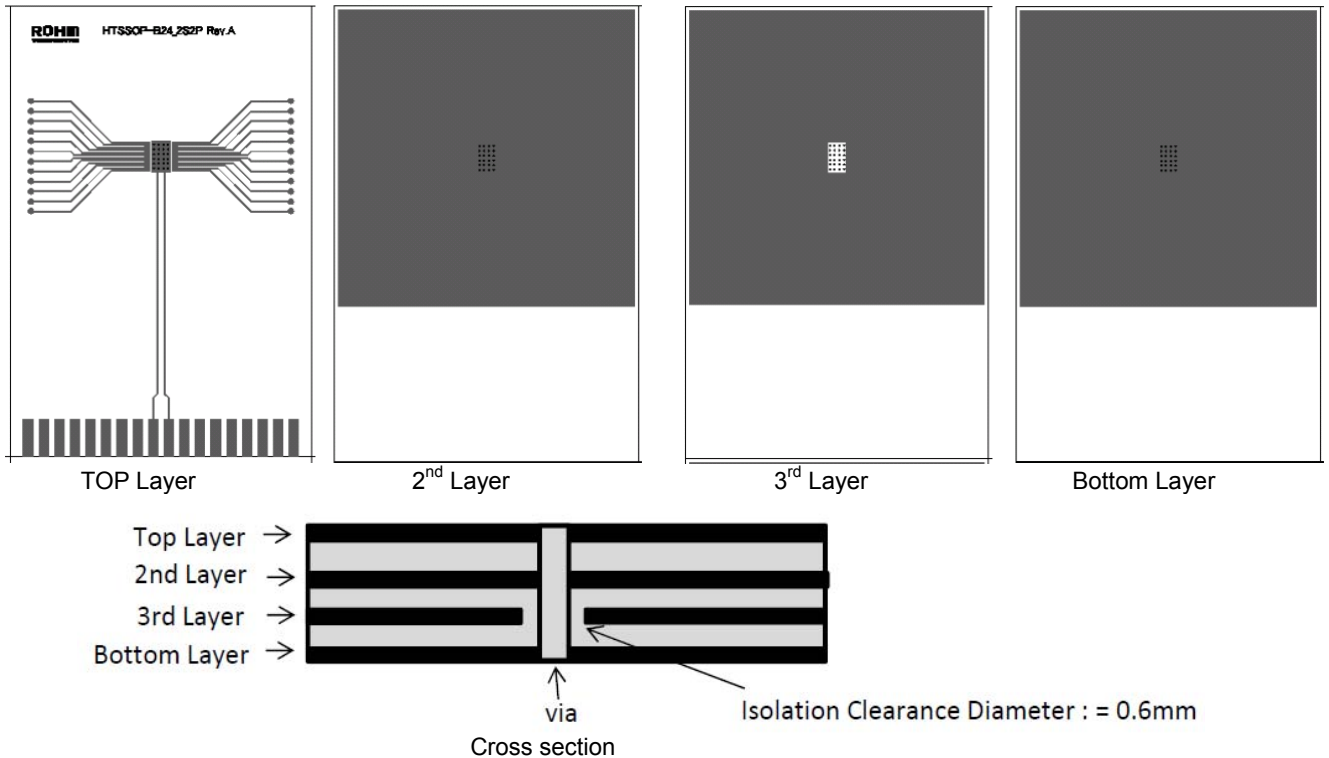


Figure 38. PCB Layout 2s2p

Dimension	Value
Board finish thickness	1.60 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu + Plating)
Copper thickness (Inner layers)	0.035mm
Therml vias separation / diameter	1.2mm / 0.3mm

④ Thermal impedance (Single pulse)

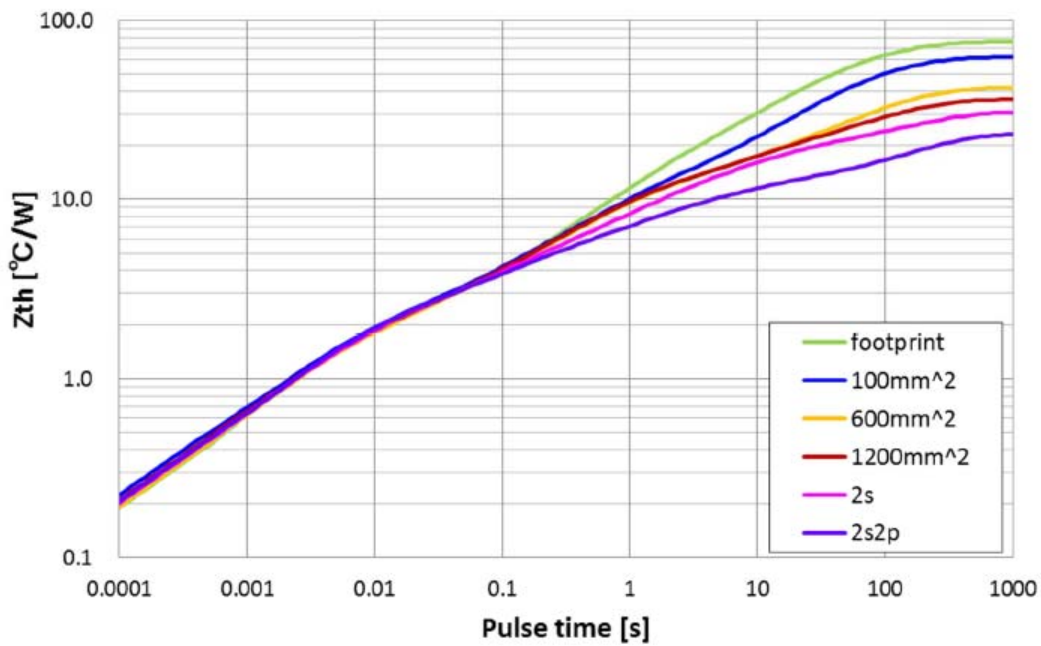


Figure 39. Thermal impedance

⑤ Thermal resistance (θ_{JA} / Ψ_{JT} vs PCB copper area - 1s)

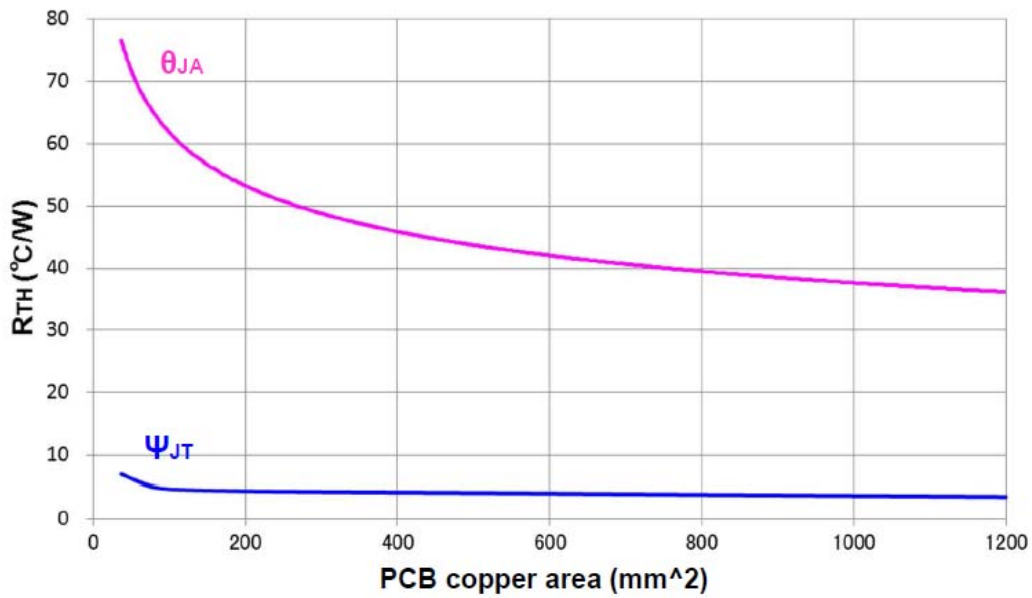


Figure 40. Thermal resistance