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Switching Regulator with external FET

3.9 to 30V, 2ch Synchronous Rectification Step-Down Controller

BD9015KV-M BD9016KV-M

General Description

The BD9015KV-M and BD9016KV-M are high performance synchronous rectification switching controllers with wide input range and dual channel output.
The synchronous rectification method comes with high efficiency making controller ideal for eco-designs(low power consumption) of numerous electronics.
All channels have enable pins, soft start functionality and power good outputs. Startup and shutdown can be controlled independently.
An integrated PLL circuit can be synchronized to an external 250kHz to 600kHz clock signal.

Features

- N channel MOSFET direct drive
- Synchronous rectification for increased efficiency
- Acceptable Low ESR ceramic capacitor at output
- Integrated PLL circuit for external synchronization; 250kHz to 600kHz
- Current mode control
- High side MOSFET current sensing
- Pre-bias functionality
- Independent ON/OFF control for all channels
- At Max Duty the oscillation frequency is slowed down to 1/5, reducing the input/output voltage difference.
- Low voltage and over voltage detection circuit at all outputs
  When the over voltage is detected, the L-side FET is OFF (BD9015KV-M). The L-side FET is ON (BD9016KV-M).
  Low side FET is ON (BD9016KV-M)
- Power good indicator pin (PGOOD)
- Integrated overcurrent protection with self recovery.

Key Specifications

- Input voltage range: 3.9 V to 30 V
- Output voltage range: 0.8 V to 10 V
- Accurate voltage reference:±1.5%(-40°C to +105°C)
- Switching frequency: 250 kHz to 550 kHz
- Shutdown current: 0μA (Typ)
- Operating temperature range: -40°C to + 105 °C

Package

	W (Typ) x D (Typ) x H (Max)
VQFP48C	9.00 mm x 9.00 mm x 1.60 mm

VQFP48C

Applications

- Car audio, Car navigation
- LCDTV, PDPTV, DVD, PC, etc..

Typical Application Circuit

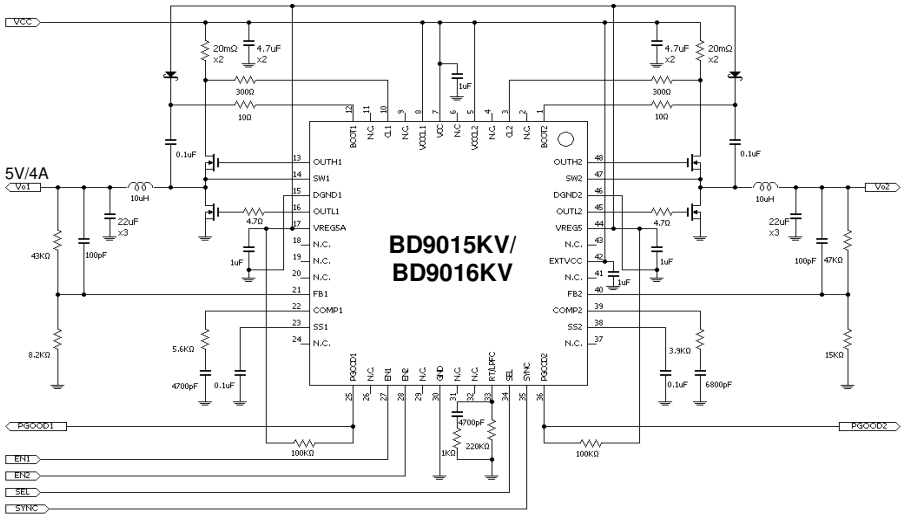


Figure 1. Typical Application Circuit

Pin Configuration

(TOP VIEW)

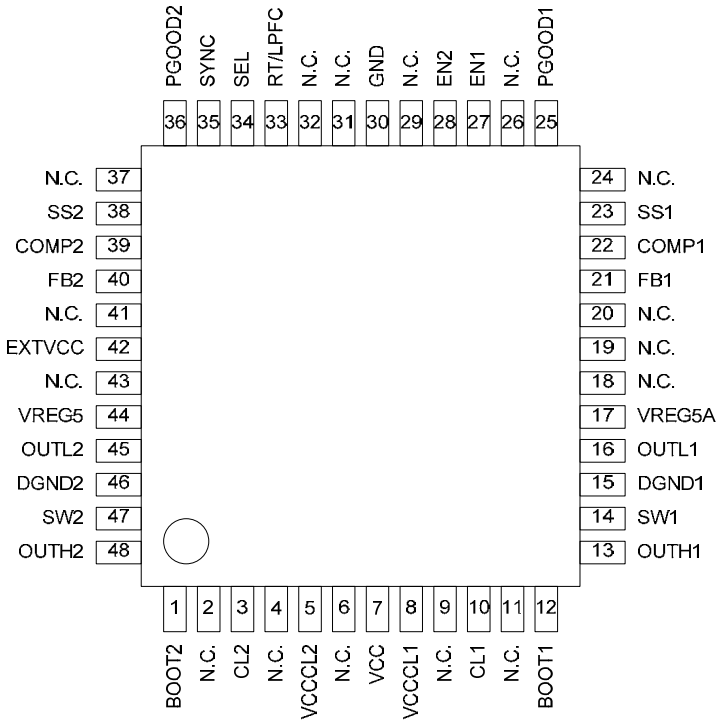


Figure 2. Pin Configuration

Pin Description

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	BOOT2	Power supply for OUTH2 driver	25	PGOOD1	Power good output pin 1
2	N.C.	Not connected	26	N.C.	Not connected
3	CL2	Current detection setting pin 2	27	EN1	Output 1 ON / OFF pin
4	N.C.	Not connected	28	EN2	Output 2 ON / OFF pin
5	VCCCL2	Power supply for current detection 2	29	N.C.	Not connected
6	N.C.	Not connected	30	GND	Ground pin
7	VCC	Power supply pin	31	N.C.	Not connected
8	VCCCL1	Power supply for current detection 1	32	N.C.	Not connected
9	N.C.	Not connected	33	RT/LPFC	Oscillation frequency setting / filter connection pin
10	CL1	Current detection setting pin 1	34	SEL	External synchronization select pin
11	N.C.	Not connected	35	SYNC	External synchronization pulse input pin
12	BOOT1	Power supply for OUTH1 driver	36	PGOOD2	Power good output pin 2
13	OUTH1	High side FET gate pin 1	37	N.C.	Not connected
14	SW1	High side FET source pin 1	38	SS2	Soft start time setting pin 2
15	DGND1	Low side FET source pin 1	39	COMP2	Error amp output 2
16	OUTL1	Low side FET gate pin 1	40	FB2	Error amp input 2
17	VREG5A	REG input for FET driver pin	41	N.C.	Not connected
18	N.C.	Not connected	42	EXTVCC	External power supply input pin
19	N.C.	Not connected	43	N.C.	Not connected
20	N.C.	Not connected	44	VREG5	REG output for FET driver pin
21	FB1	Error amp input 1	45	OUTL2	Low side FET gate pin 2
22	COMP1	Error amp output 1	46	DGND2	Low side FET source pin 2
23	SS1	Soft start time setting pin 1	47	SW2	High side FET source pin 2
24	N.C.	Not connected	48	OUTH2	High side FET gate pin 2

Block Diagram

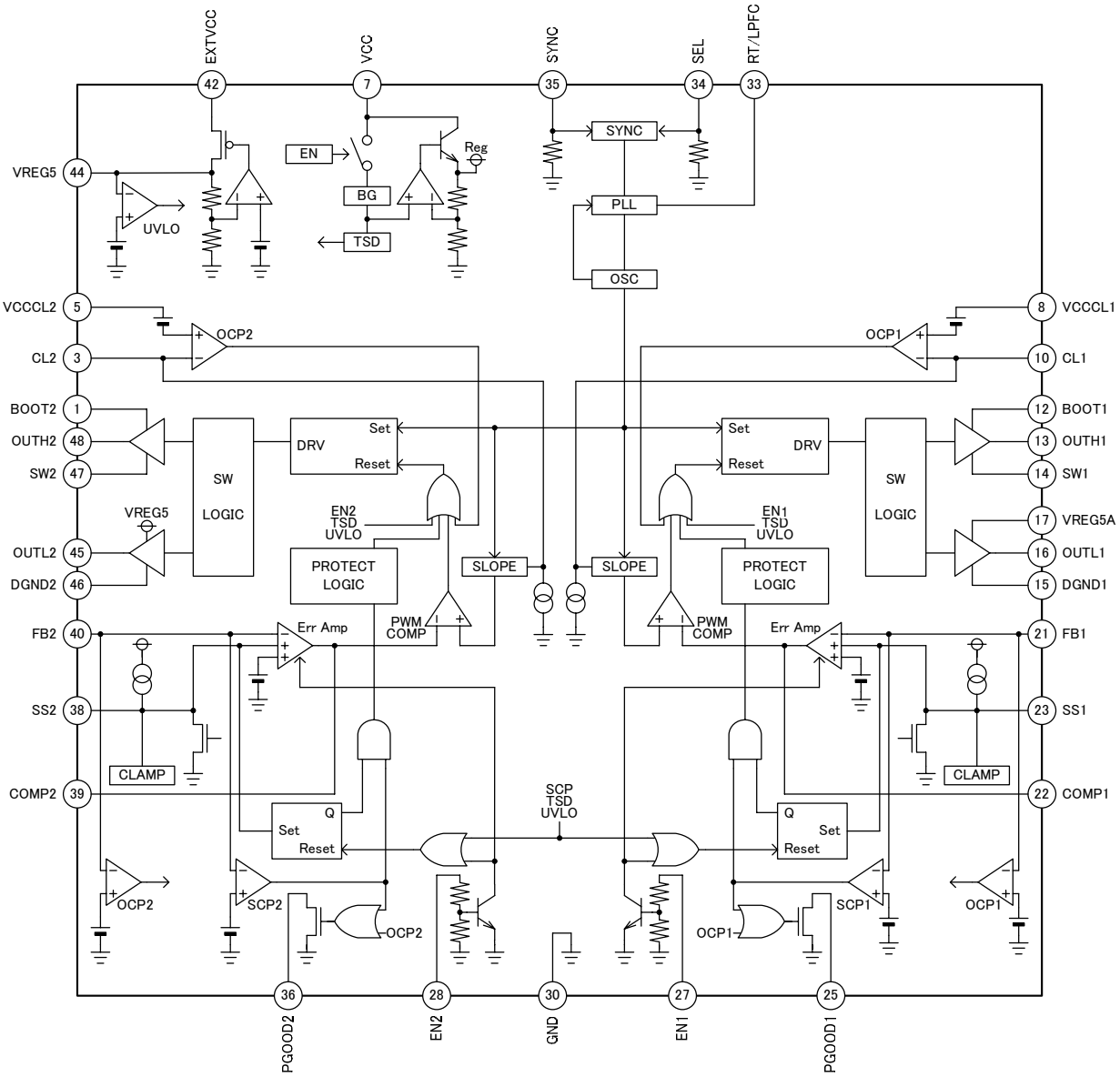


Figure 3. Block Diagram

Description of Blocks

(1) Error amplifier

The error amplifier compares the output feedback voltage to the 0.8V reference voltage and provides the comparison result as COMP voltage, which is used to determine the switching duty cycle. As at startup the soft start is based on the SS pin voltage, the COMP voltage is limited to the SS voltage.

(2) Oscillator

An internal fixed current source sets the oscillation frequency with the help of a single resistor connected to the RT pin. The frequency can be set in the range between 250 kHz to 550 kHz by proper selection of the external resistor. The phase difference between the outputs is 180° to help reduce the input capacitor voltage ripple and power losses.
Also, in case the input/output voltage difference is small, the oscillation frequency is divided 5times from the set value. This increase the maximum duty cycle time and helps to reduce the input to output voltage drop.
The maximum Duty is determined by the following equation.

$$\text{Maximum Duty} = (1 - (T_{OFF} \times f_{OSC}) / 5) \times 100 \quad [\%]$$

T_{OFF}: OUTH Minimum OFF time (Max=400ns)
$f_{OSC:}$ Setting frequency

Also above equation is theory value. The maximum duty may be influenced by PCB layout, FET, inductor, etc. Verification and confirmation with the actual application is recommended.

(3) Slope

The slope block uses the clock produced by the oscillator to generate a saw-tooth wave and sends this wave to the PWM comparator.

(4) PWM COMP

The PWM comparator determines the switching duty cycle by comparing the error amplifier COMP voltage, with the saw-tooth signal from the slope block. The switching duty cycle is limited internally to a fixed maximum duty, and thus cannot become 100 %.

(5)Driver(DRV, SW LOGIC)

This block receives the switching Duty determined by the PWM COMP block and generates OUTH and OUTL signals which drive the external FETs.
Also, the minimum ON time of OUTH is designed 250ns at the minimum and the minimum OFF time is designed 400ns at the maximum.

(6) Reference voltage (VREG5)

This block generates the internal reference voltage: 5 V. VREG5 requires an external capacitor. The FET driver supply input (VREG5A) also requires a capacitor. A ceramic capacitor with a value of 2 µF or more with low ESR matching the VREG5 and VREG5A pin is recommended.

(7) External synchronization (SYNC, PLL)

The internal oscillator circuit can be synchronized with an external signal applied to the SYNC pin. This is done with the help of an internal PLL circuit. In this situation the SEL pin must pulled “H”. After applying a clock to the SYNC pin and pulling the SEL pin “H”, the internal frequency will synchronize with the applied clock frequency. For synchronization, a clock with a frequency of 250 kHz to 600 kHz and duty of 20 % to 80 % must be used.
Note, the SEL pin should be set to H before the EN pin or it should be set to H after the soft start time.
In case of using external synchronization, a low pass filter is required for the LPF / RT pin.

(8) PGOOD pin

This pin monitors the output voltage (FB voltage). If it is within 8.5 % (typ) of the nominal output voltage, PGOOD output is “H”. When outside the range of 8.5% the PGOOD output is pulled “L”.
The PGOOD pin is an open drain output so a pull up resistor is required when used.

(9) Overcurrent protection (OCP)

The overcurrent protection is activated when the VCCCL to CL voltage drop reaches or exceeds 90mV.
Once activated the OUTH duty will be limited and the output voltage lowered.

(10) Short circuit protection (SCP)

The short circuit protection is activated after the output voltage (FB voltage) drops below 91.5 % and the overcurrent protection is detected 256 times (all SW pulses). Also, if the overcurrent protection is activated in a situation where the FB voltage is equal or less than 0.5 V, this will resemble an output short and the short circuit protection will be activated.
If the short circuit protection is activated, for a period of 1024 cycles of oscillation frequency, the output will be turned off and the SS and COMP discharged.

(11) Overvoltage protection (OVP)
BD9015KV-M, If the output voltage (FB voltage) rises above 108.5 %, OUTH and OUTL will turn off.
Once the output returns to a normal state the chip will recover. However, in case of light load or if recovery takes time, the COMP voltage will drop and recovery will be done with the minimum duty cycle, which may lead to undershoot of the output. In case this undershoot becomes an application problem, the output capacitor should be increased or the phase compensation RC constant should be adjusted.
BD9016KV-M, If the output voltage (FB voltage) rises above 108.5 %, only OUTH will turn off. OUTL continues to turn on and L-side FET will discharge the output capacitance. The ON pulse width of OUTL is determined by PWM COMP. If a short to VCC is considered the countermeasures needed are described in the “Operational Notes” at page 24.

(12) Under voltage lockout circuit (UVLO)
If the VREG5 voltage drops below 3.6 V (typ) the UVLO is activated and the device will shut down.

(13) Thermal shutdown (TSD)
If the chip temperature (Tj) reaches or exceeds ca. 150 °C the output is turned off.

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
VCC Voltage	VCC	-0.3 to +35 (1)	V
EXTVCC Voltage	EXTVCC	-0.3 to +35 (1)	V
VCCCL1, 2 Voltage	VCCCL1, 2	-0.3 to +35 (1)	V
CL1, 2 Voltage	$V_{CL1, 2}$	-0.3 to VCCCL1,2	V
SW1, 2 Voltage	$V_{SW1, 2}$	-1.5 to VCCCL1,2	V
BOOT1, 2 Voltage	$V_{BOOT1, 2}$	-0.3 to +40	V
BOOT1, 2 - SW1, 2 Voltage	$V_{BOOT1, 2-SW1, 2}$	-0.3 to +7	V
VREG5, 5A Voltage	VREG5, 5A	-0.3 to +7 or EXTVCC	V
EN1, 2 Voltage	$V_{EN1, 2}$	-0.3 to EXTVCC	V
SS1, 2 Voltage	$V_{SS1, 2}$	-0.3 to VREG5	V
FB1, 2 Voltage	$V_{FB1, 2}$	-0.3 to VREG5	V
COMP1,2 Voltage	$V_{COMP1, 2}$	-0.3 to VREG5	V
RT/LPFC Voltage	$V_{RT / LPFC}$	-0.3 to VREG5	V
PGOOD1,2 Voltage	$V_{PGOOD1, 2}$	-0.3 to +7	V
SEL Voltage	V_{SEL}	-0.3 to +7	V
SYNC Voltage	V_{SYNC}	-0.3 to +7	V
Power Dissipation	Pd	1.1 (2)	W
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	+150	°C

(1) Pd should not be exceeded.
(2) 8.8 mW / °C reduction when Ta ≥ 25 °C if mounted on a glass epoxy board of 70 mm × 70 mm × 1.6 mm

Recommended Operating Ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage 1	VCC, EXTVCC	3.9 to 30 (1)	V
Supply Voltage 2	VCCCL1, 2, $V_{CL1, 2}$	3 to VCC	V
BOOT1,2−SW1,2 Voltage	$V_{BOOT1, 2 - SW1, 2}$	3.2 to VREG5	V
Output Voltage	V_O	0.8 to 10	V
Oscillation Frequency Range	f_{OSC}	250 to 550	kHz
Synchronous Frequency Range	f_{SYNC_IN}	250 to 600	kHz

(1) In case of using less than 6V, short VCC, EXTVCC and VREG5.
Note, this is the minimum value after 4.5V or higher has been supplied to the supply pin.

Electrical Characteristics

(Unless otherwise specified: Ta=25°C, VCC=12V, EXTVCC=12V, VCCCL1, VCCCL2=12V, V_{EN1}, V_{EN2}=5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Circuit Current	I_{CC}	-	4	10	mA	
Shutdown Current	I_{ST}	-	0	1	μA	V_{EN1}, V_{EN2} = 0 V Ta = -40 °C to +105 °C
EN Pin Threshold Voltage	V_{ENTH}	1.00	2.15	2.70	V	Ta = -40 °C to +105 °C
EN Pin Pull Down Resistor	R_{EN}	100	200	400	kΩ	V_{EN1}, V_{EN2} = 5 V
VREG5						
VREG5 Output Voltage	VREG5	4.7	5.0	5.3	V	I_{VREG5} = 6 mA
UVLO						
UVLO Operating Voltage	V_{UVLO}	3.3	3.6	3.9	V	VREG5 SWEEP DOWN Ta = -40 °C to 105 °C
Hysteresis Voltage	V_{UVLO_HYS}	200	400	600	mV	VREG5 SWEEP UP
Error Amp Block						
FB Pin Source Current	I_{FB}	0	0.13	1.00	μA	V_{FB1}, V_{FB2} = 0.8 V Ta = -40 °C to +105 °C
Reference Voltage 1	$V_{REF}1$	0.792	0.800	0.808	V	FB1, FB2 pin voltage
Reference Voltage 2	$V_{REF}2$	0.788	0.800	0.812	V	FB1, FB2 pin voltage Ta = -40 °C to +105 °C
Oscillator Block						
Oscillation Frequency	f_{OSC}	270	300	330	kHz	RT = 200 kΩ
External Synchronous Frequency	f_{SYNC}	-	500	-	kHz	RT=200 kΩ f_{SYNC_IN} = 500 kHz Ta = -40 °C to +105 °C
SYNC Pin Threshold Voltage	V_{SYNCTH}	0.5	1.8	2.5	V	Ta = -40 °C to +105 °C
SYNC Pin Pull Down Resistor	R_{SYNC}	125	250	500	kΩ	V_{SYNC} = 5 V
SEL Pin Threshold Voltage	V_{SELTH}	0.5	1.8	2.5	V	Ta = -40 °C to +105 °C
SEL Pin Pull Down Resistor	R_{SEL}	125	250	500	kΩ	V_{SEL} = 5 V
LPFC Charge Current	I_{LPFCC}	20	30	40	μA	$V_{RT\ /\ LPFC}$ = 1 V
LPFC Discharge Current	I_{LPFCDC}	20	30	40	μA	$V_{RT\ /\ LPFC}$ = 1 V
Soft Start Block						
SS Pin Charge Current	I_{SS}	5	10	15	μA	V_{SS1}, V_{SS2} = 1 V Ta = -40 °C to +105 °C
SS Pin Discharge Current	R_{SS}	0.3	0.5	1.7	kΩ	V_{SS1}, V_{SS2} = 1 V VCC = 3 V
Maximum Voltage	V_{SS_MAX}	2.05	2.25	2.45	V	
Standby Voltage	V_{SS_STB}	0	0.01	0.10	V	VCC = 3 V Ta = -40 °C to +105 °C

* This product is not designed to be radiation-resistant.

Electrical Characteristics

(Unless otherwise specified: Ta=25°C, VCC=12V, EXTVCC=12V, VCCCL1, VCCCL2=12V, V_{EN1}, V_{EN2}=5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Driver Block						
OUTH Minimum ON Time	T_{ON}	-	130	-	ns	
OUTH Minimum OFF Time	T_{OFF}	-	200	-	ns	
OUTH→OUTL Dead Time	T_{DETHL}	-	35	-	ns	
OUTL→OUTH Dead Time	T_{DETLH}	-	35	-	ns	
OUTH High Side ON Resistor	R_{ON_HH}	-	2.5	-	Ω	
OUTH Low Side ON Resistor	R_{ON_HL}	-	1.7	-	Ω	
OUTL High Side ON Resistor	R_{ON_LH}	-	2.5	-	Ω	
OUTL Low Side ON Resistor	R_{ON_LL}	-	1.1	-	Ω	
BOOT Pin Current Consumption	I_{BOOT}	-	1	-	mA	V_{BOOT} = 17 V V_{SW1}, V_{SW2} = VCCCL
Overcurrent Protection Block						
CL Pin Threshold Voltage 1	V_{CL1}	78	90	103	mV	
CL Pin Threshold Voltage 2	V_{CL2}	75	90	105	mV	Ta = -40°C to +105°C
CL Pin Sink Current	I_{CL}	7	20	40	μA	Ta = -40°C to +105°C
Output Short Detection Voltage	V_{SHORT}	0.45	0.50	0.55	V	FB1, FB2 pin voltage
PGOOD Block						
PGOOD ON Resistor	R_{PGOOD}	0.5	1.5	2.5	kΩ	V_{FB1}, V_{FB2} = 0 V Ta = -40 °C to +105 °C
PGOOD Pin Leakage Current	I_{PGOOD}	-	0	1	μA	V_{PGOOD} = 5 V, V_{FB1},V_{FB2} = 0.8 V Ta = -40 °C to +105 °C
Output Overvoltage Detection Voltage	V_{OVER}	0.848	0.868	0.888	V	FB1, FB2 pin voltage
Output Low Voltage Detection Voltage	V_{LOW}	0.712	0.732	0.752	V	FB1, FB2 pin voltage

* This product is not designed to be radiation-resistant.

Typical Performance Curves

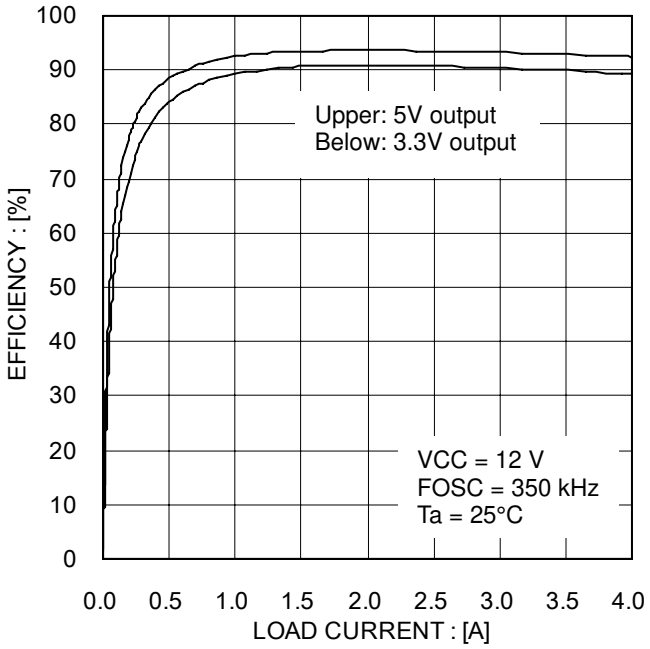


Figure 4. Efficiency

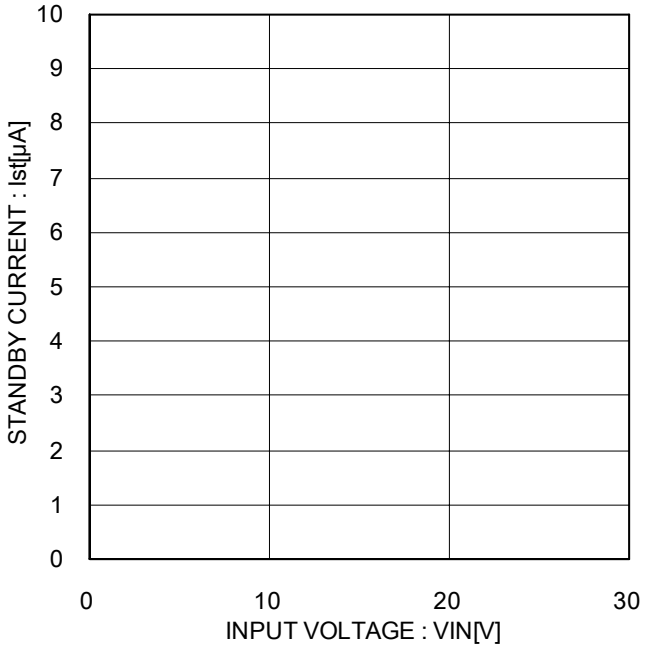


Figure 5. Shutdown Current

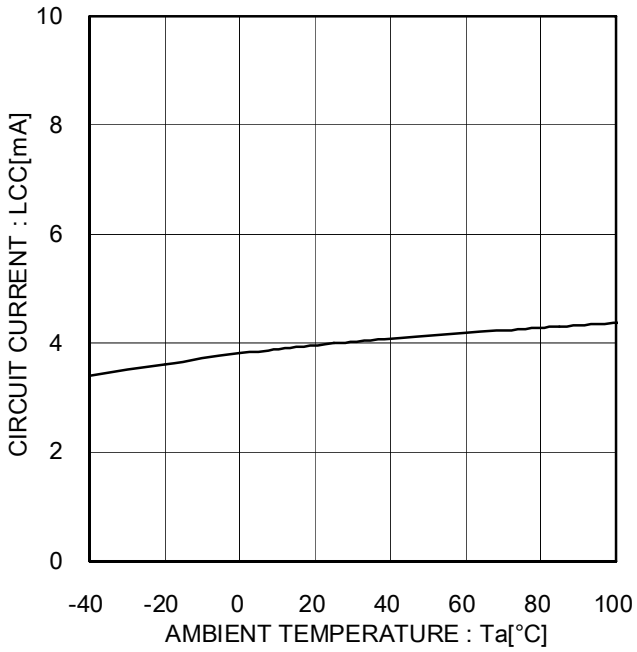


Figure 6. Curcuit Current

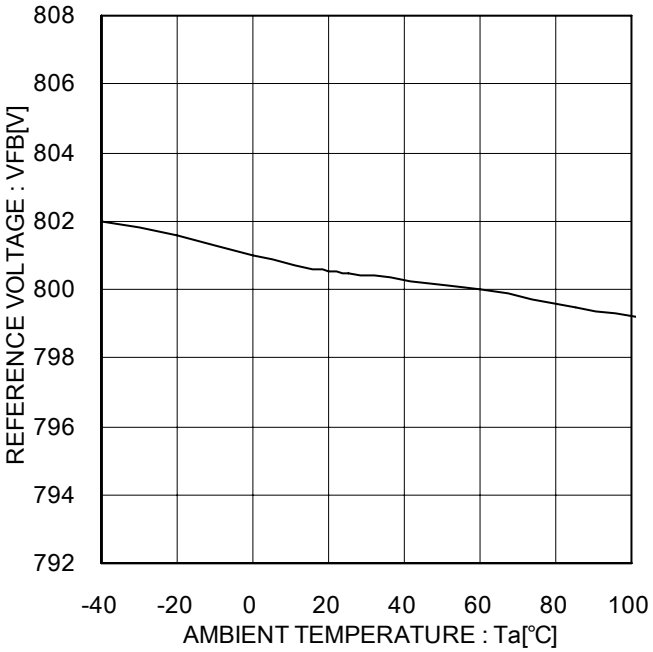


Figure 7. Reference Voltage vs. Temperature Characteristics

Typical Performance Curves

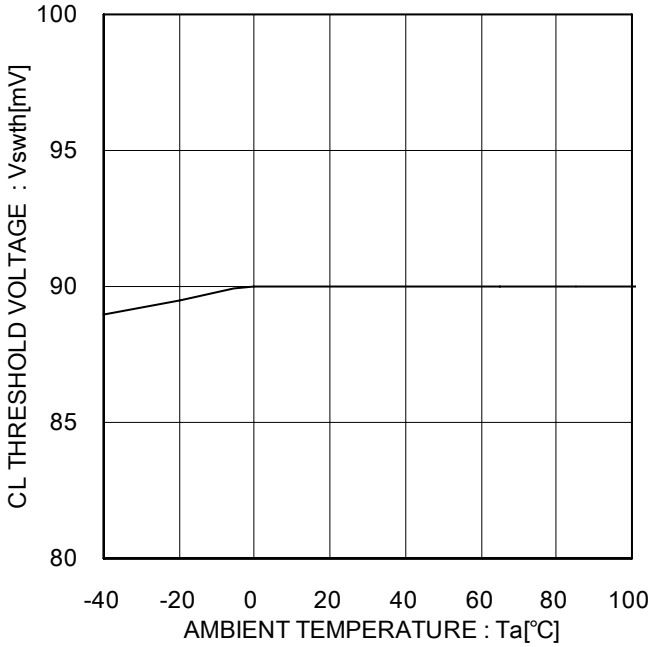


Figure 8. CL Pin Threshold Voltage vs. Temperature Characteristics

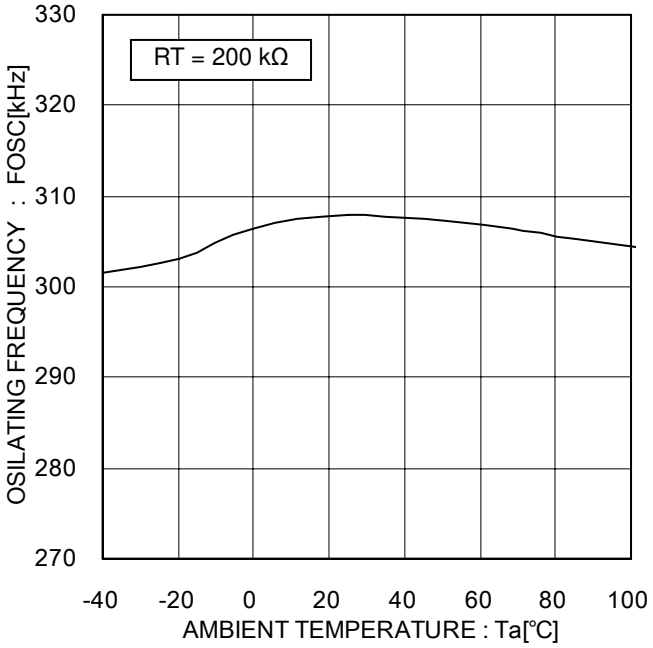


Figure 9. Frequency vs. Temperature Characteristics

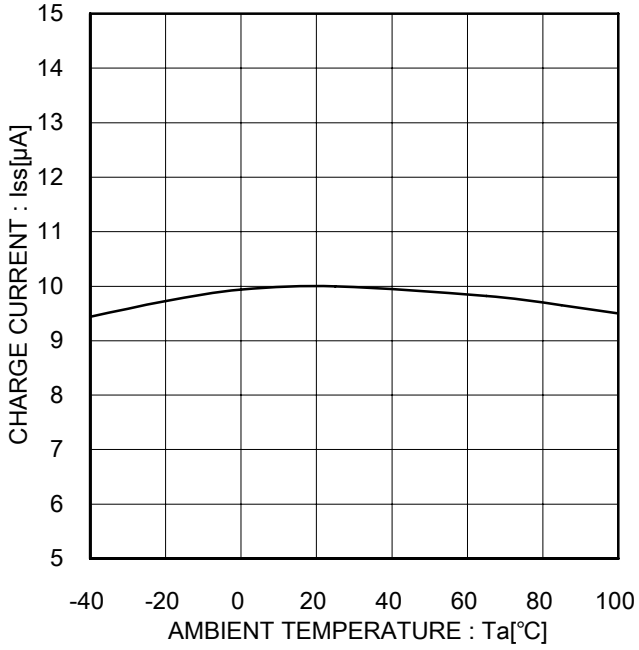


Figure 10. SS Charge Current vs. Temperature Characteristics

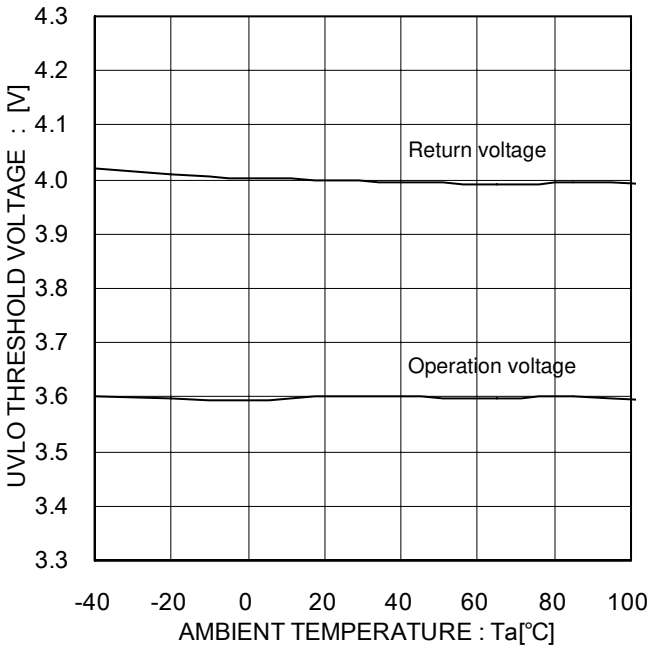


Figure 11. UVLO Operation/Return Voltage vs. Temperature Characteristics

Typical Performance Curves

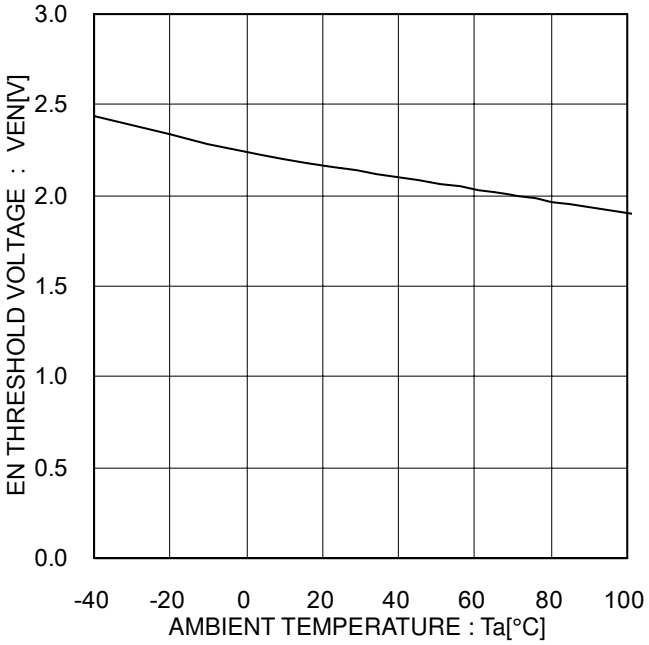


Figure 12. EN Threshold Voltage vs. Temperature Characteristics

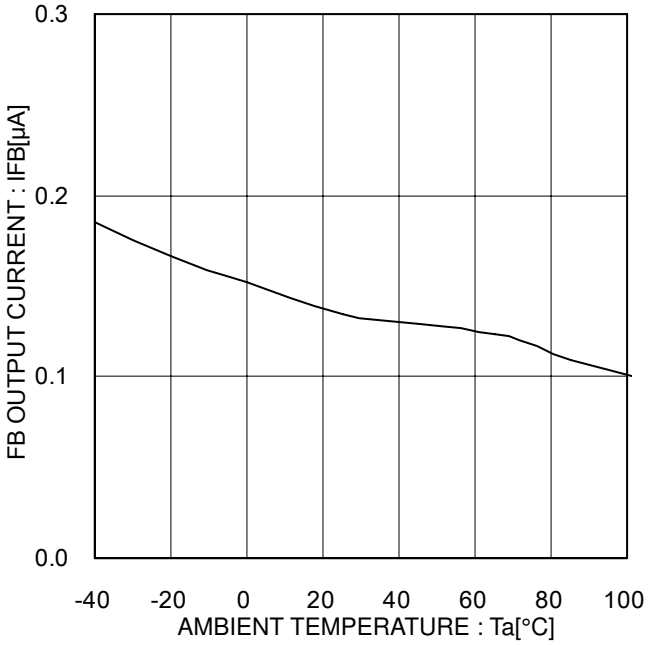


Figure 13. FB Pin Source Current vs. Temperature Characteristics

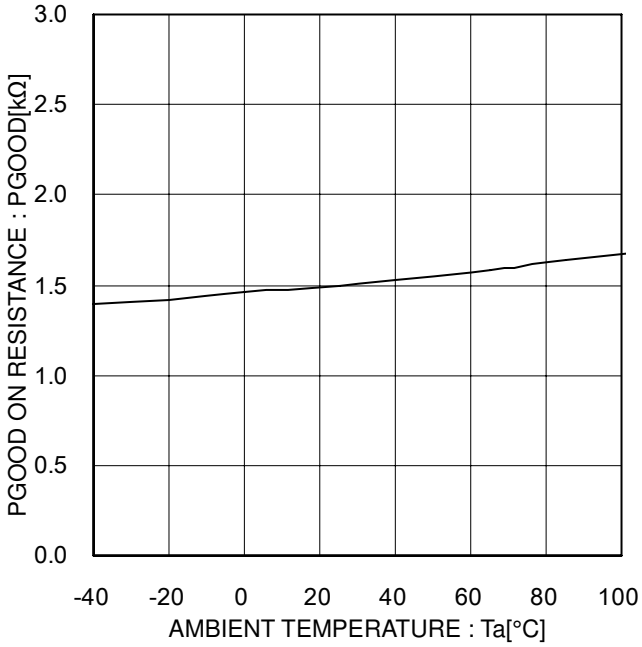


Figure 14. PGOOD Pin ON Resistance vs. Temperature Characteristics

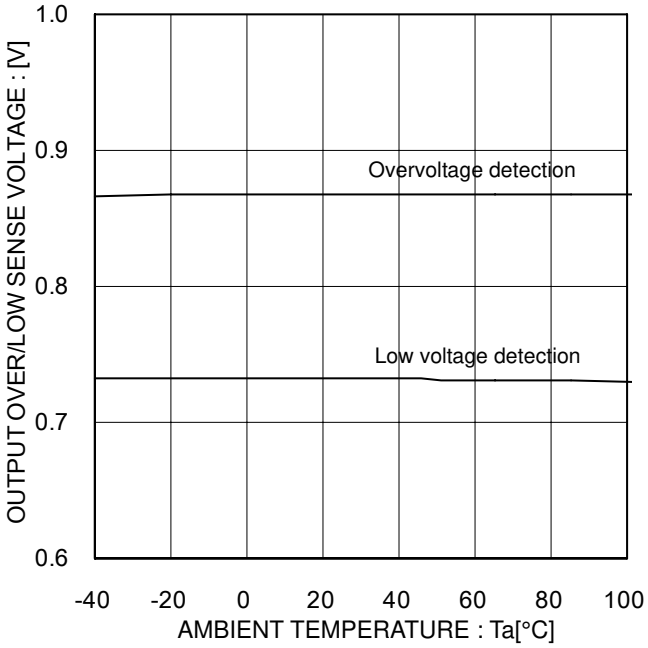


Figure 15. Output Overvoltage / Low Voltage Detection Voltage vs. Temperature Characteristics

Timing Chart

Startup operations

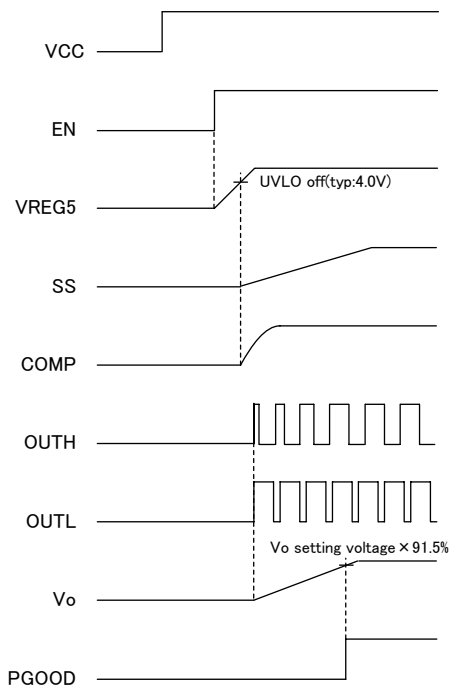


Figure 16. Startup Operations Timing Chart

Protection operations

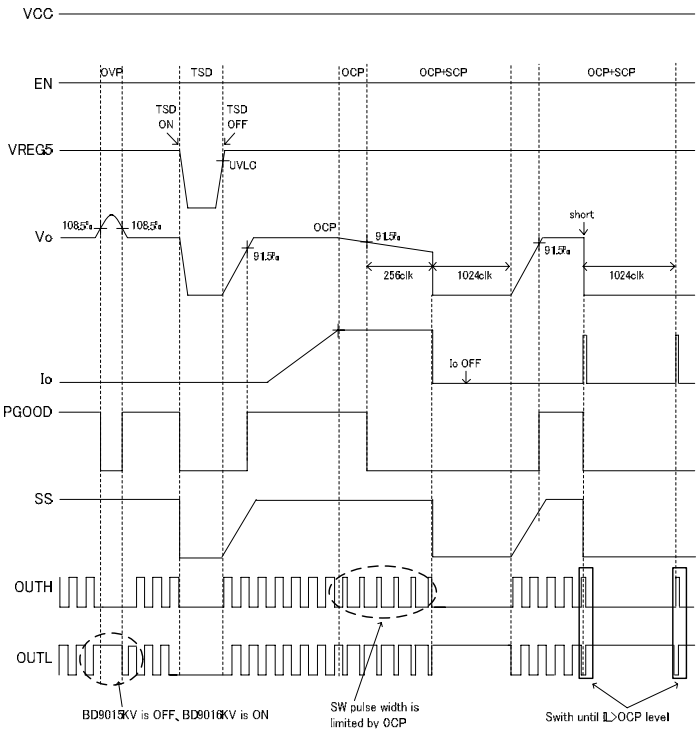


Figure 17. Protection Operations Timing Chart

Pre-bias function

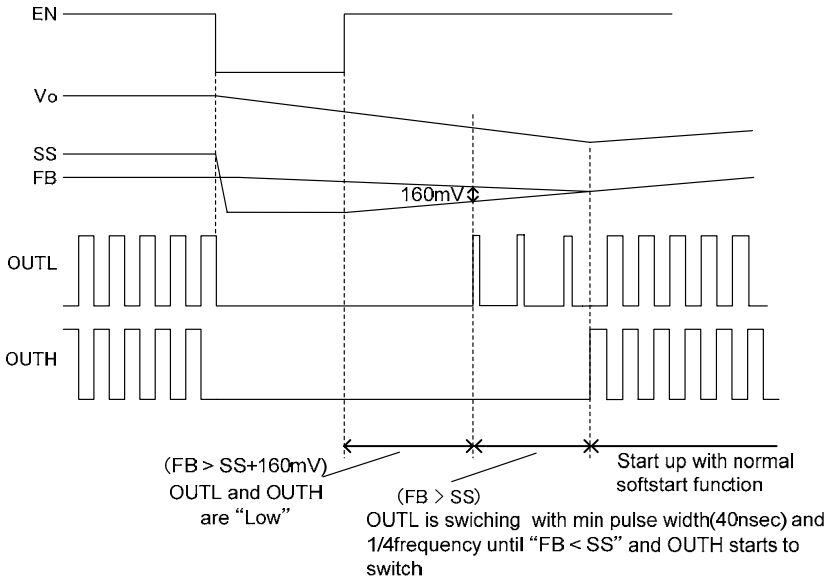


Figure 18. Pre-bias Functionality Timing Chart

Selection of External Components

(1)Setting the output L value

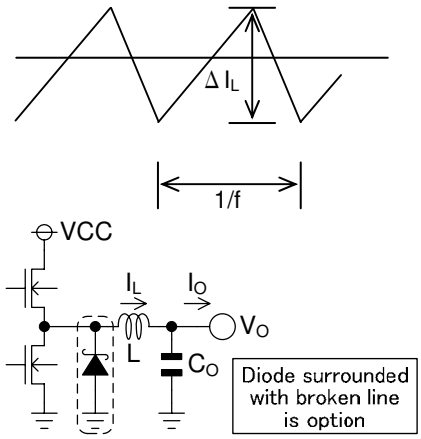


Figure 19. Output Ripple Current

The coil value significantly influences the output ripple current. As shown in the following equation, the larger the coil, and the higher the switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(VCC - V_O) \times V_O}{L \times VCC \times f} \quad [A]$$

The optimal output ripple current setting is ca. 30% of the maximum output current.

$$\Delta I_L = 0.3 \times I_O max \quad [A]$$

$$L = \frac{(VCC - V_O) \times V_O}{\Delta I_L \times VCC \times f} \quad [H]$$

(ΔI_L : output ripple current, f : switching frequency)

Outputting a current in excess of the coil current rating will cause magnetic saturation of the coil and will decrease efficiency. It is recommended to allow for sufficient margin to ensure that the peak current does not exceed the coil current rating.
Use low resistance (DCR, ACR) coils to minimize coil loss and increase efficiency.

(2)Setting the output capacitor Co value

Select the output capacitor with consideration to acceptable ripple voltage (Vpp).
The following equation is used to determine the output ripple voltage.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{C_O} \times \frac{V_O}{VCC} \times \frac{1}{f} \quad [V]$$

Note. f : switching frequency

The output Co setting needs to be kept within the allowable ripple voltage range. Allow for a sufficient voltage output margin in establishing the capacitor rating. Low ESR capacitors enable a lower output ripple voltage. Also, to meet the requirement for setting the output startup time parameter within the soft start time range, take the conditions described in the following capacitance equation for output capacitors into consideration.

$$C_O \leq \frac{T_{SS} \times (I_{LIMIT} - I_O)}{V_O}$$

T_{SS} : soft start time

I_{LIMIT} : over current detection limit

Note: non-optimal capacitance values may cause startup problems. Especially in cases of extremely large capacitance values, the possibility exists that the inrush current at startup will activate the overcurrent protection, thus not starting the output. Therefore, verification and conformation with the actual application is recommended.

(3)Setting the input capacitor (C_{IN})

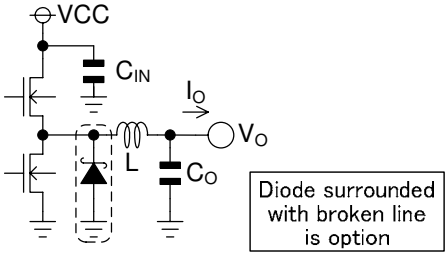


Figure 20. Input Capacitor

The input capacitor serves to lower the output impedance of the power source connected to the input pin (VCC,VCCCL,EXTVCC). Increased power supply output impedance can cause input voltage (VCC) instability and may negatively impact oscillation and ripple rejection characteristics. Therefore, it is necessary to place an input capacitor in close proximity to the VCC and GND pins. Select a low ESR capacitor with the required ripple current capacity and the capability to withstand temperature changes without wide tolerance fluctuations. The ripple current I_{RMS} is determined by the following equation.

$$I_{RMS} = I_O \times \frac{\sqrt{V_O \ (VCC - V_O)}}{VCC} \quad [A]$$

Also, be certain to ascertain the operating temperature, load range and MOSFET conditions for the application in which the capacitor will be used since capacitor performance is heavily dependent on the application's power supply characteristics, PCB wiring pattern and MOSFET gate-drain capacity.

(4)Setting the output voltage (V_O)

The output voltage is determined by the equation below. Select a combination of R1 and R2 to obtain the required voltage.

Note that a small resistor value leads to a drop in power efficiency and that a large resistor value leads to an increase of the offset voltage due to FB pin source current of 0.13μA (Typ).

$$V_O = 0.8 \times \frac{R1 + R2}{R2}$$

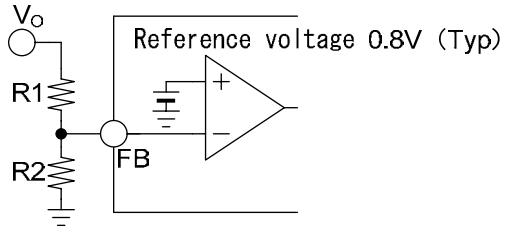


Figure 21. Setting the Output Voltage

(5)Setting the oscillation frequency (f_{OSC})

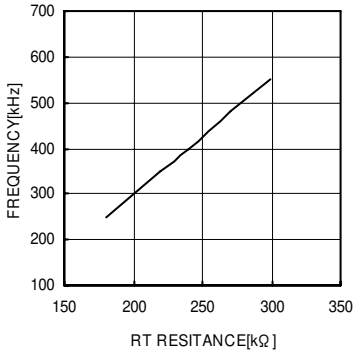
The setting of the internal oscillation frequency is possible by use of the resistor value connecter to RT.

The setting range is 250kHz to 550kHz. The correlation between the resistor value and the oscillation frequency is as shown in the table and Figure 22. below.

Setting a resistor outside the range shown below may cause the switching to stop after witch operation is no longer guaranteed.

Note that in case the input/output voltage difference is small, the oscillation frequency is divided by 5, reducing the output voltage drop.

The detail behavior is described in the description of Oscillator on page 4.

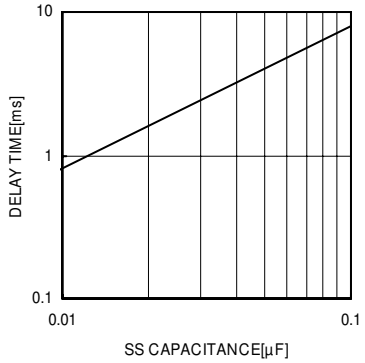


RT Resistor	Oscillation Frequency
180kΩ	250kHz
200kΩ	300kHz
220kΩ	350kHz
240kΩ	400kHz
270kΩ	480kHz
300kΩ	550kHz

Figure 22. RT resistor vs. oscillation frequency

(6)Setting the soft start time (T_{SS})

The soft start function is necessary to prevent inrush of coil current and output voltage overshoot at startup. The Figure 23. shows the relation between soft start time and capacitance, which can be calculated by using the equation.



$$T_{SS} = \frac{0.8V(Typ) \times C_{SS}}{I_{SS}\ (10\mu A\ (Typ))}\ [sec]$$

Figure 23. Capacitance vs. Soft Start Time

Capacitance values between 0.01μF and 0.1μF are recommended. There is a possibility that an overshoot is generated in the output due to the phase compensation, output capacitor, etc. Therefore, verification and confirmation with the actual application is recommended. Use high accuracy components (X5R) when implementing sequential startups involving other power sources.

(7)Setting the overcurrent detection value (I_{LIMIT})

When the peak of the current in the coil exceeds the overcurrent detection value, overcurrent protection is activated. The detection value is determined by the resistor R_{CS} connected between VCCCL and CL and the CL pin threshold voltage (Typ：90mV). It can be calculated using the formula below.

$$I_{LIMIT} = \frac{90mV}{R_{CS}} \quad [A]$$

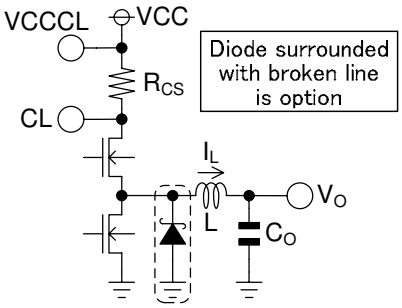


Figure 24. Setting the Overcurrent Detection Value

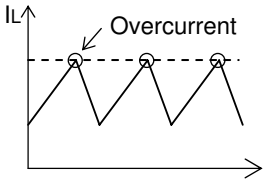


Figure 25. The Point of Detecting Overcurrent

When the overcurrent protection is activated, the output duty is limited to prevent an increase in output current. The overcurrent protection is an auto-recovery type; when the output load returns to normal state, the output duty and output voltage also return to the normal state. The voltage generated by the overcurrent detection resistor provides feedback to the internal SLOPE and is also used in determining the switching duty. To prevent sub-harmonic oscillation at time of high duty cycles, the equation below needs to be satisfied.

$$\frac{V_O \times R_{CS} \times Duty}{L \times f_{OSC}} \leq 0.09$$

In case the equation above is not satisfied, revise the constants or settings.

(8)Selecting MOSFET

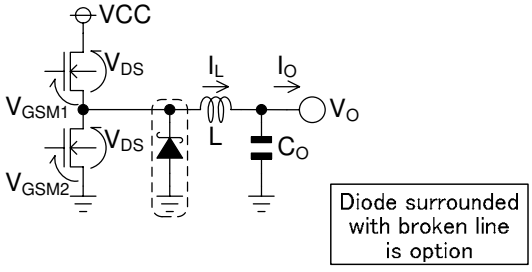


Figure 26. Selecting MOSFET

FET used Nch MOS

- V_{DS} > VCC
- V_{GSM1} > $V_{BOOT-SW}$
- V_{GSM2} > VREG5
- Allowable current > output current + ripple current

※ Value higher than the overcurrent protection value is recommended

※Select a low ON resistance MOSFET for high efficiency

※Note

In case the input capacitance of the output FET is extremely large, the possibility exists that the efficiency decreases due to the shortening a dead time of the upper and lower output FET. For the input capacitance of the output FET, a value of 1200pF or lower is recommended. As these characteristics are influenced by the PCB layout and the type of the components verification and confirmation with the actual application is recommended.

(9)Selecting Schottky barrier diode

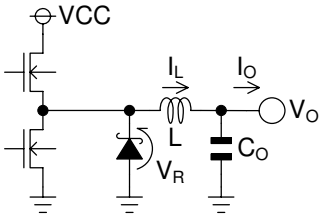


Figure 27. Selecting Schottky Barrier Diode

- Reverse voltage V_R > VCC
- Allowable current > output current + ripple current

※ Value higher than the over current protection value is recommended.

※Select a diode with a low forward voltage and fast recovery for high efficiency.

(10)Setting the phase compensation circuit

Negative feed back stability conditions are as follows.

・At time of unity gain (0dB) the phase delay should be 135˚ or less. (i.e. the phase margin is 45˚ or higher)

Also, the crossover frequency (frequency of 0dB) of the whole system is set to 1/10 of less of the switching frequency because DC/DC converter applications are sampled by the switching frequency.

In summary, the characteristics that the application target is as follows.

・At time of unity gain (0dB), the phase delay should be 135˚ or less. (i.e. the phase margin is 45˚ or higher)

・fc is less than 1/10 of switching frequency

The response is determined by the limitation of fc. Therefore, the switching frequency is required to high in order to increase the response.

The phase compensation is set by the capacitor and resistor which are connected in series to the COMP pin.

Achieving stability by using the phase compensation is done by cancelling the fp1 and fp2 (error amp pole and power stage pole) of the regulation loop by use of fz1. fp1, fp2 and fz1 are determined in the following equations.

$$fp1 = \frac{g_m}{2\pi \times C1 \times A_V}$$

$$fp2 = \frac{1}{2\pi \times C_O \times R_{LOAD}}$$

$$fz1 = \frac{1}{2\pi \times C1 \times R1}$$

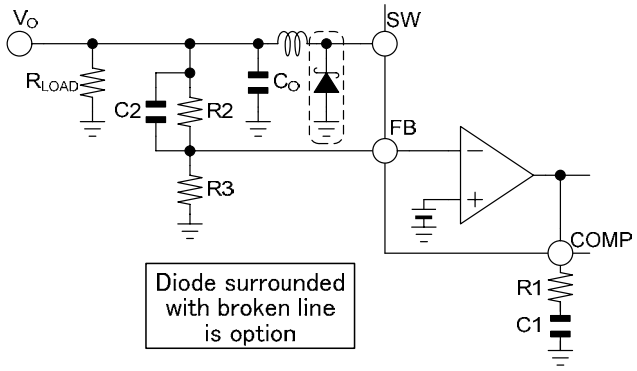


Figure 28. Setting Phase Compensation Circuit

Also, by inserting a capacitor in C2, phase lead fz2 can be added.

$$fz2 = \frac{1}{2\pi \times C2 \times R2}$$

In the formula above, g_m is the error amp transconductance (400μA/V) and A_V is the error amp voltage gain (200V/V). This setting is obtained by using a simplified calculation, therefore, adjustment on the actual application may be required. Also as these characteristics are influenced by the PCB layout, load conditions, etc. verification and confirmation with the actual application at time of mass production design is recommended.

(11)Setting the BOOT pin serial resistors (R_{BOOT})

By connecting resistors to the BOOT pin, it becomes possible to adjust the turn on delay and rise time at switching. Placing the resistors also allows for the adjustment of the upper and lower FET dead time and is effective as noise countermeasure at time of switching.

As shown in Figure 29., place the resistor at R_{BOOT} so as not to limit the charge current I_{CHARGE} of the capacitor C_{BOOT} for the BOOT pin boost. In case the resistor R_{BOOT} is large, the possibility exists that voltage drop is generated between the BOOT pin voltage is no longer guaranteed. Therefore set R_{BOOT} to no higher than 10Ω.

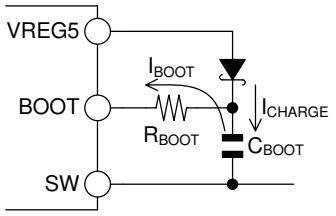


Figure 29. Setting the BOOT pin Serial Resistors

(12)Concerning switching pulse jitter and split

There are cases in which, when the switching pulse duty is at ca. 50%, it is influenced by the other switching pulse resulting in jitter or split (small duty and large duty are alternately output) on/off the switching output. If the jitter and split cause a problem take the steps listed below.

(a) Serially place resister R_{CL} to pin CL

(b) Place resister R_{OUTL} to the lower gate.

Generally, the jitter and split are suppressed with R_{CL} resister of 200Ω to 300Ω and R_{OUTL} resister of 4.7Ω to 10Ω.

However, as these characteristics are influenced by the PCB layout, used FET, etc. Verification and confirmation with the actual application is recommended.

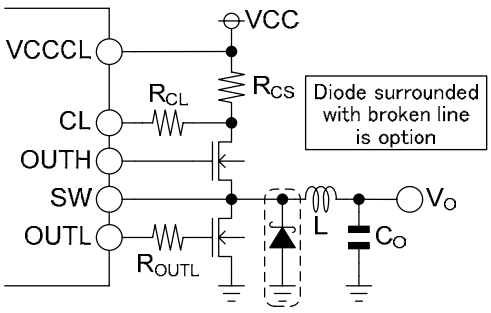
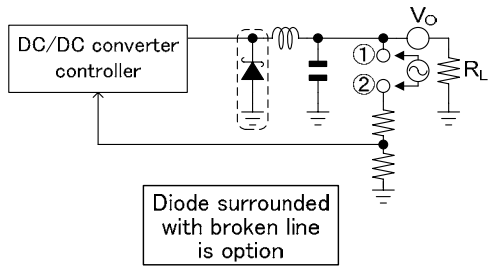


Figure 30. Measures of Jitter and Split

Frequency Characteristic Evaluation

The DC/DC converter's frequency characteristics (phase margin, gain margin) can be measured by using a gain-phase analyzer or FRA.



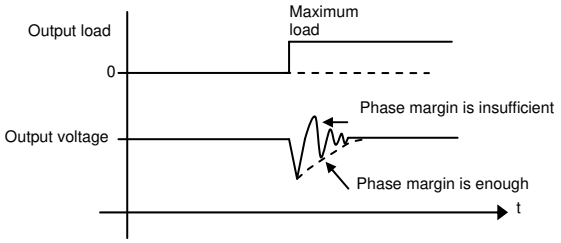


Figure 31. Measurement of Frequency Characteristic

<Procedure>

1. Confirm that output does not oscillate in a closed loop with maximum load.
2. Isolate ① and ② and insert Vm (amplitude of ca. 20mVpp to 100mVpp).
3. Measure (probe) the oscillation of ① to that of ②.

The phase margin can also be measured with the load responsiveness. Measure the variation in output voltage when instantaneously changing the load from no load to maximum load. If ringing occurs, the phase margin is insufficient. If no ringing occurs, the phase margin is sufficient. The actual phase margin can not be measured.

Application circuit example

※Application circuit is same both BD9015KV-M and BD9016KV-M

Parameter	Symbol	Spec example
Input voltage	VCC	6V to 28V
Output voltage/ current	V_O1 / I_O1	5V / 4A
	V_O2 / I_O2	3.3V /4A
Output ripple voltage	ΔV_{PP}	20mVp-p
Switching frequency	f_{OSC}	350kHz
Operating temp. range	Ta	-40°C to 105°C

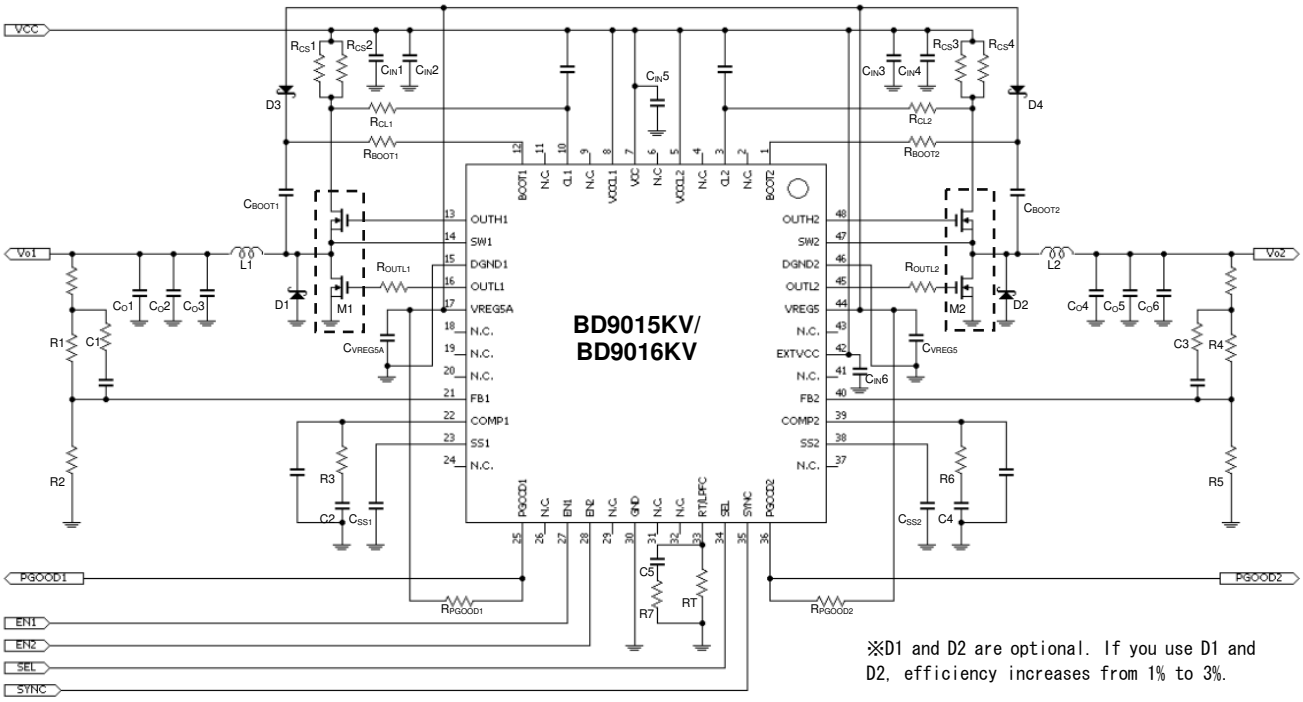


Figure 32. Reference circuit

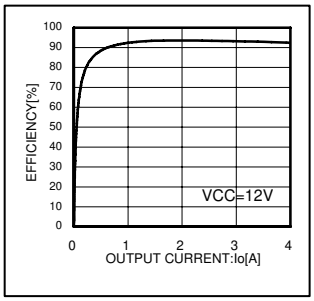


Figure 33. Efficiency (V_O1=5V)

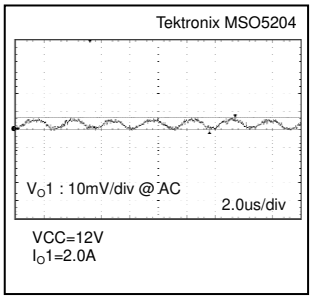


Figure 34. Output Ripple voltage (V_O1=5V)

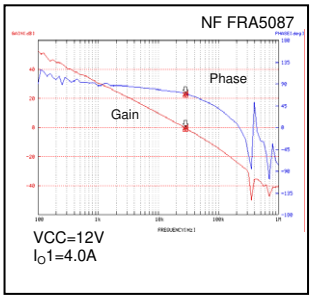


Figure 35. Frequency Characteristic (V_O1=5V)

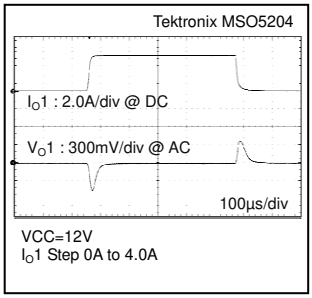


Figure 36. Load Response (V_O1=5V)

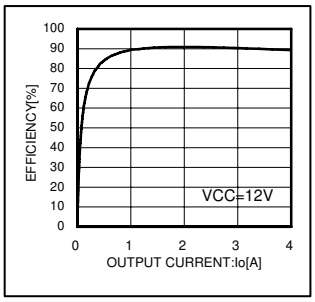


Figure 37. Efficiency (V_O2=3.3V)

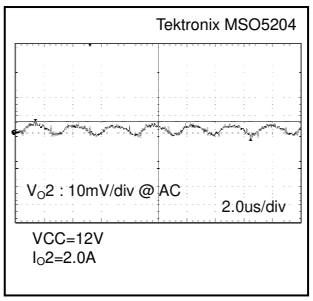


Figure 38. Output Ripple voltage (V_O2=3.3V)

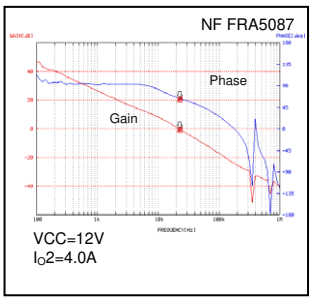


Figure 39. Frequency Characteristic (V_O2=3.3V)

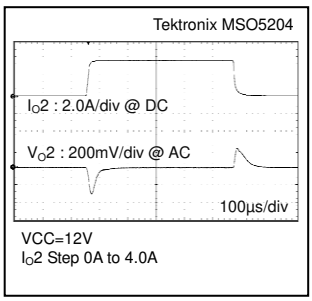


Figure 40. Load Response (V_O2=3.3V)

No	Package	Parameters	Part Name(series)	Type	Manufacturer
R1	1005	43kΩ,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R2	1005	8.2kΩ,1%,1/16W	MCR01 Series	Chip resister	ROHM
R3	1005	5.6kΩ,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R4	1005	47kΩ,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R5	1005	15kΩ,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R6	1005	3.9kΩ,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R7	1005	1kΩ,1%,1/16W	MCR01 Series	Chip resistor	ROHM
RT	1005	220kΩ,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R_{CL1}	1005	300Ω,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R_{CL2}	1005	300Ω,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R_{BOOT1}	1005	10Ω,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R_{BOOT2}	1005	10Ω,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R_{OUTL1}	1005	4.7Ω,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R_{OUTL2}	1005	4.7Ω,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R_{PGOOD1}	1005	100kΩ,1%,1/16W	MCR01 Series	Chip resistor	ROHM
R_{PGOOD2}	1005	100kΩ,1%,1/16W	MCR01 Series	Chip resistor	ROHM
$R_{CS}1$	2012	20mΩ,1%,1/3W	UCR10 Series	Chip resistor	ROHM
$R_{CS}2$	2012	20mΩ,1%,1/3W	UCR10 Series	Chip resistor	ROHM
$R_{CS}3$	2012	20mΩ,1%,1/3W	UCR10 Series	Chip resistor	ROHM
$R_{CS}4$	2012	20mΩ,1%,1/3W	UCR10 Series	Chip resistor	ROHM
C1	1005	100pF,CH,50V	GCM Series	Ceramic	MURATA
C2	1005	4700pF,R,50V	GCM Series	Ceramic	MURATA
C3	1005	100pF,CH,50V	GCM Series	Ceramic	MURATA
C4	1005	6800pF,R,50V	GCM Series	Ceramic	MURATA
C5	1005	4700pF,R,50V	GCM Series	Ceramic	MURATA
C_{SS1}	1005	0.1uF,R,16V	GCM Series	Ceramic	MURATA
C_{SS2}	1005	0.1uF,R,16V	GCM Series	Ceramic	MURATA
C_{BOOT1}	1005	0.1uF,R,16V	GCM Series	Ceramic	MURATA
C_{BOOT2}	1005	0.1uF,R,16V	GCM Series	Ceramic	MURATA
C_{VREG5A}	1608	1uF,X7R,16V	GCM Series	Ceramic	MURATA
C_{VREG5}	1608	1uF,X7R,16V	GCM Series	Ceramic	MURATA
$C_{IN}1$	3225	4.7uF,X7R,50V	GCM Series	Ceramic	MURATA
$C_{IN}2$	3225	4.7uF,X7R,50V	GCM Series	Ceramic	MURATA
$C_{IN}3$	3225	4.7uF,X7R,50V	GCM Series	Ceramic	MURATA
$C_{IN}4$	3225	4.7uF,X7R,50V	GCM Series	Ceramic	MURATA
$C_{IN}5$	3216	1uF,X7R,50V	GCM Series	Ceramic	MURATA
$C_{IN}6$	3216	1uF,X7R,50V	GCM Series	Ceramic	MURATA
C_O1	3225	22uF,X7R,16V	GCM Series	Ceramic	MURATA
C_O2	3225	22uF,X7R,16V	GCM Series	Ceramic	MURATA
C_O3	3225	22uF,X7R,16V	GCM Series	Ceramic	MURATA
C_O4	3225	22uF,X7R,16V	GCM Series	Ceramic	MURATA
C_O5	3225	22uF,X7R,16V	GCM Series	Ceramic	MURATA
C_O6	3225	22uF,X7R,16V	GCM Series	Ceramic	MURATA
D1	PMDS	AVERAGE I = 3A MAX	RB050L-40	Schottky Diode	ROHM
D2	PMDS	AVERAGE I = 3A MAX	RB050L-40	Schottky Diode	ROHM
D3	PMDU	AVERAGE I = 1A MAX	RB160M-40	Schottky Diode	ROHM
D4	PMDU	AVERAGE I = 1A MAX	RB160M-40	Schottky Diode	ROHM
M1	SOP8	Drain Current = 9A MAX	SP8K4	Transistor	ROHM
M2	SOP8	Drain Current = 9A MAX	SP8K4	Transistor	ROHM
L1	6.36 x 3.56 x 6.1mm	10µH	XAL6060 Series	Coil	Coilcraft
L2	6.36 x 3.56 x 6.1mm	10µH	XAL6060 Series	Coil	Coilcraft

※These setting values are the reference. As these characteristics may be influenced by the PCB layout pattern, used components, etc. Verification and confirmation with the actual application is recommended.

Input filter

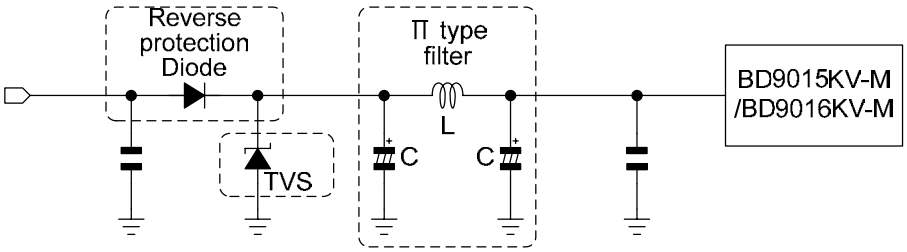


Figure 41. Filter circuit

For reference, lists the input filter circuits for EMC measure to Figure 41..

The π type filter is 3rd order LC filter. This is used when it is not sufficient to use only the decoupling capacitor.
The π type filter can behave good performance as EMC filter by large attenuation characteristic.
TVS(Transient Voltage Suppressors) is used for primary protection of automotive battery power supply line.
The general zener diode is insufficient because it is necessary to tolerate the high energy of load dump condition.
The TVS is in below list is recommended. The reverse polarity diode is required for protection when the power supply, such as battery, is connected in reverse by mistake.

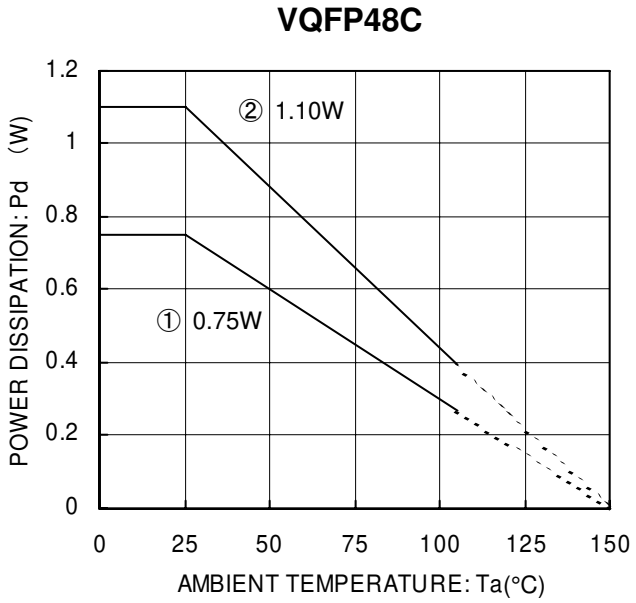
No	Part Name(series)	Manufacturer
L	XAL Series	Coilcraft
	CLF Series	TDK
C	CD Series	NICHICON
	UD Series	NICHICON
TVS	SM8 Series	VISHAY
D	S3A thru S3M series	VISHAY

Recommendation Parts Vender List

Show recommendation parts vender below.

No	Type	Manufacturer	URL
C	Electrolytic Capacitor	NICHICON	www.nichicon.com
C	Ceramic Capacitor	MURATA	www.murata.com
L	Coils	Coilcraft	www.coilcraft.com
L	Coils	TDK	www.global.tdk.com
L	Coils	Sumida	www.sumida.com
D	Diodes	VISHAY	www.vishay.com
D	Diodes/Resister	ROHM	www.rohm.com

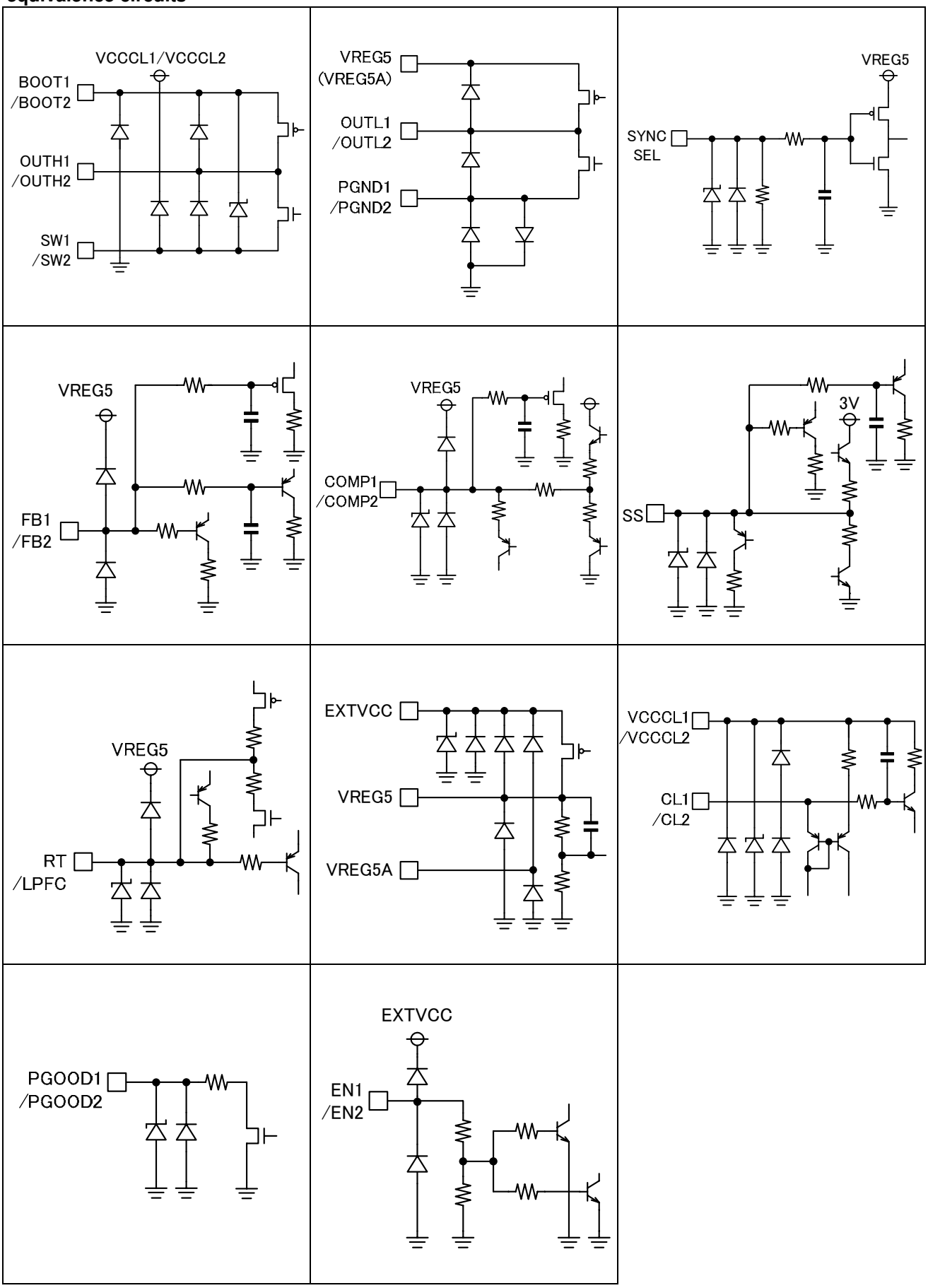
Power Dissipation



①：IC Unit
②：IC mounted on ROHM standard board
（Glass epoxy board of 70mm×70mm×1.6mm）

Figure 42. Thermal derating characteristic

I/O equivalence circuits



Operational Notes

1) Absolute maximum ratings
Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters can result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

2) GND electric potential
Keep the GND pin potential at the lowest (minimum) potential under any operating condition. Furthermore, excluding the SW pin, the voltage of all pin should never drop below that of GND. In case there is a pin with a voltage lower than GND implement countermeasures such as using a bypass route.

3) Power dissipation
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. Therefore allow for sufficient margins to ensure use within the power dissipation rating.

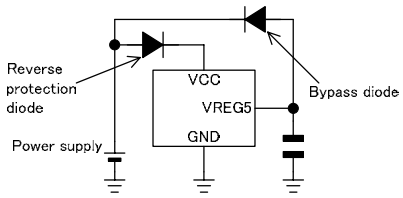
4) Input power supply
Concerning the input pins VCC, VCCCL and EXTVCC, the layout pattern should be as short as possible and free from electrical interferences.

5) Electrical characteristics
The electrical characteristics given in this specification may be influenced by conditions such as temperature, supply voltage and external components. Transient characteristics should be sufficiently verified.

6) Thermal shutdown (TSD)
This IC incorporates and integrated thermal shutdown circuit to prevent heat damage to the IC. Normal operation should be within the power dissipation rating, if however the rating is exceeded for a continued period, the junction temperature(Tj) will rise and the TSD circuit will be activated and turn all output pins OFF. After the Tj falls below the TSD threshold the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

7) Inter-pin shorting and mounting errors
Ensure that when mounting the IC on the PCB the direction and position are correct. Incorrect mounting may result in damaging the IC. Also, shorts caused by dust entering between the output, input and GND pin may result in damaging the IC.

8) In some applications, the VCC and pin potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, while the external capacitor is charged, the VCC shorts to the GND. For the VREG5 output pin use a capacitor with a capacitance with less than 100µF. We also recommend using reverse polarity diodes in series or a bypass diode between all pins and the VCC pin.



9) Operation in strong electromagnetic fields
Use caution when operating in the presence of strong electromagnetic fields, as this may cause the IC to malfunction.

10) In applications where the output pin is connected to a large inductive load, a counter-EMF (electromotive force) might occur at startup or shutdown. A diode should be added for protection.

11) Testing on application boards
The IC needs to be discharged after each test process as, while using the application board for testing, connecting a capacitor to a low-impedance pin may cause stress to the IC. As a protection from static electricity, ensure that the assembly setup is grounded and take sufficient caution with transportation and storage. Also, make sure to turn off the power supply when connecting and disconnecting the inspection equipment.

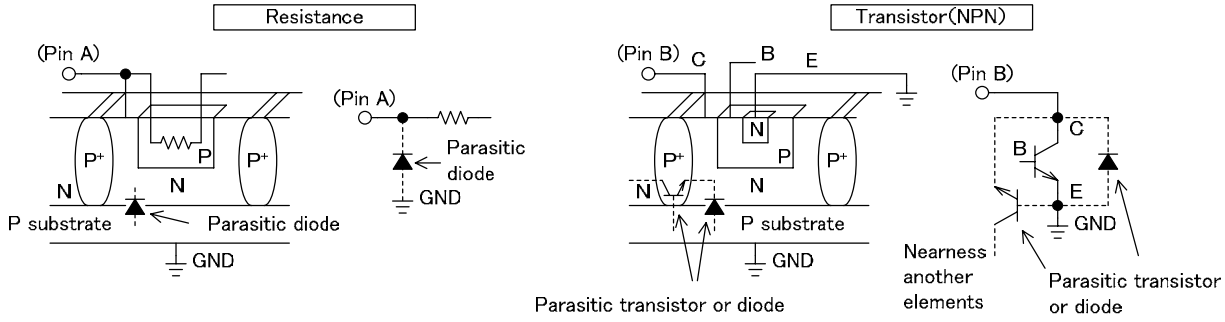
12) GND wiring pattern
When both a small-signal GND and a high current GND are present, single-point grounding (at the set standard point) is recommended. This in order to separate the small-signal and high current patterns and to ensure that voltage changes stemming from the wiring resistance and high current do not cause any voltage change in the small-signal GND. Similarly, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

13) SS pin
Note that the SS pin will go into test mode when supplied with 5V or more.

14) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. Relations between each potential may form as shown in the example below, where a resistor and transistor are connected to a pin:

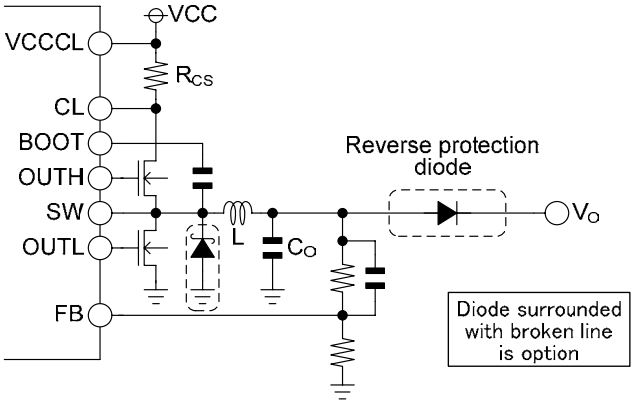
- With the resistor, when GND＞Pin A, and with the transistor(NPN), when GND＞Pin B:
  The P-N junction operates as a parasitic diode
- With the transistor (NPN), when GND＞Pin B:
  The P-N junction operates as a parasitic transistor by interacting with the N layers of elements in proximity to the parasitic diode described above

Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits and can cause malfunctions and, in turn, physical damage to or destruction of the chip. Therefore do not employ any method in which parasitic diodes can operate such as applying a voltage to an input pin that is lower than the (P substrate) GND.



The structure example of the IC

15) Vo short to VCC (BD9016KV-M)
When the over voltage protection is activated by supplying voltage to Vo from externally, for instance Vo is shorted to VCC in application, the large current may appear in coil and L-side FET since the output capacitor is discharged by the over voltage protection. A reverse protection diode should be added for protection.



Ordering Information

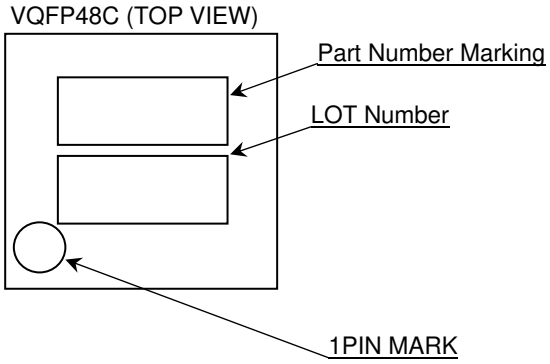
B D 9 0 1 x K V - M E 2

Part Number
BD9015KV or BD9016KV

Package
KV: VQFP48C

Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



Part Number	Marking
BD9015KV-M	BD9015KV
BD9016KV-M	BD9016KV