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Input Voltage 5.0V to 35V Output Switch Current 2A 1ch Step-Down DC/DC Converter

BD9060HFP-C BD9060F-C

General Description

The BD9060HFP-C BD9060F-C are high-accuracy frequency-flexible step-down switching regulators with built-in POWER MOS FET which can withstand high pressure. The operational frequency is freely configurable with external resistance. It features a wide input voltage range (5V to 35V) and a high frequency accuracy of ±5% (f=200kHz to 500kHz). Furthermore, an external synchronization input pin enables synchronous operation with external clock. The output capacitor corresponds to the ceramic capacitor.

Features

- Minimal external components
- P-ch POWER MOS FET included in the package
- Low dropout:100% ON duty cycle
- External synchronization enabled
- Soft start function: soft start time fixed to 2.7ms (Typ)
- Built-in overcurrent protection circuit
- Built-in thermal shutdown protection circuit

Applications

Battery-powered in-vehicle unit (Cluster, Car multimedia, etc.), communication such as ETC, all fields of industrial equipment, Flat TV, Printer, DVD, AV, OA

Key Specifications

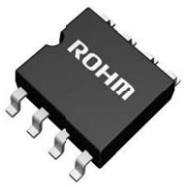
- Input Voltage Range: 5V to 35V
- Output Voltage Range: 0.8V to VINV
- Output Switch Current: 2 A (Max)
- Selectable Oscillating Frequency: 50kHz to 500kHz
- Oscillating Frequency Accuracy: ±5% (f=200kHz to 500kHz)
- POWER MOS FET On Resistance: 0.6Ω(Max)
- Reference Voltage Accuracy: ±2% (Typ)
- Standby Circuit Current: 0 µA (Typ)
- Operating Temperature Range: -40°C to +125°C
- AEC-Q100 Qualified

Package

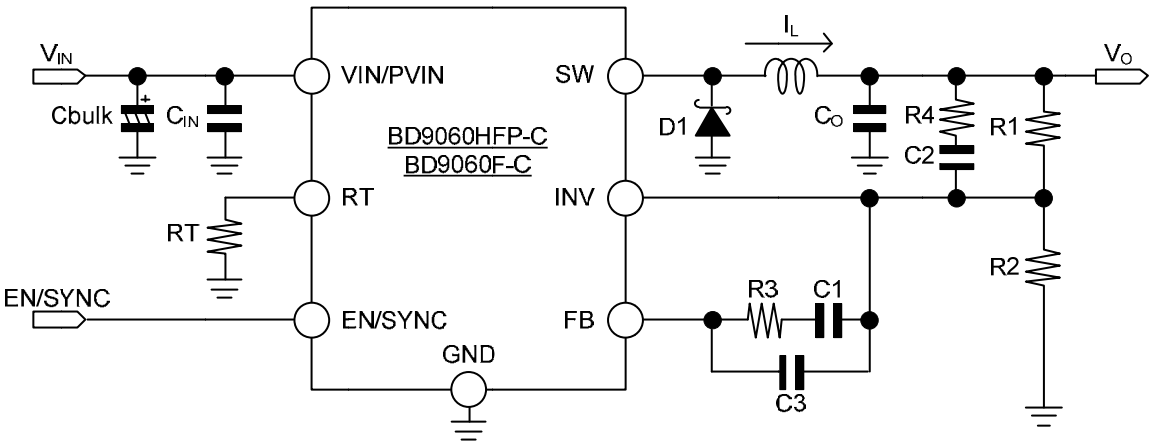
W(Typ) x D(Typ) x H(Max)

HRP7 9.395mm x 10.540mm x 2.005mm

SOP8 5.00mm x 6.20mm x 1.71mm



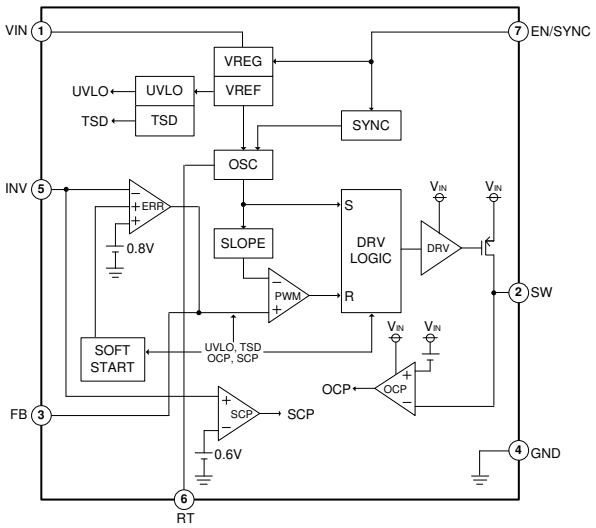
Typical Application Circuit



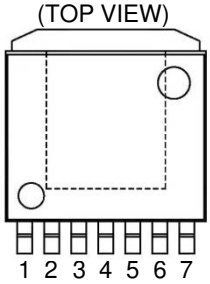
○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Block Diagram, Pin Configuration, Pin Description

(BD9060HFP-C)

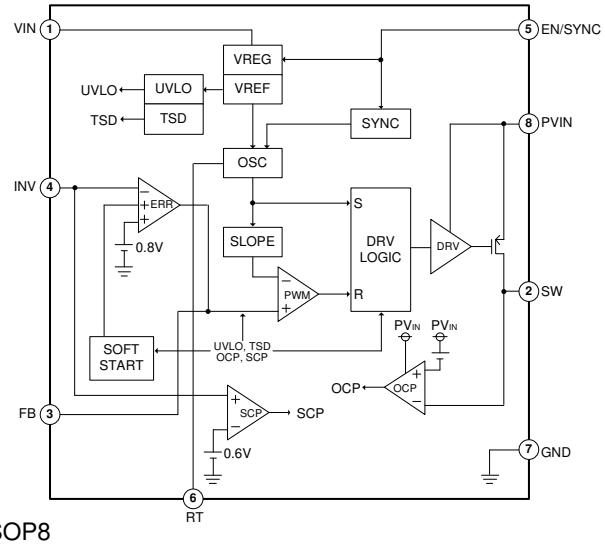


HRP7
(TOP VIEW)

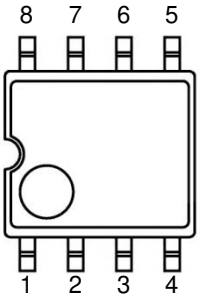


Pin No.	Pin Name	Function
1	VIN	Power supply input
2	SW	Output
3	FB	Error Amp output
4	GND	Ground
5	INV	Output cottage feedback
6	RT	Frequency setting resistor connection
7	EN/SYNC	Enable/Synchronizing pulse input
FIN	-	Ground

(BD9060F-C)



SOP8
(TOP VIEW)



Pin No.	Pin Name	Function
1	VIN	Power supply input(Note1)
2	SW	Output
3	FB	Error Amp output
4	INV	Output cottage feedback
5	EN/SYNC	Enable/Synchronizing pulse input
6	RT	Frequency setting resistor connection
7	GND	Ground
8	PVIN	Power supply input(Note1)

(Note 1) PVIN and VIN are shorted

Description of Blocks

・ERR(Error Amp)
The Error Amp block is an error amplifier used to input the reference voltage (0.8V (Typ)) and the INV pin voltage. The output FB pin controls the switching duty and output voltage Vo. These INV and FB pins are externally mounted to facilitate phase compensation. Inserting a capacitor and resistor between these pins enables adjustment of phase margin. (Refer to recommended examples on P. 15 to 17)

・SOFT START
The SOFT START block provides a function to prevent the overshoot of the output voltage Vo through gradually increasing the normal rotation input of the error amplifier when power supply turns ON to gradually increase the switching duty. The soft start time is set to 2.7ms (Typ).

・SYNC(EN/SYNC)
By making the “EN/SYNC” terminal less than 0.8V, the circuit can be shut down. Furthermore, by applying higher frequency pulse than the configured oscillation frequency to the “EN/SYNC” pin, external synchronization is possible. Frequency range of external synchronization is F_{OSC} x 1.05 ≤F_{sync}≤500kHz and 1.5 times of the set frequency. (Refer to P.11)

・OSC (Oscillator)
This circuit generates the pulse wave to be inputted to the SLOPE, and by connecting a resistor to the “RT”, 50kHz to 500kHz oscillating frequency can be configured. (Refer to P.15 Figure 23)

・SLOPE
This block generates sawtooth waves from the clock generated by the OSC. The generated sawtooth waves are sent to PWM.

・PWM
The PWM Comparator block is a comparator to make comparison between the FB pin and internal sawtooth wave and outputs a switching pulse. The switching pulse duty varies with the FB value. (Min Duty width: 250ns)

・TSD (Thermal Shutdown)
In order to prevent thermal destruction/thermal runway of the IC, the TSD block will turn OFF the output when the chip temperature reaches approximately 150°C or more. When the chip temperature falls to a specified level, the output will be reset. However, since the TSD is designed to protect the IC, the chip junction temperature should be provided with the thermal shutdown detection temperature of less than approximately.150°C.

・OCP (Over Current Protection)
While the output POWER P-ch MOS FET is ON, if the voltage between drain and source (on-resistancexload current) exceeds the reference voltage internally set with the IC, OCP will start up.This OCPis a self-return type. If OCP operates, the duty will be small, and output voltage will decrease. However, this protection circuit is only effective in preventing destruction from sudden accident. It does not support for continuous operation of the protection circuit (e.g. if a load, which significantly exceeds the output current capacitance, is normally connected). Furthermore, since the overcurrent protection detection value has negative temperature characteristics, consider thermal design.

・SCP (Short Current Protection)
While OCP operates, and if the output voltage falls below 70%, SCP will start up. If SCP operates, the output will be turned OFF after a period of 1024 pulse. It extends the output OFF time to reduce the average output current. In addition, during power start-up, this feature is masked until it reaches the set output voltage to prevent wrong trigger of SCP.

・UVLO (Under Voltage Lock-Out)
UVLO is a protection circuit for low voltage malfunction. It preventsmalfunction of the internal circuit at the time of sudden rise and fall of power supply voltage. It monitors the V_{IN} powersupply voltage and internal regulator voltage. If V_{IN} is less than 4.3V (Typ), Pch POWER MOS FET output is OFF. This threshold voltage has a hysteresis of 200mV (Typ). If V_{IN} is more than 4.5V (Typ) , UVLO will be released and the soft start circuit will be restarted.

・DRV (Driver)
This is a driver circuit for driving the gate electrode of the Pch POWER MOS FET output. By switching the driving voltage when the power supply voltage drop, it reduces the deterioration ofPOWER MOS FET on-resistance. It monitors the V_{IN} power supply voltage and internal regulator voltage. If V_{IN} is less than 7.5V (Typ), the driving voltage is switched.This threshold voltage has a hysteresis of 1.5V (Typ).

Absolute Maximum Ratings(Ta=25°C)

Parameter		Symbol	Limits	Unit
Power Supply Voltage		V_{IN}, PV_{IN}	42	V
Output Switch Pin Voltage		V_{SW}	V_{IN}	V
Output Switch Current		I_{SW}	4 (Note 1)	A
EN/SYNC Pin Voltage		$V_{EN/SYNC}$	V_{IN}	V
RT,FB,INV Pin Voltage		V_{RT},V_{FB}, V_{INV}	7	V
Power Dissipation	HRP7	Pd	5.51 (Note 2)	W
	SOP8	Pd	0.69(Note 3)	W
Storage Temperature Range		Tstg	-55 to +150	°C
Maximum Junction Temperature		Tjmax	150	°C

(Note 1) Pd should not be exceeded.
(Note 2) Reduce by 44mW/°C,when mounted on 2-layerPCB of 70mmx70mmx16mm
(PCB incorporates thermal via. Copper foil area on the reverse side of PCB: 10.5mmx10.5mm
Copper foil area on the reverse side of PCB: 70mmx70mm).
(Note 3) Reduce by 5.52mW/°C,when mounted on 1-layerPCB of 70mm x70mm x1.6mm

Caution: Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
Operating Power Supply Voltage	V_{IN}, PV_{IN}	5 to 35	V
Operating Temperature Range	Topr	-40 to +125	°C
Output Switch Current	I_{SW}	to 2	A
Output Voltage (min pulse width)	PW_{MIN}	250	ns
Oscillating Frequency	fosc	50 to 500	kHz
Oscillating Frequency Set Resistance	RT	27 to 360	kΩ
External Sync Frequency	f_{SYNC}	F_{OSC} x 1.05 ≤F_{sync}≤F_{OSC} x 1.5 (Note 1)	kHz

(Note 1) It should be configured at less than 500kHz.

Electrical Characteristics(Unless otherwise specified, Ta=- 40°C to +125°C, V_{IN}=13.2V,$V_{EN/SYNC}$ =5V)

Parameter	Symbol	Guaranteed Limit			Unit	Conditions
		Min	Typ	Max		
Standby Circuit Current	I_{STB}	—	0	5	μA	$V_{EN/SYNC}$=0V, Ta=-40°Cto +105°C
Circuit Current	I_{CC}	—	3.7	8.0	mA	I_{OUT}=0A, RT=51kΩ, V_{INV}=0.7V
SW Block						
POWER MOS FET ON Resistance	R_{ON}	—	0.3	0.6	Ω	
Operating Output Switch Current Of Overcurrent Protection (Note 1)	I_{LIMIT}	2.5	4	—	A	
Output Leak Current	I_{OLEAK}	—	0	5	μA	V_{IN}=35V, $V_{EN/SYNC}$ =0V, Ta=-40°C to +105°C
Error Amp Block						
Reference Voltage 1	$V_{REF}1$	0.784	0.800	0.816	V	V_{FB}= V_{INV}
Reference Voltage 2	$V_{REF}2$	0.780	0.800	0.820	V	V_{FB}= V_{INV}, V_{IN} =5V to 35V
Reference Voltage Input Regulation	ΔV_{REF}	—	0.5	—	%	V_{IN} =5V to 35V
Input Bias Current	I_B	-1	—	—	μA	V_{INV} =0.6V
Maximum FB Voltage	V_{FBH}	2.0	2.5	—	V	V_{INV} =0V
Minimum FB Voltage	V_{FBL}	—	0.51	0.80	V	V_{INV} =2V
FB Sink Current	I_{FBSINK}	-2.45	-1.23	-0.45	mA	V_{FB}=1V, V_{INV}=1V
FB Source Current	$I_{FBSOURCE}$	1.0	6.3	15.0	mA	V_{FB}=1V, V_{INV}=0.6V
Soft Start Time (Note 1)	T_{SS}	1.7	2.7	5.0	ms	
Oscillator Block						
Oscillating Frequency	fosc	285	300	315	kHz	RT=51kΩ
Frequency Input Regulation	Δfosc	—	0.5	—	%	V_{IN} =5V to 35V
Enable/Sync Input Block						
Output ON Voltage	V_{ENON}	2.6	—	—	V	$V_{EN/SYNC}$ Sweep Up
Output OFF Voltage	V_{ENOFF}	—	—	0.8	V	$V_{EN/SYNC}$ Sweep Down
Sink Current	$I_{EN/SYNC}$	—	19	60	μA	

(Note 1)This item is not 100% production tested.
(Caution) EN / SYNC and RT are shorted at VIN and EN / SYNC short-circuited, IC is destroyed in VIN ≥ 7V,

Typical Performance Curves

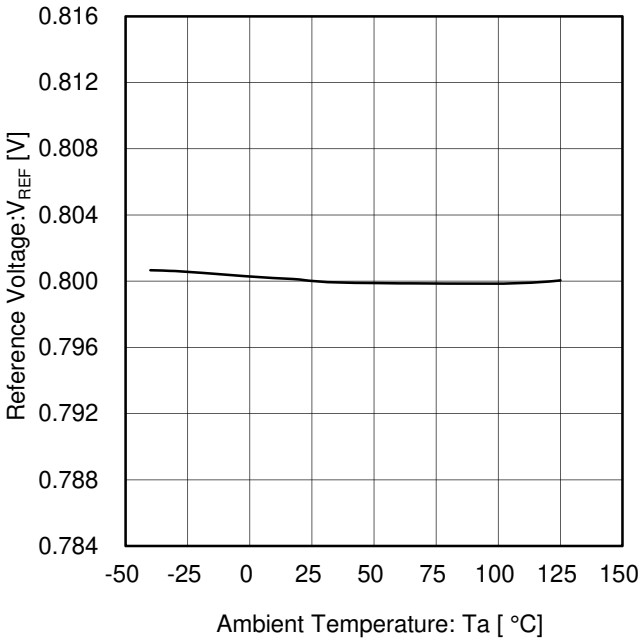


Figure 1. Reference Voltage vs Temperature

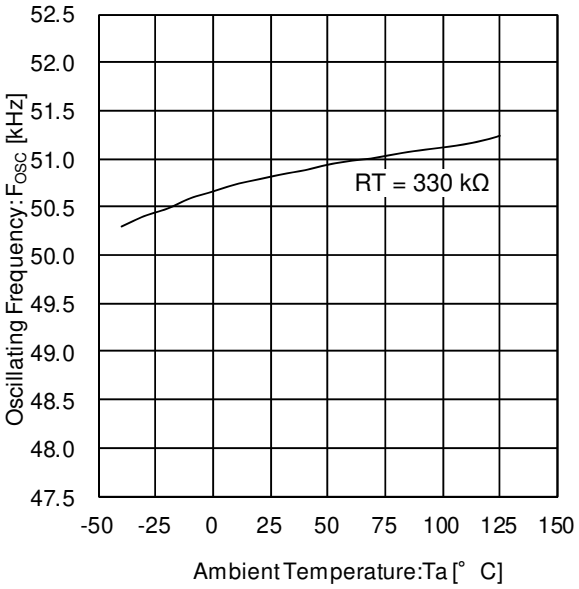


Figure 2. Oscillating Frequency vs Temperature (RT=330kΩ)

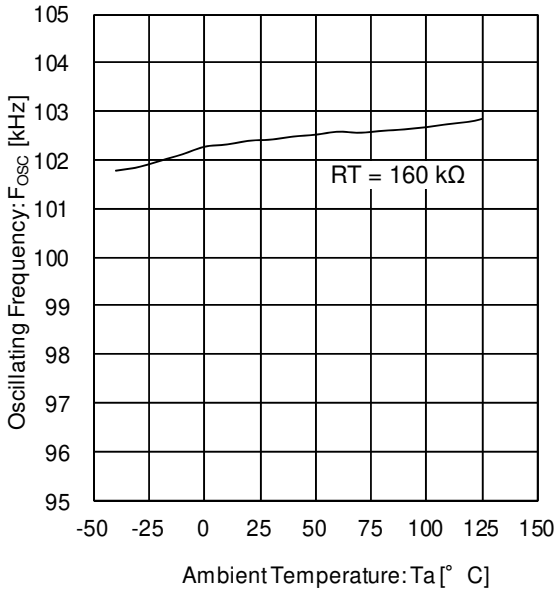


Figure 3.Oscillating Frequency vs Temperature (RT=160kΩ)

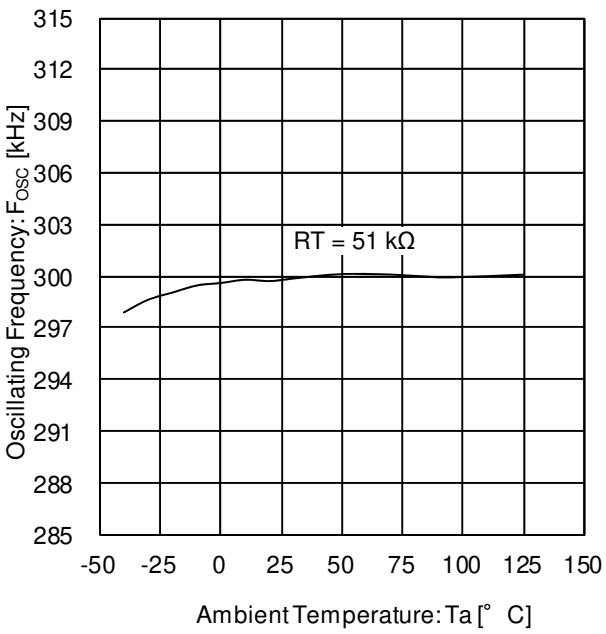


Figure 4.Oscillating Frequency vs Temperature (RT=51kΩ)

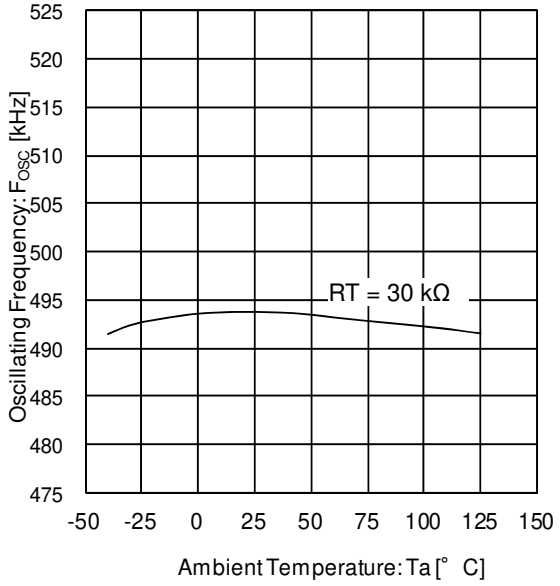


Figure 5.Oscillating Frequency vs Temperature (RT=30kΩ)

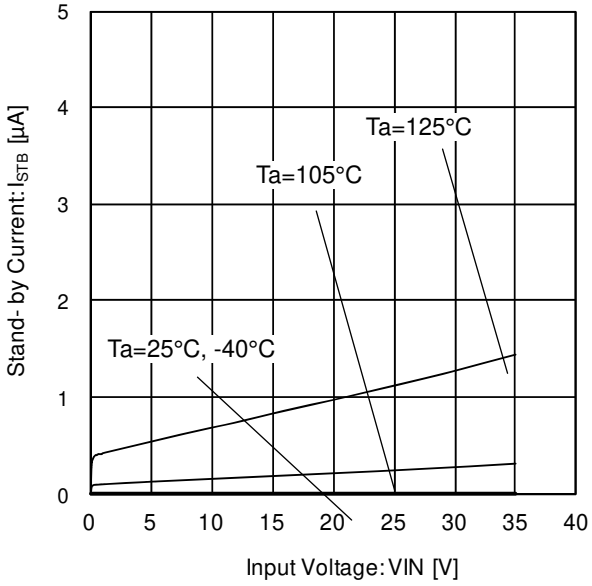


Figure 6.Standby Circuit Current vs Input Voltage

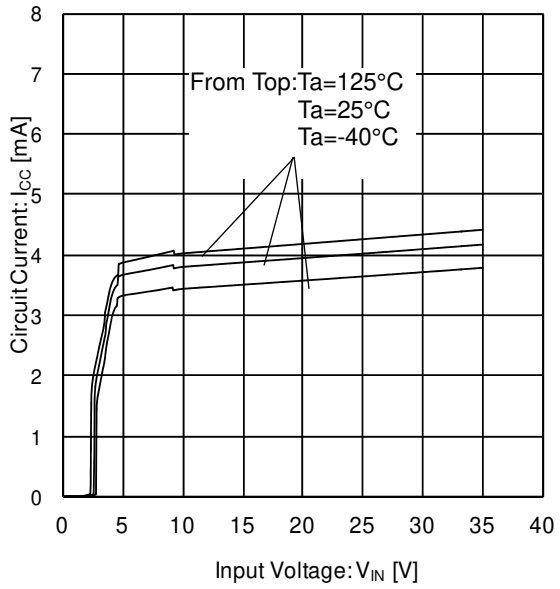


Figure 7. Circuit Current vs Input Voltage

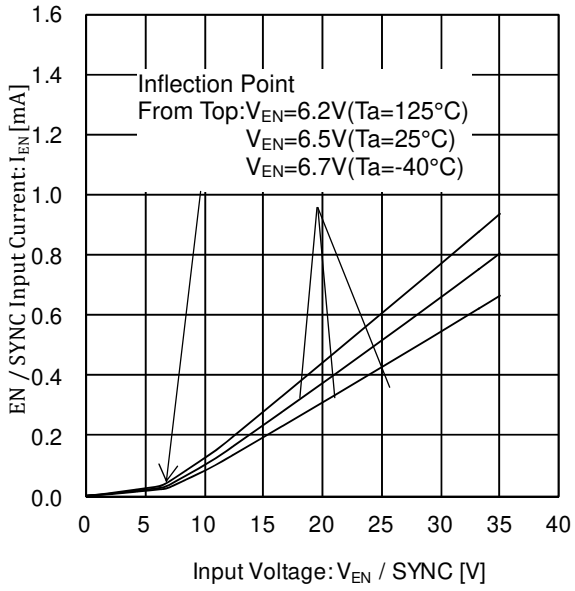


Figure 8.EN/SYNC Input Current vs Input Voltage

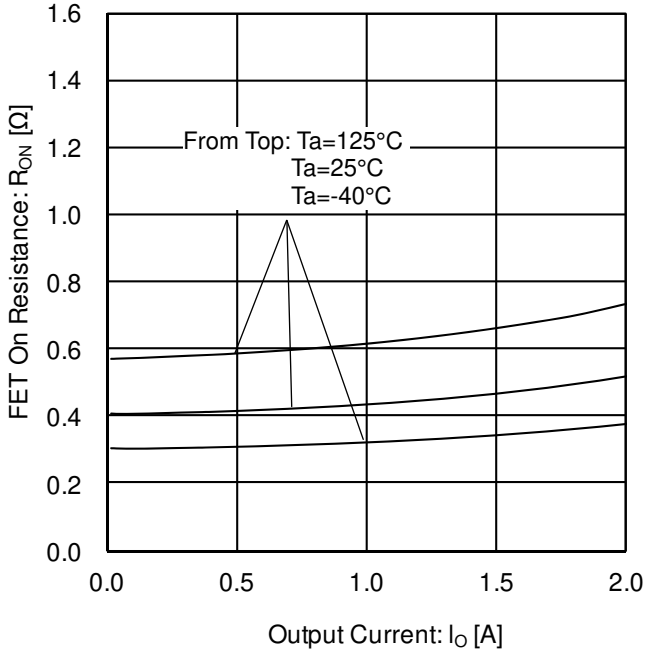


Figure 9. ON Resistance vs Output Current
(V_{IN}=5V)

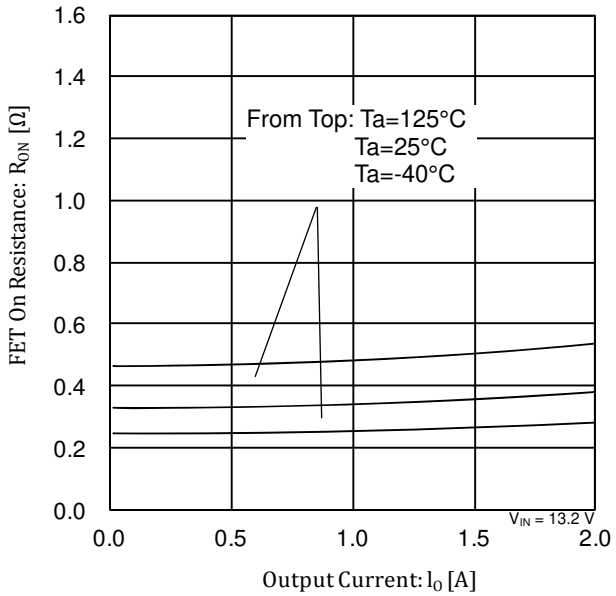


Figure 10. ON Resistance vs Output Current
(V_{IN} =13.2V)

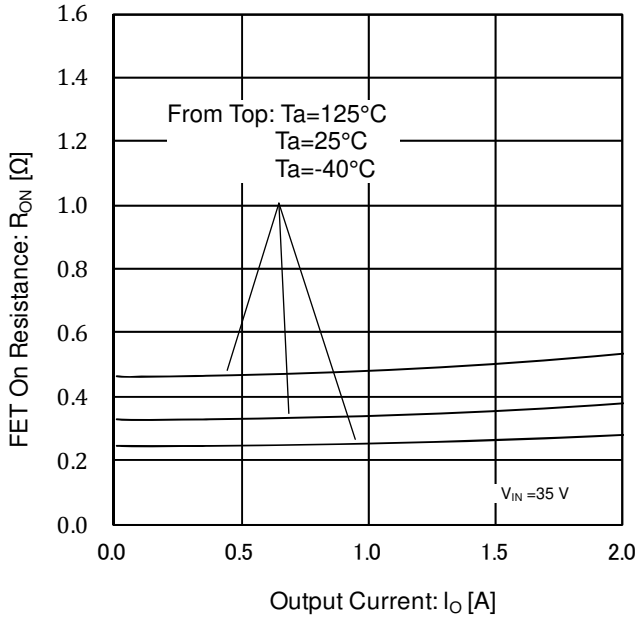


Figure 11. ON Resistance vs Output Current
(V_{IN} =35V)

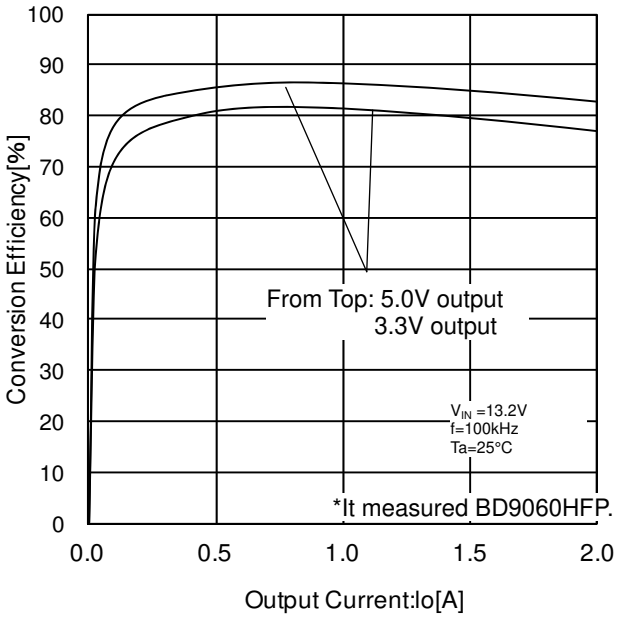


Figure 12.Conversion Efficiency vs Output Current
(f=100kHz)

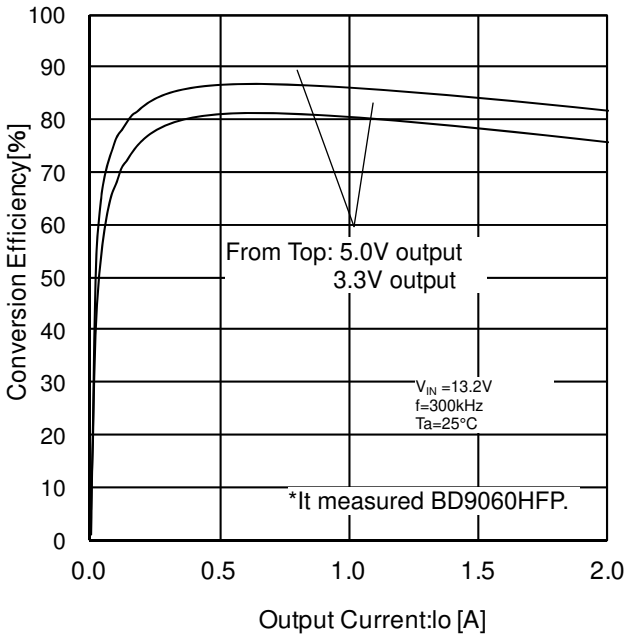


Figure 13.Conversion Efficiency vs Output Current (f=300kHz)

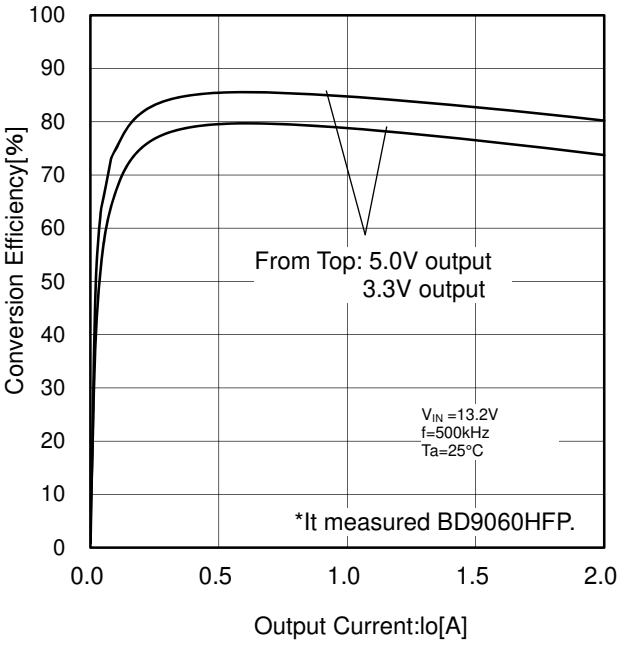


Figure 14.Conversion Efficiency vs Output Current (f=500kHz)

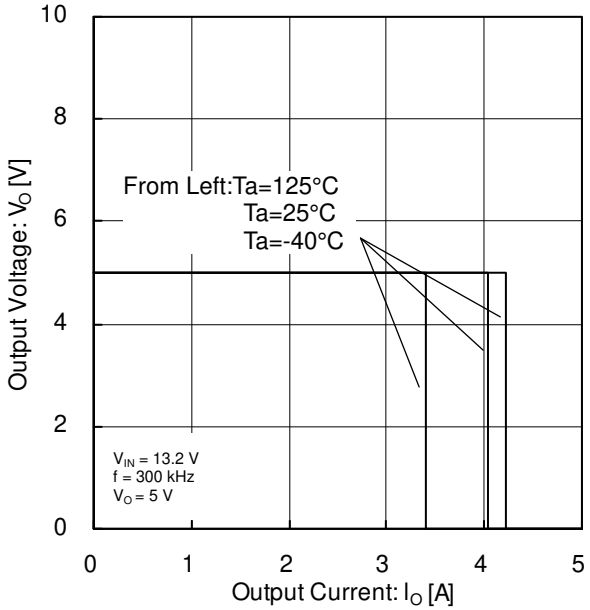


Figure 15.Overcurrent Protected Operation Current

Timing Chart

・Basic Operation

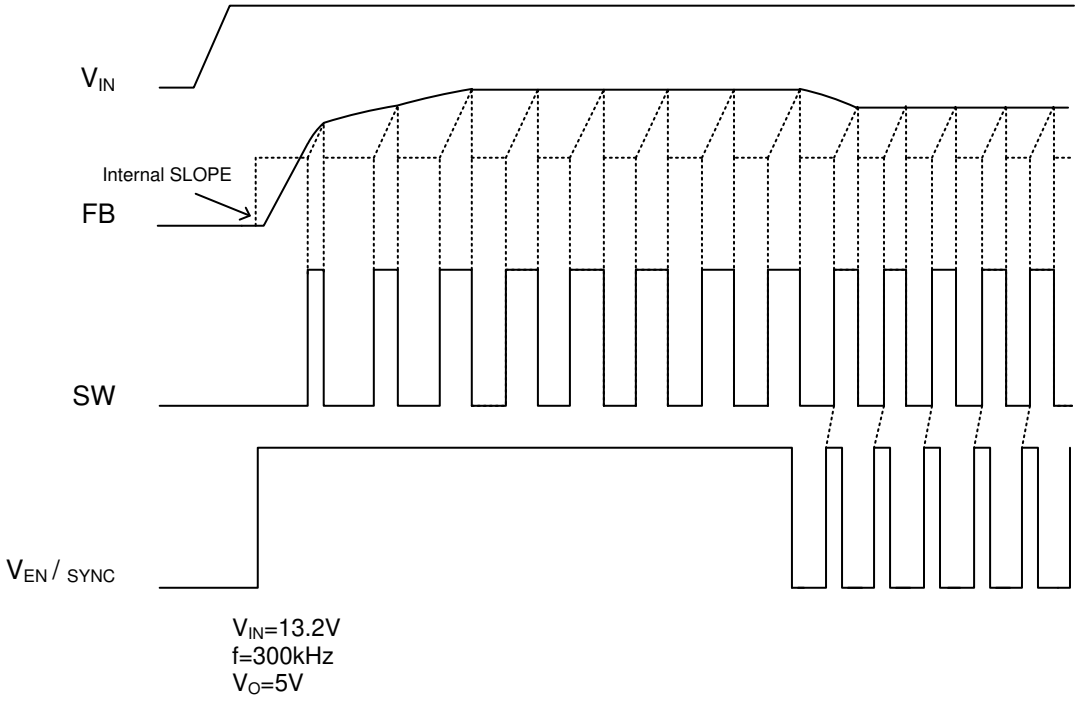


Figure 16. Timing Chart (Basic Operation)

・Over Current Protection Operation

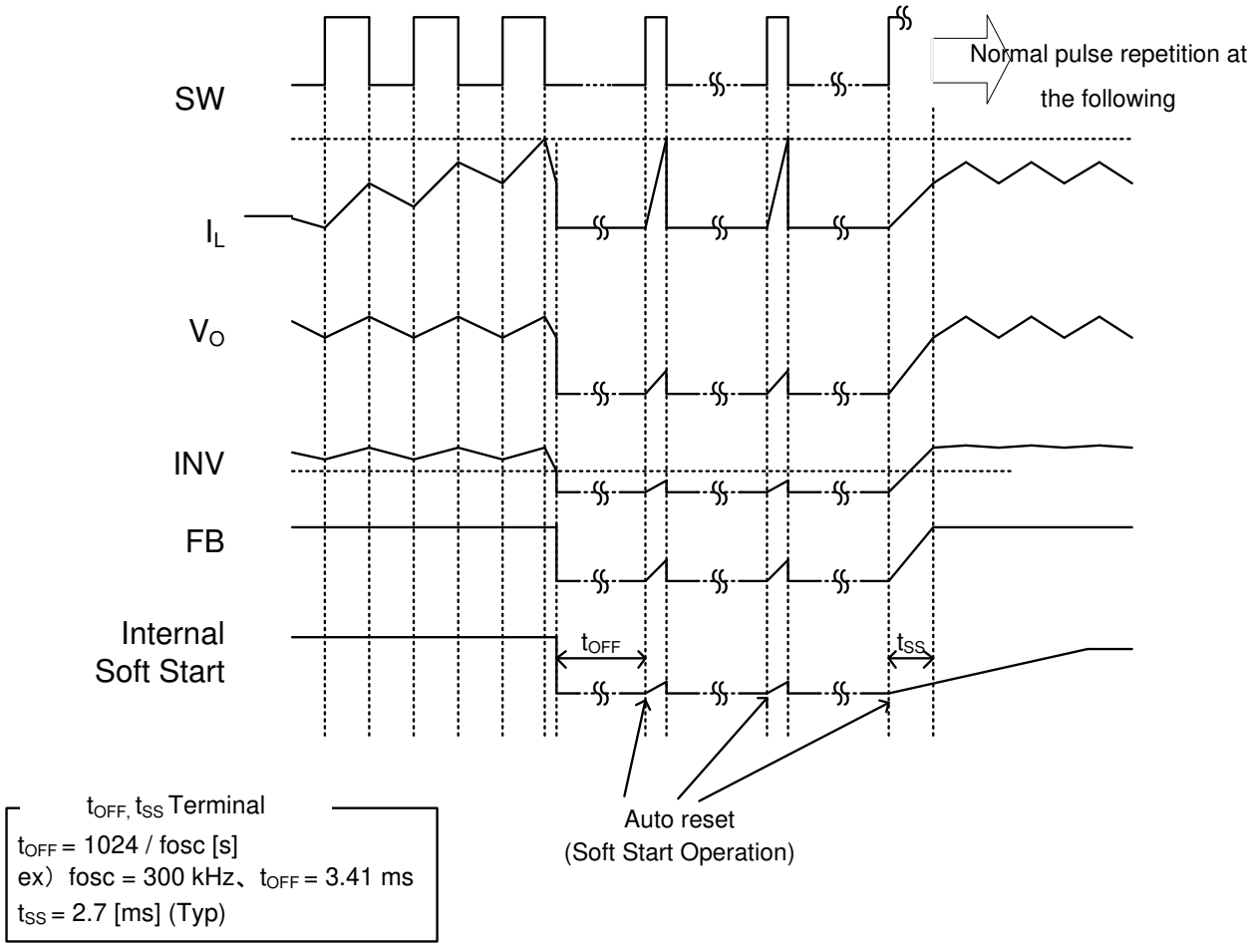


Figure 17.Timing Chart (Over Current Protection Operation)

External Synchronizing Function

In order to activate the external synchronizing function, connect the frequency-setting resistor to the RT pin and then input a synchronizing signal to the EN/SYNC pin. As the synchronizing signal, input a pulse wave higher than a frequency determined with the setting resistor(RT).However, the external sync frequency should be configured between 1.05 to 1.5 times the set frequency.
(Frequency determined with RT x 1.05 ≤ External sync frequency ≤ Frequency determined with RT x 1.5)
(ex.) When the configured frequency is 300kHz, the external sync frequency should be between 315kHz to 450kHz.
Furthermore, the pulse wave's LOW voltage should be under 0.8V and the HIGH voltage over 2.6V,(when the HIGH voltage is over 6V the EN/SYNC input current increases [Refer to p.7 Fig.8])the through rate of stand-up(and stand-down)under 20V/µs. The duty of External sync pulse should be configured between 20% to 80%.

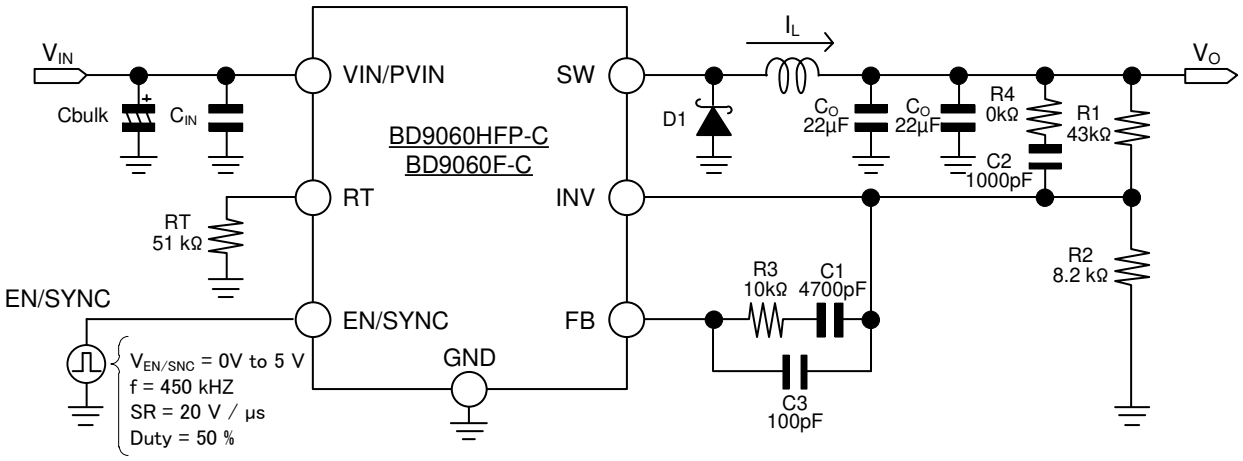


Figure 18.External Sync Sample Circuit
(V_O=5V,I_O=1A,f=300kHz,EN/SYNC=450kHz)

Selection of Components Externally Connected

Necessary parametersare as followsin designingthe power supply.

Parameter	Symbol	SpecificationCase
Input Voltage	V_{IN}	8V to 33V
Output Voltage	V_O	5V
Output Ripple Voltage	ΔV_{PP}	20mVp-p
Input Range	I_O	Min 0.5A / Typ1.0A / Max 1.5A
Switching Frequency	f_{SW}	300kHz
Operating Temperature Range	Topr	-40°Cto+125°C

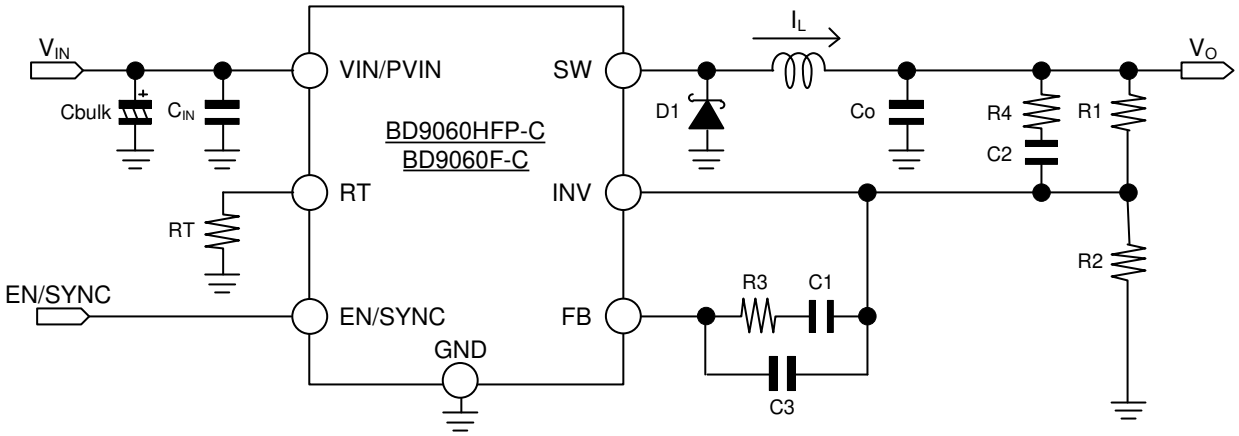


Figure 19.Application Sample Circuit

1. Setofoutputinductor L constant

In DC/DC converter, to supply electric current continuously to the load, the LC filter is necessary for the smoothness of the output voltage.ΔI_L that flows to the inductor becomes small when a big inductor of the inductance value is selected, and the voltage of the output ripple becomes small. It is a trade-off against the responsiveness, the size and the cost of the inductor.

The inductance value of the inductor is shown in the next expression.

$$L = \frac{(V_{IN(MAX)} - Vo) \times Vo}{V_{IN(MAX)} \times f_{SW} \times \Delta I_L} \quad \cdot \cdot \cdot \text{(a)}$$

($V_{IN(MAX)}$:Maximum input voltage,ΔI_L:Inductor ripple current)

ΔI_L is set to make SW the continuous control action (I_L keeps continuously flowing) usually.The condition of thecontinuous operation is shown in the next expression.

$$Io > \frac{(V_{IN} - Vo) \times Vo}{2 \times V_{IN} \times f_{SW} \times L} \quad \cdot \cdot \cdot \text{(b)}$$

(I_O :Load current)

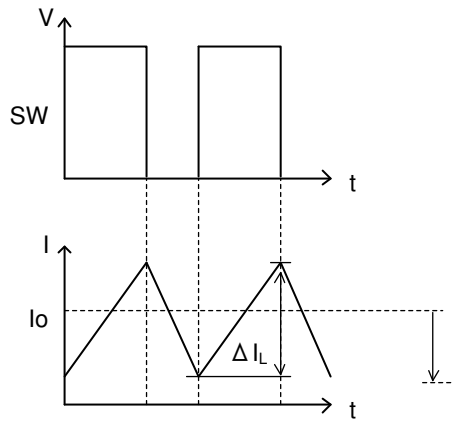


Figure 20. Continuous Action

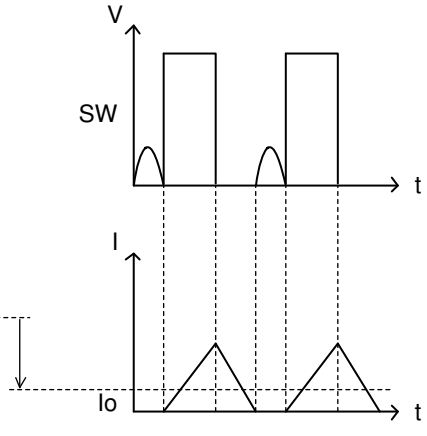


Figure 21. Discontinuous Action

The smaller the ΔI_L, the Inductor core loss(iron loss) and loss due to ESR of the output capacitor, ΔV_{PP} will be reduced. $\Delta V_{PP}$is shown in the next expression.

$$\Delta V_{PP} = \Delta I_L \times ESR + \frac{\Delta I_L}{8 \times Co \times f_{SW}} \quad \cdot \cdot \cdot \text{(c)}$$

(ESR: Equivalent series resistance of output capacitor, C_O: Output condenser capacity)

ΔI_L is set to approximately 10% to 40% of I_O. Generally, even if ΔI_L is somewhat large, ΔV_{PP} of the target is satisfied because the ceramic capacitor has super-low ESR. In that case, it is also possible to use it by the discontinuous action. The inductance value of the inductor can be set small as an advantage.
It contributes to the miniaturization of the set because of the large rated current, small inductor is possible if the inductance value is small.The disadvantagesare the increase in core losses in the inductor, the decrease in maximum output current, and the deterioration of theresponse. When other capacitors (electrolytic capacitor, tantalum capacitor, and electroconductive polymer etc) are used for output capacitor C_O,check theESRfromthe manufacturer's data sheetand determine the ΔI_L to fitwithin the acceptable range of ΔV_{PP}.Especially inthe case ofelectrolytic capacitor, because the capacity decrease at the low temperature is remarkable, ΔV_{PP}increases. When using capacitor at the low temperature, it is necessary to note this.The maximum output electric current is limited to the overcurrent protection working current as shown in the next expression.

$$Io_{(MAX)} = I_{LIMIT(MIN)} - \frac{\Delta I_L}{2} \quad \cdot \cdot \cdot \text{(d)}$$

Where: $I_{O(MAX)}$ is Maximum output current, $I_{LIMIT(min)}$:Minimum operating output switch current of overcurrent protection2.5A

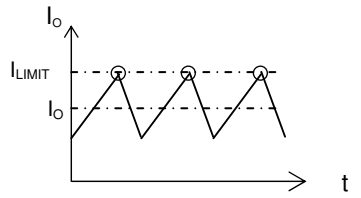


Figure 22.OvercurrentDetection

The shield type (closed magnetic circuit type) is the recommended type of inductor. There is no problem in the open magnetic circuit type if the application is low cost and does not consider noise.In that case, there is magnetic field radiation between the parts.There should be enough space between the parts.
For ferrite core inductor type, in particular, please note the magnetic saturation.It is necessary not to saturate the core in allcases.Care must be taken giventhe provisions of thecurrent rating because it differs according to each manufacturer. Pleaseconfirm the rated current at the maximum ambient temperature of the application to the manufacturer.

2. SetofoutputCapacitor C_O constant

The output capacitor is selected on the basis of ESR that is required from the expression (c).ΔV_{PP} can be reduced by using a capacitor with a small ESR.The ceramic capacitor is the best selection that meets this requirement.The ceramic capacitor contributes to the miniaturization of the set because it has small ESR.Please confirm frequency characteristic of ESR from the datasheet of the manufacturer, and select the one that ESR in the switching frequency used is low.It is necessary to note the ceramic capacitor because the DC biasing characteristic is remarkable. For the voltage rating of the ceramic capacitor, twice or more of the maximum output voltage is usually required.By selecting those high voltage rating, it is possible to reduce the influence of DC bias characteristics.Moreover, in order to maintain good temperature characteristics, the one with the characteristic of X7R and X5R or more is recommended.Because the voltage rating of a mass ceramic capacitor is low, the selection becomes difficult in the application with high output voltage. In that case, please select electrolytic capacitor. Please select the one with voltage rating of 1.2 times or more of the output voltage when you use electrolytic capacitor.Electrolytic capacitors are high blocking voltage, a large capacity, and the little DC biasing characteristic, and are generally cheap.Because main failure mode is OPEN, it is effective to use electrolytic capacitor selection in the application when reliability is demandedsuch as in-vehicle. There are disadvantages as, ESR is relatively large, and decrease of capacity at low temperatures.It is necessary to note this so that the low temperature, and in particular, ΔV_{PP} may increase.Moreover, the feature of this capacitor is to define the lifetime because there is possible dry up. A very excellent characteristic of the tantalum capacitor and the electro-conductive polymer is the thermal characteristic unlike the electrolytic capacitor.The design is facilitated because there is little DC biasing characteristic like the electrolytic capacitor.Typically, for voltage rating, a tantalum capacitor is selected twice the output voltage, and for conductive polymer is selected 1.5 times more than the output voltage.The disadvantage of the tantalum capacitor is that the failure mode is SHORT, and the breakdown voltage is low.It is not generally selected in the application that reliability such as in-vehicle is demanded.The disadvantage of the electroconductive polymer is that the failure mode is SHORT(SHORT happens by accident chiefly, though it is OPEN),the breakdown voltage is low , and generally expensive.Although in most cases ignored, these capacitors are rated in ripple current. The RMS values of the ripple electric current obtained in the next expression must not exceed the ratings ripple electric current.

$$I_{CO(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \quad \cdot\cdot\cdot \text{(e)}$$

Where:$I_{CO(RMS)}$ is RMS value of the ripple electric current

In addition,with respect toC_O, choose capacitance value lessthan the valueobtainedby the following equation.

$$Co_{(MAX)} = \frac{1.7\ ms \times (I_{LIMIT(MIN)} - I_{O\ (MAX)})}{V_O} \quad \cdot\cdot\cdot \text{(f)}$$

Where: $I_{LIMIT(MIN)}$ is OCP operation output switch current(Min) 2.5A,1.7ms: Soft Start Time(Min)

There is a possibility that boot failure happens when the limits from the above-mentioned are exceeded.Especiallyif thecapacitance valueis extremely large, you may activate over-current protectionby theinrush currentat startup, and theoutputdoes not start. Please confirm this well on the actual circuit.The capacitance value is an important parameter that decides the LC resonant frequency. For stable transient response, the loop is dependent on the C_O.Please select after confirming the setting of the phase compensation circuit.

3. Setting constant of capacitor C_{IN} / C_{bulk} input

The input capacitor is usually required for two types of decoupling: capacitorsC_{IN} and bulk capacitorsC_{bulk}.Ceramic capacitor 1μF to 10μF is necessary for the decoupling capacitor.Ceramic capacitor is effective by being placed as close as possible to the VIN pin.Voltage rating is recommended to more than 1.2 times the maximum input voltage, or twice the normal input voltage.About the bulk capacitor, the decrease in the line voltage is prevented, and the role of the backup power supply to keep the input potential constant is realized.The low ESR electrolytic capacitor with large capacity is suitable for the bulk capacitor.It is necessary to select the best capacitance value as per set application.When impedance on the input side is high because wiring from the power supply to VIN is long, etc., then high capacitance is needed.In actual use conditions,it is necessary to verify that there is no problem when IC operation turns off the output due to the decrease of V_{IN} at transient response.In that case, please be careful not to exceed the rated ripple current of the capacitor. The RMS value of the input ripple electric current is obtained in the next expression.

$$I_{CIN(RMS)} = Io_{(MAX)} \frac{\sqrt{Vo \times (V_{IN} - Vo)}}{V_{IN}} \quad \cdot\cdot\cdot \text{(g)}$$

where: $I_{CIN(RMS)}$ is RMS value of the input ripple electric current

In addition, in automotive and other applications requiring reliability, it is recommended that capacitors are connected in parallel to accommodate a multiple of electrolytic capacitors minimal dry up chances.We will recommend making it to two series + two parallel structures to decrease the risk of the ceramic capacitor by short destruction.The line has been improved to the summary respectively by 1pack in each capacitor manufacturer and confirms two series and two parallel structures to each manufacturer.

4. Setting output voltage

Output voltage is governed by the following equation.

$$Vo = 0.8 \times \frac{R1 + R2}{R2} \quad \cdot\cdot\cdot \text{(h)}$$

Please set return resistance R2 below 30kΩto reduce the error margin by the bias current.In addition, since power efficiency is reduced with a small R1 + R2, please set the current flowing through the feedback resistor to be small enough than the output current I_O.

5. Selectionof the schottky barrier diode

The schottky barrier diode that has small forward voltage and short reverse recovery time is used for Di.An important parameter for selecting it is an average rectified current and a direct current inverse-direction voltage.Average rectified current $I_{F(AVG)}$ is obtained in the next expression.

$$I_{F(AVG)} = Io_{(MAX)} \times \frac{V_{IN(MAX)} - Vo}{V_{IN(MAX)}} \quad \cdot\cdot\cdot \text{(i)}$$

where: $I_{F(AVG)}$ isAverage rectified current

The absolute maximum rating of the schottky barrier diode rectified current average is more than 1.2 times $I_{F(AVG)}$ and the absolute maximum rating of the DC reverse voltage is greater than or equal to 1.2 times the maximum input voltage. The loss of Di is obtained in the next expression.

$$P_{Di} = Io_{(MAX)} \times \frac{V_{IN(MAX)} - Vo}{V_{IN(MAX)}} \times VF \quad \cdots \text{(j)}$$

Where: VF is Forward voltage in $I_{o(MAX)}$ condition

Selecting a diode that has small forward voltage, and has short reverse recovery time is highly effective.Please select the 0.6V Max for the forward voltage. Please note that there is possibility of the internal element destruction when a diode with larger VF than this is used.Because the reverse recovery time of the schottky barrier diode is so shortthat it is possible to disregard, the switching loss can be disregarded. When it is necessary that the diode endures in the state of the output short-circuit, power dissipation ratings and the heat radiation ability are needed in addition. The rated current is required about 1.5 times the overcurrent detection value.The loss when the output is short-circuited is obtained in the next expression.

$$P_{Di(SHORT)} = I_{LIMIT(MAX)} \times VF \quad \cdots \text{(k)}$$

Where: $I_{LIMIT(MAX)}$ isOCP operation output switch current(MAX) 6A

6. Setting the oscillating frequency

An internal oscillating frequency can be set by the resistance connected with RT.
The range that can be set is 50kHz to 500kHz, and the relation between resistance and the oscillation frequency is decided as shown in the figure below.When setting beyond this range, there is a possibility of non-oscillation and IC operation cannot be guaranteed.

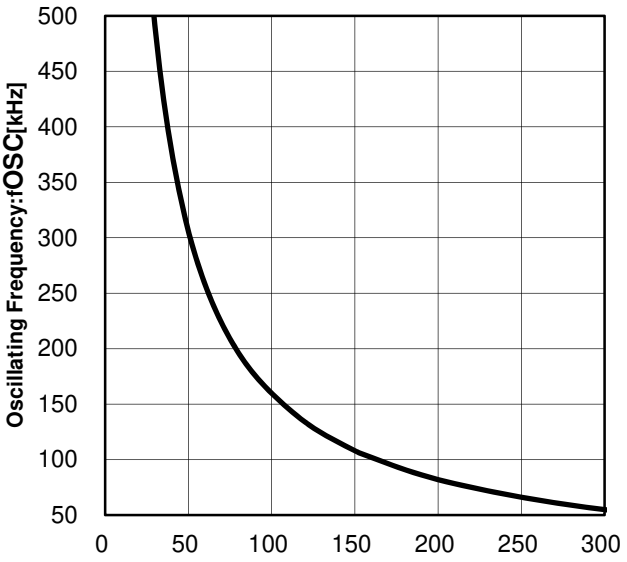


Figure 23.Oscillating Frequency vs RT

RT[kΩ]	fosc[kHz]	RT[kΩ]	fosc[kHz]
27	537	100	160
30	489	110	146
33	449	120	134
36	415	130	124
39	386	150	108
43	353	160	102
47	324	180	91
51	300	200	82
56	275	220	75
62	250	240	69
68	229	270	61
75	209	300	55
82	192	330	50
91	174	360	46

Graph'svalue is Typical and You need to consider thevariationof±5% respectively.

7. Setting the phase compensation circuit

A high response performance is achieved by setting 0dB crossing frequency fc of the total gain (frequency at the gain 0dB) high.However, you need to be aware of the relationship to be a trade-off between stability.Moreover, DC/DC converter application is sampled by switching frequency, and should suppress the gain in switching frequency.It is necessary to set 0dB crossing frequency to 1/10 or less of the switching frequency.In summary,target these characteristics with the application as follows.

- When thegain is 1(0dB), phase lagis less than or equal to135 ˚(More than45 ˚phase margin).
- 0dB crossing frequency is 1/10 times or less of the switching frequency.To improve the responsiveness, higher frequency of switching frequency is needed.

We recommend the Bode diagram to be made by using the transfer function of the control loop to obtain frequency characteristic of target for the phase compensation circuit.Make sure the frequency characteristics of the total gain by totaling the transfer function of the following three.

$$G_{LC} = \frac{1+\frac{s}{2\pi \times f_{ESR}}}{1+\frac{s}{Q \times 2\pi \times f_{LC}}+\left(\frac{s}{2\pi \times f_{LC}}\right)^2} \quad \cdot\cdot\cdot \text{(l)}$$

$$G_{FB} = \frac{\left(1+\frac{s}{2\pi \times f_{Z1}}\right)\left(1+\frac{s}{2\pi \times f_{Z2}}\right)}{s \times R1 \times C1\left(1+\frac{s}{2\pi \times f_{P1}}\right)\left(1+\frac{s}{2\pi \times f_{P2}}\right)} \quad \cdot\cdot\cdot \text{(m)}$$

$$G_{PWM} = \frac{V_{IN}}{\Delta V_{RAMP}} \quad \cdot\cdot\cdot \text{(n)}$$

Where: $G_{LC}$is Transfer functionof theLCresonance
G_{FB} is Transfer functionof thephase compensation
G_{PWM} is Transfer functionof thePWM, ΔV_{RAMP} : 0.7V

Because BD9060HFP-C/BD9060F-C is a voltage mode control, two poles and two zeroes of the phase interpolator circuitshown in the figure below can be added.Necessary frequencies of poles and zeroes are obtained in the following.

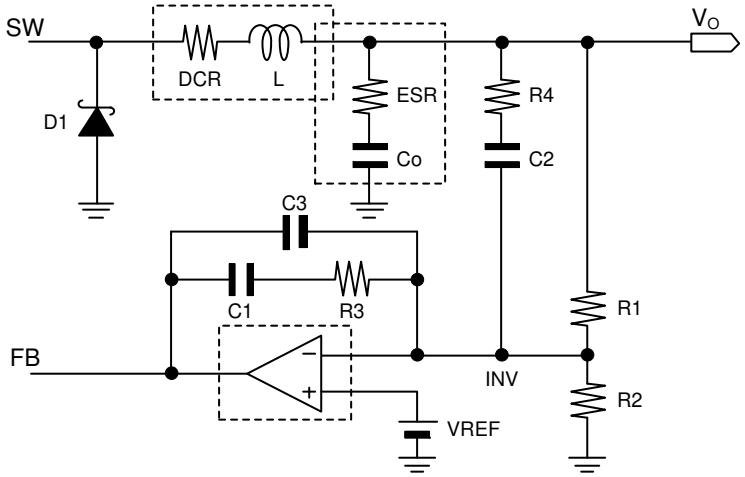


Figure 24. Phase Compensation Circuit

$$f_{LC} = \frac{1}{2\pi}\sqrt{\frac{Ro+DCR}{L \times Co(Ro+ESR)}} \quad \cdot\cdot\cdot \text{(o)}$$

$$f_{ESR} = \frac{1}{2\pi \times ESR \times Co} \quad \cdot\cdot\cdot \text{(p)}$$

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C1} \quad \cdot\cdot\cdot \text{(q)}$$

$$f_{Z2} = \frac{1}{2\pi \times (R1+R4) \times C2} \quad \cdot\cdot\cdot \text{(r)}$$

$$f_{P1} = \frac{C1+C3}{2\pi \times R3 \times C1 \times C3} \quad \cdot\cdot\cdot \text{(s)}$$

$$f_{P2} = \frac{1}{2\pi \times R4 \times C2} \quad \cdot\cdot\cdot \text{(t)}$$

Where: DCR isDCresistanceof the inductor
R_O isLoad resistance

Frequency response is optimized by placing the appropriate frequency of these poles and zeros.The standard is as follows.

$$0.2 \times f_{LC} \leq f_{Z1} \leq f_{LC} \quad \cdots \text{(u)}$$

$$0.5 \times f_{LC} \leq f_{Z2} \leq f_{LC} \times 2 \quad \cdots \text{(v)}$$

$$f_{P1} \approx f_{SW} \times 0.5 \quad \cdots \text{(w)}$$

$$f_{P2} \approx f_{ESR} \quad \cdots \text{(x)}$$

The phase delays (-180°) by the LC resonance can be canceled by setting the phase amends as mentioned above. fp2is not necessary if f_{ESR} is higher than the SW frequency (The ceramic capacitor that has low ESR is used for the output capacitor).In addition, if Q(quality factor)of the LC filter is high,the gain may peak out, and phase margin can not be secured sufficiently.When Q is high, f_{z1} and f_{z2} are brought close to f_{LC} as much as possible. Q is obtained in the next expression.

$$Q = \frac{\sqrt{L \times Co \times Ro(Ro+ESR)}}{L+Co \times Ro \times ESR} \quad \cdots \text{(y)}$$

$$\approx Ro \times \sqrt{\frac{Co}{L}} \quad \cdots \text{(z)}$$

The setting method by above-mentioned conditional expression is suitable as the starting point of the phase amends.Please confirm that you meet the frequency characteristics to create a Bode plot.Actually, the frequency characteristic changes are greatly affected by the type and the condition (temperature, etc.) of parts that are used, and the wire routing and layout for the PCB.For instance, the LC resonance point moves because of the capacity decrease at low temperature and an increase of ESR when electrolytic capacitor is used for the output capacitor that there is even possibility of oscillation.To C1, C2 and C3 for phase compensation capacitor,use of CH products or temperature compensation type C0G, etc. with an excellent thermal characteristic are recommended.

Please confirm stability and responsiveness in actual equipment.

To check on the actual frequency characteristics, use a FRA or a gain-phase analyzer.Moreover, the method of observing the degree of change by the loading response can be done, when these measuring instruments do not exist.The response is low when the output is made to change under no load to maximum load, and there is a lot of variation quantities.It can be said that the phase margin degree is low when there is a lot of ringing frequencies after it changes, usually two times or more of ringing as standard. However, a quantitative phase margin degree cannot be confirmed.

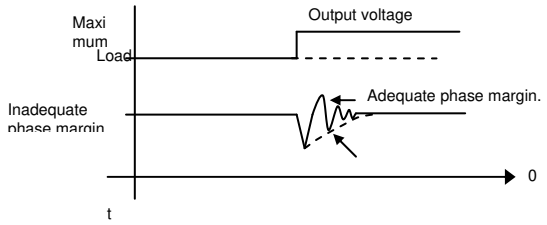


Figure 25. Load Response

Application Examples

Parameter	Symbol	Specificationcase
Input Voltage	V_{IN}	8V to 28V
Output Voltage	V_O	5V
Output Ripple Voltage	ΔV_{PP}	20mVp-p
Output Current	I_O	Min 0.5A / Typ 1.0A / Max 1.5A
Switching Frequency	f_{SW}	300kHz
Operating Temperature	Topr	-40°Cto+125°C

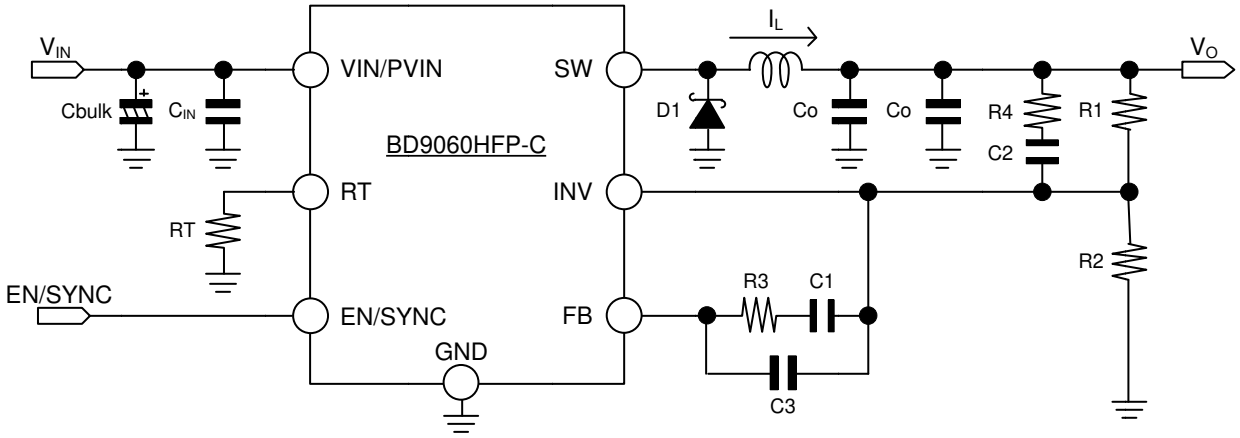
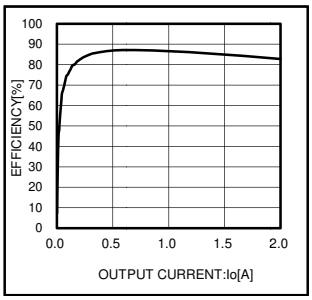
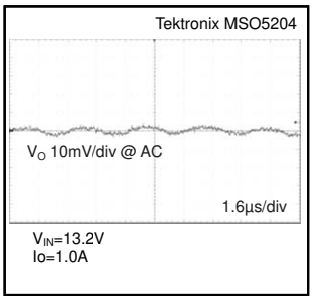


Figure 26. Application Examples 1

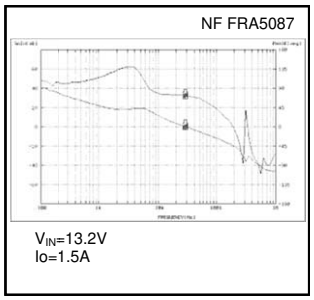
No	Package	Parameters	Part name(series)	Type	Manufacturer
R1	1005	43kΩ, 1%, 1/16W	MCR01 series	Chip resistors	ROHM
R2	1005	8.2kΩ, 1%, 1/16W	MCR01 series	Chip resistors	ROHM
R3	1005	10kΩ, 1%, 1/16W	MCR01 series	Chip resistors	ROHM
R4	1005	0kΩ, 1%, 1/16W	MCR01 series	Chip resistors	ROHM
RT	1005	51kΩ, 1%, 1/16W	MCR01 series	Chip resistors	ROHM
C1	1005	4700pF,R,50V	GCM series	Ceramic capacitors	MURATA
C2	1005	1000pF,CH,50V	GCM series	Ceramic capacitors	MURATA
C3	1005	100pF,CH,50V	GCM series	Ceramic capacitors	MURATA
C_{IN}	3216	2.2μF,X7R.50V	GCM series	Ceramic capacitors	MURATA
C_O	3216	22μF,X7R,16V	GCM series	Ceramic capacitors	MURATA
C_{bulk}		220μFx2,35V	CZ series	Electrolytic capacitors	NICHICON
L	10x10x3.8(mm^3)	33μH	CLF10040 series	Coil	TDK
D	CPD	Average I = 6A Max	RB095B-40	Schottky Diodes	ROHM



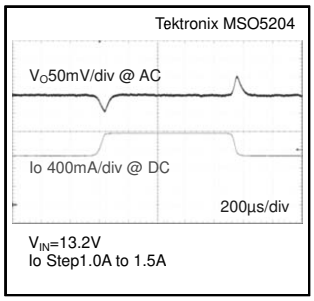
Conversion Efficiency



Output Ripple Voltage



Frequency Characteristics



Load Change

Parameter	Symbol	Specificationcase
Input Voltage	V_{IN}	5 V to 16V
Output Voltage	V_O	3.3V
Output Ripple Voltage	ΔV_{PP}	20mVp-p
Output Current	I_O	Min 0.1A / Typ 0.4A / Max 0.8A
Switching Frequency	f_{SW}	300kHz
Operating Temperature	Topr	-40°Cto+85°C

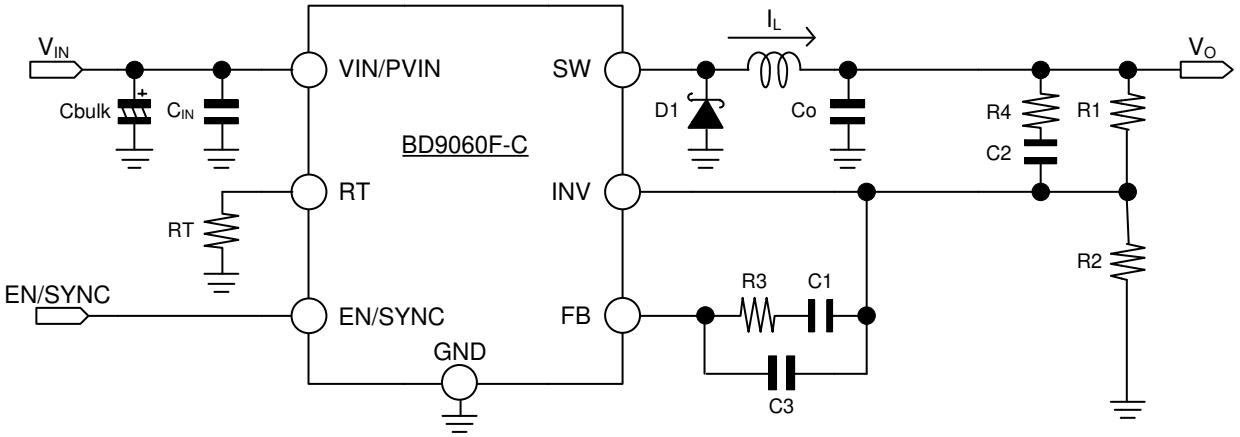
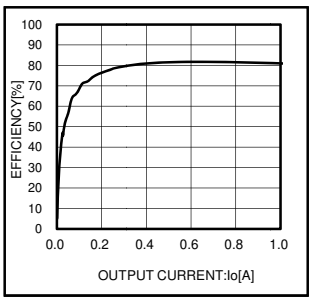
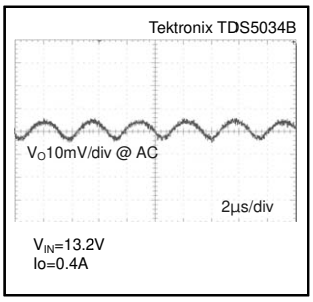


Figure 27. Application Examples 2

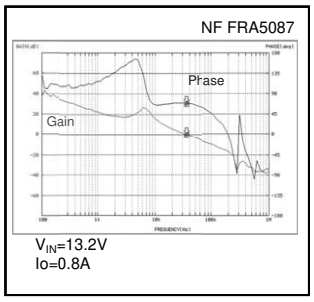
No	Package	Parameters	Part name(series)	Type	Manufacturer
R1	1005	47kΩ, 1%, 1/16W	MCR01 series	Chip resistors	ROHM
R2	1005	15kΩ, 1%, 1/16W	MCR01 series	Chip resistors	ROHM
R3	1005	8.2kΩ, 1%, 1/16W	MCR01 series	Chip resistors	ROHM
R4	1005	0kΩ, 1%, 1/16W	MCR01 series	Chip resistors	ROHM
RT	1005	51kΩ, 1%, 1/16W	MCR01 series	Chip resistors	ROHM
C1	1005	4700pF, R, 50V	GCM series	Ceramic capacitors	MURATA
C2	1005	820pF, CH, 50V	GCM series	Ceramic capacitors	MURATA
C3	1005	100pF, CH, 50V	GCM series	Ceramic capacitors	MURATA
C_{IN}	3216	2.2μF, X7R, 50V	GCM series	Ceramic capacitors	MURATA
C_O	3216	22μF, X7R, 16V	GCM series	Ceramic capacitors	MURATA
C_{bulk}		220μF, 50V	CD series	Electrolytic capacitors	NICHICON
L	10x10x3.8(mm^3)	33μH	CLF6045 series	Coil	TDK
D	PMDS	Average I = 2A Max	RB060L-40	Schottky Diodes	ROHM



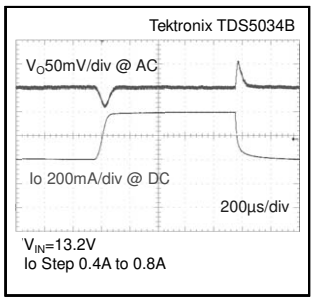
Conversion Efficiency



Output Ripple Voltage



Frequency Characteristics



Load Change

Input Filter

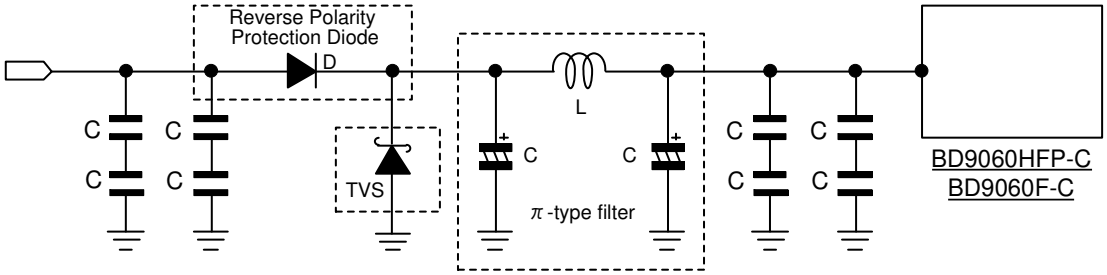


Figure 28. Frequency Characteristics

The input filter circuit for EMC measures is depicted in Figure 28.

The π type filters are the third LC filters. When the decoupling capacitor for high frequency is insufficient, it uses π type filters.
Because a large attenuation characteristic is obtained, an excellent characteristic can be obtained as an EMI filter.
TVS(TransientVoltageSuppressors) is used for the first protection of the in-vehicle power supply line.Because it is necessary to endure high energy that dumps the load, a general zener diode is insufficient. The following are recommended. To protect it when the power supply such as BATTERY is accidentally connected in reverse, reverse polarity protection diode is needed.

No	Part name (series)	Manufacturer
L	CLF series	TDK
	XAL series	Coilcraft
C	CJ series	NICHICON
	CZ series	NICHICON
TVS	SM8 series	VISHAY
D	S3A thru S3M series	VISHAY

Recommended Parts Manufacturer List

Show the parts manufacturer for the recommended reference.

Device	Type	Manufacturer	URL
C	Electrolytic capacitors	NICHICON	www.nichicon.com
C	Ceramic capacitors	MURATA	www.murata.com
L	Coils	TDK	www.global.tdk.com
L	Coils	Coilcraft	www.coilcraft.com
L	Coils	Sumida	www.sumida.com
D	Diodes	VISHAY	www.vishay.com
D	Diodes/Resistors	ROHM	www.rohm.com

Directions For Pattern Layout of PCB

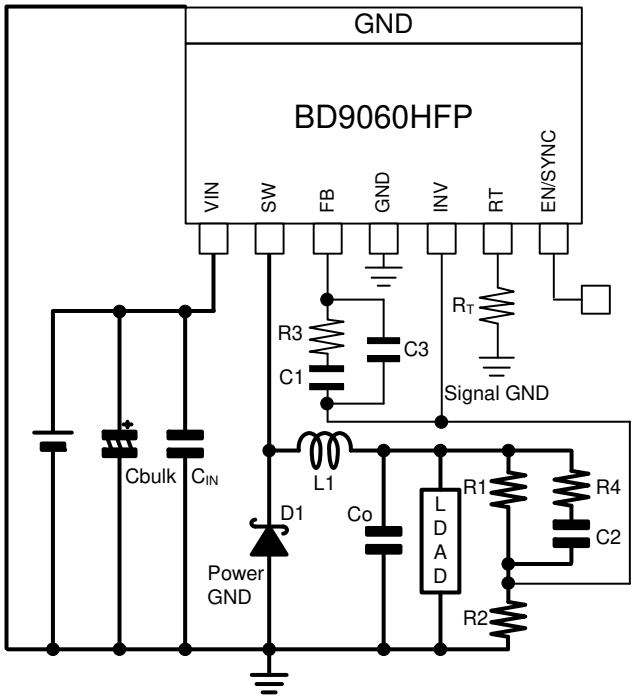


Figure 29. Filter Circuit Diagram
(BD9060HFP-C)

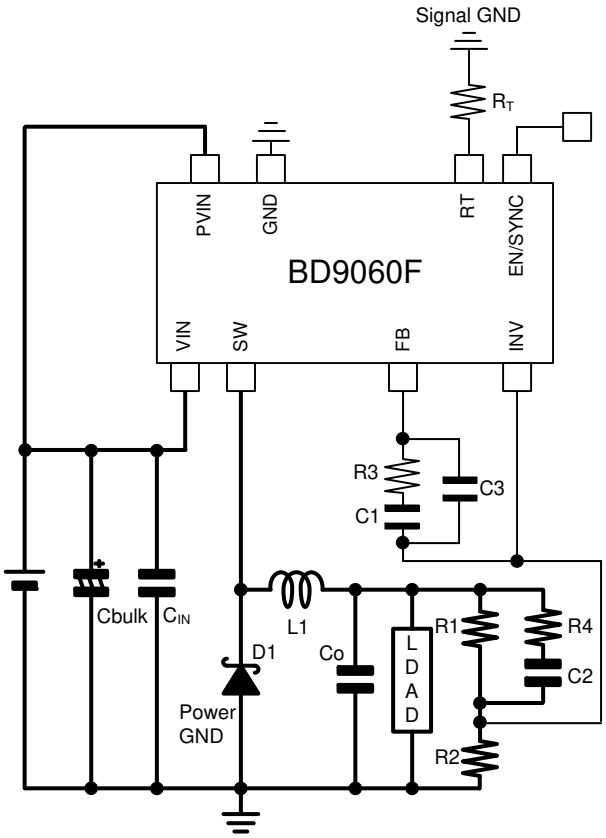


Figure 30. Application Circuit
(BD9060F-C)

1. Arrange the wirings shown by wide lines as short as possible in a broad pattern.
2. Locate the input ceramic capacitor C_{IN} as close to the VIN-GND pin as possible.
3. Locate the R_T as close to the GND pin as possible.
4. Locate the R1 and R2 as close to the INV pin as possible, and provide the shortest wiring from the R1 and R2 to the INV pin.
5. Locate the R1 and R2 as far away from the L1 as possible.
6. Separate Power GND (schottky diode, I/O capacitor`s GND) and Signal GND (R_T,GND), so that SW noise doesnot have an effect on SIGNAL GND at all.
7. Design the POWER wire line as wide and short as possible.

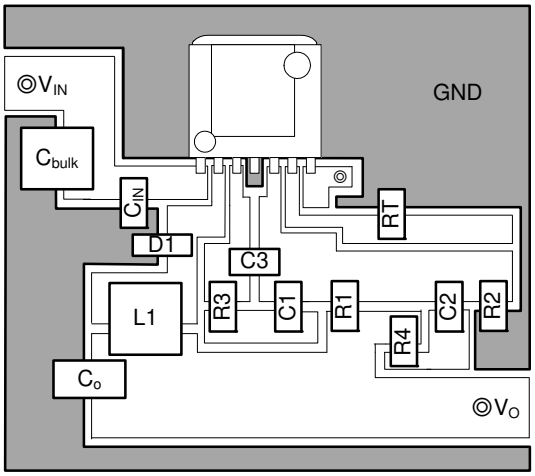


Figure 31. BD9060HFP-C Reference Layout Pattern

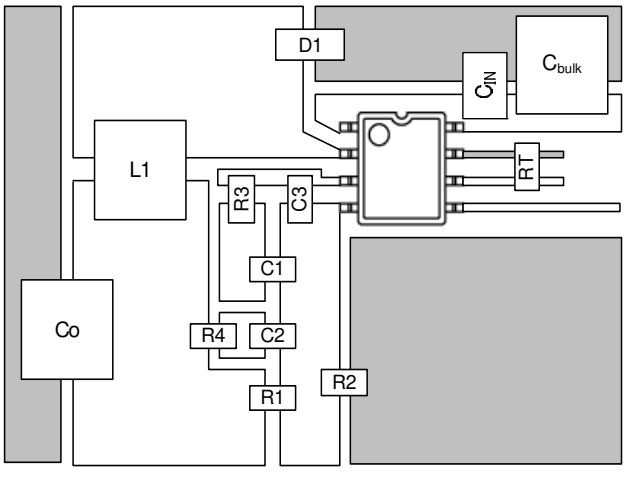


Figure 32. BD9060F-C Reference Layout Pattern

*Please make GND to cover the wide area with no parts.
*Gray areas mean GND in the above Layout Pattern.

Power Dissipation

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperature, take margin into account.)

1.The ambient temperature Ta is to be 125°C or less.
2.The chip junction temperature Tj is to be 150°C or less.

The chip junction temperature Tj can be considered in the following two patterns: °C

1. To obtain Tj from the IC surface temperatureTc in actual use

$$Tj = Tc + \theta jc \times W$$

＜Reference value＞ θjc : HRP7 7°C/W
θjc : SOP8 32.5°C/W

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta ja \times W$$

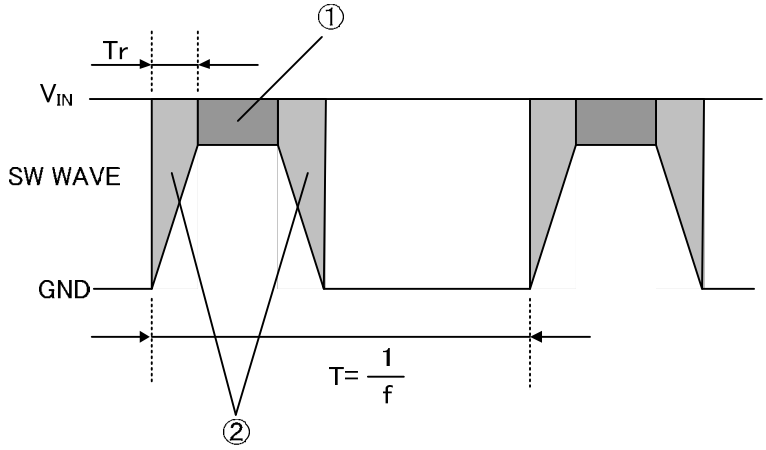
＜Reference value＞ θja : HRP7 125.0°C/W Single piece of IC
54.3°C/W 2-layer PCB (Copper foil area on the front side of PCB : 15mm×15mm)
22.7°C/W 2-layer PCB (Copper foil area on the front side of PCB : 70mm×70mm)
17.1°C/W 4-layer PCB (Copper foil area on the front side of PCB : 70mm×70mm)
PCB Size: 70mm×70mm×1.6mm (PCB incorporates thermal via)
Copper foil area on the front side of PCB: 10.5mm×10.5mm

θja : SOP8 222.2°C/W Single piece of IC
181.3°C/W 1-layer PCB(Copper foil area on the front side of PCB : 70mm×70mm)

The heat loss W of the IC can be obtained by the formula shown below:

$$W = Ron \times Io^2 \times \frac{Vo}{V_{IN}} + V_{IN} \times Icc + Tr \times V_{IN} \times Io \times f$$

Where:
$R_{ON}$is the ON resistance of IC (refer to page.8)
Io isthe Load current
$V_O$isthe Output Voltage
V_{IN}istheinput Voltage
I_{CC}isthe Circuit current(refer to page.5)
Tr isthe Switching rise/fall time (approximately 15n/35ns)
fis the Oscillating Frequency



$①Ron \times Io^2$

$②2 \times \frac{1}{2} \times Tr \times \frac{1}{T} \times V_{IN} \times Io$

$= Tr \times V_{IN} \times Io \times f$

Figure 33. SW waveform

I/O Equivalent Circuit

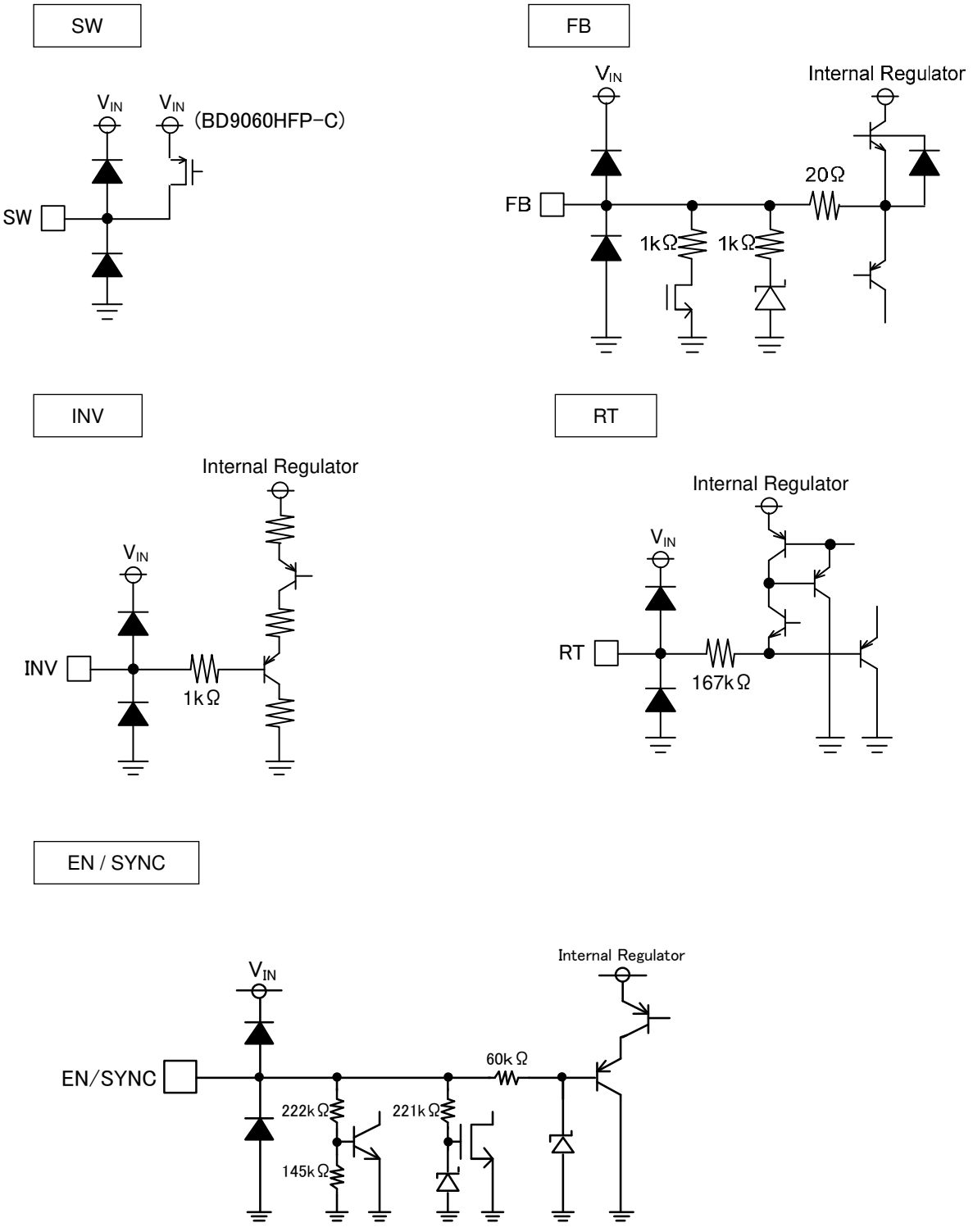


Figure 34. I/O Equivalent Circuit

Operational Notes

1. Reverse Connection of Power Supply
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity whenconnecting the power supply, such as mounting an external diode between the power supply and the IC's powersupply terminals.

2. Power Supply Lines
   Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supplylines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affectingthe analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect oftemperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage
   The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that nopins are at a voltage below the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern
   When using both small-signal and large-current GND traces, the two ground traces should be routed separately butconnected to a single ground at the reference point of the application board to avoid fluctuations in the small-signalground caused by large currents. Also ensure that the GND traces of external components do not cause variations onthe GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result indeterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is whenthe IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating,increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained.The electrical characteristics are guaranteed under the conditions of each parameter.

7. Rush Current
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrushcurrent may flow instantaneously due to the internal powering sequence and delays, especially if the IChas more than one power supply. Therefore, give special consideration to power coupling capacitance,power wiring, width of GND wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin maysubject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supplyshould always be turned off completely before connecting or removing it from the test setup during the inspectionprocess. To prevent damage from static discharge, ground the IC during assembly and use similar precautions duringtransport and storage.

10. Inter-pin Short and Mounting Errors
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridgedeposited in between pins during assembly to name a few.

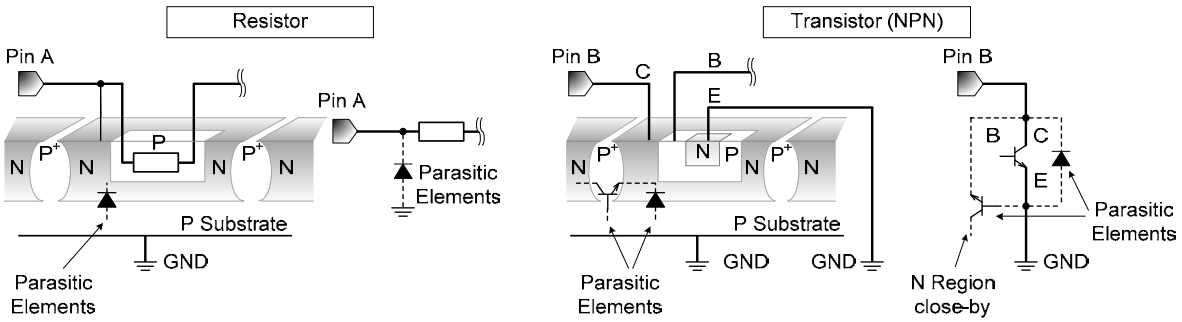
11. Unused Input Terminals
    Input terminals of an IC are often connected to the gate of a CMOS transistor. The gate has extremely high impedanceand extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The smallcharge acquired in this way is enough to produce a significant effect on the conduction through the transistor andcause unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connectedto the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep themisolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating aparasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutualinterference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes tooperate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should beavoided.



13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance withtemperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC incorporates and integrated thermal shutdown circuit to prevent heat damage to the IC. Normal operationshould be within the power dissipation rating, if however the rating is exceeded for a continued period, the junctiontemperature (Tj) will rise and the TSD circuit will be activated and turn all output pins OFF. After the Tj falls below theTSD threshold the circuits are automatically restored to normal operation.Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under nocircumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC fromheat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. Thisprotection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC shouldnot be used in applications characterized by continuous operation or transitioning of the protection circuit.