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Input Voltage 3.5 V to 36 V Output SW Current 4 A / 2.5A / 1.25A 1ch Step-Down Switching Regulator

BD906xx-C series

General Description

BD906xx-C series is a step-down switching regulator with integrated POWER MOS FET and have the capability to withstand high input voltage, providing a free setting function of operating switching frequency with external resistor. This switching regulator features a wide input voltage range (3.5 V to 36 V, Absolute maximum 42 V) and operating temperature range (-40 °C to +125 °C). Furthermore, an external synchronization input pin enables synchronous operation with external clock.

Features

- AEC-Q100 Qualified (Note 1)
- Integrated Pch POWER MOS FET
- Low Dropout: 100 % ON Duty Cycle
- External Synchronization Function
- Soft Start Function: 1.38 ms (f_{SW} = 500 kHz)
- Current Mode Control
- Over Current Protection
- Low Supply Voltage Error Prevention
- Thermal Shut Down Protection
- Short Circuit Protection
- High power HRP7 package mounted
- Compact and High power HTSOP-J8 package mounted
- Load dump up to 42 V.

(Note 1 : Grade 1)

Applications

- Automotive Battery Powered Supplies (Cluster Panels, Car Multimedia)
- Industrial / Consumer Supplies
- Other electronic equipment

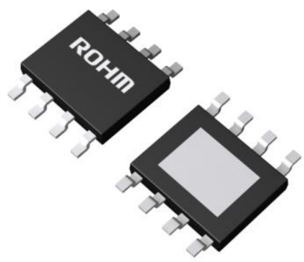
Key Specifications

- Input Voltage Range : 3.5 V to 36 V (Initial startup is over 3.9 V)
- Output Voltage Range : 0.8 V to V_{IN}
- Output Switch Current : 4 A / 2.5 A / 1.25 A (Max)
- Switching Frequency : 50 kHz to 600 kHz
- Reference Voltage Accuracy :±2% (-40 °C to +125 °C)
- Shutdown Circuit Current : 0 µA (Typ)
- Operating Temperature Range(Ta) : -40 °C to +125 °C

Package

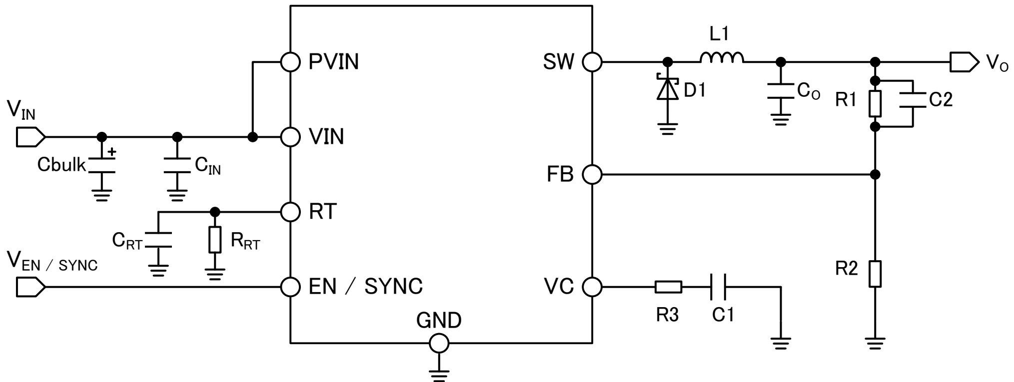
Package	W(Typ) x D(Typ) x H(Max)
HRP7	9.395mm x 10.540mm x 2.005mm
HTSOP-J8	4.90mm x 6.00mm x 1.00mm

HRP7



HTSOP-J8

Typical Application Circuit



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

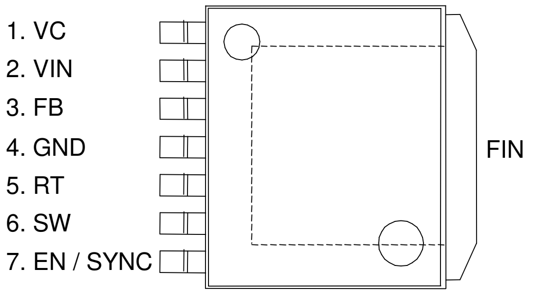
Lineup

Product Name	HRP7	BD90640HFP-C	BD90620HFP-C	-
	HTSOP-J8	BD90640EFJ-C	BD90620EFJ-C	BD90610EFJ-C
Output Switch Current		4 A	2.5 A	1.25 A
Input Maximum Ratings		42 V		
Input Voltage Range (Note 1)		3.5 V to 36 V		
POWER MOSFET ON Resistance		0.16 Ω (Typ)		
Power Dissipation	HRP7 (Note 2)	6.98 W		
	HTSOP-J8 (Note 3)	3.10 W		

(Note 1) Initial startup is over 3.9 V
(Note 2) Reduce by 55.8 mW / °C (Above 25°C),
(JESD51 -5 / -7 standard FR4 114.3 mm × 76.2 mm × 1.60 mmt 4-layer Top copper foil: ROHM recommended footprint + wiring to measure / 2,3 inner layers and Copper foil area on the reverse side of PCB 74.2 mm × 74.2 mm, copper (top & reverse side / inner layers) 70 μm / 35 μm. Thermal via : pitch 1.2 mm, diameter Φ0.30 mm)
(Note 3) Reduce by 24.8 mW / °C (Above 25°C),
(JESD51 -5 / -7 standard FR4 114.3 mm × 76.2 mm × 1.60 mmt 4-layer Top copper foil: ROHM recommended footprint + wiring to measure / 2,3 inner layers and Copper foil area on the reverse side of PCB 74.2 mm × 74.2 mm, copper (top & reverse side / inner layers) 70 μm / 35 μm. Thermal via : pitch 1.2 mm, diameter Φ0.30 mm)

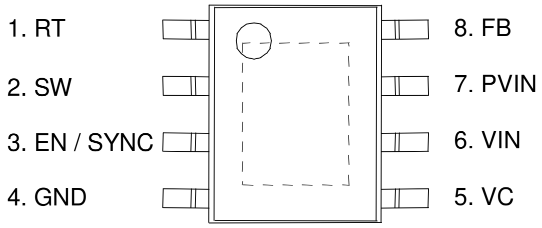
Pin Configuration

(TOP VIEW)



HRP7

(TOP VIEW)



HTSOP-J8

Pin Description

Pin No.	Symbol	Function
1	VC	Error Amp Output
2	VIN	Power Supply Input
3	FB	Output Voltage Feedback
4	GND	GND
5	RT	Switching Frequency Setting Resistor Connection
6	SW	Switching Output
7	EN / SYNC	Enable / External Clock Input
FIN	-	GND

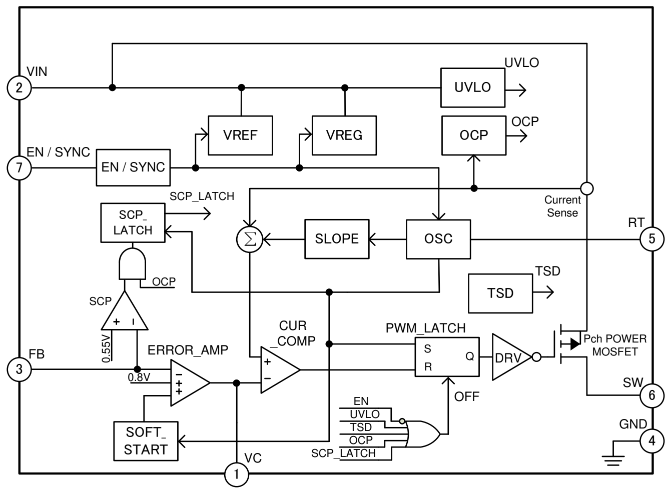
HRP7

Pin No	Symbol	Function
1	RT	Switching Frequency Setting Resistor Connection
2	SW	Switching Output
3	EN / SYNC	Enable / External Clock Input
4	GND	GND
5	VC	Error Amp Output
6	VIN (Note 1)	Power Supply Input
7	PVIN (Note 1)	Power Supply Input
8	FB	Output Voltage Feedback

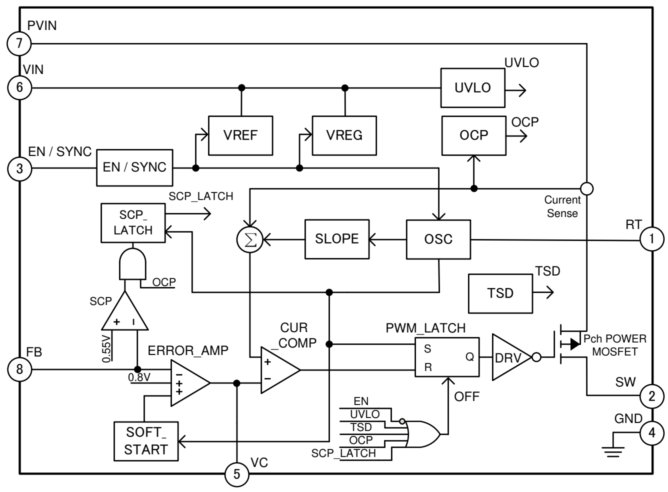
(Note 1) VIN and PVIN must be shorted.

HTSOP-J8

Block Diagram



HRP7



HTSOP-J8

Description of Blocks

1. ERROR_AMP
   The ERROR_AMP block is an error amplifier and its inputs are the reference voltage 0.8 V (Typ) and the “FB” pin voltage. (Refer to recommended examples on p.16 to 17). The output “VC” pin controls the switching duty, the output voltage is set by “FB” pin with external resistors. Moreover, the external resistor and capacitor are required to COMP pin as phase compensation circuit (Refer to phase compensation selection method on p.17 to 18).

2. SOFT_START
   The function of the SOFT_START block is to prevent the overshoot of the output voltage V_O through gradually increasing the input of the error amplifier when the power supply turns ON, which also results to the gradual increase of the witching duty. The soft start time is set to 1.38 ms (Typ , f_{SW} = 500 kHz).
   The soft start time is changed by setting of the switching frequency. (Refer to p.18)

3. EN / SYNC
   The IC is in normal operation when the voltage on the “EN / SYNC” pin is more than 2.6 V. The IC is shut down when the voltage on the “EN / SYNC” pin is less than 0.8 V. Furthermore, external synchronization is possible when external clock are applied to the “EN / SYNC” pin. The switching frequency range of the external synchronization is within ±20 % of the switching frequency and is limited by the external resistance connected to the RT pin.
   ex) When R_{RT} is 27 kΩ (f = 500 kHz), the switching frequency range of the external synchronization is 400 kHz to 600 kHz.

4. OSC (Oscillator)
   This circuit generates the clock pulses that are input to SLOPE block. The switching frequency is determined by the current going through the external resistor RT at constant voltage of ca. 0.8V. The switching frequency can be set in the range between 50 kHz to 600 kHz (Refer to p.16 Figure 13). The output of the OSC block send clock signals to PWM_LATCH. Moreover the generated pulses of the OSC block are also used as clock of the counter of SS and SCP_LATCH blocks.

5. SLOPE
   This block generates saw tooth waves using the clock generated by the OSC block. The generated saw tooth waves are combined with the current sense and sent to the CUR_COMP.

6. CUR_COMP (Current Comparator)
   The CUR_COMP block compares the signals between the ERROR_AMP and the combined signals from the SLOPE block and current sense. The output signals are sent to the PWM_LATCH block.

7. PWM_LATCH
   The PWM_LATCH block is a LATCH circuit. The OSC block output (set) and CUR_COMP block output (reset) are the inputs of this block. The PWM_LATCH block outputs PWM signals.

8. TSD (Thermal Shut down)
   The TSD block prevents thermal destruction / thermal runaway of the IC by turning OFF the Pch POWER MOSFET output when the temperature of the chip reaches more than about 175 °C (Typ). When the chip temperature falls to a specified level, the switching will resume. However, since the TSD is designed to protect the IC, the chip temperature should be provided with the thermal shutdown detection temperature of less than approximately Tjmax = 150 °C.

9. OCP (Over Current Protection)
   OCP is activated when the voltage between the drain and source (on-resistance × load current) of the Pch POWER MOSFET when it is ON, exceeds the reference voltage which is internally set within the IC. This OCP is a self-return type. When OCP is activated, the ON duty will be small, and the output voltage will decrease. However, this protection circuit is only effective in preventing destruction from sudden accident. It does not support the continuous operation of the protection circuit (e.g. if a load, which significantly exceeds the output current capacitance, is connected).

10. SCP (Short Circuit Protection) and SCP-LATCH
    While OCP is activated, and if the output voltage falls below 70 %, SCP will be activated. When SCP is active, the output will be turned OFF after a period of 1024 pulse. It extends the time that the output is OFF to reduce the average output current. In addition, during startup of the IC, this feature is masked until it reaches a certain output voltage to prevent the startup failure.

11. UVLO (Under Voltage Lock-Out)
    UVLO is a protection circuit that prevents low voltage malfunction. It prevents malfunction of the internal circuit from sudden rise and fall of power supply voltage. It monitors the V_{IN} power supply voltage and the internal regulator voltage. If V_{IN} is less than the threshold voltage 3.24 V (Typ), the Pch POWER MOSFET output is OFF and the soft-start circuit will be restarted. This threshold voltage and release voltage have a hysteresis of 280 mV (Typ).

12. DRV (Driver)
    This circuit drives the gate electrode of the Pch POWER MOSFET output. It reduces the increase of the Pch POWER MOSFET’s on-resistance by switching the driving voltage when the power supply voltage drop.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter		Symbol	Rating	Unit
Input Power Supply Voltage		V_{IN}, PV_{IN}	-0.3 to +42	V
EN / SYNC Pin Voltage		$V_{EN / SYNC}$	-0.3 to V_{IN}	V
RT, VC, FB Pin Voltage		V_{RT}, V_{VC}, V_{FB}	-0.3 to +7	V
Power Dissipation(Note1)	HRP7 (Note2)	Pd	6.98	W
	HTSOP-J8 (Note3)		3.10	
Storage Temperature Range		Tstg	-55 to +150	°C
Maximum Junction Temperature		Tjmax	150	°C

(Note 1) Do not however exceed Pd.
(Note 2) Reduce by 55.8 mW / °C, **(Above 25°C),**
(JESD51 -5 / -7 standard FR4 114.3 mm × 76.2 mm × 1.60 mmt 4-layer Top copper foil: ROHM recommended footprint + wiring to measure / 2,3 inner layers and Copper foil area on the reverse side of PCB 74.2 mm × 74.2 mm, copper (top & reverse side / inner layers) 70 µm / 35 µm. Thermal via : pitch 1.2 mm, diameter Φ0.30 mm)
(Note 3) Reduce by 24.8 mW / °C, **(Above 25°C),**
(JESD51 -5 / -7 standard FR4 114.3 mm × 76.2 mm × 1.60 mmt 4-layer Top copper foil: ROHM recommended footprint + wiring to measure / 2,3 inner layers and Copper foil area on the reverse side of PCB 74.2 mm × 74.2 mm, copper (top & reverse side / inner layers) 70 µm / 35 µm. Thermal via : pitch 1.2 mm, diameter Φ0.30 mm)
Caution**:** Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters can result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

Recommended Operating Conditions

Parameter		Symbol	Limit		Unit
			Min	Max	
Operating Power Supply Voltage (Note 1)		V_{IN}, PV_{IN}	3.5	36	V
Operating Temperature Range		Topr	-40	+125	°C
Output Switch Current (Note2)	BD90640HFP/EFJ-C	I_{SW40}	-	4	A
	BD90620HFP/EFJ-C	I_{SW20}	-	2.5	A
	BD90610EFJ-C	I_{SW10}	-	1.25	A
Output Voltage		V_O	0.8	V_{IN}	V
Min ON Pulse Width		T_{ON_MIN}	250	-	ns
Switching Frequency		f_{SW}	50	600	kHz
Switching Frequency Set Resistance		R_{RT}	22	330	kΩ
Synchronous Operation Frequency Range		f_{SYNC}	50	600	kHz
Synchronous Operation Frequency		f_{SYNC_RT}	-20	+20	%
External Clock ON Duty		D_{SYNC}	10	90	%
Capacitance of Input Capacitor		C_{IN}	2.4(Note 3)	-	µF

(Note 1) Initial startup is over 3.9 V.
(Note 2) The Limits include output DC current and output ripple current.
(Note 3) Ceramic capacitor is recommended. The capacitor value including temperature change, DC bias change, and aging change must be larger than minimum value (Refer to p.15). Also, the IC might not function properly when the PCB layout or the position of the capacitor is not good. Please check “Notes on the PCB Layout” on page 30.

Electrical Characteristics (Unless otherwise specified, Ta = - 40 °C to +125 °C, V_{IN} = 13.2 V, $V_{EN / SYNC}$ = 5 V)

Parameter		Symbol	Limit Min	Limit Typ	Limit Max	Unit	Conditions
Whole chip							
Shutdown Circuit Current		I_{SDN}	-	0	5	μA	$V_{EN / SYNC}$ = 0 V, Ta < 105 °C
Circuit Current		I_{IN}	-	2.2	3.3	mA	Io = 0 A, V_{FB} = 2 V
SW Block							
POWER MOSFET ON Resistance		R_{ON}	-	0.16	0.32	Ω	I_{SW} = 30 mA
Operating Output Switch Current Of Overcurrent Protection (Note 1)	BD90640HFP / EFJ-C	$I_{SWLIMIT40}$	4.0	6.4	-	A	
	BD90620HFP / EFJ-C	$I_{SWLIMIT20}$	2.5	4.3	-	A	
	BD90610EFJ-C	$I_{SWLIMIT10}$	1.25	2.20	-	A	
Output Leak Current		I_{OLK}	-	0	5	μA	V_{IN} = 36 V, $V_{EN / SYNC}$ = 0 V, Ta < 105 °C
Error Amp Block							
Reference Voltage 1		V_{REF1}	0.792	0.800	0.808	V	V_{VC} = V_{FB}, Ta = 25 °C
Reference Voltage 2		V_{REF2}	0.784	0.800	0.816	V	V_{VC} = V_{FB}
Reference Voltage Input Regulation		ΔV_{REF}	-	0.5	-	%	3.5 V ≤ V_{IN} ≤ 36 V
Input Bias Current		I_B	-1.0	-	+1.0	μA	
VC Sink Current		I_{VCSINK}	-76.5	-54.0	-31.5	μA	V_{VC} = 1.25 V, V_{FB} = 1.3 V
VC Source Current		$I_{VCSOURCE}$	31.5	54.0	76.5	μA	V_{VC} = 1.25 V, V_{FB} = 0.3 V
Trans Conductance		G_{EA}	135	270	540	μA / V	I_{VC} = ±10 μA, V_{VC} = 1.25 V
Soft Start Time		T_{SS}	1.13	1.38	1.63	ms	R_{RT} = 27 kΩ
Current Sense Part							
Trans Conductance		G_{CS}	-	5.2	-	A / V	
OSC Block							
Switching Frequency		f_{SW}	450	500	550	kHz	R_{RT} = 27 kΩ
Frequency Input Regulation		Δf_{SW}	-	1	-	%	3.5 V ≤ V_{IN} ≤ 36 V
Enable / Sync Input Block							
Threshold Voltage		$V_{EN / SYNC}$	0.8	1.9	2.6	V	
SYNC Current		$I_{EN / SYNC}$	-	23	50	μA	$V_{EN / SYNC}$ = 5 V
UVLO							
UVLO ON Mode Voltage		V_{UVLO_ON}	-	3.24	3.50	V	
UVLO OFF Mode Voltage		V_{UVLO_OFF}	-	3.52	3.90	V	
UVLO Hysteresis		V_{UVLO_HYS}	-	280	-	mV	

(Note 1) The Limit include output DC current and output ripple current.

Typical Performance Curves

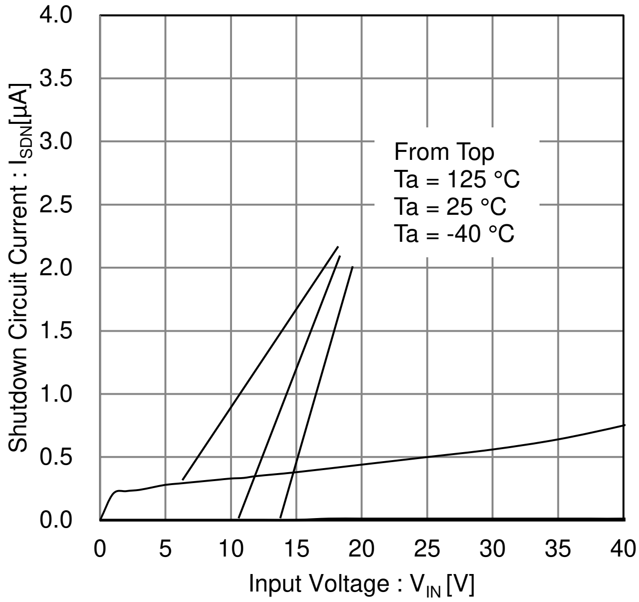


Figure 1. Shutdown Circuit Current vs Input Voltage

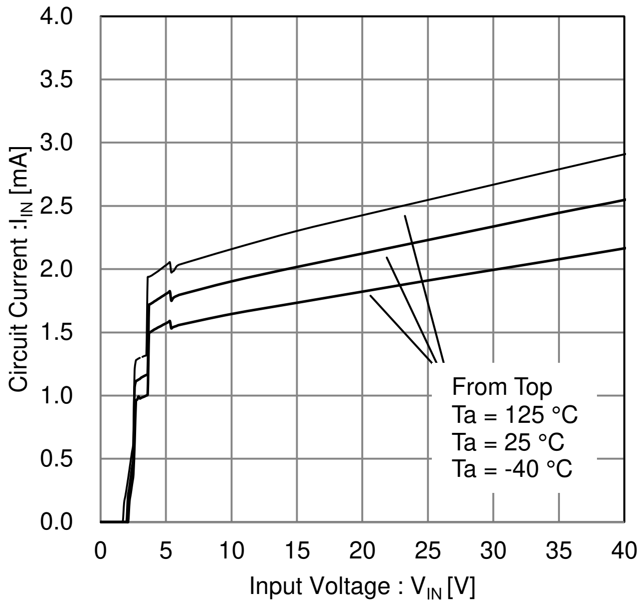


Figure 2. Circuit Current vs Input Voltage

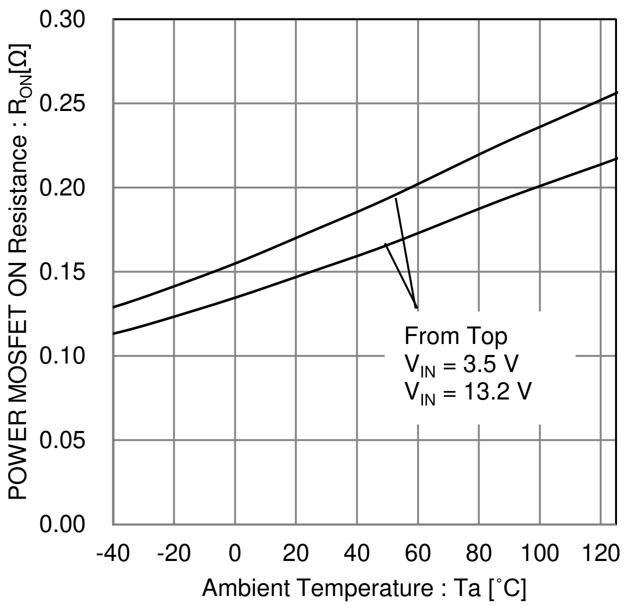


Figure 3. POWER MOSFET ON Resistance vs Ambient Temperature

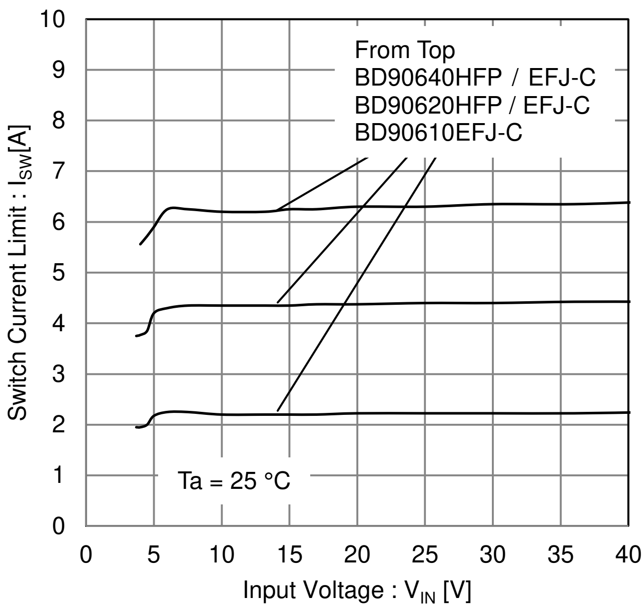


Figure 4. Switch Current Limit vs Input Voltage

Typical Performance Curves – continued

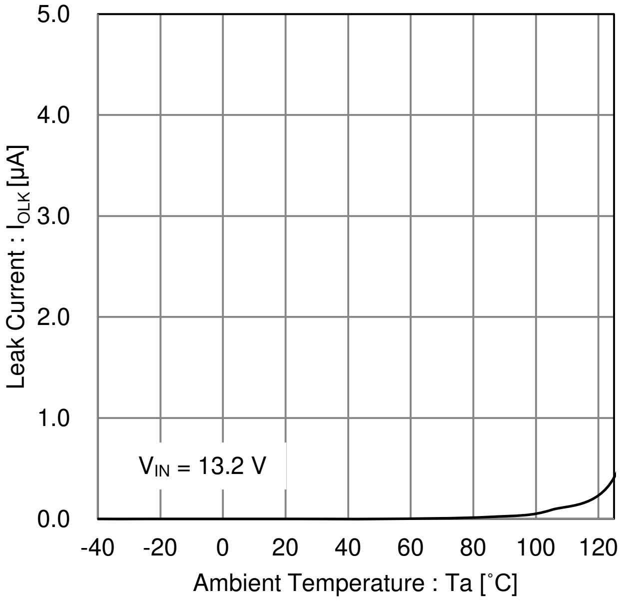


Figure 5. Leak Current vs Ambient Temperature

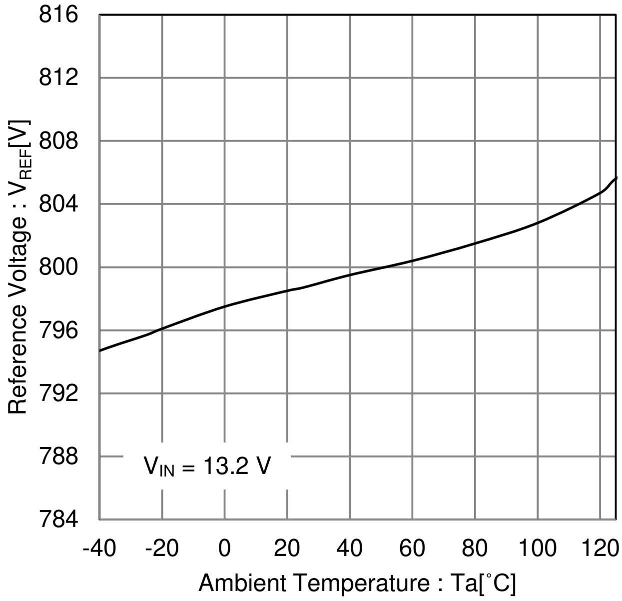


Figure 6. Reference Voltage vs Ambient Temperature

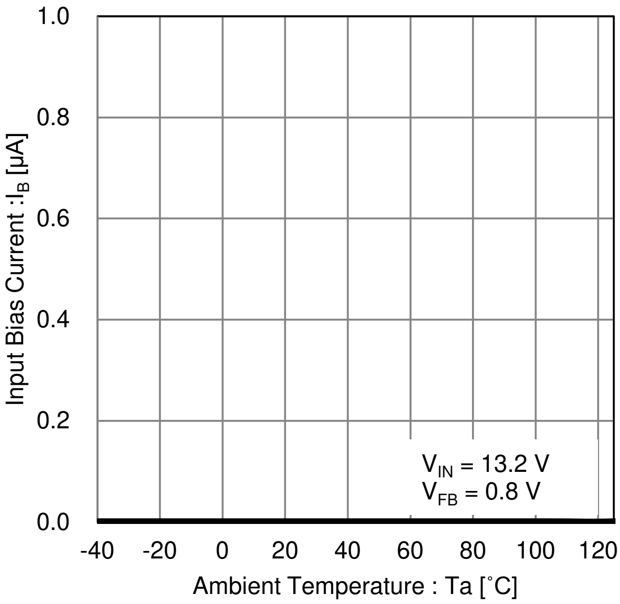


Figure 7. Input Bias Current vs Ambient Temperature

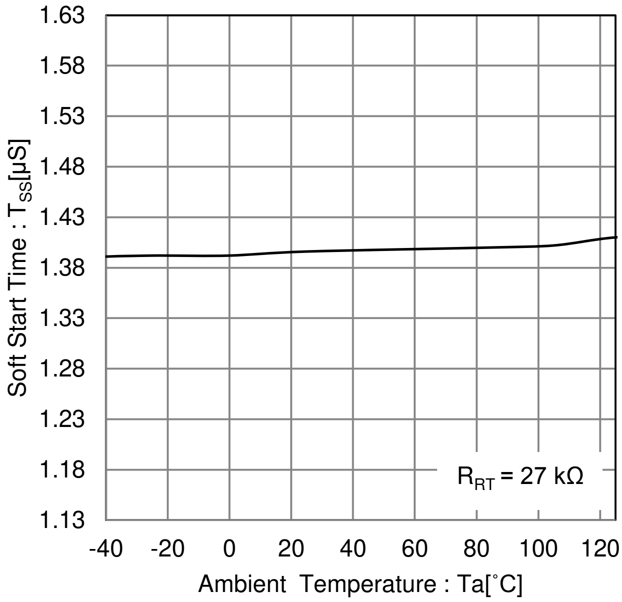


Figure 8. Soft Start Time vs Ambient Temperature

Typical Performance Curves – continued

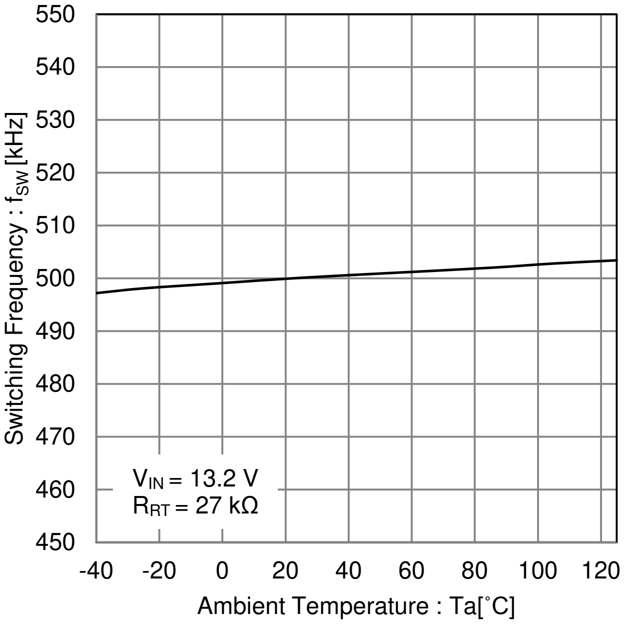


Figure 9. Switching Frequency vs Ambient Temperature

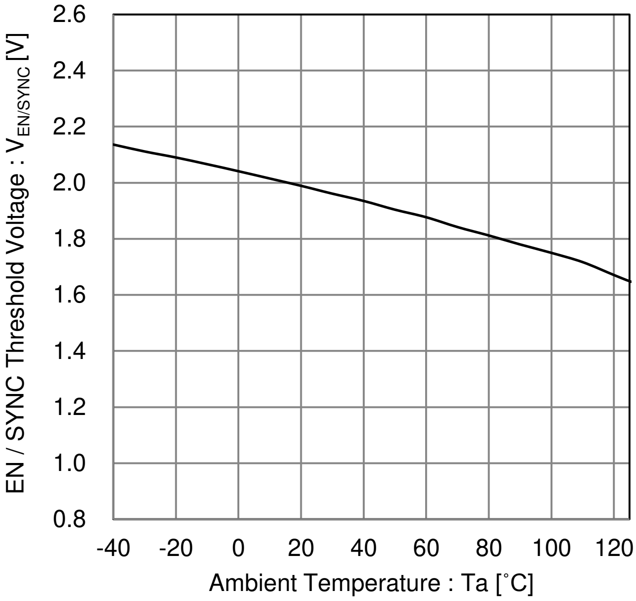


Figure 10. EN / SYNC Threshold Voltage vs Ambient Temperature

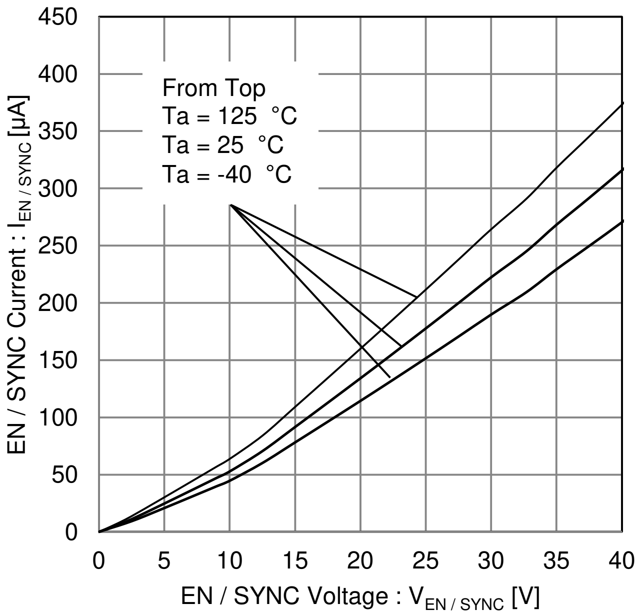


Figure 11. EN / SYNC Current vs EN / SYNC Voltage

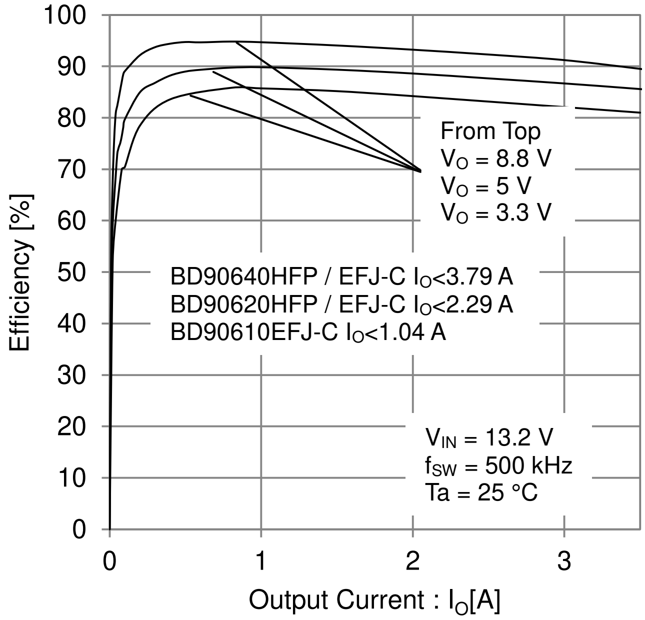
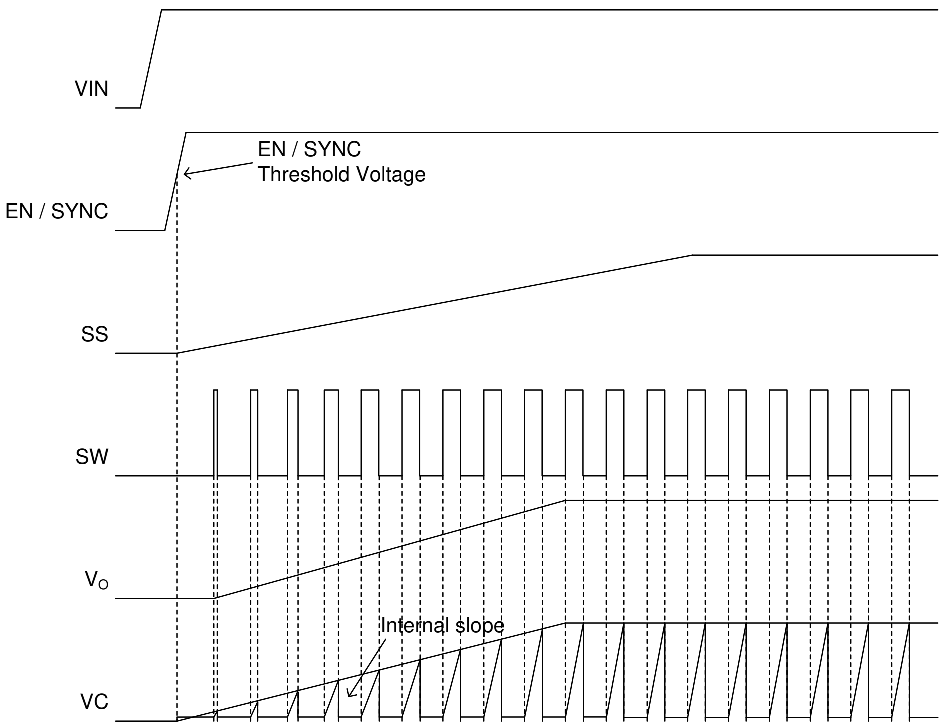


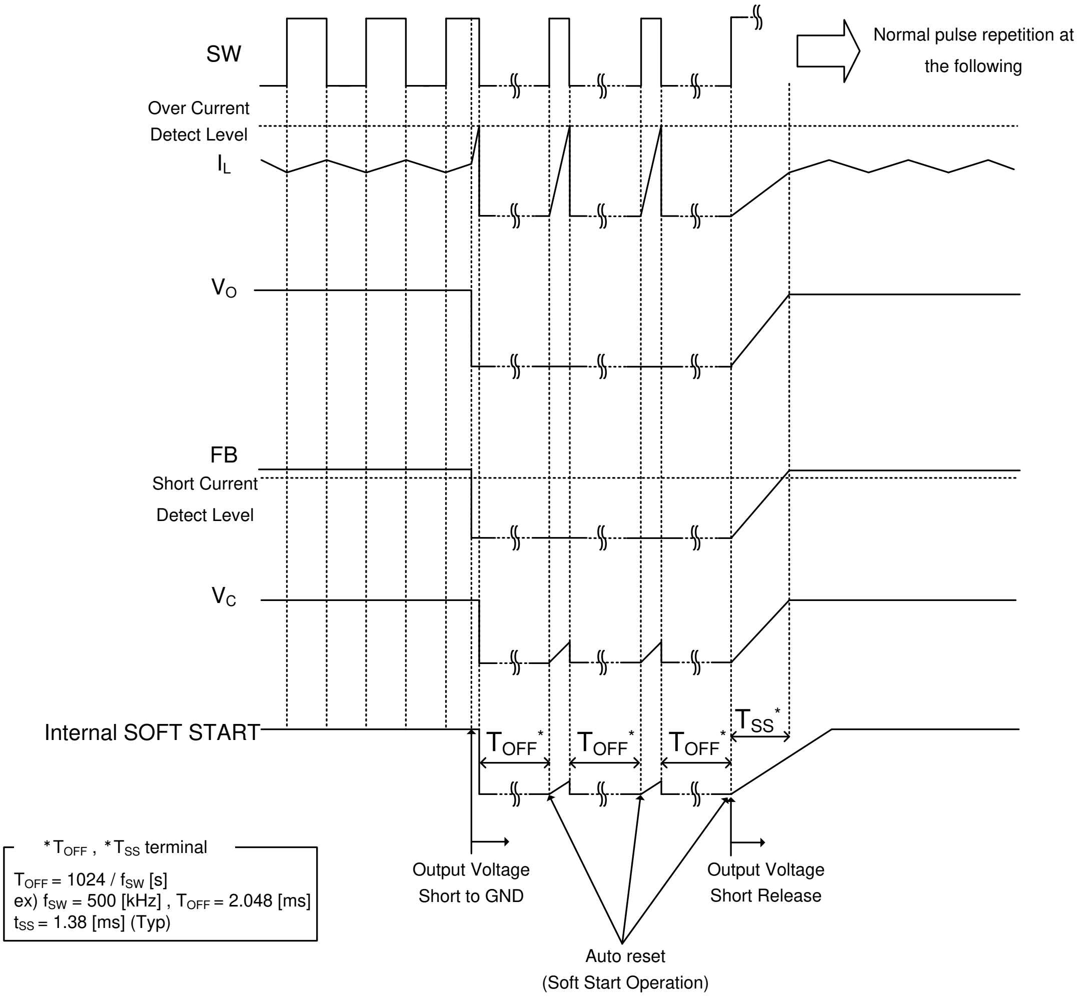
Figure 12. Efficiency vs Output Current

Timing Chart

1. Start Up Operation



2. Over Current Protection Operation



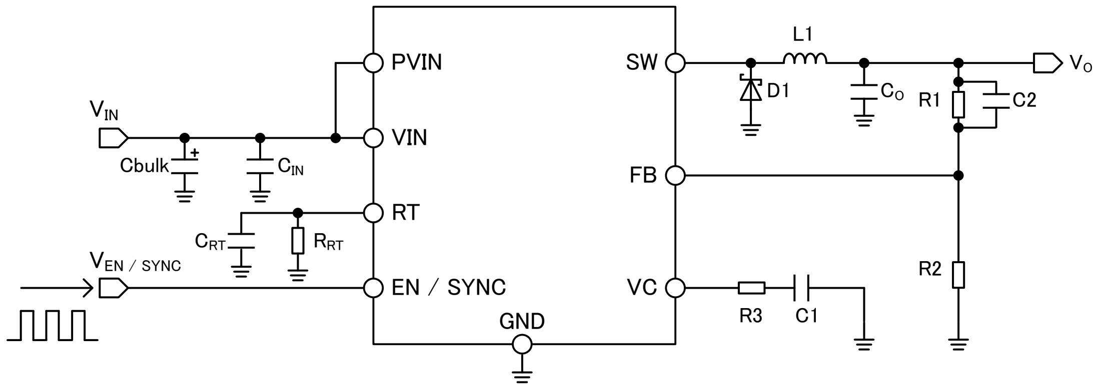
External Synchronization Function

In order to activate the external synchronization function, connect the frequency-setting resistor to the RT pin and then input a synchronizing signal to the EN / SYNC pin.
The external synchronization operation frequency is limited by the external resistance of R_{RT} pin. The allowable setting limit is within ±20 % of the switching frequency.

ex) When R_{RT} is 27 kΩ (f = 500 kHz), the frequency range of the external synchronization is 400 kHz to 600 kHz.

Furthermore, the pulse wave's LOW voltage should be under 0.8 V and the HIGH voltage over 2.6 V (when the HIGH voltage is over 11 V the EN / SYNC input current increases), and the slew rate (rise and fall) under 20 V / µS. The ON Duty of External clock should be configured between 10 % and 90 %.

The frequency will synchronize with the external clock operation frequency after three external sync pulses is sensed.

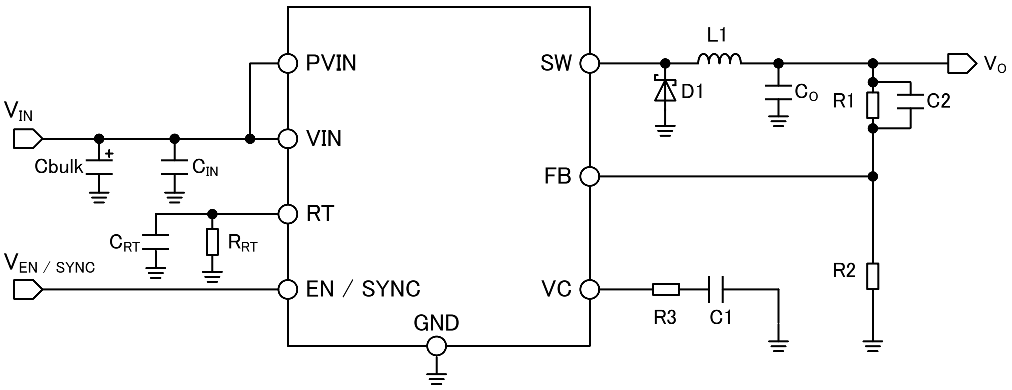


Eternal SYNC Sample Circuit

Selection of Components Externally Connected

Necessary parameters in designing the power supply are as follows:

Parameter	Symbol	Specification Case
Input Voltage	V_{IN}	6 V to 18 V
Output Voltage	V_O	5 V
Output Ripple Voltage	ΔV_{PP}	20 mVp-p
Input Range	I_O	Min 1.0 A / Typ 1.5 A / Max 2.0 A
Switching Frequency	f_{SW}	500 kHz
Operating Temperature Range	Topr	-40 °C to +105 °C



Application Sample Circuit

1. Selection of the inductor L1 value

When the switching regulator supplies current continuously to the load, the LC filter is necessary for the smoothness of the output voltage. The Inductor ripple current ΔI_L that flows to the inductor becomes small when an inductor with a large inductance value is selected. Consequently, the voltage of the output ripple also becomes small. It is the trade-off between the size and the cost of the inductor.

The inductance value of the inductor is shown in the following equation:

$$L = \frac{(V_{IN(Max)} - Vo) \times Vo}{V_{IN(Max)} \times f_{SW} \times \Delta I_L} \text{ [H]}$$

Where:

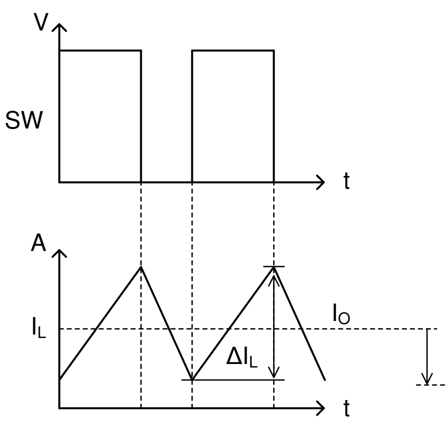
$V_{IN\,(Max)}$ is the maximum input voltage

ΔI_L is set to approximately 30 % of I_O. To avoid discontinuous operation, ΔI_L shall be set to make SW continuously pulsing (I_L keeps continuously flowing). The condition of the continuous operation is shown in the following equation:

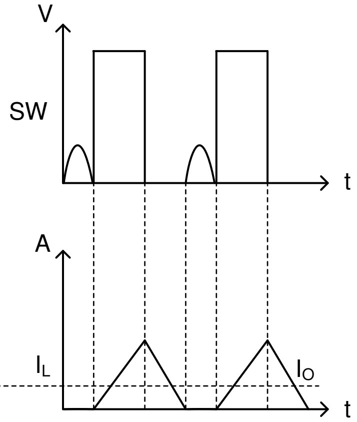
$$I_O > \frac{(V_{IN(Max)} - V_O) \times V_O}{2 \times V_{IN(Max)} \times f_{SW} \times L} \text{ [A]}$$

Where:

I_O is the Load Current



Continuous Operation



Discontinuous Operation

Selection of Components Externally Connected – continued

The smaller the ΔI_L, each the Inductor core loss (iron loss), the loss due to ESR of the output capacitor, and the ΔV_{PP} will be reduced. ΔV_{PP} is shown in the following equation.

$$\Delta V_{PP} = \Delta I_L \times ESR + \frac{\Delta I_L}{8 \times C_O \times f_{SW}} \quad [V] \quad \cdot\cdot\cdot\cdot\cdot \text{(a)}$$

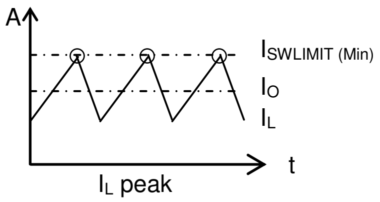
Where:
ESR is the equivalent series resistance of output capacitor
C_O is the output condenser capacity

Generally, even if ΔI_L is somewhat large, ΔV_{PP} of the target is satisfied because the ceramic capacitor has super-low ESR. In that case, it is also possible to use it by the discontinuous operation. The inductance value can be set small as an advantage.
It contributes to the miniaturization of the application because of the lower rated current, smaller inductor is possible if the inductance value is small. The disadvantages are the increase in core losses in the inductor, the decrease in maximum output current, and the deterioration of the response. When other capacitors (electrolytic capacitor, tantalum capacitor, and electro conductive polymer etc.) are used for output capacitor C_O, check the ESR from the manufacturer's data sheet and determine the ΔI_L to fit within the acceptable range of ΔV_{PP}. Especially in the case of electrolytic capacitor, because the capacity decrease at the low temperature is remarkable, ΔV_{PP} increases. When using capacitor at the low temperature, it is necessary to note this.

The maximum output electric current is limited to the overcurrent protection working current as shown in the following equation.

$$I_{O(Max)} = I_{SWLIMIT(Min)} - \frac{\Delta I_L}{2} \quad [A]$$

Where:
$I_{O(Max)}$ is the maximum output current
$I_{SWLIMIT(Min)}$ is the OCP operation current (Min)



In current mode control, when the IC is operating in ON Duty ≥ 50 % and in the condition of continuous operation,The sub-harmonic oscillation may happen. The slope compensation circuit is integrated into the IC in order to prevent sub-harmonic oscillation. The sub-harmonic oscillation depends on the rate of increase of output switch current. If the inductor value is too small, the sub-harmonic oscillation may happen. And if the inductor value is too large, the feedback loop may not achieve stability. The inductor value which prevents sub-harmonic oscillation is shown in the following equation.

$$L \geq \frac{2D-1}{2(1-D)} \times Rs \times \frac{V_{IN\ (Min)} - V_O}{m} \quad [H]$$

$$D = \frac{V_O}{V_{IN(Min)}}$$

$$m = 6 \times f_{SW} \times 10^{-6}$$

Where:
D is the switching pulse ON Duty.
R_S is the coefficient of current sense(4.0 µA / A)
m is the slope of slope compensation current

The shielded type (closed magnetic circuit type) is the recommended type of inductor. Open magnetic circuit type can be used for low cost applications if noise issues are not concerned. But in this case, an influence other parts by magnetic field radiation is considered. An enough space layout between each parts should be noted.

For ferrite core inductor type, please note that magnetic saturation may occur. It is necessary not to saturate the core in all cases. Precautions must be taken into account on the given provisions of the current rating because it differs according to each manufacturer.
Please confirm the rated current at the maximum ambient temperature of the application to the manufacturer.

Selection of Components Externally Connected – continued

2. Selection of output Capacitor C_O

The output capacitor is selected on the basis of ESR that is required from the equation (a). ΔV_{PP} can be reduced by using a capacitor with a small ESR. The ceramic capacitor is the best option that meets this requirement. The ceramic capacitor contributes to the size reduction of the application because it has small ESR. Please confirm frequency characteristic of ESR from the datasheet of the manufacturer, and consider ESR value is low in the switching frequency being used. It is necessary to consider the ceramic capacitor because the DC biasing characteristic is remarkable. For the voltage rating of the ceramic capacitor, twice or more than the maximum output voltage is usually required. By selecting these high voltages rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristic of X7R or more is recommended. Because the voltage rating of a mass ceramic capacitor is low, the selection becomes difficult in the application with high output voltage. In that case, please select electrolytic capacitor. Please consider having a voltage rating of 1.2 times or more of the output voltage when using electrolytic capacitor. Electrolytic capacitors have a high voltage rating, large capacity, small amount of DC biasing characteristic, and are generally cheap. Because main failure mode is OPEN, it is effective to use electrolytic capacitor for applications when reliability is required such as in-vehicle. But there are disadvantages such as, ESR is relatively high, and decreases capacitance value at low temperatures. In this case, please take note that ΔV_{PP} may increase at low temperature conditions. Moreover, consider the lifetime characteristic of this capacitor because there is a possibility for it to dry up.
A tantalum capacitor and a conductive polymer hybrid capacitor have excellent temperature characteristic unlike an electrolytic capacitor. Moreover, as these ESR is smaller than an electrolytic capacitor, a ripple voltage is relatively-small over wide temperature range. The design is facilitated because there is little DC bias characteristic like an electrolytic capacitor. Normally, for voltage rating, a tantalum capacitor is selected twice the output voltage, and for conductive polymer hybrid capacitor is selected 1.2 times more than the output voltage. The disadvantage of a tantalum capacitor is that the failure mode is SHORT, and the breakdown voltage is low. It is not generally selected in the application that reliability such as in automotive is demanded. The failure mode of an electro conductive polymer hybrid capacitor is OPEN. Though it is effective for reliability, the disadvantage is generally expensive.
In case of Pch step-down switching regulator, when the input voltage decreases and the voltage between input and output becomes small, switching pulse begin to skip before the Pch MOSFET completely turns on. Because of this the output ripple voltage may increase. To improve performance in this condition, following is recommended:

1. To use low ESR capacitor like ceramic or conductive polymer hybrid capacitor.
2. Higher value of capacitance.

These capacitors are rated in ripple current. The RMS values of the ripple current that can be obtained in the following equation must not exceed the ratings ripple current.

$$I_{CO(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \quad \text{[A]}$$

Where:
$I_{CO(RMS)}$ is the value of the ripple electric current

In addition, total value of capacitance with output line $C_{o(Max)}$, respect to C_O, choose capacitance value less than the value obtained by the following equation.

$$C_{O(Max)} = \frac{T_{SS(Min)} \times (I_{OLIMIT(Min)} - I_{OSTART(Max)})}{V_O} \quad \text{[F]}$$

Where:
$I_{SWLIMIT(Min)}$ is the OCP operation switch current (Min)
$T_{SS(Min)}$ is the Soft Start Time (Min)
$I_{SWSTART(Max)}$ is the maximum output current during startup

The startup failure may happen when the limits from the above-mentioned are exceeded. Especially if the capacitance value is extremely large, over-current protection may be activated by the inrush current at startup, and the output does not start. Please confirm this on the actual application. For stable transient response, the loop is dependent on the C_O. Please select after confirming the setting of the phase compensation circuit.
Also, in case of large changing input voltage and load current, select the capacitance in accordance with verifying that the actual application meets with the required specification.

Selection of Components Externally Connected – continued

3. Selection of capacitor C_{IN} / Cbulk input

The input capacitor is usually required for two types of decoupling: capacitors C_{IN} and bulk capacitors Cbulk. Ceramic capacitors with values more than 2.4 µF are necessary for the decoupling capacitor. Ceramic capacitors are effective by being placed as close as possible to the VIN pin. Voltage rating is recommended to more than 1.2 times the maximum input voltage, or twice the normal input voltage. The capacitor value including temperature change, DC bias change, and aging change must be larger than minimum value. Also, the IC might not function properly when the PCB layout or the position of the capacitor is not good. Please check “Notes on the PCB Layout” on page 24.

The bulk capacitor is option. The bulk capacitor prevents the decrease in the line voltage and serves a backup power supply to keep the input potential constant. The low ESR electrolytic capacitor with large capacity is suitable for the bulk capacitor. It is necessary to select the best capacitance value as per set of application. n that case, please consider not to exceed the rated ripple current of the capacitor.

The RMS value of the input ripple electric current is obtained in the following equation.

$$I_{CIN(RMS)} = I_{O(MAX)} \cdot \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \quad \text{[A]}$$

Where:

$I_{CIN(RMS)}$ is the RMS value of the input ripple electric current

In addition, in automotive and other applications requiring high reliability, it is recommended that capacitors are connected in parallel to accommodate a multiple of electrolytic capacitors to minimize the chances of drying up. It is recommended by making it into two series + two parallel structures to decrease the risk of ceramic capacitor destruction due to short circuit conditions. The line has been improved to the summary respectively by 1pack in each capacitor manufacturer and confirms two series and two parallel structures to each manufacturer.

When impedance on the input side is high because of wiring from the power supply to VIN is long, etc., and then high capacitance is needed. In actual conditions, it is necessary to verify that there is no problem when IC operation turns off or overshoot the output due to the change in V_{IN} at transient response.

4. Selection of output voltage setting registance R1, R2

Output voltage is governed by the following equation.

$$V_O = 0.8 \times \frac{R1+R2}{R2} \quad \text{[V]}$$

Please set feedback resistor R2 below 30 kΩ to reduce the error margin by the bias current. In addition, since power efficiency is reduced with a small R1 + R2, please set the current flowing through the feedback resistor to be small as possible than the output current I_O.

Selection of Components Externally Connected – continued

5. Selection of the schottky barrier diode D1

The schottky barrier diode that has small forward voltage and short reverse recovery time is used for D1. The important parameters for the selection of the schottky barrier diode are the average rectified current and direct current inverse-direction voltage. Average rectified current $I_{F\ (AVG)}$ is obtained in the following equation:

$$I_{F(AVG)} = I_{O(MAX)} \times \frac{V_{IN(MAX)} - V_O}{V_{IN(MAX)}} \quad [A]$$

Where:
$I_{F(AVE)}$ is the average rectified current

The absolute maximum rating of the schottky barrier diode rectified current average is more than 1.2 times $I_{F(AVG)}$ and the absolute maximum rating of the DC reverse voltage is greater than or equal to 1.2 times the maximum input voltage. The loss of D1 is obtained in the following equation:

$$P_{Di} = I_{O(MAX)} \times \frac{V_{IN(MAX)} - V_O}{V_{IN(MAX)}} \times VF \ [W]$$

Where:
VF is the forward voltage in $I_{O(MAX)}$ condition

Selecting a diode that has small forward voltage, and short reverse recovery time is highly effective. Please select a diode with 0.65 V Max of forward voltage. Please note that there is possibility of internal element destruction when a diode with a larger VF than this is used. Because the reverse recovery time of the schottky barrier diode is so short, that it is possible to disregard, the switching loss can be disregarded. When it is necessary for the diode to endure the state of output short-circuit, power dissipation ratings and the heat radiation ability are needed to be considered. The rated current that is required is about 1.5 times the overcurrent detection value.

6. Selection of the switching frequency setting resistance R_{RT}, C_{RT}

The internal switching frequency can be set by connecting a resistor between RT and GND.
The range that can be set is 50 kHz to 600 kHz, and the relation between resistance and the switching frequency is decided as shown in the figure below. When setting beyond this range, there is a possibility that there is no oscillation and IC operation cannot be guaranteed.
C_{RT} is required to stabilize switching frequency. Typical capacitance value is 100pF. Actually, the changes in the frequency characteristic are greatly affected by the type and the condition (temperature, etc.) of parts that are used, the wire routing and layout of the PCB.

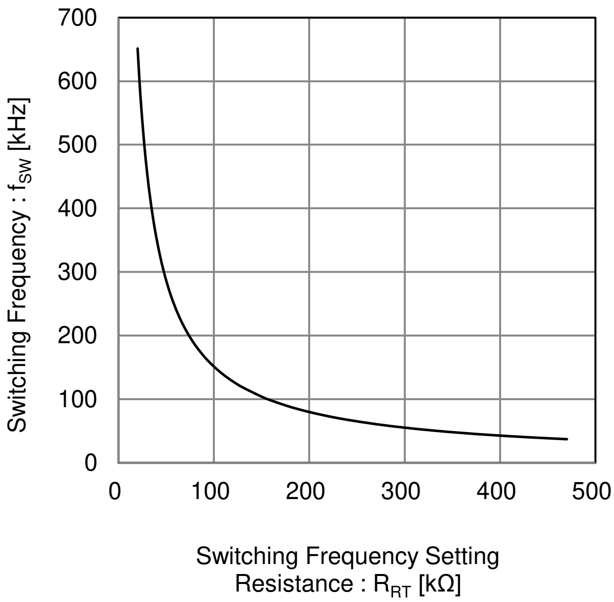


Figure 13. Switching Frequency vs Switching Frequency Setting Resistance

R_{RT} [kΩ]	f_{SW} [kHz]
22	599
24	555
27	500
30	455
33	418
36	386
39	359
43	329
47	303
51	281
56	258
62	235
68	216
75	197
82	182
91	165

R_{RT} [kΩ]	f_{SW} [kHz]
100	151
110	139
120	128
130	119
150	104
160	98.
180	88
200	80
220	73
240	68
270	61
300	55
330	51

Selection of Components Externally Connected – continued

7. Selection of the phase compensation circuit R3, C1, C2

A good high frequency response performance is achieved by setting the 0 dB crossing frequency, fc, (frequency at 0 dB gain) high. However, you need to be aware of the trade-off correlation between speed and stability. Moreover, DC / DC converter application is sampled by switching frequency, so the gain of this switching frequency must be suppressed. It is necessary to set the 0 dB crossing frequency to 1 / 10 or less of the switching frequency. In summary, target these characteristics as follows:

・When the 0 dB crossing frequency, fc, phase lag is less than or equal to 135 ˚(More than 45 ˚ phase margin).

・0 dB crossing frequency, fc, is 1 / 10 times or less of the switching frequency. To improve the responsiveness, higher the phase compensation is set by the capacitor and resistor which are connected in series to the VC pin.

Achieving stability by using the phase compensation is done by cancelling the f_{P1} and f_{P2} (error amp pole and power stage pole) of the regulation loop by use of f_{Z1}. f_{P1}, f_{P2} and f_{Z1} are determined in the following equations.

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C1} \quad \text{[Hz]}$$

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_O} \quad \text{[Hz]}$$

$$f_{P2} = \frac{G_{EA}}{2\pi \times C1 \times A_V} \quad \text{[Hz]}$$

Also, by inserting a capacitor in C2, phase lead f_{Z2} can be added.

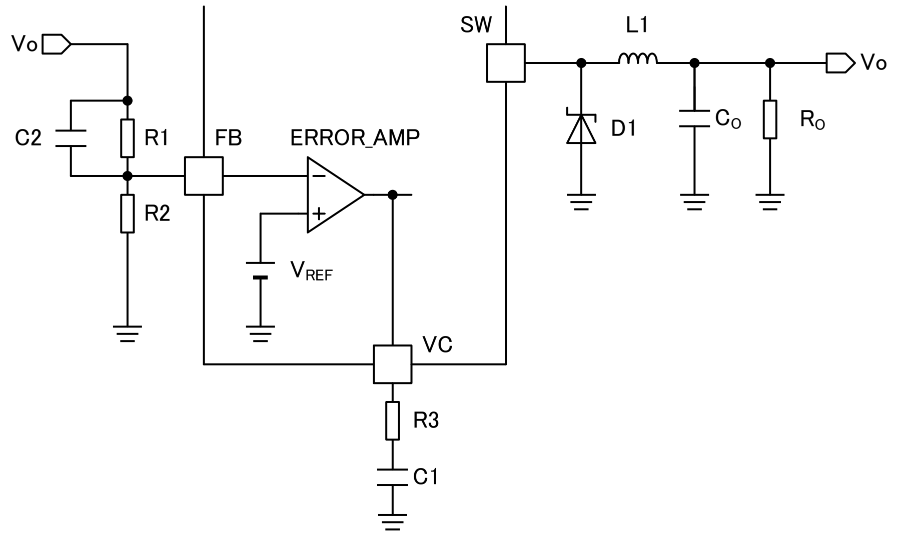
$$f_{Z2} = \frac{1}{2\pi \times R1 \times C2} \quad \text{[Hz]}$$

Where:

R_O is the resistance assumed actual load[Ω] = Output Voltage[V] / Output Current[A]、

G_{EA} is the Error Amp trans conductance (270 µA / V)

A_V is the Error Amp Voltage Gain (78 dB)



Setting Phase Compensation Circuit

Selection of Components Externally Connected – continued

By setting zero and pole settings to suitable position, stable frequency characteristic can be achieved. The typical setting of f_{Z1}, f_{Z2} is as below.

1. f_{Z1} setting is to cancel f_{P1}.
   For instance, application which load current is 500 mA ~ 3.5 A, typical setting of F_{Z1}, F_{P1} setting in Application Examples1 (P.19) is as below.

$$0.5 \times f_{p1} \le f_{Z1} \le 5 \times f_{p1}$$

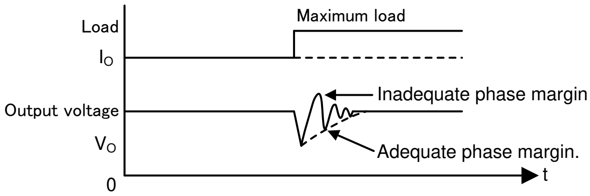
   (f_{P1}=362 Hz [I_O=500 mA], 2.53 kHz [I_O =3.5 A] f_{Z1}=1.69 kHz)

2. f_{Z2} setting is to shift the 0 dB crossing frequency to higher frequency or to improvephase margin near the 0 dB crossing frequency.
   Typical setting of F_{Z2}, F_{P1} inApplication Examples3 (P.23) is as below.

$$0.5 \times f_{zero} \le f_{Z2} \le 2 \times f_{zero}$$

   (f_{ZERO}=31.6 kHz [I_O=400 mA] f_{Z2}=20.6 kHz)

Actually, the changes in the frequency characteristic are greatly affected by the type and the condition (temperature, etc.) of parts that are used, the wire routing and layout of the PCB.
Please confirm stability and responsiveness in actual equipment.
To check the actual frequency characteristics, use a FRA or a gain-phase analyzer. Moreover, the method of observing the degree of change by the loading response can be performed when these measuring instruments are not available. The phase margin degree is said to be low when there are lots of variation quantities after the output is made to change under no load to maximum load. It can also be observed that the phase margin degree is low when there is a lot of ringing frequencies after the transition of no load to maximum load, usually two times or more ringing than the standard. However, a quantitative phase margin degree cannot be confirmed.



Measurement of Load Response

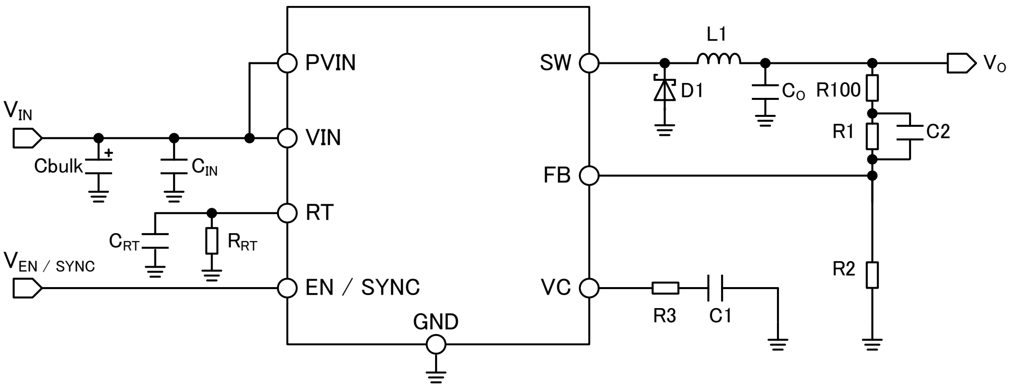
8. Setting of soft start time (T_{SS})
   The soft start function is necessary to prevent inrush of coil current and output voltage overshoot at startup.
   T_{SS} will be changed by setting the switching frequency.
   The production tolerance of T_{SS} is ±18.1%.T_{SS} can be calculated by using the equation.

$$T_{SS} = \frac{690.8}{fsw} \text{ [s]}$$

Application Examples1

Parameter	Symbol	Specification case
Product Name	IC	BD90640HFP / EFJ-C
Input Voltage	V_{IN}	6 V to 18 V
Output Voltage	V_O	5 V
Output Ripple Voltage	ΔV_{PP}	20 mVp-p
Output Current	I_O	Min 1.0 A / Typ 1.5 A / Max 2.0 A
Switching Frequency	f_{SW}	500 kHz
Operating Temperature	Topr	-40 °C ~ +105 °C

Specification Example 1



Reference Circuit 1

No	Package	Parameters	Part name (series)	Type	Manufacturer
R1	1608	43 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R2	1608	8.2 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R3	1608	20 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R100	-	SHORT	-	-	-
R_{RT}	1608	27 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
C1	1608	4700 pF, R, 50 V	GCM series	Ceramic capacitor	Murata
C2	-	OPEN	-	-	-
C_{RT}	1608	100 pF, CH, 50 V	GCM series	Ceramic capacitor	Murata
C_{IN}	3225	4.7 µF, X7R, 50 V	GCM series	Ceramic capacitor	Murata
C_O	3225	44 µF (22 µF, X7R, 16 V × 2)	GCM series	Ceramic capacitor	Murata
Cbulk	-	220 µF, 50 V	CD series	Electrolytic capacitor	NICHICON
L1	W 9.7 x H 3.8 x L 10 mm^3	15 µH	CLF10040T-150M-H	Inductor	TDK
D1	CPD	Average I = 6 A Max	RB095BM-40FH	Schottky Diode	ROHM

Parts List 1

Characteristic Data (Application Examples 1)

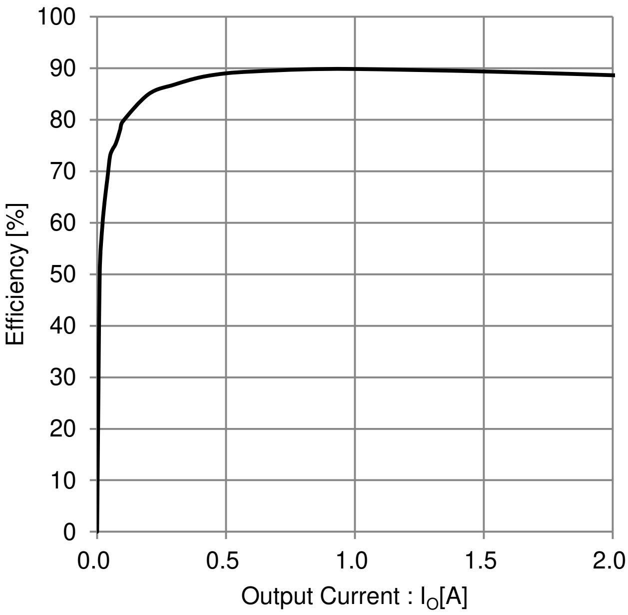


Figure 14. Efficiency vs Output Current
(Conversion Efficiency 1 V_{IN} = 13.2 V)

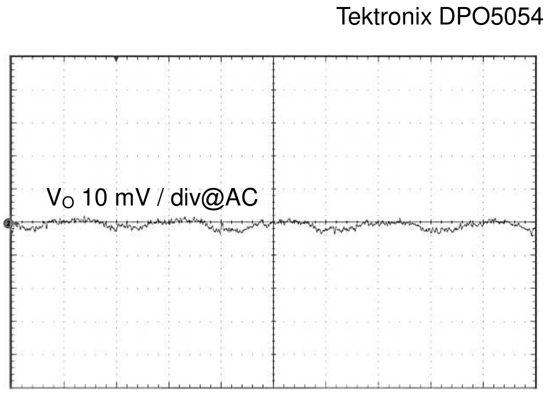


Figure 15. Output Ripple Voltage 1
(V_{IN} = 13.2 V, I_O = 1.5 A, 1 μs / div)

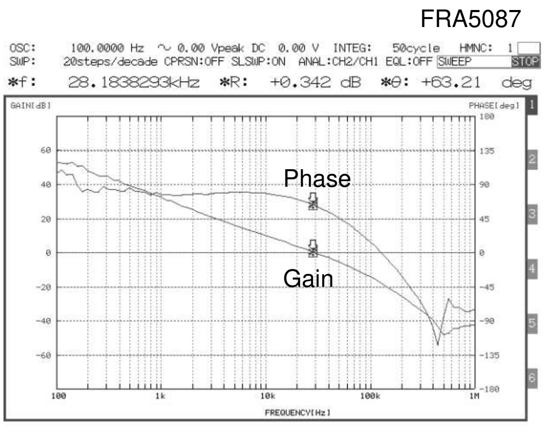


Figure 16. Frequency Characteristic 1
(V_{IN} = 13. 2 V, I_O = 1.5 A)

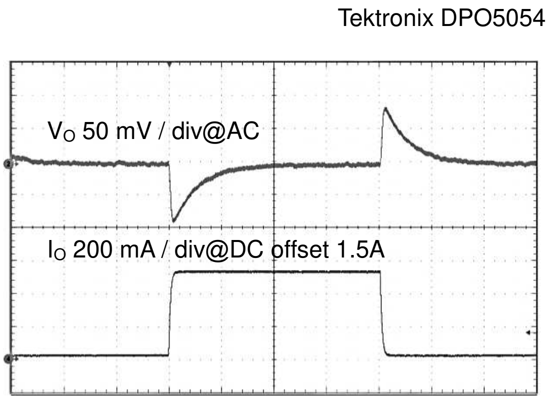
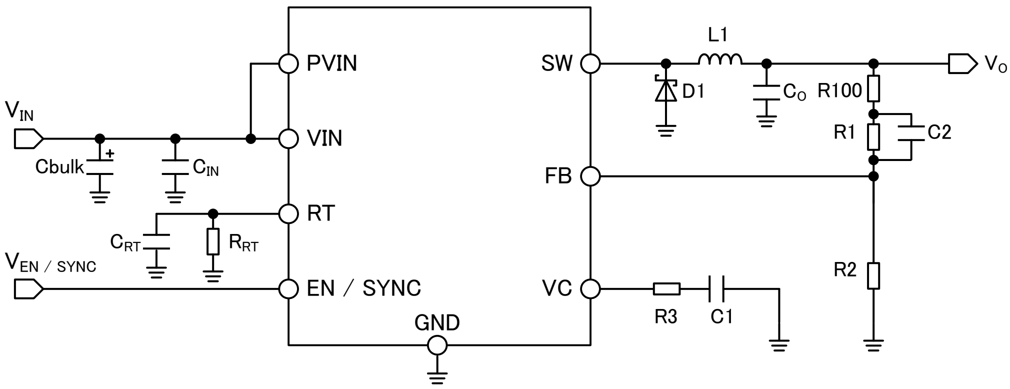


Figure 17. Load Response 1
(V_{IN} = 13.2 V, I_O = 1.5 A → 2.0 A, 200 μs / div)

Application Examples 2

Parameter	Symbol	Specification case
Product Name	IC	BD90620HFP / EFJ-C
Input Voltage	V_{IN}	6 V to 18 V
Output Voltage	V_O	5 V
Output Ripple Voltage	ΔV_{PP}	20 mVp-p
Output Current	I_O	Min 0.4 A / Typ 0.8 A / Max 1.5 A
Switching Frequency	f_{SW}	500 kHz
Operating Temperature	Topr	-40 °C ~ +105°C

Specification Example 2



Reference Circuit 2

No	Package	Parameters	Part name (series)	Type	Manufacturer
R1	1608	43 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R2	1608	8.2 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R3	1608	20 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R100	-	SHORT	-	-	-
R_{RT}	1608	27 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
C1	1608	4700 pF, R, 50 V	GCM series	Ceramic capacitor	Murata
C2	-	OPEN	-	-	-
C_{RT}	1608	100 pF, CH, 50 V	GCM series	Ceramic capacitor	Murata
C_{IN}	3225	4.7 µF, X7R, 50 V	GCM series	Ceramic capacitor	Murata
C_O	3225	44 µF (22 µF, X7R, 16 V × 2)	GCM series	Ceramic capacitor	Murata
Cbulk	-	220 µF, 50 V	CD series	Electrolytic capacitor	NICHICON
L1	W 9.7 x H 3.8 x L 10 mm^3	22 µH	CLF10040T-220M-H	Inductor	TDK
D1	CPD	Average I = 6 A Max	RB095BM-40FH	Schottky Diode	ROHM

Parts List 2

Characteristic Data (Application Examples 2)

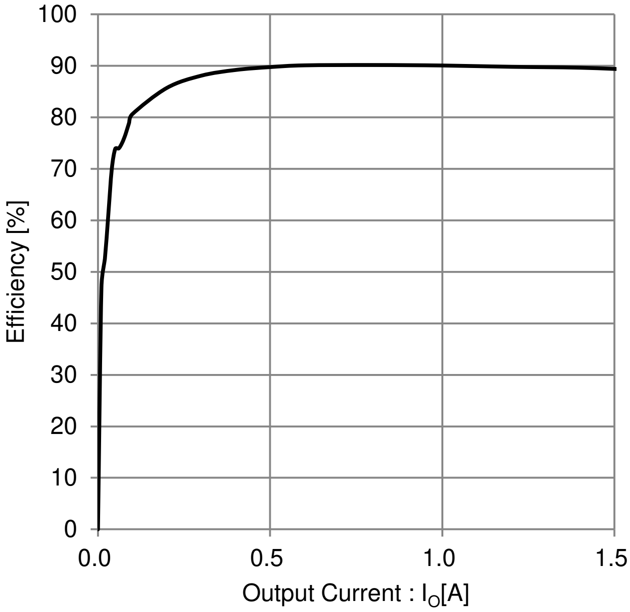


Figure 18. Efficiency vs Output Current
(Conversion Efficiency 2 V_{IN} = 13.2 V)

Tektronix DPO5054

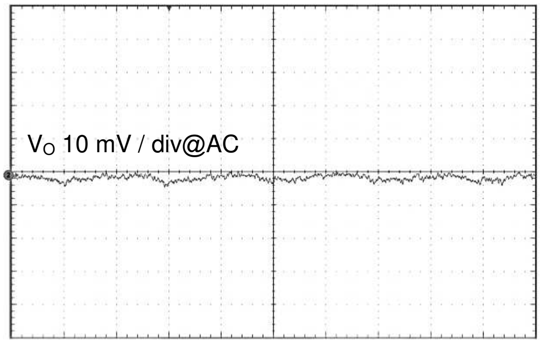


Figure 19. Output Ripple Voltage 2
(V_{IN} = 13.2 V, I_O = 0.8 A, 1 μs / div)

FRA5087

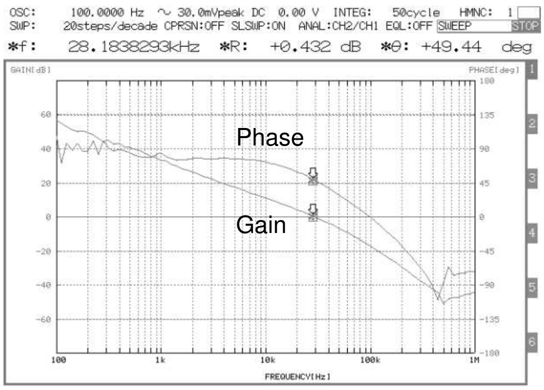


Figure 20. Frequency Characteristic 2
(V_{IN} = 13.2 V, I_O = 0.8 A)

Tektronix DPO5054

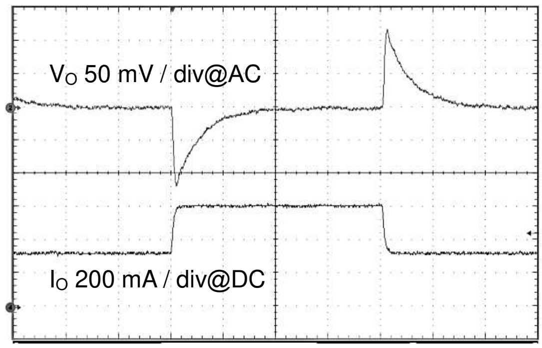
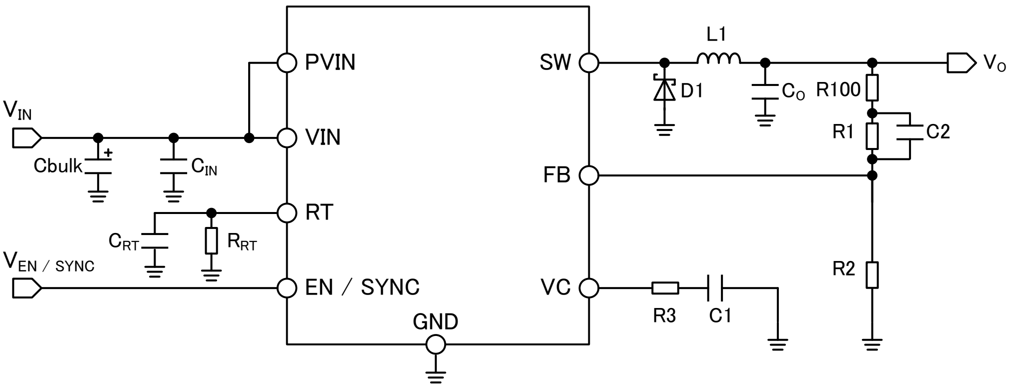


Figure 21. Load ResponseResponse 2
(V_{IN} = 13.2 V, I_O = 0.8 A → 1.5 A, 200 μs / div)

Application Examples 3

Parameter	Symbol	Specification case
Product Name	IC	BD90610EFJ-C
Input Voltage	V_{IN}	6 V to 18 V
Output Voltage	V_O	5 V
Output Ripple Voltage	ΔV_{PP}	20 mVp-p
Output Current	I_O	Min 0.1 A / Typ 0.4 A / Max 0.8 A
Switching Frequency	f_{SW}	500 kHz
Operating Temperature	Topr	-40 °C ~ +105°C

Specification Example 3



Reference Circuit 3

No	Package	Parameters	Part name (series)	Type	Manufacturer
R1	1608	43 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R2	1608	8.2 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R3	1608	33 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R100	-	SHORT	-	-	-
R_{RT}	1608	27 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
C1	1608	10000 pF, R, 50 V	GCM series	Ceramic capacitor	Murata
C2	1608	180pF,CH,50V	GCM series	Ceramic capacitor	Murata
C_{RT}	1608	100 pF, CH, 50 V	GCM series	Ceramic capacitor	Murata
C_{IN}	3225	4.7 µF, X7R, 50 V	GCM series	Ceramic capacitor	Murata
C_O	3225	44 µF (22 µF, X7R, 16 V × 2)	GCM series	Ceramic capacitor	Murata
Cbulk	-	220 µF, 50 V	CD series	Electrolytic capacitor	NICHICON
L1	W 9.7 x H 3.8 x L 10 mm^3	100 µH	CLF10040T-101M-H	Inductor	TDK
D1	PMDS	Average I = 3 A Max	RB055L-40TF	Schottky Diode	ROHM

Parts List 3

Characteristic Data (Application Examples 3)

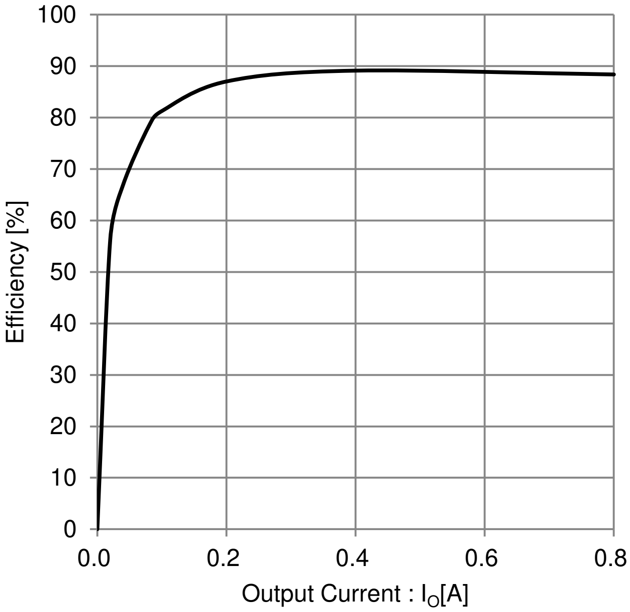


Figure 22. Efficiency vs Output Current
(Conversion Efficiency 3 V_{IN} = 13.2 V)

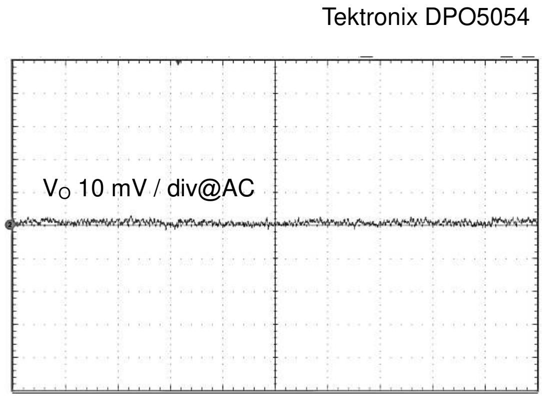


Figure 23. Output Ripple Voltage 3
(V_{IN} = 13.2 V, I_O = 0.4 A, 1 μs / div)

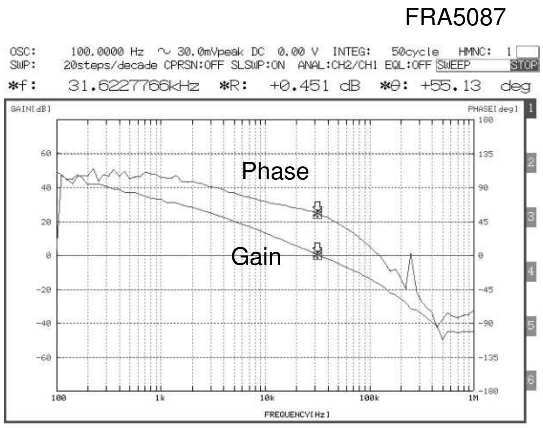


Figure 24. Frequency Characteristic 3
(V_{IN} = 13.2 V, I_O = 0.4 A)

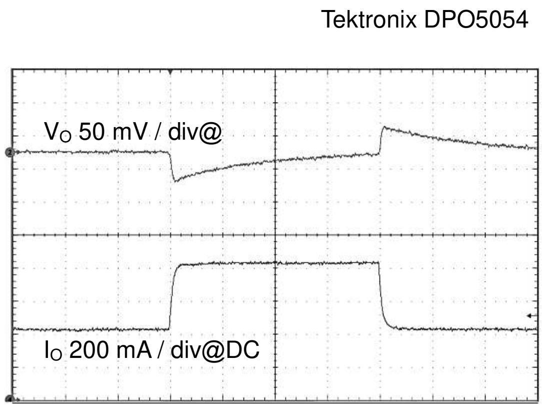
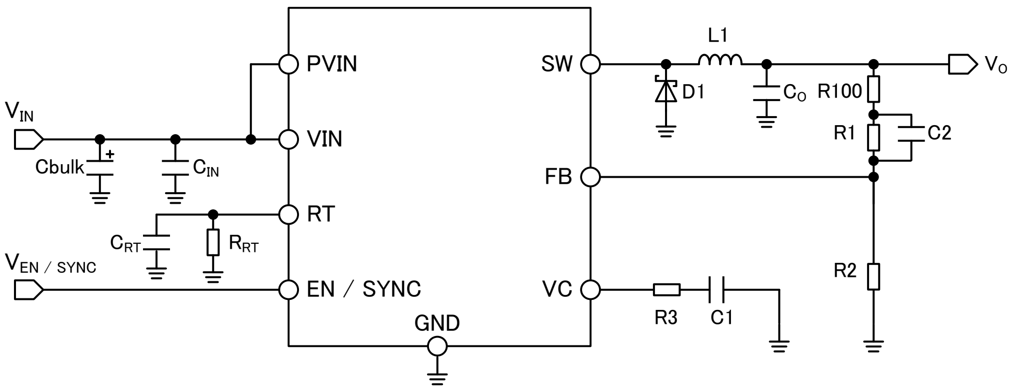


Figure 25. Load Response 3
(V_{IN} = 13.2 V, I_O = 0.4 A → 0.8 A, 200 μs / div)

Application Examples 4

Parameter	Symbol	Specification case
Product Name	IC	BD90640HFP / EFJ-C
Input Voltage	V_{IN}	3.5 V to 18 V
Output Voltage	V_O	3.3 V
Output Ripple Voltage	ΔV_{PP}	20 mVp-p
Output Current	I_O	Min 1.0 A / Typ 1.5 A / Max 2.0A
Switching Frequency	f_{SW}	500 kHz
Operating Temperature	Topr	-40 °C ~ +125°C

Specification Example 4



Reference Circuit 4

No	Package	Parameters	Part name (series)	Type	Manufacturer
R1	1608	47 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R2	1608	15 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R3	1608	10 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
R100	-	SHORT	-	-	-
R_{RT}	1608	27 kΩ, 1 %, 1 / 10 W	MCR03 series	Chip resistor	ROHM
C1	1608	6800 pF, R, 50 V	GCM series	Ceramic capacitor	Murata
C2	-	OPEN	-	-	-
C_{RT}	1608	100 pF, CH, 50 V	GCM series	Ceramic capacitor	Murata
C_{IN}	3225	4.7 µF, X7R, 50 V	GCM series	Ceramic capacitor	Murata
C_O	3225	44 µF (22 µF, X7R, 16 V × 2)	GCM series	Ceramic capacitor	Murata
Cbulk	-	220 µF,35 V × 2	CZ series	Electrolytic capacitor	NICHICON
L1	W 9.7 x H 3.8 x L 10 mm^3	15 µH	CLF10040T-150M-D	Inductor	TDK
D1	CPD	Average I = 6 A Max	RB095BM-40FH	Schottky Diode	ROHM

Parts List 4