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PFC Direct current resonance type White LED Driver for Large LCD

BD92111F

General Description

BD92111F is a current resonance type LED Driver with frequency-controlled LED current. It can connect to PFC directly and can use half-bridge structure reducing the number of external components.
It incorporates some protection functions against fault conditions such as Over-Voltage Protection and LED Open Detection (IS Low Detection).

Features

- 20V High Rating Process
- 1 Channel Push-pull Control
- Current and Voltage Feedback by Driving Frequency
- Adjustable Soft Start
- Adjustable Timer Latch
- Under-Voltage Detection for IC's Power Line
- Output Over-Voltage Protection
- Output Error Signal from FAIL Terminal
- Shift to Save Mode by STB Terminal
- Burst Control by External PWM Signal

Applications

- TV, Computer Display, LCD Backlighting.

Key Specifications

- Operating Power Supply Voltage Range: 8.0V to 18.0V
- Minimum Oscillator Frequency: 65.8kHz (R_{RT}=22kΩ,R_{ADJ}=36kΩ,V_{FB}=3.2V)
- Operating Current: 2.3mA (Typ)
- Operating Temperature Range: -40°C to +85°C

Package

	W(Typ) x D(Typ) x H(Max)
SOP18	11.20mm x 7.80mm x 2.01mm
	Pin pitch 1.27mm

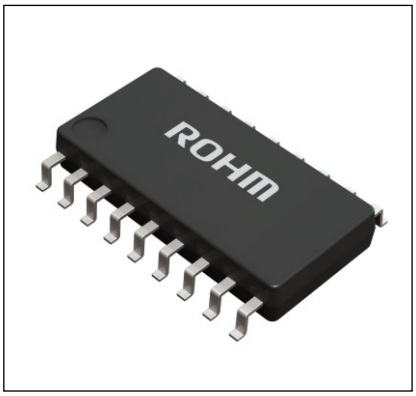


Figure. 1 SOP18

Typical Application Circuit

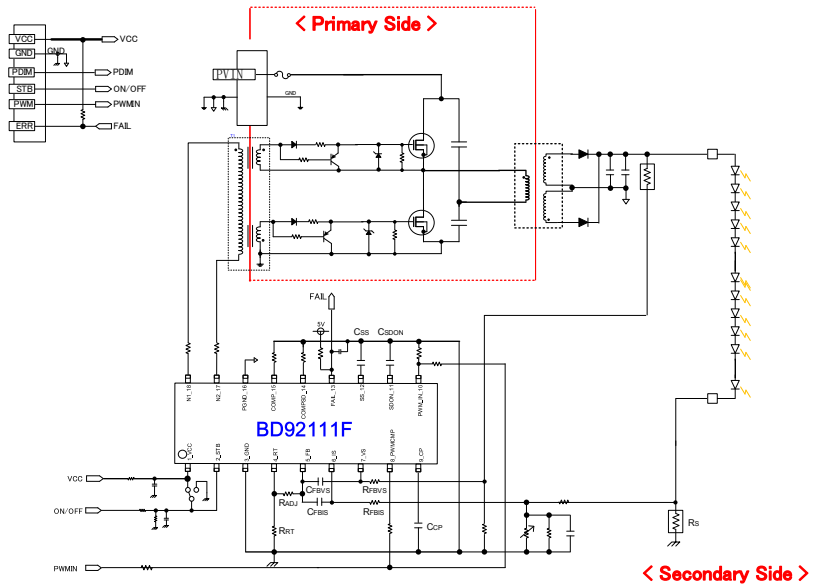


Figure. 2 Typical Application Circuit(s)

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	20	V
STB, N2, N1 Terminal Voltage	V_{STB},V_{N2},V_{N1}	20	V
RT,FB,IS,VS,PWMCMP,CP, PWMIN,SS,FAIL,COMP,SDON, COMPSD Terminal Voltage	V_{RT},V_{FB},V_{IS},V_{VS},V_{PWMCMP}, V_{CP},V_{PWMIN},V_{ADIM},V_{SS}, V_{FAIL},V_{COMP},V_{SDON},V_{COMPSD}	5.5	V
Power Dissipation	Pd	0.69 (Note 1)	W
Operating Temperature Range	Topr	-40 to +85	°C
Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) Derating in done 5.5 mW/°C for operating above Ta≥25°C (Mount on 1-layer 70.0mm x 70.0mm x 1.6mm board)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -40°C to +85°C)

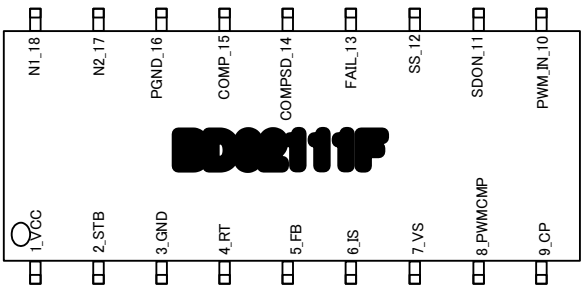
Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	8.0 to 18.0	V
PWMIN Input Frequency Range	f_{PWMIN}	60 to 500	Hz
Oscillation Frequency	f_{OUT}	30 to 200	kHz

External Components Recommended Range (Ta= -40°C to +85°C)

Parameter	Symbol	Range	Unit
RT Connection Resistance	R_{RT}	24 to 160	kΩ
Set up Resistance for operation frequency range	R_{ADJ}	51 ～ OPEN	kΩ
CP Connection Capacitance	C_{CP}	0.01 to 2.2 (Note 2)	μF
SS Connection Capacitance	C_{SS}	0.01 to 0.1 (Note 2)	μF
SDON Connection Capacitance	C_{SDON}	0.01 to 2.2 (Note 2)	μF

(Note 2) Please set connection capacitance above Min value of Recommended Range according to temperature characteristic and DC bias characteristic.

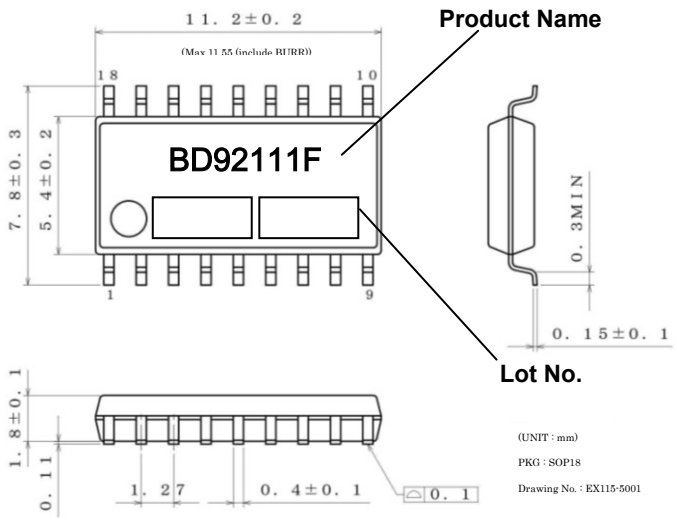
Pin Configuration



(TOP VIEW)

Figure. 3 Pin Configuration

Physical Dimension and Marking Diagram



SOP18(Unit:mm)

Figure. 4 Physical Dimension and Marking Diagram

Electrical Characteristics (Unless otherwise specified Ta=25°C, V_{CC}=12V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
【Whole Device】						
Circuit Current	I_{CC1}	-	2.3	5.0	mA	f_{OUT}=60kHz, $V_{PWMCOMP}$=0V
Circuit Current at Stand-by	I_{CC2}	-	0	20	μA	V_{STB}=0V
【STB Block】						
STB Pin High Voltage	V_{STH}	2.0	-	V_{CC}	V	System ON
STB Pin Low Voltage	V_{STL}	-0.3	-	+0.8	V	System OFF
【VCC UVLO Block】						
VCC Operation Voltage	V_{VCCUVP}	6.17	6.50	6.83	V	
VCC UVLO Hysteresis	ΔV_{VCCUVP}	0.37	0.50	0.63	V	
【OSC Block】						
RT Terminal voltage	V_{RT}	1.05	1.50	1.95	V	
【PWMIN Block】						
PWMIN Pin High Voltage	V_{PWMINH}	2.0	-	5.0	V	
PWMIN Pin Low Voltage	V_{PWMINL}	-0.3	-	+0.8	V	
【Soft Start Block】						
Setting Current for Soft Start Timer	I_{SS}	1.5	2.0	2.5	μA	
Soft Start Ended Voltage	V_{SSEND}	2.8	3.0	3.2	V	
【Feed Back Block】						
IS Threshold Voltage	V_{IS}	1.225	1.250	1.275	V	
VS Threshold Voltage	V_{VS}	1.212	1.250	1.288	V	
IS Source Current 1	I_{IS1}	-	-	0.9	μA	V_{PWMIN}=2.5V
IS Source Current 2	I_{IS2}	40	50	60	μA	V_{PWMIN}=0V, V_{IS}=1.0V
VS Source Voltage	I_{VS}	-	-	0.9	μA	
IS COMP Detection Voltage	V_{ISCOMP}	0.606	0.625	0.644	V	

Electrical Characteristics – continued (Unless otherwise specified Ta=25°C, V_{CC}= 12V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Min		
【Output Block】						
N1 Output Sink Resistance	R_{N1SI}	1.5	3.0	6.0	Ω	
N1Output Source Resistance	R_{N1SO}	4.5	9.0	18.0	Ω	
N2 Output Sink Resistance	R_{N2SI}	1.5	3.0	6.0	Ω	
N2 Output Source Resistance	R_{N2SO}	4.5	9.0	18.0	Ω	
MAX DUTY	MAX DUTY	43.0	45.0	47.0	%	f_{OUT}=60kHz
N1-N2,N2-N1Dead Time	t_{OFF}	100	200	400	ns	
Output Frequency (minimum frequency setting)	f_{OUTMIN}	59.3	65.8	72.3	kHz	R_{RT}=22kΩ,R_{ADJ}=36kΩ, V_{FB}=3.2V
【Timer Block】						
Setting Voltage for CP Time	V_{CP}	1.90	2.00	2.10	V	
Setting Current for CP Time	I_{CP}	0.85	1.00	1.15	μA	
【COMP Block】						
Over voltage Detection level of COMP	V_{COMP}	3.88	4.00	4.12	V	
Hysteresis width (COMP)	ΔV_{COMP}	0.15	0.20	0.25	V	
COMPSD Detection Voltage	V_{COMPSD}	3.88	4.00	4.12	V	
【FAIL Block】						
FAIL Pin ON-Resistance	R_{FAIL}	-	100	200	Ω	

Pin Description

Pin No.	Pin Name	IN/OUT	Function	Rating [V]
1	VCC	IN	Power Supply Pin for IC (Built-In UVLO Function)	-0.3 to +20
2	STB	IN	Power ON/OFF Control Pin for IC Power OFF when STB=L and Power ON when STB=H.	-0.3 to +20
3	GND	IN	Ground Pin for Internal Signal in IC	-
4	RT	OUT	Drive Frequency Setting Pin Basic Frequency is set by the resistor between RT and GND and Drive Frequency Modulation Range is set by the resistor between RT and FB.	-0.3 to +5.5
5	FB	OUT	Error Amplifier Output pin for LED Current feedback and LED Voltage feedback	-0.3 to +5.5
6	IS	IN	Error Amplifier Input pin for LED Current feedback	-0.3 to +5.5
7	VS	IN	Error Amplifier Input pin for LED Open Voltage feedback	-0.3 to +5.5
8	PWMCMP	IN	PWM Comparator Input Pin which controls PWM operation during brightness adjustment. N1 and N2 output stop when PWMCMP=L, and they output Max Duty when PWMCMP=H	-0.3 to +5.5
9	CP	OUT	Timer Latch Setting Pin In abnormal case, 1μA (Typ) will be charged to the capacitor connected to CP, and IC becomes latch status after output operation stops at CP>2V(Typ)	-0.3 to +5.5
10	PWMIN	IN	PWM Signal Input Pin for burst brightness adjustment	-0.3 to +5.5
11	SDON	OUT	Enable COMPSD inputs over voltage detection When start up, 1μA(Typ) will be charged to connected capacitor. When SDON>2.0V(Typ), it will be possible to detect over voltage.	-0.3 to +5.5
12	SS	OUT	Soft Start timer and COMPSD timer Setting Pin During start-up, 2μA (Typ) will be charged to connected capacitor. At SS>2.0V(typ), COMPSD can start to detect. At SS>2.5V (typ), CP can accept charge operation.	-0.3 to +5.5
13	FAIL	OUT	Error Indication Signal Output Pin Normal : L, Error : Open	-0.3 to +5.5
14	COMPSD	IN	Quickly Over Voltage Detection Pin When detecting abnormality, output operation stops and IC becomes latch status after 2 clocks.	-0.3 to +5.5
15	COMP	IN	Detection pin for over voltage	-0.3 to +5.5
16	PGND	IN	Power Ground for external MOSFET drive	-
17	N2	OUT	Output pin for external FET drive circuit (Channel N2)	-0.3 to +20
18	N1	OUT	Output pin for external FET drive circuit (Channel N1)	-0.3 to +20

I/O Equivalent Circuits

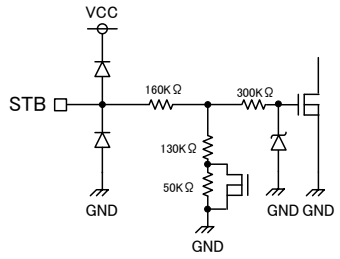
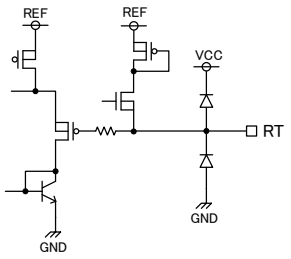
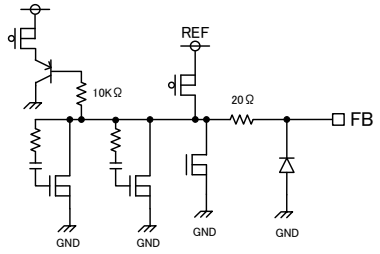
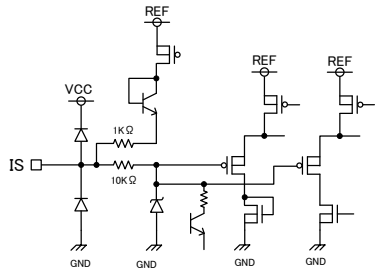
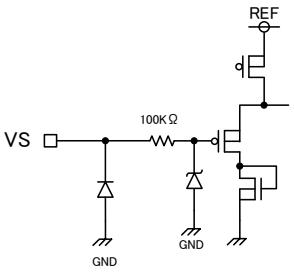
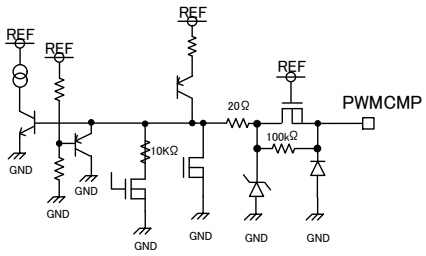
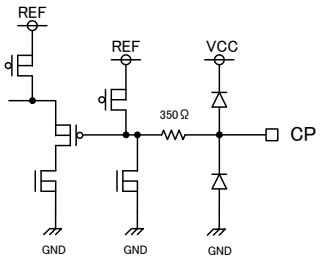
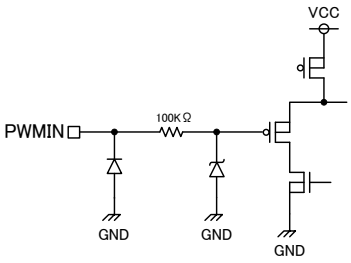
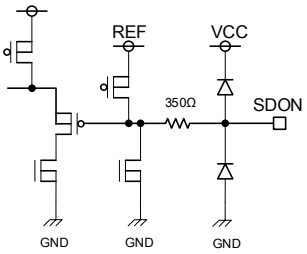
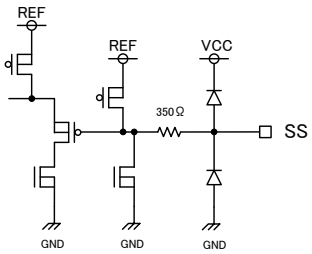
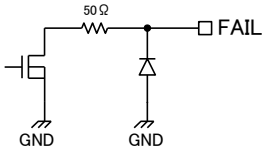
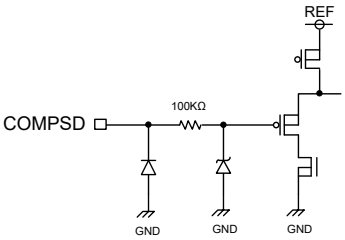
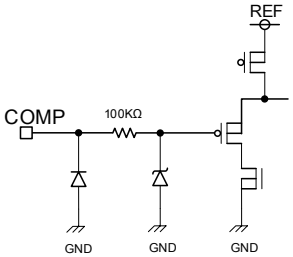
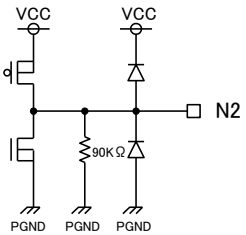
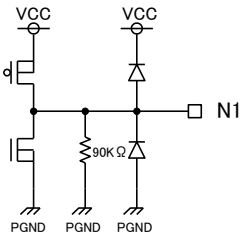
STB	RT	FB
		
IS	**VS**	**PWMCMP**
		
CP	**PWMIN**	**SDON**
		
SS	**FAIL**	**COMPSD**
		
COMP	**N2**	**N1**
		

Figure. 5 I/O equivalent circuit

Block Diagram

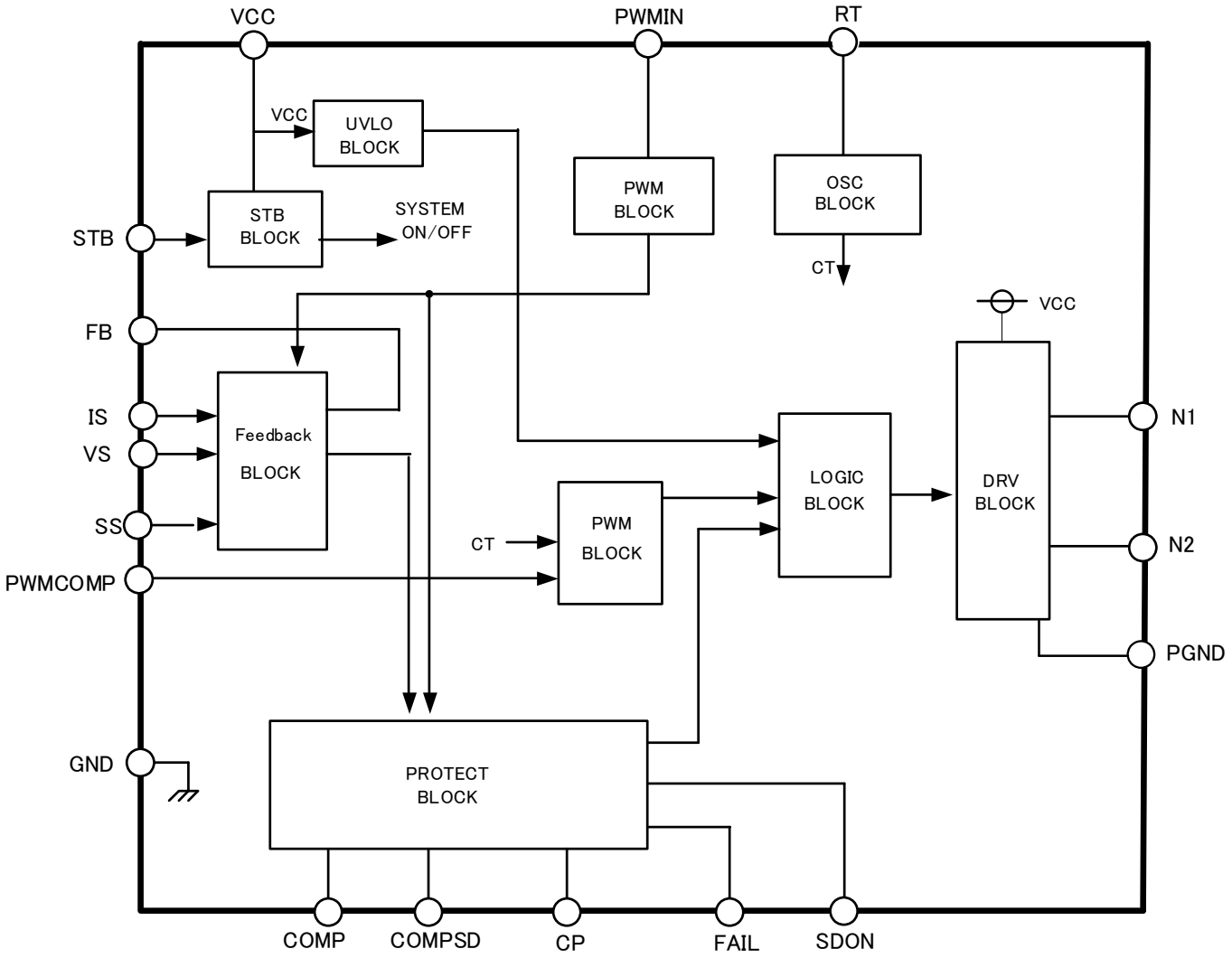


Figure. 6 Block Diagram

Typical Performance Curves

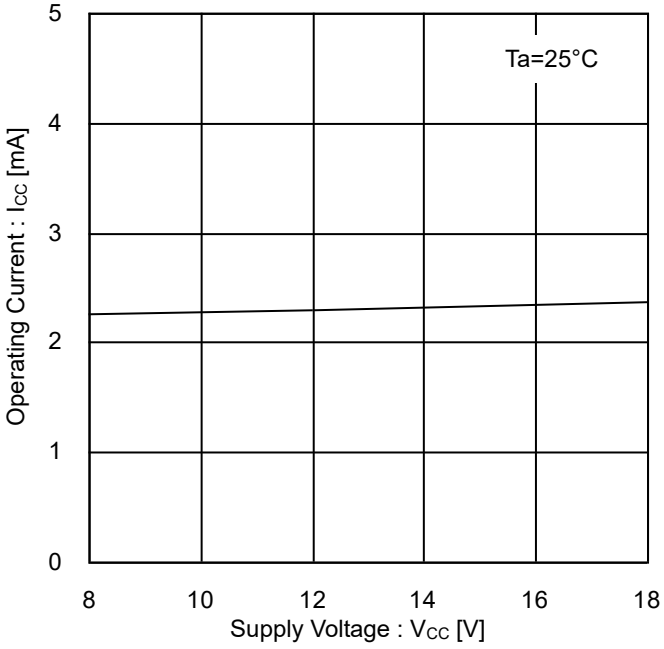


Figure 7. Operating Current vs Power Supply Voltage

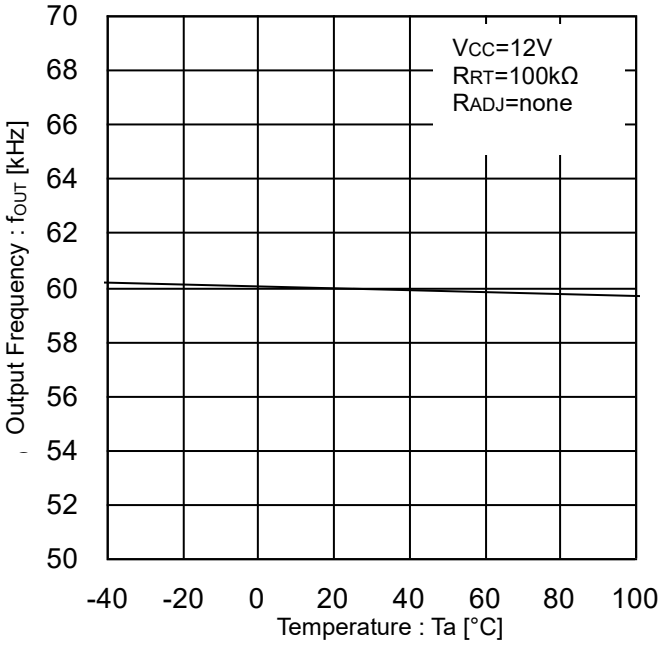


Figure 8. Output Frequency vs Temperature

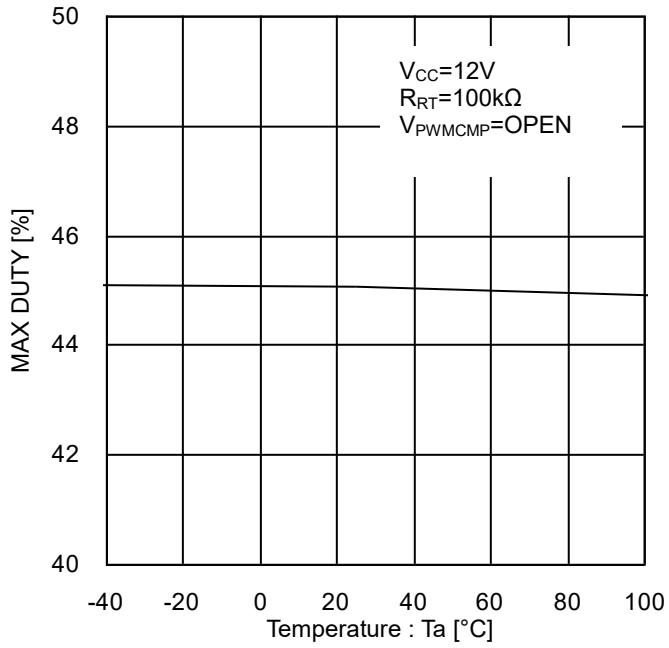


Figure 9. MAX DUTY vs Temperature

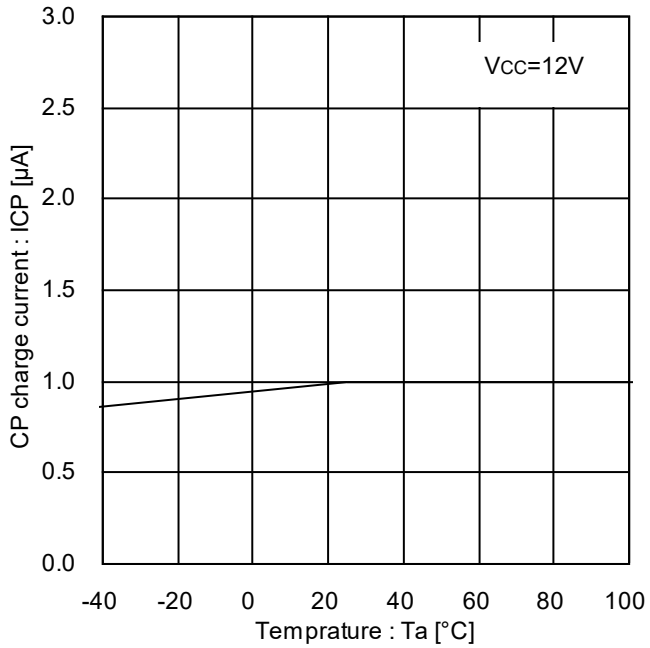


Figure. 10 CP time setting current vs Temperature

Pin Function Description

PIN.1 VCC

This is power supply pin for the IC. Normal operation range (Typ) is from 9V to 18V. Please place ceramic capacitor bigger than 0.1μF as bypass capacitor between VCC and GND. It is for noise elimination.

PIN.2 STB

This PIN is for setting of ON/OFF. It is possible to use as reset when shutting down.
Please set the STB terminal voltage below VCC voltage. In addition, please set below 4V if the voltage is applied earlier than VCC.
Depending on input voltage to STB pin, the status of IC might be switched (ON/OFF). Please avoid using between the two status (0.8V to 2.0V)

PIN.3 GND

This is signal system GND for IC inside. Please make it independent from PGND as much as possible (We recommend this because it has less influence with switching noise which comes from short circuit of PGND and GND at connector close to GND pin.

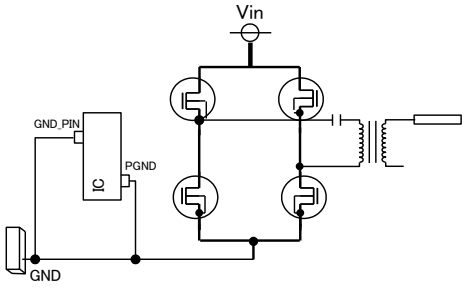


Figure. 11

PIN.4 RT

Set up the charge/discharge current by frequency of IC inside.
By changing the resistance value of resistor between RT pin and GND, it is possible to set up basic drive frequency as following formula;
Basic frequency means output N1, N2 frequency which is determined only with resistor between RT pin and GND.

$$f_{OUT}=\frac{1.217-(3.32\times10^{-5}\times R_{RT}[k\Omega])}{(2.4948\times10^{-4})+(2.5371\times10^{-4}\times R_{RT}[k\Omega])}[kHz]$$

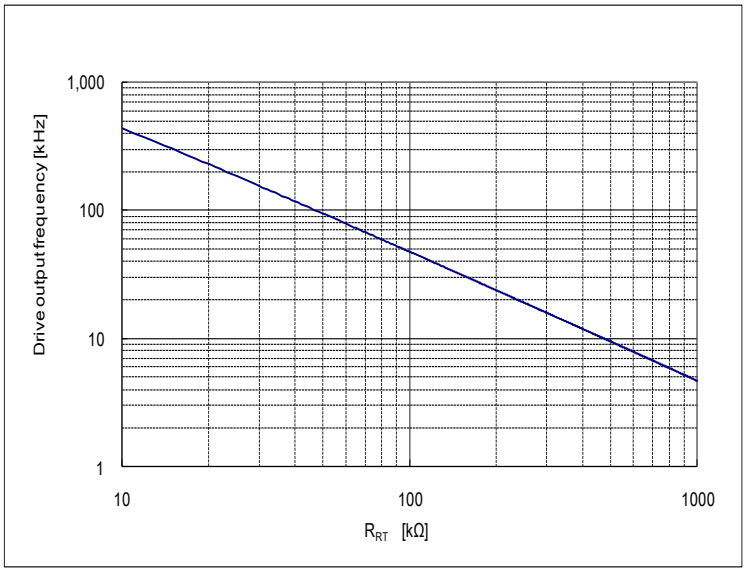


Figure. 12 RT Resistance vs Output Frequency

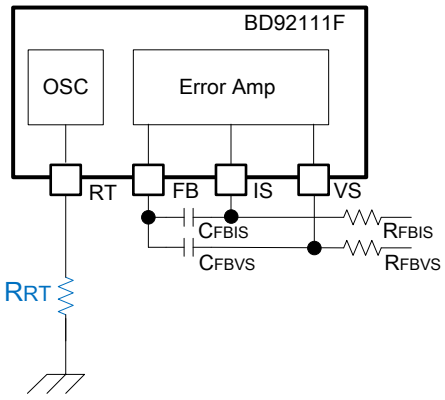


Figure. 13 RRT Resistor connection method

There is a discrepancy between theoretical formula and actual device. For frequency setting, please thoroughly verify it with actual application. In addition, frequency may change upon resistor RADJ which is placed between RT and FB pins

PIN.5 FB

This is output pin for LED current feedback (IS pin) error amplifier and open LED voltage feedback (VS pin) error amplifier. The capacitance between FB and IS (1500pF to 0.01μF) also determines start up time of LED current necessary during phase compensation and brightness adjustment. Capacitance between FB and VS (1500pF to 0.01μF) is for phase compensation of error amplifier.

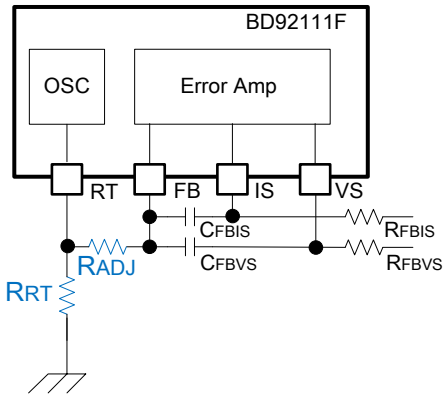
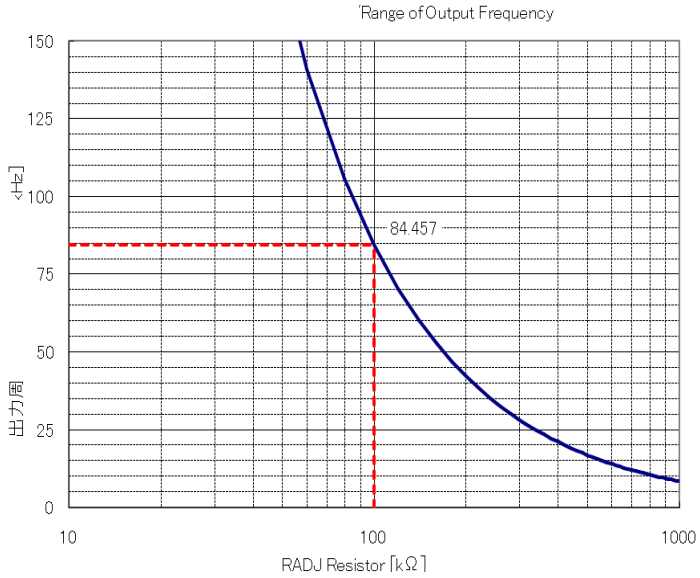


Figure. 14 R_{RT} and R_{ADJ} Resistor connection method

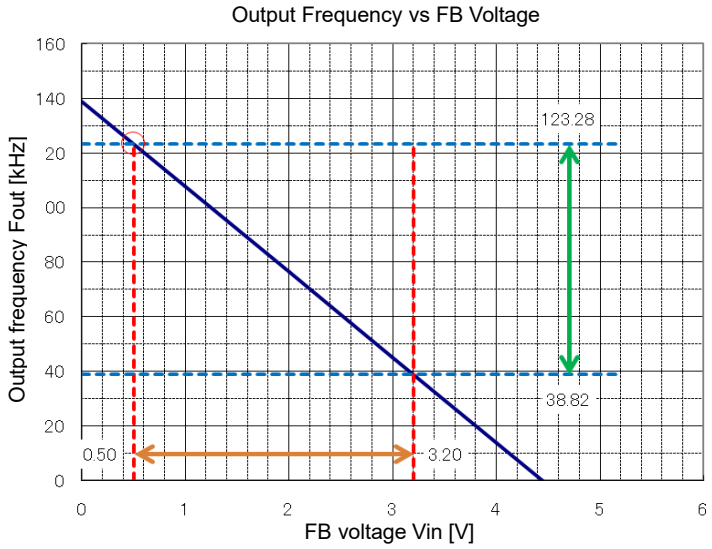


As shown by left graph, by changing resistor R_{ADJ} between FB and RT, it is possible to determine the modulation width of frequency.

Modulation width of frequency determined by the resistor between FB and RT resistor (Theoretical formula : Example)

When R_{ADJ}=100kΩ , Δ f_{OUT}=84.46kHz

Figure. 15 Modulation width of Output Frequency vs R_{ADJ} Resistance



Modulation width of frequency determined by the resistor between FB and RT resistor (Theoretical formula : Example)

When R_{ADJ}=100kΩ , Δ f_{OUT}=84.46kHz

Figure. 16 Output Frequency vs FB Voltage

The basic drive frequency is determined by resistor R_{RT} which is connected from RT pin to GND. The basic frequency is the one at V_{FB}=1.5V, and operation frequency range will be fixed with frequency modulation width that is determined by R_{ADJ} under this condition.

PIN.6 IS

This is input pin of LED current feedback (IS pin) error amplifier. Please set up as normal voltage 1.25V. When IS pin voltage becomes less than 0.625V(Typ), the output will be stopped and latched.

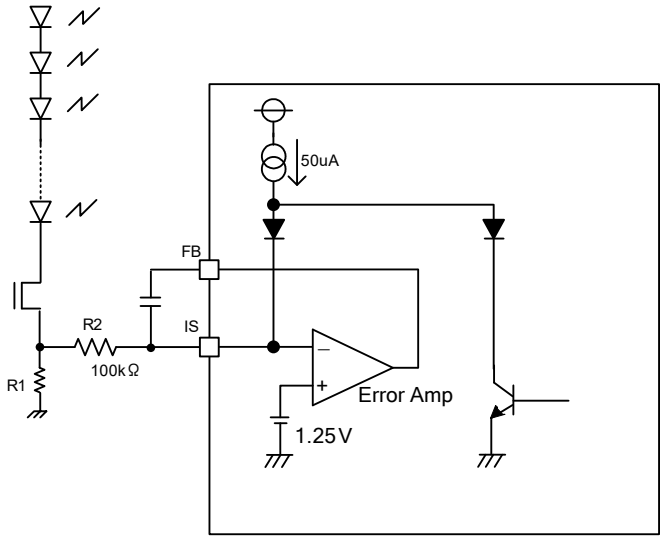


Figure. 17 IS Block Diagram

50μA (Typ) current flows from IS pin to external resistor during OFF period of burst brightness adjustment.

Considering Min value of IS source current during burst brightness adjustment, please set that total resistance from IS Pin to GND is more than 32kΩ. When R_2 is 100kΩ in above diagram, please set $R_1 + R_2 > 32K\Omega$.

PIN.7 VS

This is input pin of Open LED voltage feedback (VS pin) error amplifier. It has to be 1.25V during LED is open. When LED is ON, it will be 0.5V to 1.0V. When VS pin becomes over 1.25V, protection circuit will start operation, and if it becomes more than CP timer set up time (Timer Latch), it will shut down.

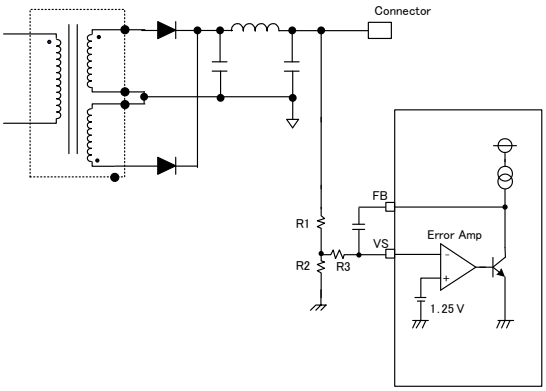


Figure. 18 VS Block Diagram

Please set C_1, C_2, R_1, R_2, and R_3 value to input 1.25V to VS pin during LED bar's connector disconnects.

PIN.8 PWMCMP

PWMCOMP pin voltage is fixed by DUTY of drive output N1, N2 in comparison with a saw wave of IC inside. This pin has 100μA sink/source current capability and when external capacitor is connected between PWMCMP and GND, IC will operate PWM at brightness start up stage. When N1 and N2 only drive at MaxDuty, please set PWMCMP=open.

PIN.9 CP

This pin sets up the time from the point of abnormal detection till shut down (Timer Latch). Having 1μA constant current charges at external capacitor connected to CP pin, it will shut down when it becomes over 2.0V. During soft start, there is no charge to CP external capacitor even fulfilling CP pin charge condition (timer latch). External capacitor is set around 0.01μF to 2.2μF).

$$T_{CP} = C_{CP} \times \frac{V_{CP}}{I_{CP}} = \frac{C_{CP} \times 2.0}{1.0 \times 10^{-6}} = 2.0 \times 10^{6} \times C_{CP} \quad [\text{sec}]$$

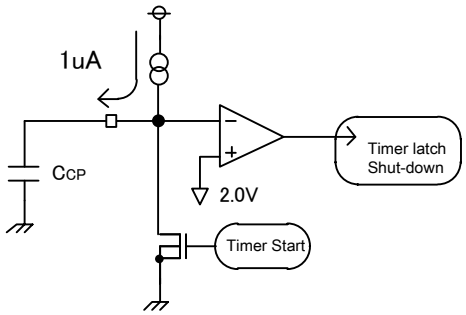


Figure. 19 CP Block Diagram

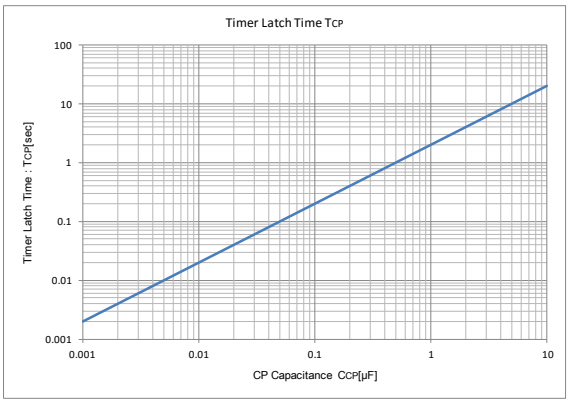


Figure. 20 Timer Latch Time vs CP Capacitance

PIN.10 PWMIN

By inputting PWM pulse signal at PWMIN pin, it is possible to adjust burst brightness. (High level: over 2.0V, Low level: below 0.8V).

condition	LED condition
PWMIN : 2.0V to 5.0V	Turn On
PWMIN : -0.3V to 0.8V	Turn Off

PIN.11 SDON

This is for the set up of time till COMPSD starts operation when start up. After STB starts to become ON, there will be 1μA constant current charging at external capacitor that is connected to SDON pin. Then if it becomes over 2.0V, it is possible to detect COMPSD. When it is below 2.0V, immediately latch protection current will no operate. External capacitor is around 0.01μF to 2.2μF.

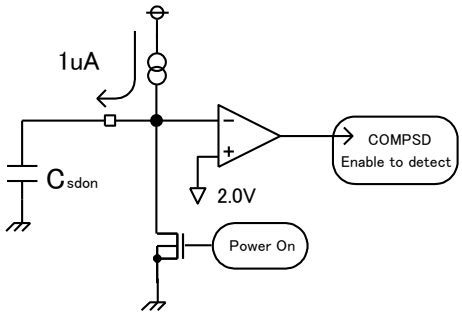
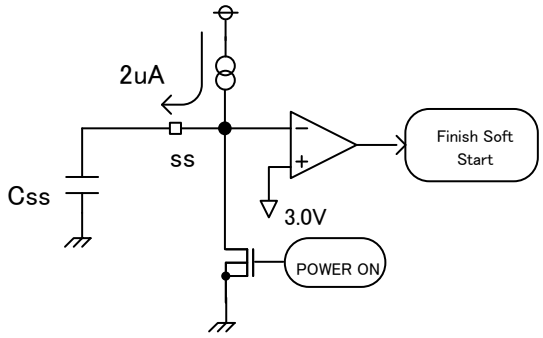


Figure. 21 IS SDON block diagram

$$T_{SDON} = C_{SDON} \times \frac{V_{SDON}}{I_{SDON}} = \frac{C_{SDON} \times 2.0}{1.0 \times 10^{-6}} = 2.0 \times 10^{6} \times C_{SDON} \quad [\text{sec}]$$

PIN.12 SS

This is soft start time and SDON time set up pin. Constant current 2.0μA(Typ) is charged to external capacitor (0.01μF to 0.1μF). When soft start is under operation (SS pin voltage is less than 3.0V), timer latch protection circuit by CP charge will not operate.



Where:
C_{SS} is the capacitance of SS pin

Figure. 22 SS Block Diagram

$$T_{SSEND} = C_{SS} \times \frac{V_{SSEND}}{I_{SS}} = \frac{C_{SS} \times 3.0}{2.0 \times 10^{-6}} = 1.5 \times 10^{6} \times C_{SS} \quad [\text{sec}]$$

PIN.13 FAIL

This is fail signal output pin of IC. At normal situation, it outputs GND Level and it becomes Open after timer latch in case any abnormality is detected. The pull up voltage during Open must be set less than rated voltage 5.5V of FAIL pin. Please connect about 0.1uF capacitor for noise reduction to FAIL pin.

Condition	FAILOutput
Normal operation	GND Level
Abnormal operation	Open

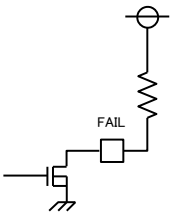


Figure. 23 FAIL Block Diagram

PIN.14 COMPSD

This is input pin for shut down detection comparator. When SDON pin voltage is over 2.0V(Typ) and COMPSD is 4.0V(Typ), it will latch after the next clock.

PIN.15 COMP

This is input pin for over voltage protection comparator. The detection voltage of comparator is 4.0V(Typ) and will start charging to CP pin after over voltage detection. After CP is charged, it will shut down by timer latch.

PIN.16 PGND

This is Power GND pin for output pin N1, N2 at driver part. Please make it independent from GND (Pin 3) pin on inverter PCB. This pin is not connected to GND pin in IC inside.

PIN.17 N2

This is gate drive output pin for Low Side external Nch FET. Normally please connect it to FET gate through about 10Ω resistor. It is for noise reduction. Gate has to be pull-down to source by resistor of 1kΩ to 10kΩ.

PIN.18 N1

This is gate drive output pin for Low Side external Nch FET. Normally please connect it to FET gate through about 10Ω resistor. It is for noise reduction. Gate has to be pull-down to source by resistor of 1kΩ to 10kΩ.

Detection Condition List of the Protection Functions (Typ Condition)

Protect Function	Detection Pin	Detect Condition		Release Condition	Timer Operation	Protection Type
		Detection Condition	SS,SDON			
LED OPEN	IS	IS < 0.625V	SDON>2.0V	IS > 0.625V	2CLK	Latch off
OVP	VS	VS > 1.25V	SS>3.0V	VS < 1.25V	CP	Latch off
COMP	COMP	COMP > 4.0V	SS>3.0V	COMP < 3.8V	CP	Latch off
VCC UVLO	VCC	VCC < 6.0V	-	VCC > 6.5V	-	Restart by release
COMPSD	COMPSD	COMPSD > 4.0V	SDON>2.0V	COMPSD < 3.8V	2CLK	Latch off

To reset the latch type protection, please set STB logic to 'L' once. Otherwise the detection of VCCUVLO is required. The count number in the list is calculated with double of output frequency.

Behavior List of the Protect Function

Protect Function	Operation of the Protect Function		
	N1,N2 Output	SS pin	FAIL pin
LED OPEN	Stop after latch	Low after latch	High after latch
OVP	Stop after latch	Low after latch	High after latch
COMP	Stop after latch	Low after latch	High after latch
VCC UVLO	Stop immediately	Low Immediately	High Immediately
COMPSD	Stop after latch	Low after latch	High after latch

Application Example

Introduce an application example with BD92111F

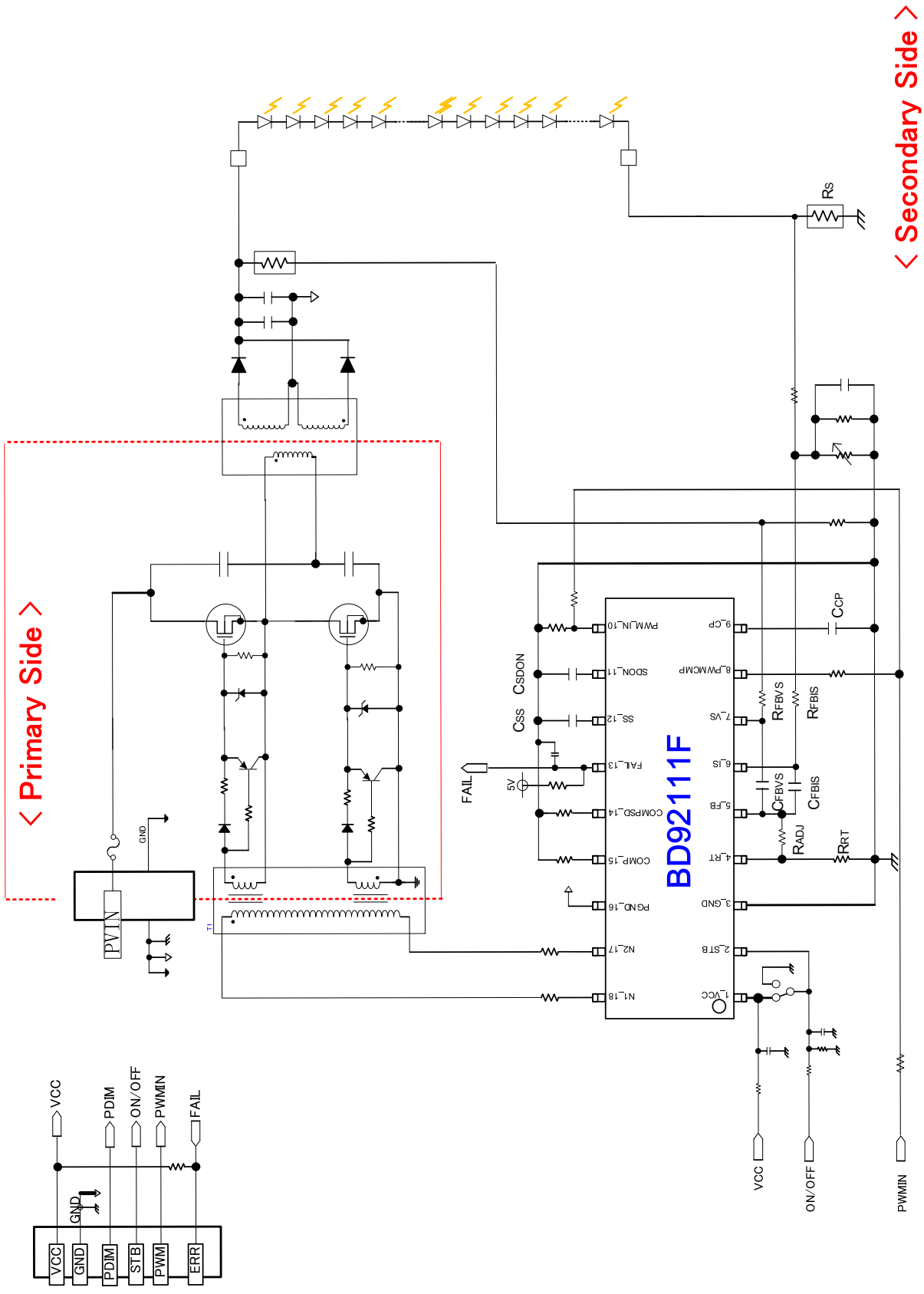


Figure. 24 Application Example

Timing Chart

When it Detects Quick Detection Type Error

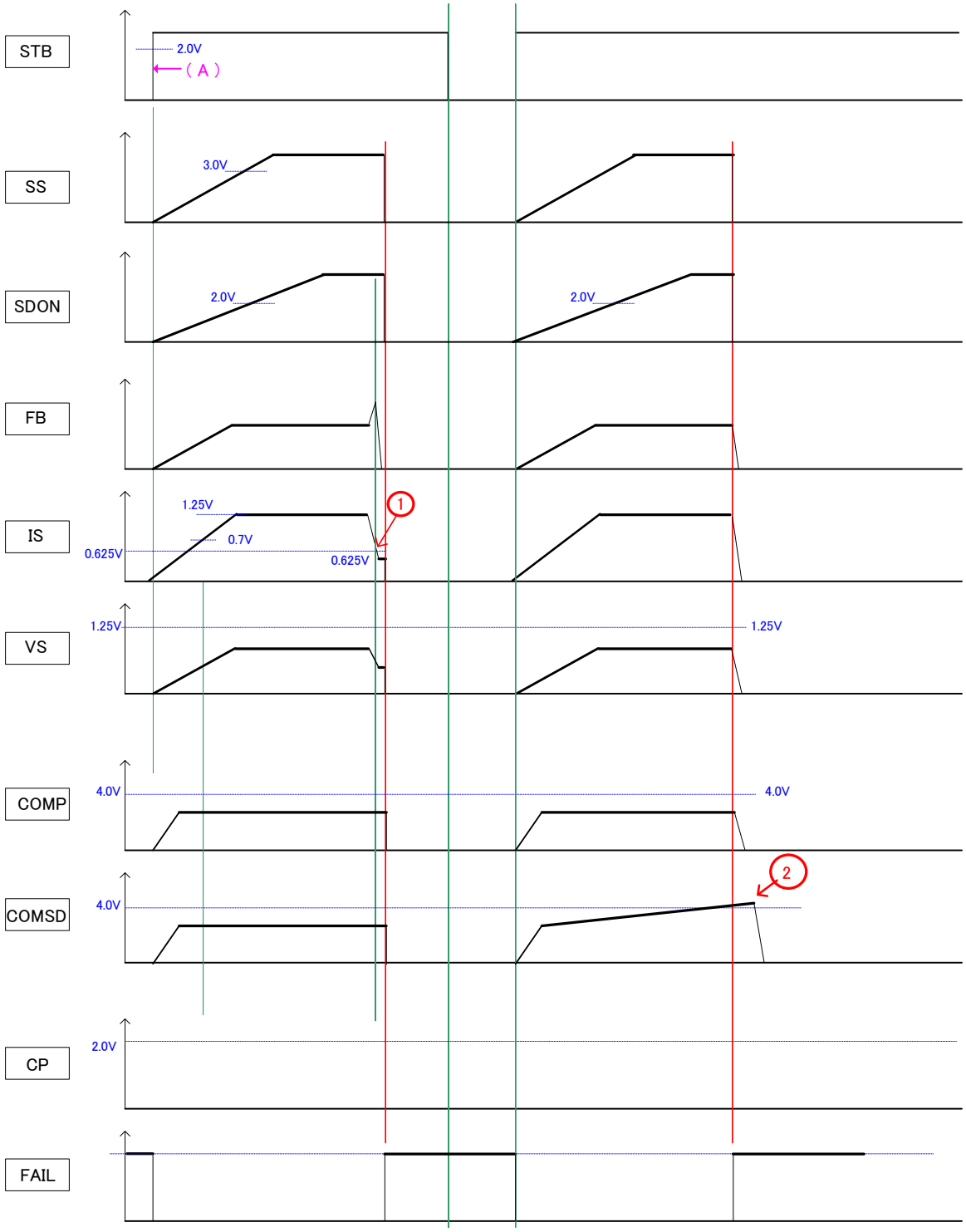


Figure. 25 Timing Chart 1

[The explanation of quick abnormal detection]

Due to the timing of ① to② in the above chart, the IC detects malfunction and starts the output-mute latch without CP Charge . For ① to②, the malfunction is detected according to the conditions in the table shown below.

No.	Content of Abnormal Detection	Condition of Abnormal Detection
①	Abnormal LED current detection	IS<0.625V
②	COMPSD Over Voltage detection	COMPSD≥ 4.0V

When it Detects Timer Latch Type Error

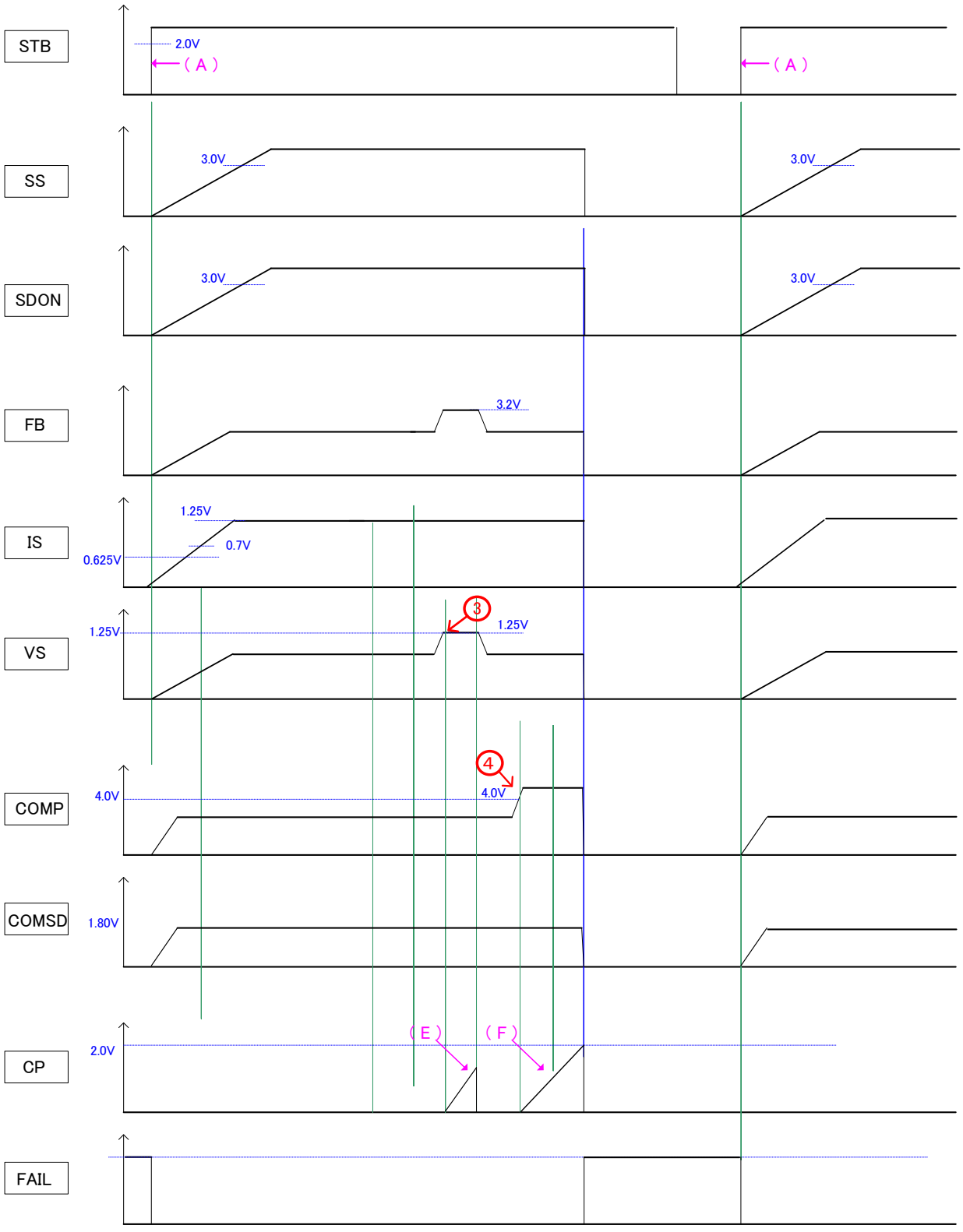


Figure. 26 Timing Chart 2

[The explanation of Time latch type error detection]

Due to the timing of③ and ④ in the above chart, the IC detects abnormal and starts the timer latch charging. For ③ and ④, the abnormal is detected according to the conditions in the table shown below.

No.	Content of Abnormal Detection	Condition of Abnormal Detection
③	Abnormal LED voltage detection	VS≥ 1.25V
④	Over voltage detection (multipurpose protection function)	COMP≥ 4.0V (release at COMP<3.8V)

Output Timing Chart

BD92111F outputs the signal that operates the Push-Pull or Half-Bridge which is made up of Nch FET. The output timing of drive signal is shown in the following chart

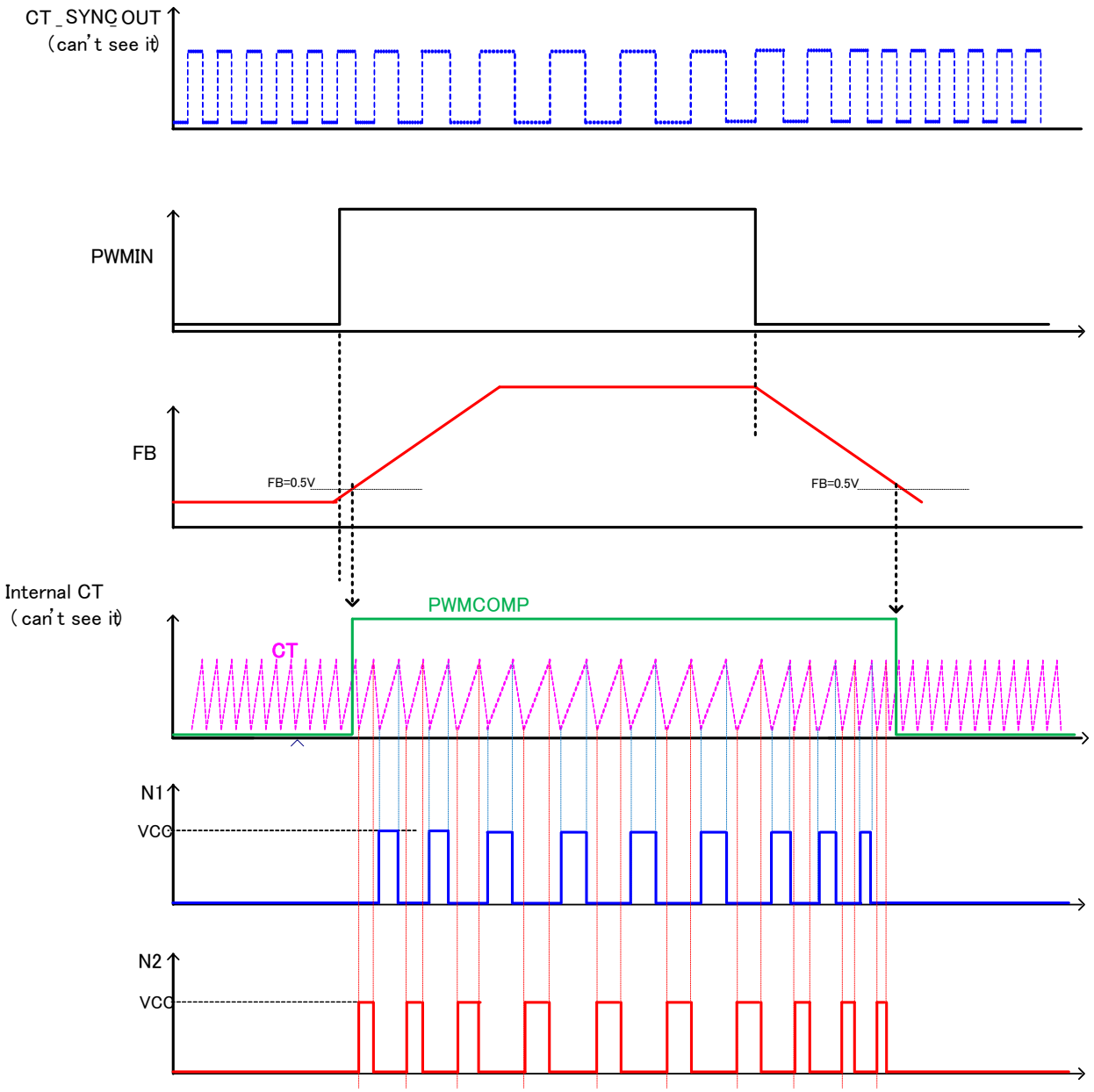


Figure. 27 Output Timing Chart

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

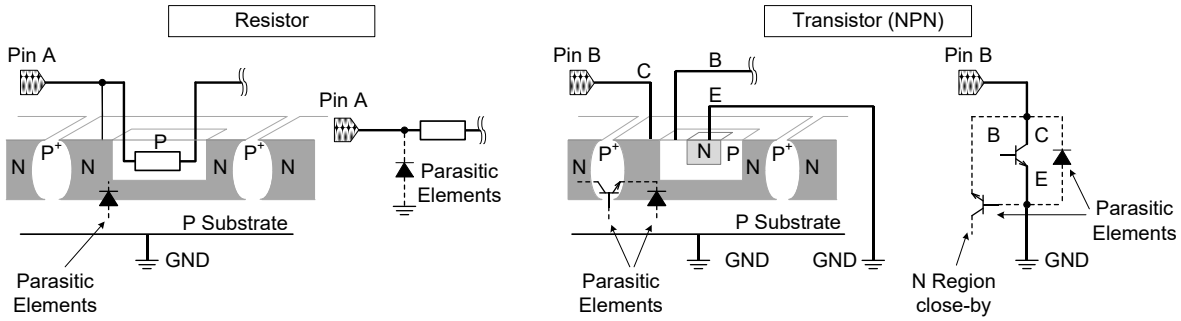


Figure xx. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

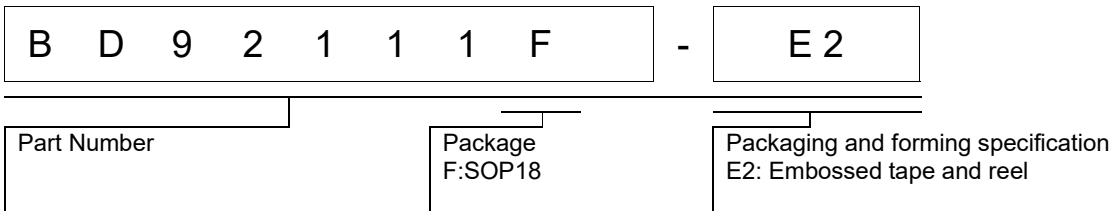
14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

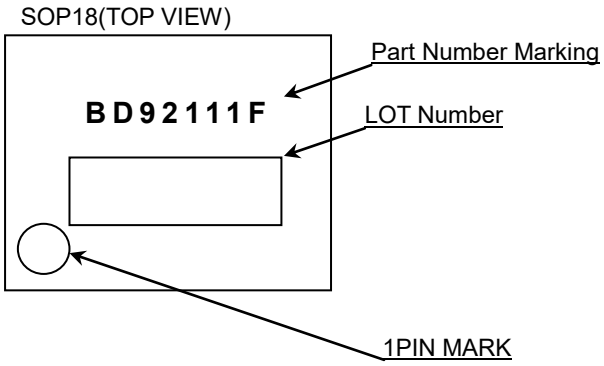
15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated over current protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

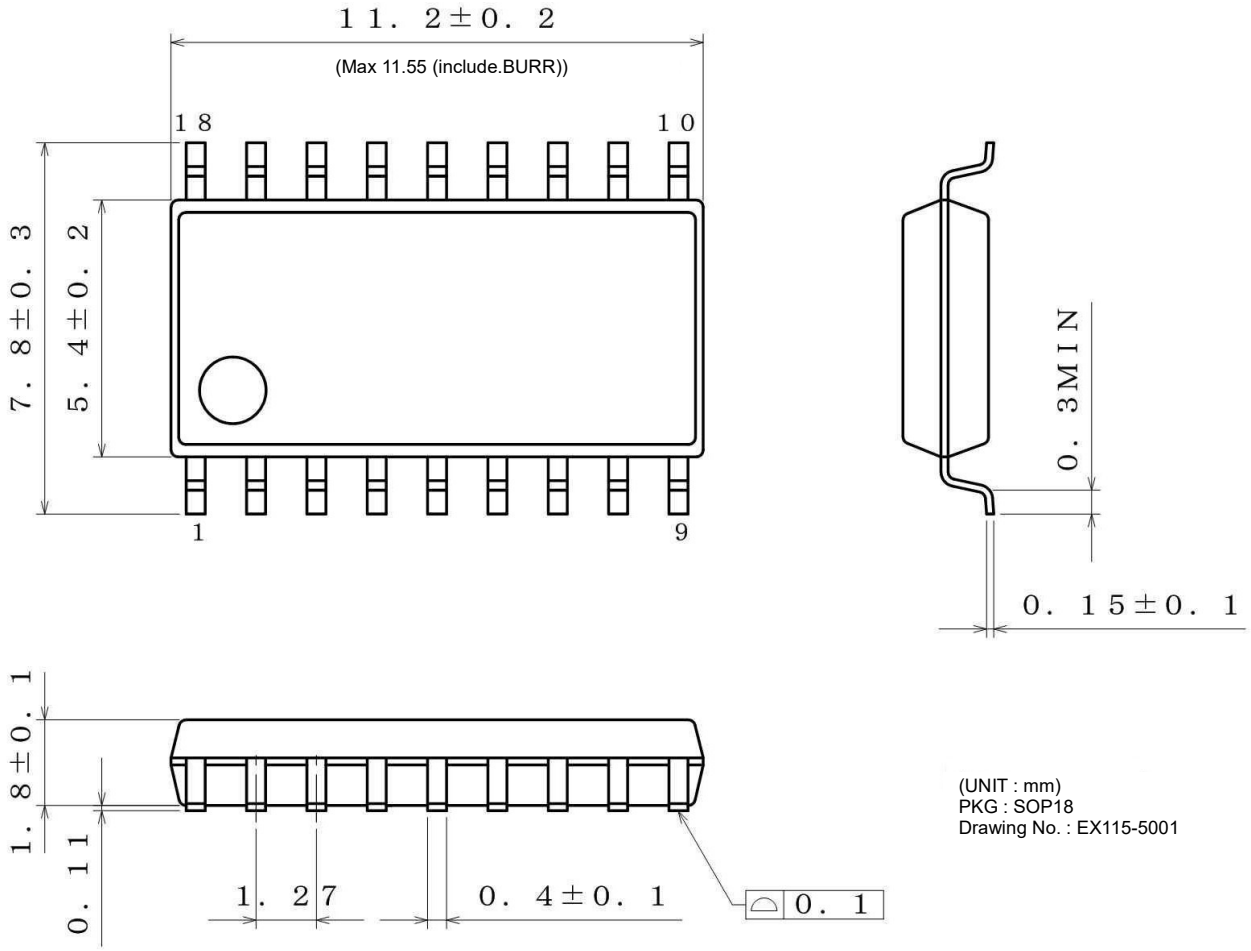


Marking Diagrams



Physical Dimension, Tape and Reel Information

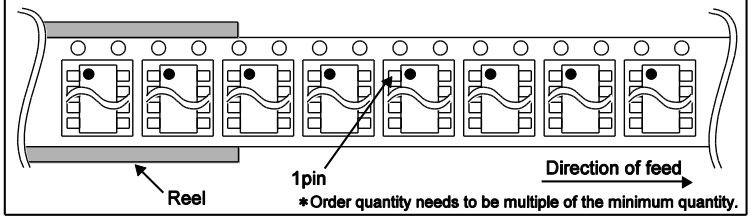
Package Name	SOP18



(UNIT : mm)
PKG : SOP18
Drawing No. : EX115-5001

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Revision No.	Date	Page	Changes
001	31.Jan.2016	All	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification