Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Large Current External FET Controller Type Switching Regulators

Single-output Step-up,High-efficiency Switching Regulator(Controller Type)

BD9306AFVM

Single-output Step-up,High-efficiency Switching Regulator(Controller Type)

BD9305AFVM   No.09028EAT04

●Description

BD9305AFVM / BD9306AFVM are 1-channel DC/DC converter controllers. Step-down DC/DC converter can be configured by BD9305AFVM, and Step-up DC/DC converter can be configured by BD9306AFVM. In addition, the master slave function, which is that the synchronization is possible at the time of multi-connection, is mounted.

●Features

1) 1ch PWM Control DC/DC Converter Controller
2) Input Voltage Range:4.2 to 18V
3) Feed Back Voltage:1.25±1.6%
4) Oscillating Frequency Variable:100 to 800kHz
5) Built-in Soft Start Function
6) Standby Current of 0 μA (Typ.)
7) Built-in Master / Slave Function
8) Protection Circuit : Under Voltage Lockout Protection Circuit
   Thermal Shutdown Circuit
   Short Protection Circuit of Timer Latch type
9) MSOP8 Package

●Applications

・TV, Power Supply for the TFT-LCD Panels used for LCD TVs, Back Lights
・DSC, DVC, Printer, DVD ,DVD Recorder, Generally Consumer Equipments etc.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Power supply voltage**	Vcc	20	V
Power dissipation	Pd	588*	mW
Operating temperature range	Topr	-40 to +85	℃
Storage temperature range	Tstg	-55 to +150	℃
Maximum junction temperature	Tjmax	150	℃

* Reduced by 4.7 mW/°C over 25°C, when mounted on a glass epoxy 4-layer board (70 mm × 70 mm × 1.6 mm)
** Must not exceed Pd.

●Recommended Operating Ranges (Ta=-40℃ to +85℃)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Power supply voltage	Vcc	4.2	12	18	V
Control Voltage	V_{ENB}	—	—	Vcc	V
Timing Capacity	CT	100	—	1000	pF
Timing Resistance	RT	5	—	50	kΩ
Oscillating frequency	Fosc	100	—	800	kHz

●**Electrical Characteristics** (Unless otherwise specified Ta=25℃,V$_{CC}$=12V,CT=200pF,RT=20kΩ)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
【Triangular Waveform Oscillator Block】						
Oscillating frequency	FOSC	165	220	275	kHz	Vcc=5V
Charge Threshold Voltage	VOSC⁺	0.80	0.85	0.90	V	
Discharge Threshold Voltage	VOSC⁻	0.20	0.25	0.30	V	
【Under-voltage lockout protection circuit】						
Threshold Voltage	VUT	3.5	—	4.2	V	
【Error amp Block】						
Feed Back Voltage	VFB	1.230	1.250	1.270	V	
Input Bias Current	IIB	—	0.05	1	µA	FB=1.5V
COMP Sink Current	IOI	35	50	65	µA	FB=1.5V COMP=1.25V
COMP Source Current	IOO	35	50	65	µA	FB=1.0V COMP=1.25V
【Gate Drive Block】						
ON Resistance	Ron	—	5	—	Ω	
Gate Drive Voltage L	VGDL	—	0	0.5	V	No Load
Gate Drive Voltage H	VGDH	Vcc-0.5	Vcc	—	V	No Load
MAX Duty (BD9305AFVM)	MDT	—	—	100	%	Vcc=5V
MAX Duty (BD9306AFVM)	MDT	—	83	—	%	Vcc=5V
【Control Block】						
ON Voltage	VON	2	—	—	V	
OFF Voltage	VOFF	—	—	0.3	V	
ENB Sink Current	IENB	40	60	90	µA	ENB=5V
【Soft Start Block】						
Soft Start Time	TS	—	10	—	ms	
【Timer Latch Protection Circuit】						
Latch Detection COMP Voltage	VLC	1.5	1.7	1.9	V	
Latch Delay OSC Count Number	CNT	—	2200	—	COUNT	
Latch Delay Time	DLY	—	10	—	ms	
【Overall】						
Standby Current	ISTB	—	0	10	µA	ENB=0FF
Average Consumption Current	ICC	1.0	1.5	2.5	mA	No Switching

*This product is not designed for protection against radio active rays.

●**Electrical Characteristics** (Unless otherwise specified,V_{CC}=12V, Ta=25℃)
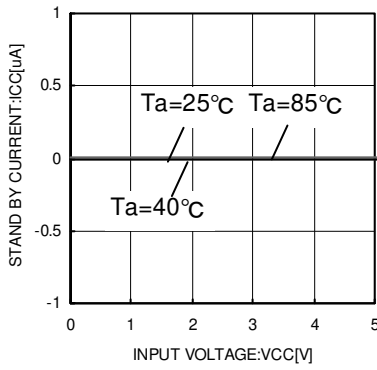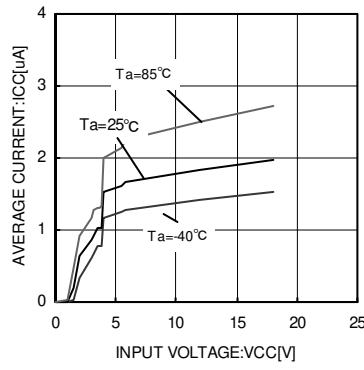
Fig.1 Standby Circuit Current
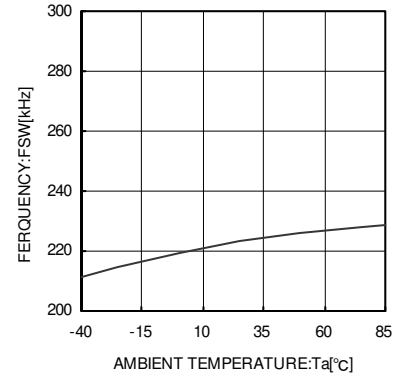
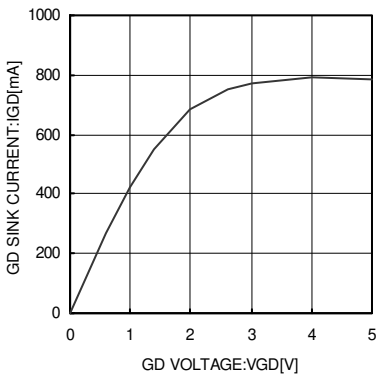Fig.2 Average Consumption Current
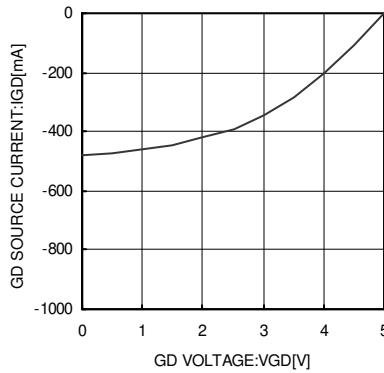
Fig.3 Frequency vs Temperature

Fig.4 GD Sink Current
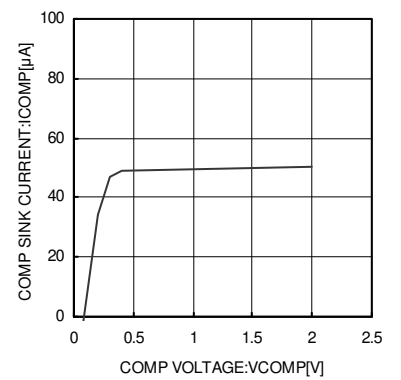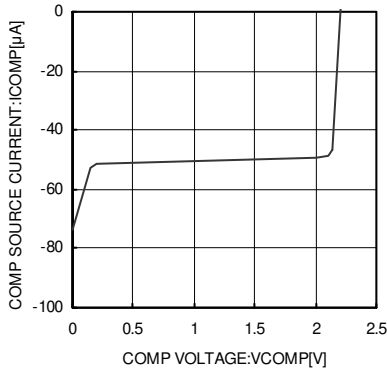
Fig.5 GD Source Current
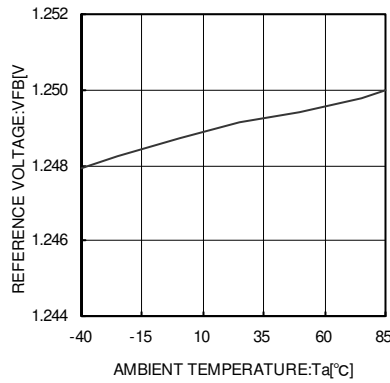
Fig.6 COMP Sink Current
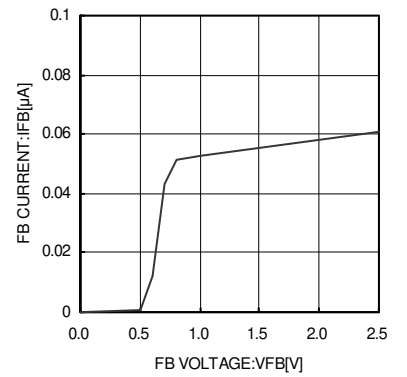
Fig.7 COMP Source Current

Fig.8 Feed Back vs Temperature

Fig.9 FB Input Bias Current

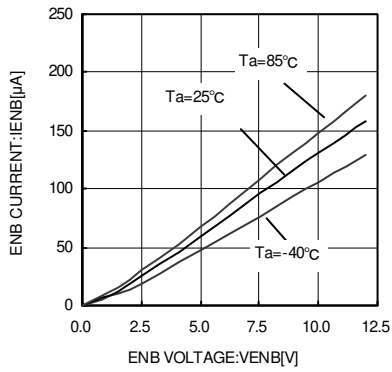●**Electrical Characteristics** (Unless otherwise specified,Ta=25℃)
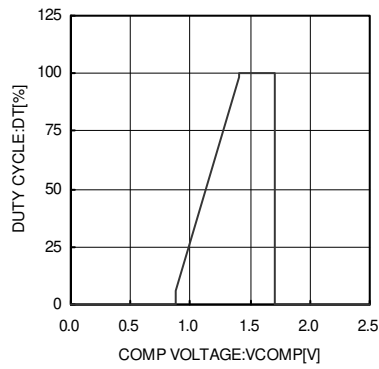

Fig.10 ENB Input Current

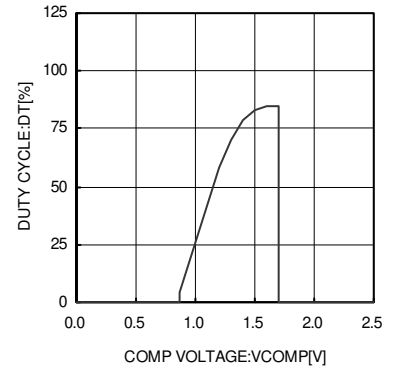

Fig.11 COMP vs DUTY
(BD9305AFVM)
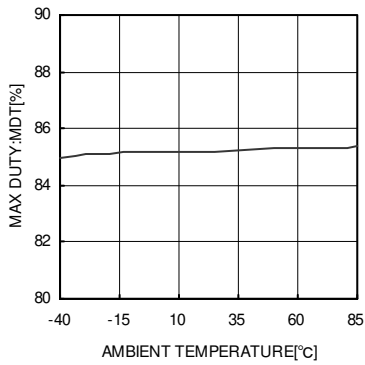

Fig.12 COMP vs DUTY
(BD9306AFVM)

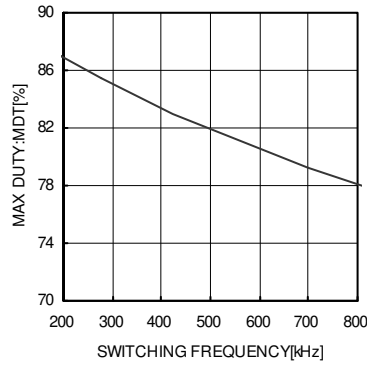Fig.13 Temperature vs MAX Duty
(BD9306AFVM)

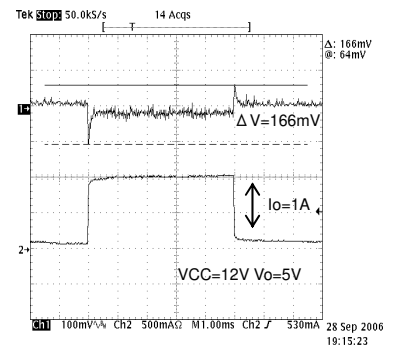Fig.14 Frequency vs MAX Duty
(BD9306AFVM)

Fig.15 Load Response
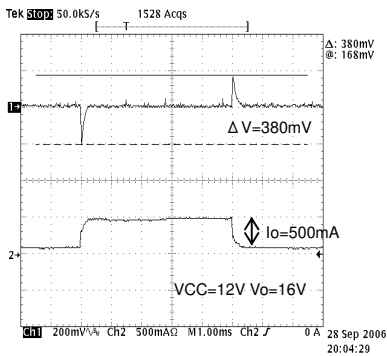(BD9305AFVM)

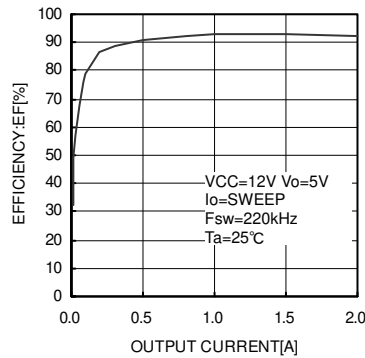Fig.16 Load Response
(BD9306AFVM)

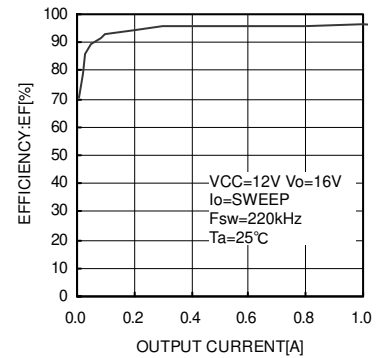
Fig.17 Efficiency Characteristics
(BD9305AFVM)

Fig.18 Efficiency Characteristics
(BD9306AFVM)

●**Block Diagram**
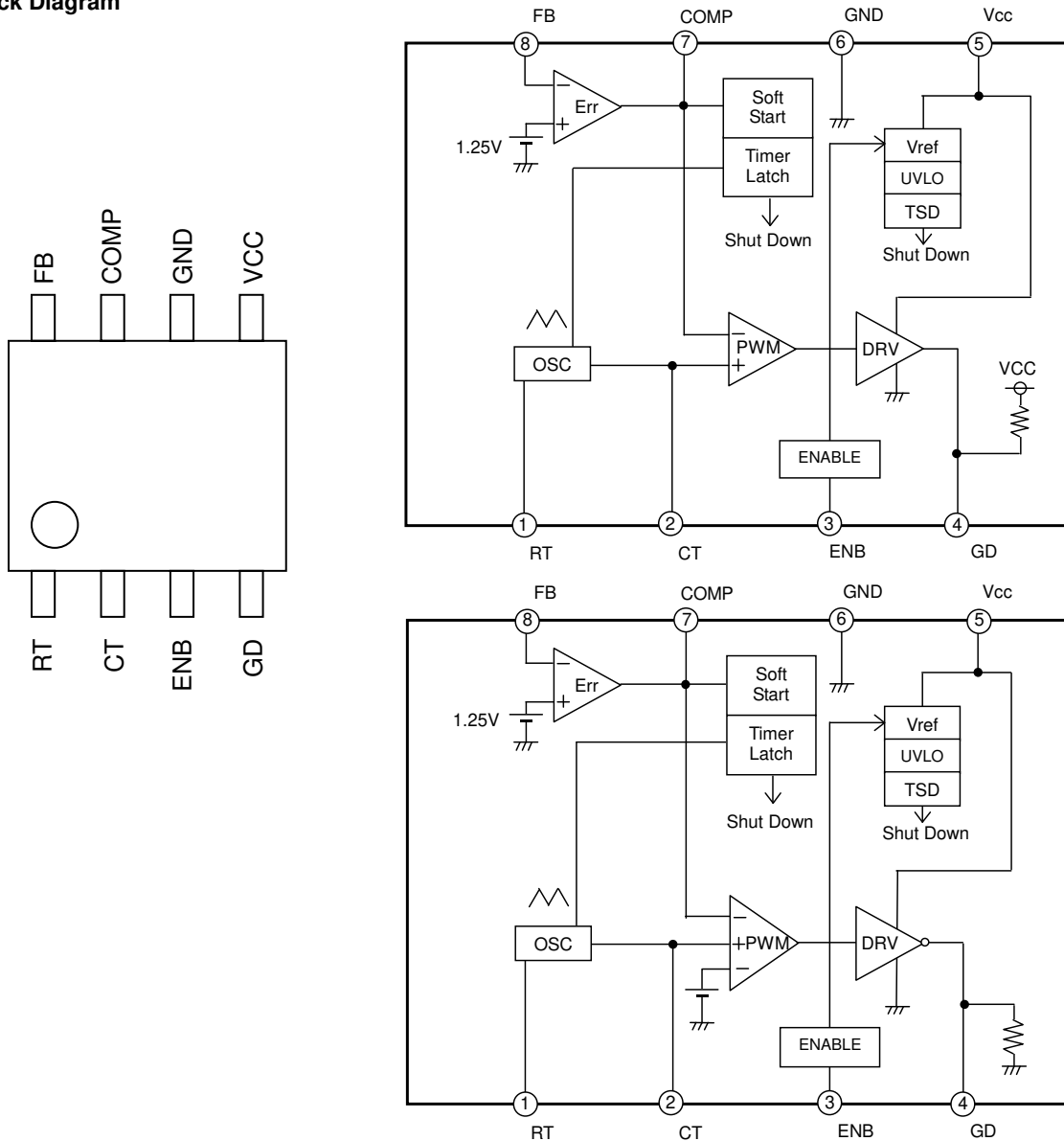
Fig19. Pin Assignment Diagram & Block Diagram (Above:BD9305AFVM / Below:BD9306AFVM)

●**Pin Assignment and Pin Function**

Pin No	Pin Name	Function
1	RT	Timing Resistance connection Pin
2	CT	Timing Capacity connection Pin
3	ENB	Control Pin
4	GD	Gate Drive Output Pin
5	Vcc	Power Supply Pin
6	GND	Ground pin
7	COMP	Error amp output Pin
8	FB	Error amp inversion input Pin

●**Block Diagram / Application Circuit**

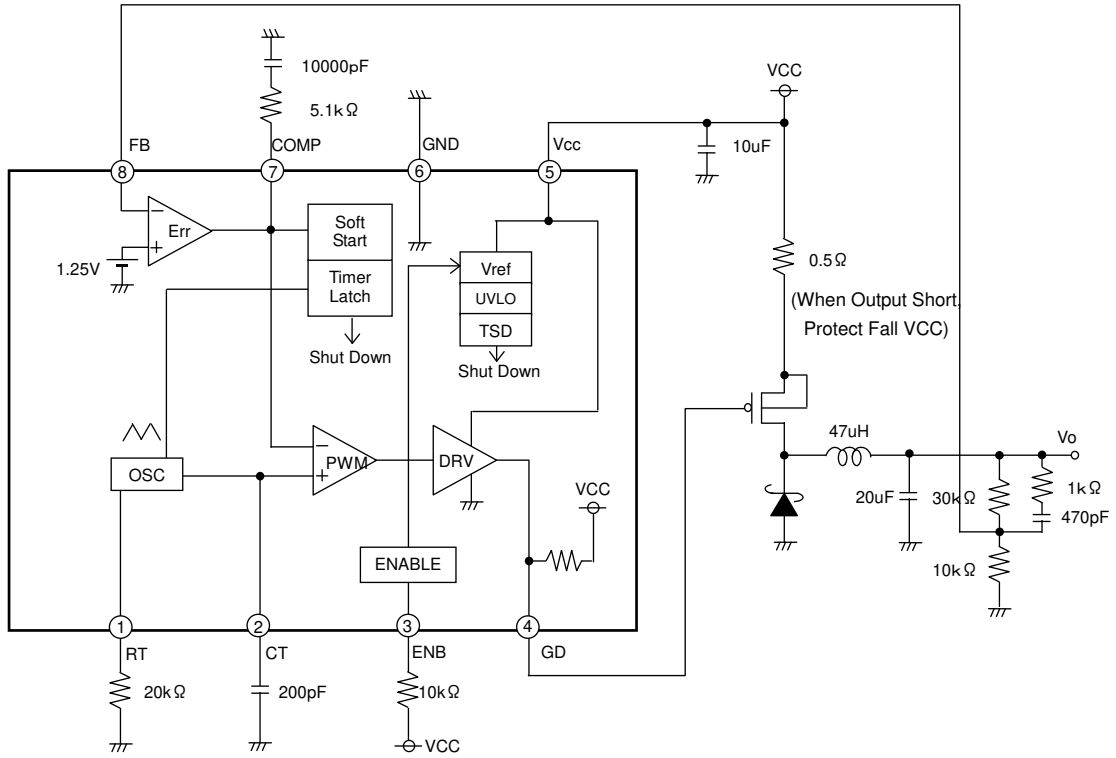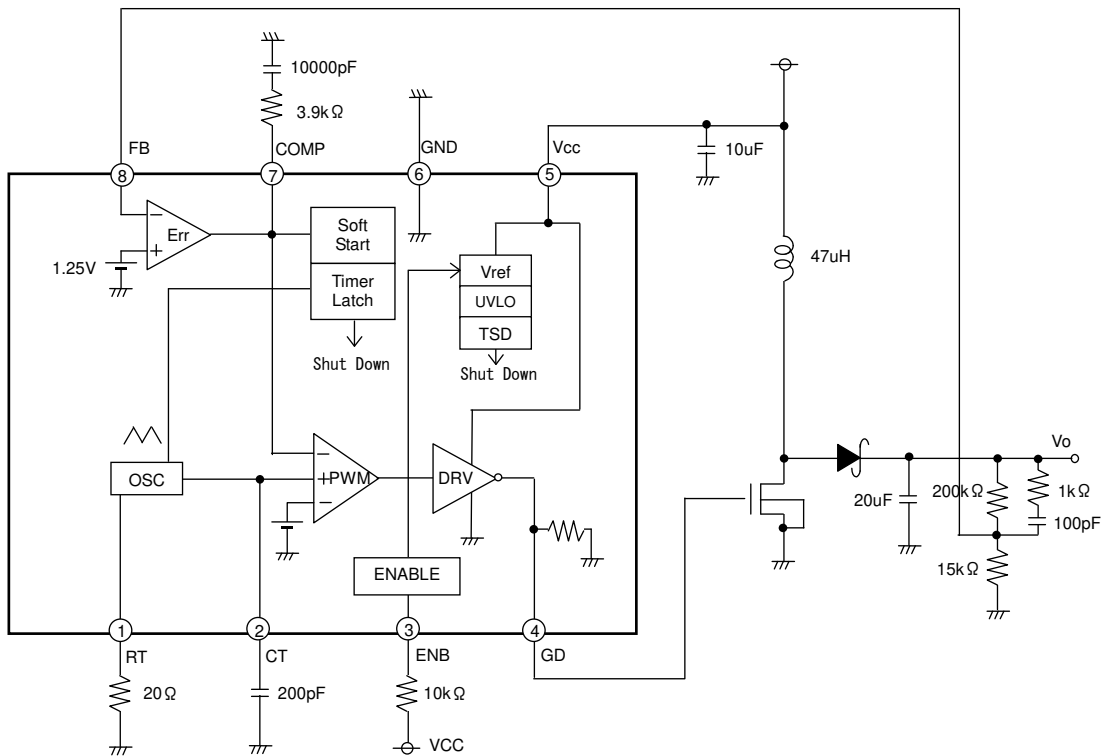Fig.20 Block Diagram / Application Circuit (BD9305AFVM)

Fig.21 Block Diagram / Application Circuit (BD9306AFVM)

●Block Operation

・Error amplifier (Err)
It is a circuit that compares the standard voltage of 1.25V (TYP) and the feedback voltage of output voltage.
The switching Duty is determined by the COMP terminal voltage of this comparison result.

・Oscillator (OSC)
It is a block, in which the switching frequency is determined by RT and CT, and the triangular wave is determined by RT and CT.

・PWM
The Duty is determined by comparing the output of Error amplifier and the angular wave of Oscillator.
The switching Duty of BD9306AFVM is limited by the maximum duty ratio that is determined by the internal part, and will not be up to 100%.

・DRV
The gate of the power FET that is connected to the outside is driven by the switching Duty determined by PWM.

・VREF
It is a block that outputs the internal standard voltage of 2.5V (TYP).
The internal circuit is entirely the bearer of this standard voltage that is turned ON / OFF by the ENB terminal.

・Protection circuits (UVLO / TSD)
UVLO (low-voltage Lock Out circuit) shuts down the circuits when the voltage is below 3.5V (MIN).
Moreover, TSD (temperature protection circuit) shuts down the IC when the temperature reaches 175℃(TYP).

・Soft Start Circuit
The Soft Start Circuit limits the current at the time of startup while ramping up the output voltage slowly.
The overshoot of output voltage and the plunging current can be prevented.

・Timer Latch
It is an output short protection circuit that detects the output short if the output of error amplifier (COMP voltage) is more than 1.7V (TYP). If the COMP voltage becomes more than 1.7V, the counter begins to operate, the LATCH is locked when the counter counts to 2200, and the GD output shuts down. (＊the frequency of counter is determined by RT and CT.)
Once the LATCH is locked, the GD output does not operate until it is restarted by ENB or VCC. If the output short is removed while the Timer latch is counting, the counter is reset.

●Selecting Application Components

(1) Setting the output L constant (Step Down DC/DC)
The inductance L to use for output is decided by the rated current ILR and input current maximum value IOMAX of the inductance.
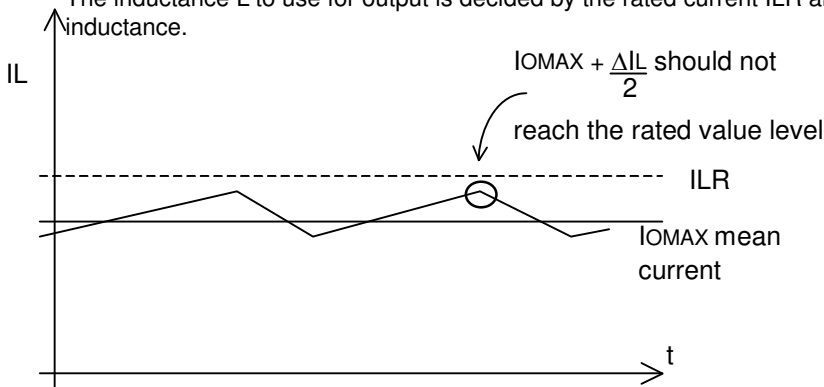

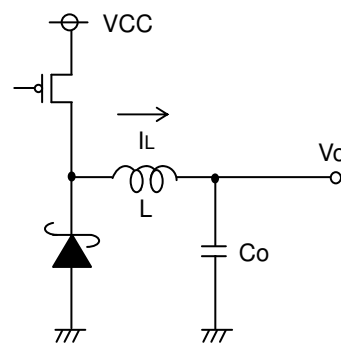Fig.22 Coil Current Waveform (Step Down DC/DC)   Fig.23 Output Application Circuit (Step Down DC/DC)

Adjust so that $I_{OMAX} + \Delta I_L / 2$ does not reach the rated current value I_{LR}.
At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (Vcc-Vo) \times \frac{Vo}{Vcc} \times \frac{1}{f} \ [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.
If the coil current exceeds the rating current I_{LR} of the coil, it may damage the IC internal element.

(2) Setting the output L constant (Step Up DC/DC)
The inductance L to use for output is decided by the rated current ILR and input current maximum value IINMAX of the inductance.

IINMAX+$\frac{\Delta IL}{2}$ should not reach the rated value level
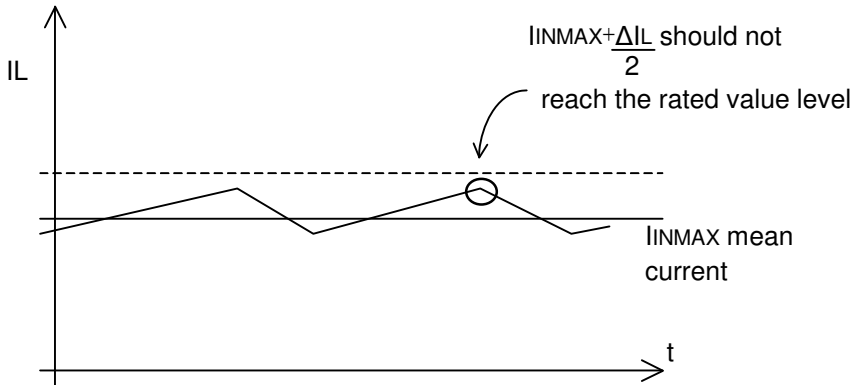
IINMAX mean current

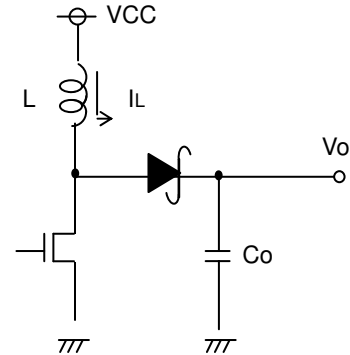Fig.24 Coil Current Waveform (Step Up DC/DC)   Fig.25 Output Application Circuit (Step Up DC/DC)

Adjust so that $I_{INMAX} + \Delta I_L / 2$ does not reach the rated current value I_{LR}.
At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} V_{CC} \times \frac{V_o - V_{CC}}{V_o} \times \frac{1}{f} \quad [A] \quad \text{Where, f is the switching frequency}$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.
If the coil current exceeds the rating current I_{LR} of the coil, it may damage the IC internal element.

(3) Setting the output capacitor
For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage VPP allowance value and the drop voltage allowance value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2C_o} \times \frac{V_o}{V_{CC}} \times \frac{1}{f} [V] \qquad \text{(Step Down DC/DC)}$$

$$\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{fC_o} \times \frac{V_{CC}}{V_o} \times \left(I_{LMAX} - \frac{\Delta I_L}{2} \right) \ [V] \qquad \text{(Step Up DC/DC)}$$

Perform setting so that the voltage is within the allowable ripple voltage range.
For the drop voltage during sudden load change; VDR, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{C_o} \times 10\mu \sec \quad [V]$$

However, 10 μs is the rough calculation value of the DC/DC response speed. Please set the capacitance considering the sufficient margin so that these two values are within the standard value range.

(4) Setting of feedback resistance constant
For both BD9305AFVM (step down) and BD9306AFVM (step up), please refer to the following formula for setting of feedback resistance.
We recommend 10kΩ~330kΩ as the setting range. If a resistance below 10kΩ is set, a drop in voltage efficiency will be caused; if a resistance more than 330kΩ is set, the offset voltage becomes large because of the internal error amplifier's input bias current of 0.05μA(Typ). Please set the maximum setting voltage of BD9306AFVM (step up) in such a way that Duty : (Vo - Vcc) / Vo is less than 70%.

$$V_o = \frac{R1 + R2}{R2} \times 1.25 \qquad [V]$$
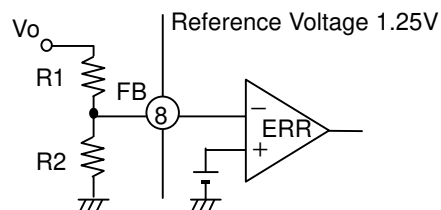

Reference Voltage 1.25V

Fig.26 Feedback Resistance Setting

(5) Setting of oscillation frequency

The angular wave oscillation frequency can be set by respectively connecting resistor and condenser to RT (1 pin) and CT (2 pins). The currents to charge and discharge the condenser of CT are determined by RT.

Please refer to the following drawing for setting the RT's resistor and the CT's condenser.

RT:5~50kΩ, CT:100~1000pF, and the frequency range of 100kHz~800kHz are recommended.

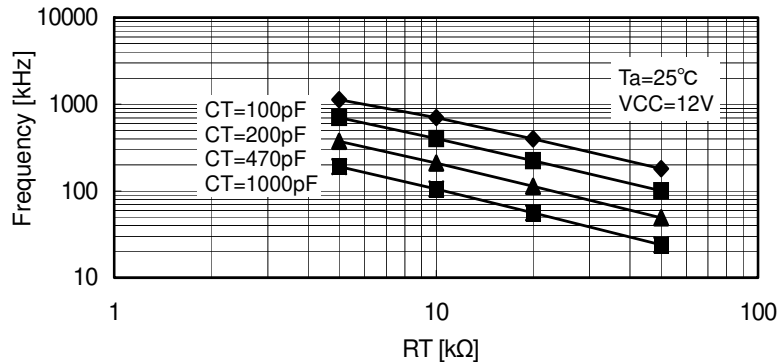Please pay attention to that, the switching will stop if your setting is off this range.

Fig.27 Frequency Setting

(6) Selection of input condenser

For DC/DC converter, the condenser at the input side is also necessary because peak current is flowing between input and output. Therefore, we recommend the low ESR condenser with over 10μF and below 100mΩ as the input condenser. If a selected condenser is off this range, excessively large ripple voltage will overlaps with the input voltage, which may cause IC malfunction.However, this condition varies with negative overcurrent, input voltage, output voltage, inductor's value, and switching frequency, so please be sure to do the margin check with actual devices.

(7) Selection of output rectifier diode

We recommend the Schottky barrier diode as the diode for rectification at the output stage of DC/DC converter. Please be careful to choose the maximum inductor current, the maximum output voltage and the power supply voltage.

＜step-down DC/DC＞

| Maximum inductor current | $I_{OMAX} + \dfrac{\triangle I_L}{2}$ | < | Diode's rated current |

| Power supply voltage | VCC | < | Diode's rated voltage |

＜step-up DC/DC＞

| Maximum inductor current | $I_{INMAX} + \dfrac{\triangle I_L}{2}$ | < | Diode's rated current |

| Maximum output voltage | V_{OMAX} | < | Diode's rated voltage |

Furthermore, each parameter has a deviation of 30%~40%, so please design in such a way that you have left a sufficient margin for deviation in your design.

(8) Setting of Power FET

If step-down DC/DC is configured by BD9305AFVM, Pch FET is necessary; if step-up DC/DC is configured by BD9306AFVM, Nch FET is necessary.

Please pay attention to the following conditions when you choose.

＜step-down DC/DC＞

| Maximum inductor current | $I_{OMAX} + \dfrac{\triangle I_L}{2}$ | < | FET's rated current |

| Power supply voltage | VCC | < | FET's rated voltage |

| Power supply voltage | VCC | > | FET's gate ON voltage |
| Gate capacity (※) | C_{GATE} | < | 2000pF |

＜step-up DC/DC＞

| Maximum inductor current | $I_{INMAX} + \dfrac{\triangle I_L}{2}$ | < | FET's rated current |

| Maximum output voltage | V_{OMAX} | < | FET's rated voltage |
| Power supply voltage | VCC | > | FET's gate ON voltage |

| Gate capacity (※) | C_{GATE} | < | 2000pF |

Furthermore, each parameter has a deviation of 30%~40%, so please design in such a way that you have left a sufficient margin for deviation in your design.

(※) If Gate capacity becomes large, the switch's switching speed gets slow, which may cause generation of heat and breakdown, so please check thoroughly with actual devices.

(9) Phase compensation
Phase Setting Method
The following conditions are required in order to ensure the stability of the negative feedback circuit.
• Phase lag should be 150° or lower during gain 1 (0 dB) (phase margin of 30° or higher).
Because DC/DC converter applications are sampled using the switching frequency, the overall GBW should be set to 1/10 the switching frequency or lower. The target application characteristics can be summarized as follows:
• Phase lag should be 150° or lower during gain 1 (0 dB) (phase margin of 30° or higher).
• The GBW at that time (i.e., the frequency of a 0-dB gain) is 1/10 of the switching frequency or below.
In other words, because the response is determined by the GBW limitation, it is necessary to use higher switching frequencies to raise response.

One way to maintain stability through phase compensation involves canceling the secondary phase lag (-180°) caused by LC resonance with a secondary phase advance (by inserting 2 phase advances).
The GBW (i.e., the frequency with the gain set to 1) is determined by the phase compensation capacitance connected to the error amp. Increase the capacitance if a GBW reduction is required.

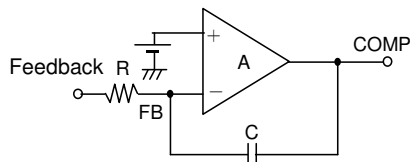(a) Standard integrator (low-pass filter)   (b) Open loop characteristics of integrator
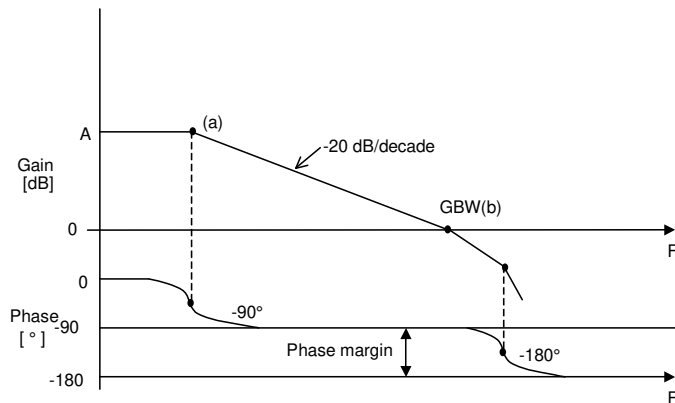

Fig. 28

Point (a) $fa = \dfrac{1}{2\pi RCA}$ [Hz]

Fig. 29

Point (b) $fb = GBW = \dfrac{1}{2\pi RC}$ [Hz]

The error amp performs phase compensation of types (a) and (b), making it act as a low-pass filter.
For DC/DC converter applications, R refers to feedback resistors connected in parallel.
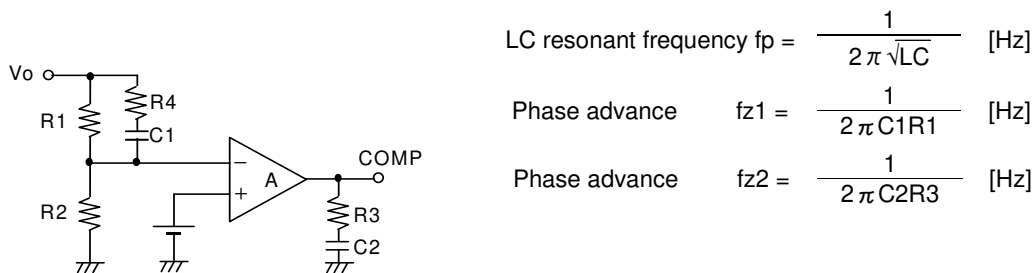From the LC resonance of output, the number of phase advances to be inserted is two.

Fig. 30

LC resonant frequency $fp = \dfrac{1}{2\pi\sqrt{LC}}$ [Hz]

Phase advance $fz1 = \dfrac{1}{2\pi C1R1}$ [Hz]

Phase advance $fz2 = \dfrac{1}{2\pi C2R3}$ [Hz]

Set a phase advancing frequency close to the LC resonant frequency for the purpose of canceling the LC resonance.

(※)If high-frequency noise is generated in the output, FB is affected through condenser C1.
Therefore, please insert the resistor R4=1kΩ or so, which is in series with condenser C1.

●**Example of application**

※We recommend the application circuit examples with confidence, but hope that you will thoroughly check the characteristics over again when putting them to use.

When you change the external circuit constant and use, please make a decision to leave a sufficient margin after taking into consideration the deviation etc. of external components and ROHM IC, in terms of not only the static characteristic but also the transient characteristic.

Moreover, please understand that our company can not confirm fully with regard to the patent right.

＜Master Slave Function＞

The master slave function, which is that the synchronous switching is possible by using these IC of BD9305AFVM / BD9306AFVM through their multi-connection, is mounted. The following drawing shows an example of connection circuit in which BD9305AFVM is connected on the master side and BD9306AFVM is connected on the slave side.
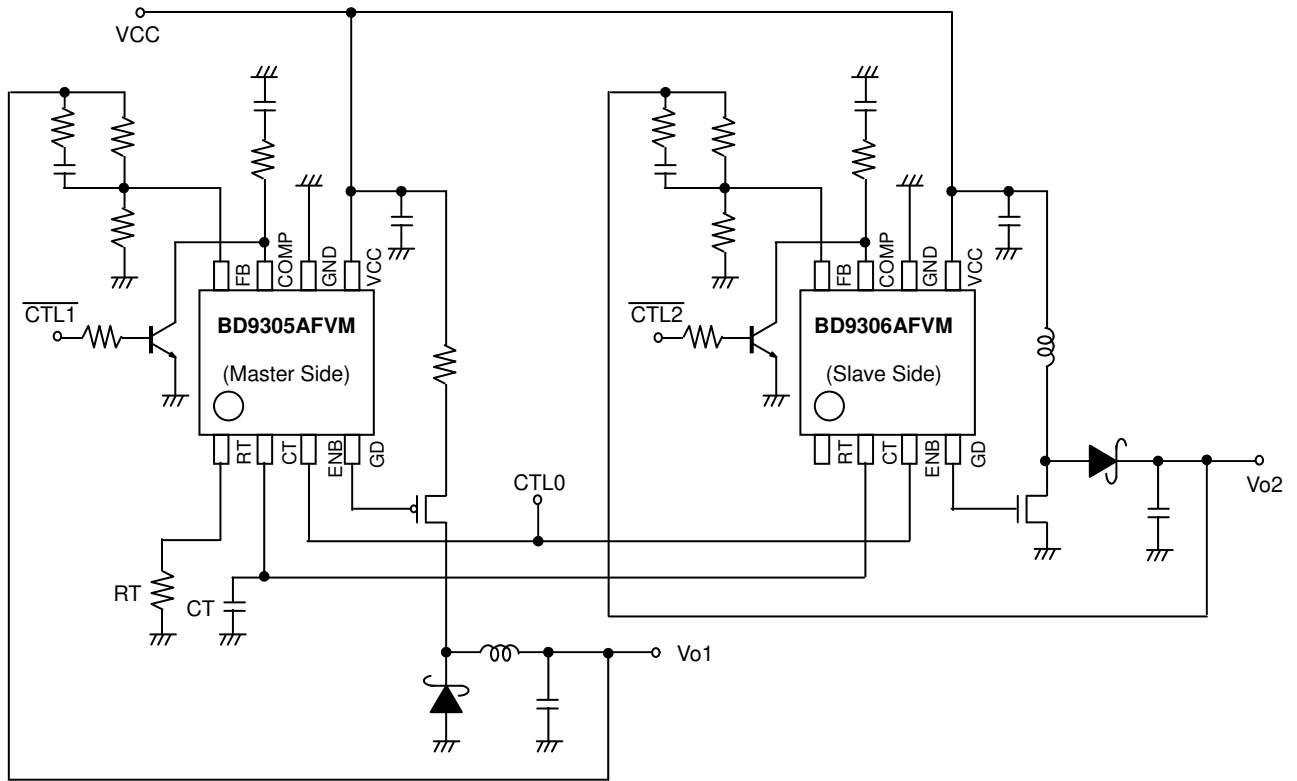
Fig.31 Master Slave Application Circuit

In the above-mentioned circuit, BD9306AFVM, which is synchronized with the switching frequency determined by RT and CT of BD9305AFVM that is the master, operates.In addition, the ON/OFF of output can be controlled by connecting the switch to the COMP terminal. (Refer to the following table)

Control signal correspondence table

Output state		Control signal		
Vo1	Vo2	CTL0	$\overline{CTL1}$	$\overline{CTL2}$
OFF	OFF	Low	*	*
OFF	ON	High	High	Low
ON	OFF	High	Low	High
ON	ON	High	Low	Low

＊The same in either case of High / Low.

Similarly in the case of connecting three or more than three, synchronization is possible by connecting the CT terminal of Master and the CT terminal of Slave
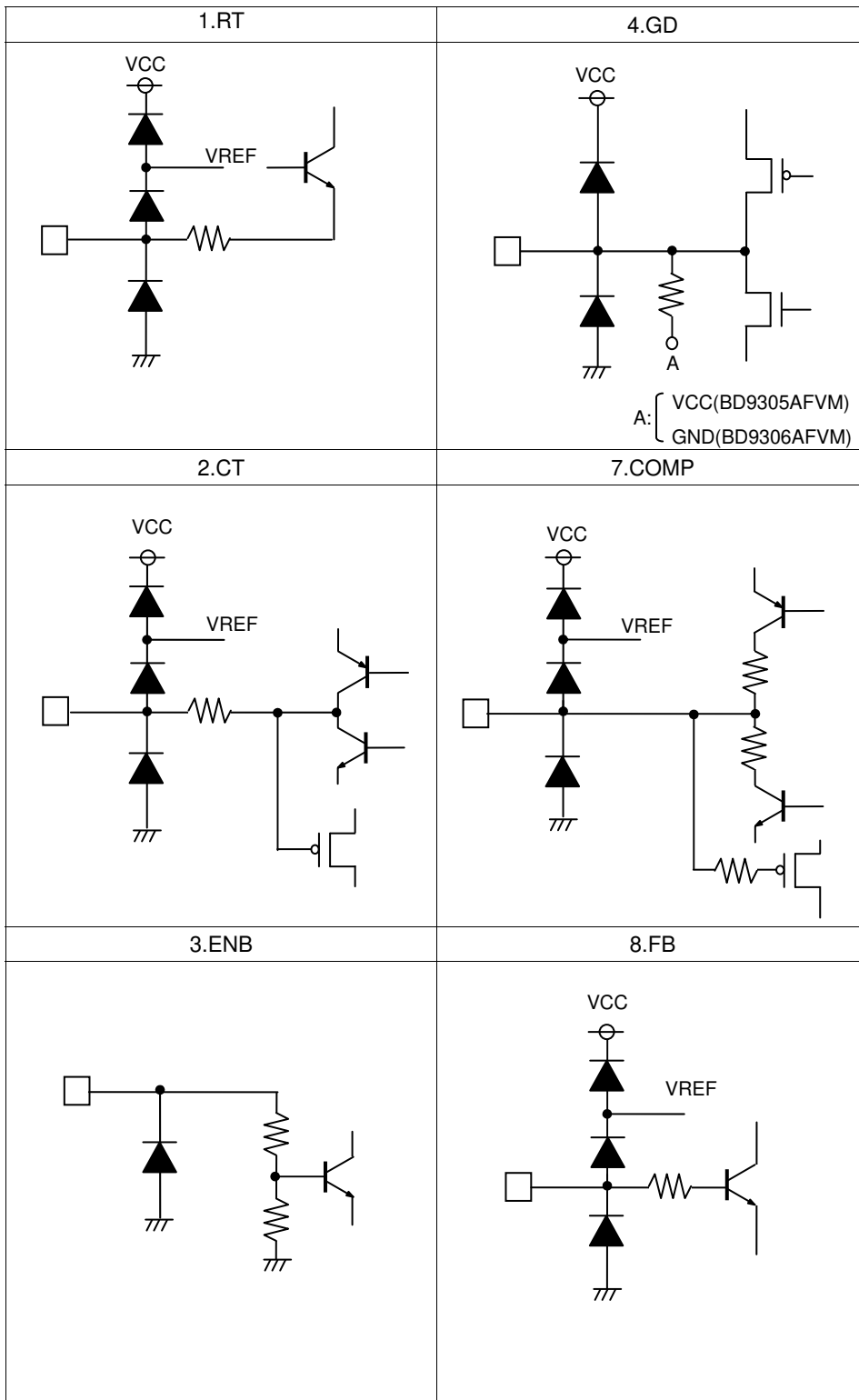
●**I/O Equivalent Circuit Diagram Fig.32**

Fig. 32

●**Notes for use**

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.For example, when the resistors and transistors are connected to the pins shown as follows, a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.
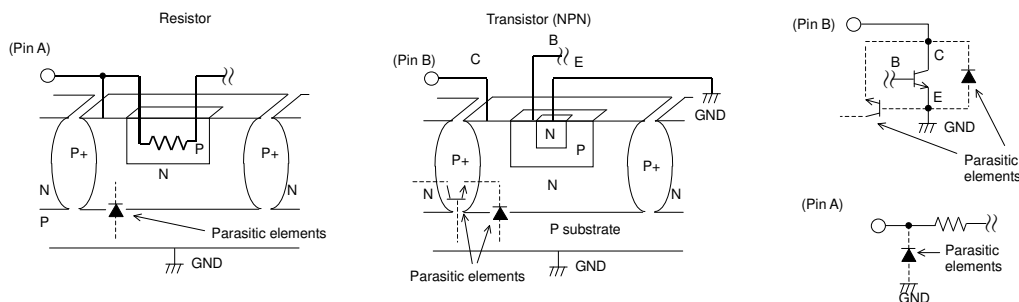
Example of a SimpleMonolithic IC Architecture
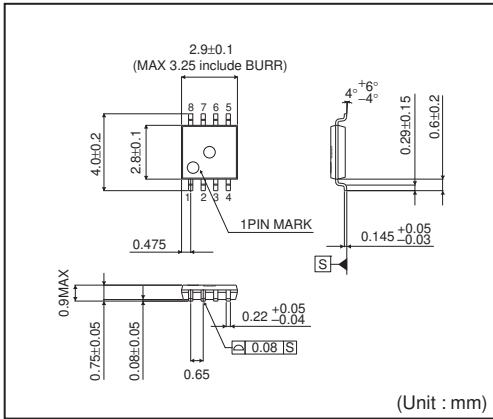

Fig. 33

9) Overcurrent protection circuits
An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

●**Ordering part number**

| B | D | | 9 | 3 | 0 | 6 | A | | F | V | M | - | T | R |

Part No.

Part No.
9306A
9305A

Package
FVM: MSOP8

Packaging and forming specification
TR: Embossed tape and reel

MSOP8

2.9±0.1
(MAX 3.25 include BURR)

4°⁺⁶°₋⁴°

0.29±0.15

0.6±0.2

4.0±0.2

2.8±0.1

1PIN MARK

0.475

0.145 ⁺⁰·⁰⁵₋₀.₀₃

S

0.9MAX

0.75±0.05

0.08±0.05

0.22 ⁺⁰·⁰⁵₋₀.₀₄

0.08 S

0.65

(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

1pin

Reel

Direction of feed

＊Order quantity needs to be multiple of the minimum quantity.

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

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