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LED Drivers for LCD Backlights

6ch boost LED driver which constant setting can be shared by I2C control

BD9423EFV

1.1 General Description

BD9423EFV is a high efficiency driver for white LEDs and designed for large LCD panel. This IC is built-in high current drive and high responsibility type 6ch LED drivers and 1ch boost DCDC converter. BD9423EFV has some protect function against fault conditions, such as the over-voltage protection (OVP), LED OPEN and SHORT protection, the over current limit protection of DCDC (OCP). Therefore BD9423EFV is available for the fail-safe design over a wide range output voltage.
Moreover the functions and the detection voltage can be controlled by the I2C. This enables for the constant setting of external parts to be shared by I2C control, nevertheless the different usage condition.

Features

- Operating power supply voltage range:9.0V to 35.0V
- Oscillator frequency: 200kHz (RT=100kΩ)
- Operating Current: 9mA (typ.)
- Operating temperature range: -40°C to +85°C

Applications

- TV, Computer Display, Notebook, LCD Backlighting

Key Specifications

- LED drivers Max curret 400mA per channel
- Constant current accuracy ±1.8% (IC only)
- Current analog (linear) dimming by ADIM pin
- Several protection functions
  DCDC part : OCP/OVP/UVLO
  LED driver part :OPEN,SHORT detection
- SHORT detection voltage is set by LSP pin
- Error detection output by FAIL pin
- Master/Slave mode inside

1.2 Package

	W(Typ) x D(Typ) x H(Max)
HTSSOP-B40:	13.60mm x 7.80mm x 1.00mm
Pin Pitch:	0.65mm

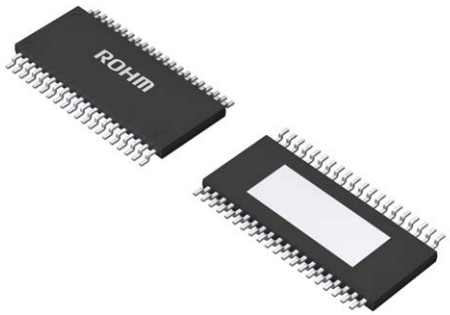


Figure 1. HTSSOP-B40

Typical Application Circuit

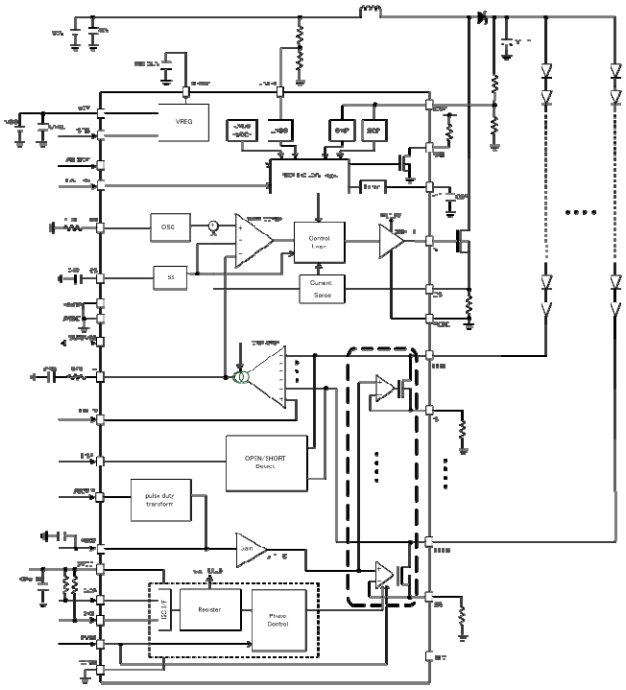


Figure 2. Typical application circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

1.3 Pin Configuration

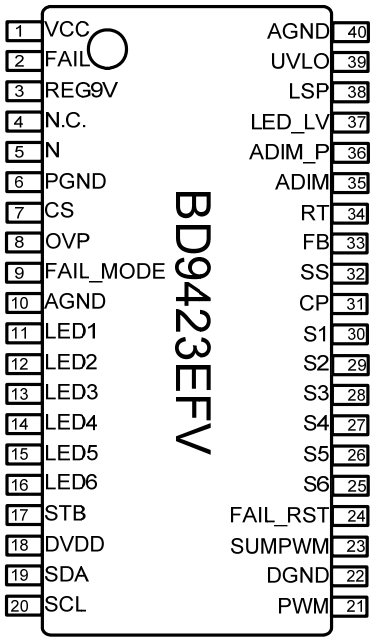


Figure 3. Pin Configuration

1.4 Pin Descriptions

No.	Name	Function	No.	Name	Function
1	VCC	Power supply pin	40	AGND	GND pin for analog part
2	FAIL	Abnormality detection output pin	39	UVLO	Low voltage malfunction detection pin
3	REG9V	9.0V regulator output pin	38	LSP	LED SHORT detection voltage setting pin
4	N.C.	-	37	LED_LV	LED feedback voltage setting pin
5	N	DC/DC switching output pin	36	ADIM_P	Pulse analog dimming signal input pin
6	PGND	Power GND pin	35	ADIM	Analog dimming DC voltage I/O pin
7	CS	DC/DC FET current detection pin	34	RT	Connecting pin for DC/DC frequency setting resistor
8	OVP	OVP detection pin	33	FB	Error AMP output pin
9	FAIL_MODE	FAIL function selection pin	32	SS	Connecting pin for soft start
10	AGND	GND pin for analog part	31	CP	setting capacitor
11	LED1	LED output 1	30	S1	Connecting pin for abnormality
12	LED2	LED output 2	29	S2	detection setting capacitor
13	LED3	LED output 3	28	S3	Connecting pin for LED1 constant current setting resistor
14	LED4	LED output 4	27	S4	Connecting pin for LED2 constant current setting resistor
15	LED5	LED output 5	26	S5	Connecting pin for LED3 constant current setting resistor
16	LED6	LED output 6	25	S6	Connecting pin for LED4 constant current setting resistor
17	STB	ON/OFF pin	24	FAIL_RST	Connecting pin for LED5 constant current setting resistor
18	DVDD	Power supply pin for I2C part and register	23	SUMPWM	Connecting pin for LED6 constant current setting resistor
19	SDA	I2C data pin	22	DGND	FAIL output reset pin
20	SCL	I2C Clock pin	21	PWM	Master/Slave setting input/output pin

1.5 Block Diagram

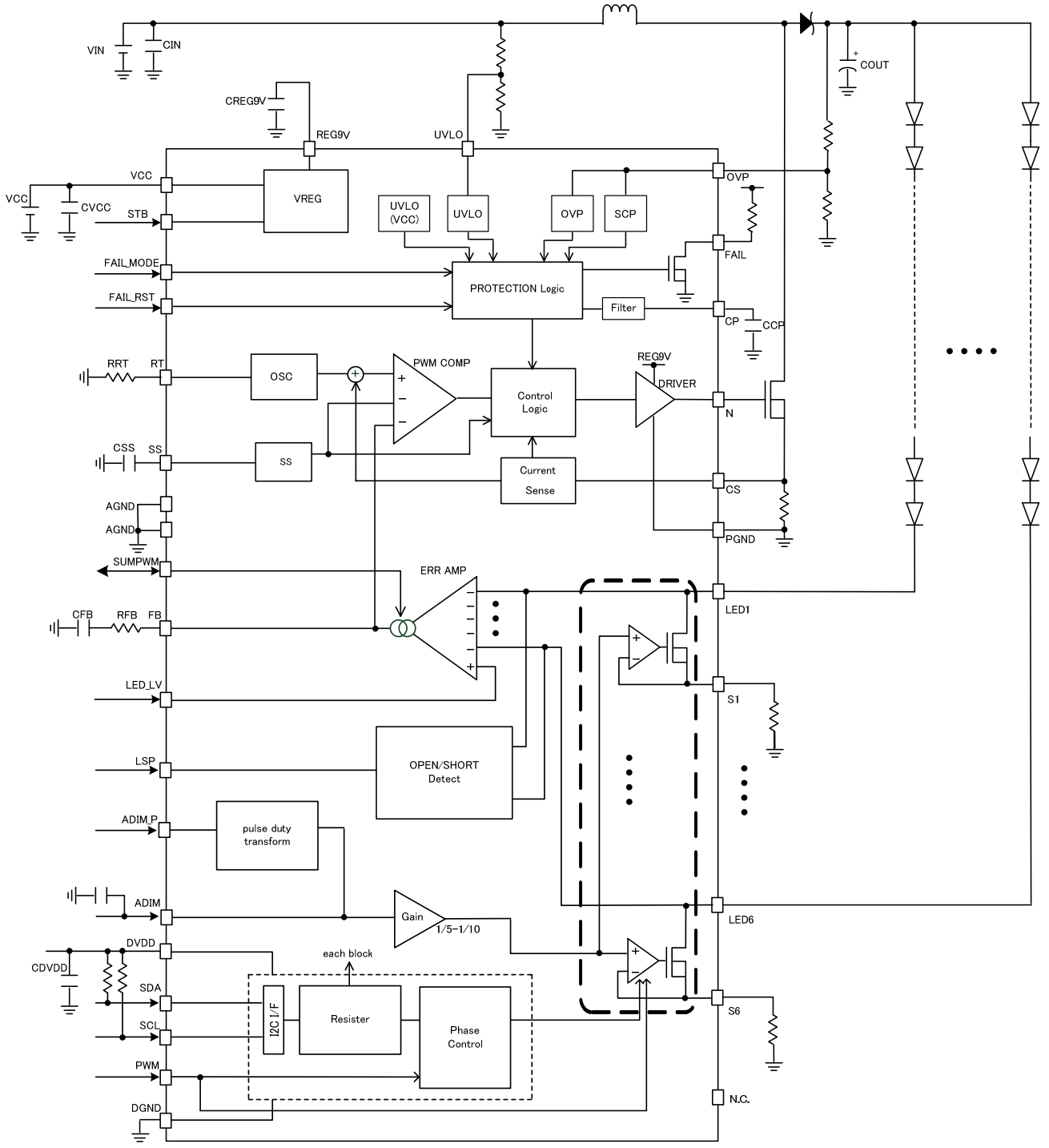


Figure 4. Block Diagram

1.6 Absolute maximum ratings(Ta = 25°C)

Parameter	Symbol	Rating	Unit
Power supply voltage	VCC	-0.3～36	V
Power dissipation	Pd	4.7(Note1)	W
Junction temperature range	Tjmax	-40 ～+150	°C
Operation temperature range	Topr	-40～+85	°C
Storage temperature range	Tstg	-55～+150	°C
Maximum LED output current	ILED	400(Note2)(Note3)	mA

No.	Pin	Rating [V]	No.	Pin	Rating [V]
1	VCC	-0.3~36	40	AGND	-
2	FAIL	-0.3~36	39	UVLO	-0.3~10.5
3	REG9V	-0.3~13	38	LSP	-0.3~7
4	N.C.	-	37	LED_LV	-0.3~7
5	N	-0.3~13	36	ADIM_P	-0.3~20
6	PGND	-	35	ADIM	-0.3~20
7	CS	-0.3~7	34	RT	-0.3~7
8	OVP	-0.3~7	33	FB	-0.3~7
9	FAIL_MODE	-0.3~7	32	SS	-0.3~7
10	AGND	-	31	CP	-0.3~7
11	LED1	-0.3~60	30	S1	-0.3~7
12	LED2	-0.3~60	29	S2	-0.3~7
13	LED3	-0.3~60	28	S3	-0.3~7
14	LED4	-0.3~60	27	S4	-0.3~7
15	LED5	-0.3~60	26	S5	-0.3~7
16	LED6	-0.3~60	25	S6	-0.3~7
17	STB	-0.3~36	24	FAIL_RST	-0.3~22
18	DVDD	-0.3~4.0	23	SUMPWM	-0.3~7
19	SDA	-0.3~4.0	22	DGND	-
20	SCL	-0.3~4.0	21	PWM	-0.3~22

(Note1) In the case of mounting 4 layer glass epoxy base-plate of 70mm × 70mm × 1.6mm, 37.6mW is reduced at 1°C above Ta=25°C.
(Note2) Wide VF variation of LED increases loss at the driver, which results in rise in package temperature. Therefore, the board needs to be designed with attention paid to heat radiation.
(Note3) This current value is per 1ch. It needs be used within a range not exceeding Pd.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

1.7 Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1層基板*(Note 3)*	4層基板*(Note 4)*	
HTSSOP-B40				
Junction to Ambient	θ_{JA}	99.8	26.0	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	5	2	°C/W

(Note 1)Based on JESD51-2A(Still-Air)
(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3)Using a PCB board based on JESD51-3.
(Note 4)Using a PCB board based on JESD51-5, 7.

1.8 Electrical Characteristics 1/3 (unless otherwise specified, V_{IN}=24V Tj=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
【Whole device】						
Operating circuit current	ICC	-	9	16	mA	STB=3.0V, LED1-6=ON, RT=100kΩ
Standby circuit current	ISTB	-	15	25	μA	STB=0V
DVDD circuit current	IDVDD	-	1.8	-	mA	DVDD=3.3V
【UVLO block】						
VCC operating supply voltage	VUVLO_VCC	7.0	7.5	8.0	V	VCC=SWEEP UP
VCC hysteresis voltage	VUHYS_VCC	150	300	600	mV	VCC=SWEEP DOWN
UVLO release voltage	VUVLO_UVLO	2.40	2.50	2.60	V	VUVLO=SWEEP UP
UVLO HYS width	VUHYS_UVLO	100	200	400	mV	VUVLO=SWEP DOWN
UVLO pin input current	IUVLO	-2	0	2	μA	VUVLO=3.0V
DVDD release voltage	VUVLO_DVDD	2.10	2.35	2.60	V	VDVDD=SWEEP UP
DVDD HYS width	VUHYS_DVDD	100	200	400	mV	VDVDD=SWEP DOWN
【REG9V block】						
REG9V output voltage	REG9V	8.91	9.0	9.09	V	IO=0mA, VCC>11.0V
REG9V max. output current	IREG9V	20	-	-	mA	
【DCDC block】						
Error AMP reference voltage	VEAMP	0.97	1.00	1.03	V	LED_LV=1.0V, LEDLV[3:0]=0000
		0.578	0.60	0.622	V	LEDLV[3:0]=1001
		0.278	0.300	0.322	V	LEDLV[3:0]=1111
FB sink current	IFBSINK	85	100	115	μA	LED_LV=1.0V, LEDx=2.0V, VFB=1.0V
FB source current (Master)	IFBSOURCEM	-115	-100	-85	μA	LED_LV=1.0V, LEDx=0.0V, VFB=1.0V,CS=0.0V
FB source current (Slave)	IFBSWRCKS	-230	-200	-170	μA	LEDx=0V,VFB=1.0V,CS=5.0V
LED_LV pin input current	ILED_LV	-2	0	2	μA	VLED_LV=3.0V
Oscillation frequency	FCT	190	200	210	kHz	RT=100kΩ, FOSC[4:0]=00000
MAX DUTY	DMAX	83	89	96	%	
SS pin source current	ISS	-3.75	-3.0	-2.25	μA	SS=0V
SS pin release voltage	VSS	3.8	4.0	4.2	V	SS=SWEEP UP
N pin source resistor	RONH	-	2.5	3.5	Ω	ION=-10mA
N pin sink resistor	RONL	-	3.0	4.2	Ω	ION=10mA

1.8 Electrical Characteristics 2/3 (unless otherwise specified, V_{IN}=24V Tj=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
【DCDC protection block】						
OCP detection voltage	VOCP	0.405	0.45	0.495	V	VCS=SWEEP UP
OVP detection voltage	VOVP	2.91	3.00	3.09	V	VOVP=SWEEP UP, OVPSET[3:0]=0000
OVP hysteresis voltage	VOVPHYS	10	50	100	mV	VOVP=SWEEP DOWN, OVPSET[3:0]=0000
OVP pin input current	IOVP	-2	0	2	µA	VOVP=3.0V
SCP detection voltage	VSCP	0.12	0.20	0.28	V	VOVP=SWEEP DOWN
【LED driver block】						
S pin voltage 1	VSLED1	196	200	204	mV	ADIM=1.0V, ADIMGAIN[3:0]=0000
		294.6	300	305.4	mV	ADIM=1.5V, ADIMGAIN[3:0]=0000
		392.8	400	407.2	mV	ADIM=2.0V, ADIMGAIN[3:0]=0000
		491	500	509	mV	ADIM=2.5V, ADIMGAIN[3:0]=0000
S pin voltage 2	VSLED2	101.7	106	110.3	mV	ADIM=1.0V, ADIMGAIN[3:0]=1111
		153.2	159	164.8	mV	ADIM=1.5V, ADIMGAIN[3:0]=1111
		204.3	212	219.7	mV	ADIM=2.0V, ADIMGAIN[3:0]=1111
		254.4	265	275.6	mV	ADIM=2.5V, ADIMGAIN[3:0]=1111
LED current rise time	ILEDtr	-	400	760	ns	ADIM=0.3V,RS=2Ω, DVDD=0V
LED current fall time	ILEDtf	-	100	280	ns	ADIM=0.3V,RS=2Ω, DVDD=0V
OPEN detection voltage	VOPEN	0.12	0.20	0.28	V	VLED=SWEEP DOWN
SHORT detection voltage	VSHORT	5.7	6.0	6.3	V	VLED=SWEEPUP, VLSP=1.2V, LSPSET[3:0]=0000
SHORT MASK voltage	VSHTMASK	2.85	3.0	3.15	V	
LSP pin input current	ILSP	-2	0	2	µA	VLSP=3.0V
【Analog dimming block】						
ADIM_P pin HIGH voltage	ADIM_PH	2.0	-	5.5	V	
ADIM_P pin LOW voltage	ADIM_PL	-0.3	-	0.8	V	
ADIM_P Pin input MASK voltage	ADIM_PPU	6.5	-	18	V	
ADIM_P pin pull-down R	RADIM_P	2.4	4.0	5.6	MΩ	VADIM_P=3.0V
ADIM pin output voltage H (During output)	ADIMH	2.462	2.500	2.538	V	VADIM_P=3.3V
ADIM pin output voltage L (During output)	ADIML	-	0.0	0.05	V	VADIM_P=0.0V
ADIM pin output R (During output)	ADIMR	6.6	10	15	kΩ	VADIM_P=0.0V
ADIM pin input current (During input)	IADIM	-2	0	2	µA	VADIM_P=9.0V, VADIM=2.5V

1.8 Electrical Characteristics 3/3 (unless otherwise specified, V_{IN}=24V Tj=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
【STB block】						
STB pin HIGH voltage	VSTBH	2.0	-	18	V	
STB pin LOW voltage	VSTBL	-0.3	-	0.8	V	
STB pin pull-down Resistor	RSTB	0.6	1.0	1.4	MΩ	STB=3.0V
【PWM block】						
PWM pin HIGH voltage	VPWMH	1.5	-	20	V	
PWM pin LOW voltage	VPWML	-0.3	-	0.8	V	
PWM pin pull-down Resistor	RPWM	180	300	420	kΩ	PWM=3.0V
【Abnormality detection block】						
FAIL pin LOW output voltage	VFAILL	0.0	0.15	0.3	V	IOL=500μA
FAIL_RST pin Input HIGH voltage	VFAIL_INH	2.0	-	20	V	
FAIL_MODE pin Input HIGH voltage	VFAIL_INH	2.0	-	5.5	V	
FAIL_MODE, FAIL_RST pin Input LOW voltage	VFAIL_INL	-0.3	-	0.8	V	
FAIL_MODE, FAIL_RST pin Input pull-down Resistor	RFAIL	60	100	140	kΩ	VIN=3.0V
CP detection voltage	VCP	2.91	3.0	3.09	V	CP=SWEEP UP
CP source current	ICP	-3.3	-3.0	-2.7	μA	CP=0V
【I2C block】						
SCL, SDA input HIGH voltage	VI2C_INH	0.8*DVDD	-	3.6	V	
SCL, SDA input LOW voltage	VI2C_INL	-0.3	-	0.2*DVDD	V	
SCL, SDA input HIGH current	II2C_INH	-	-	10	μA	DVDD=3.3V, VIN=3.3V
SCL, SDA input LOW current	II2C_INL	-10	-	-	μA	DVDD=3.3V, VIN=0V
L level SDA output	VSDA_OL	-	-	0.4	V	
【Master/Slave selection block】						
SUMPWM pin input HIGH voltage	VSUM_INH	2.0	-	5.5	V	
SUMPWM pin input LOW voltage	VSUM_INL	-0.3	-	0.8	V	
SUMPWM pin pull-down Resistor	RSUM	60	100	140	kΩ	VIN=3.0V

1.9 Typical Performance Curves
(reference data)

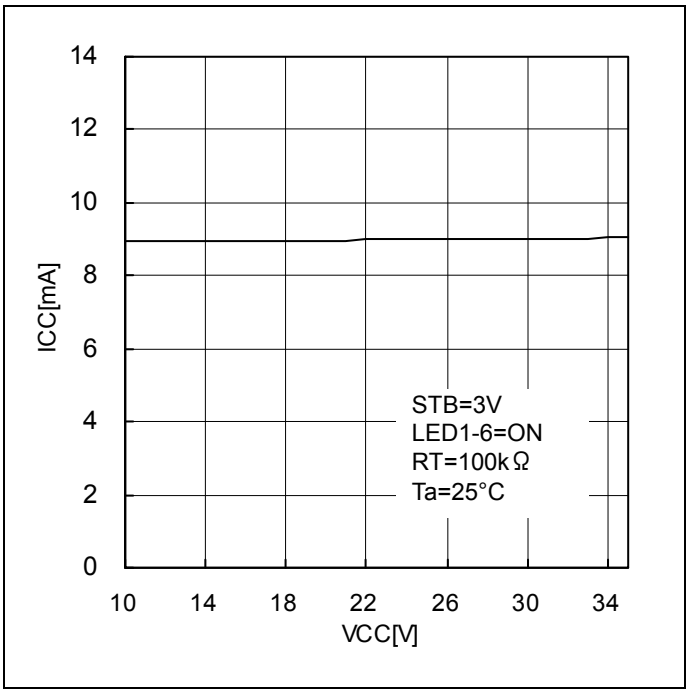


Figure 5. Operating circuit current

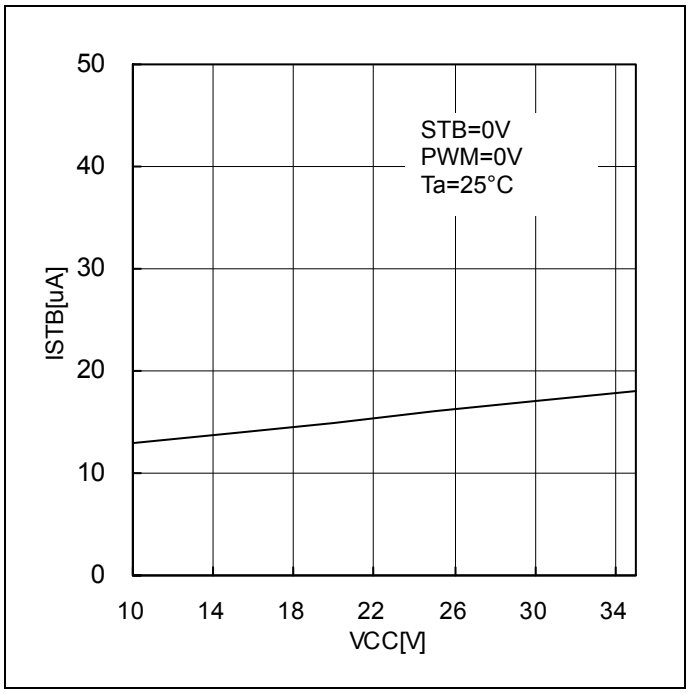


Figure 6. Standby circuit current

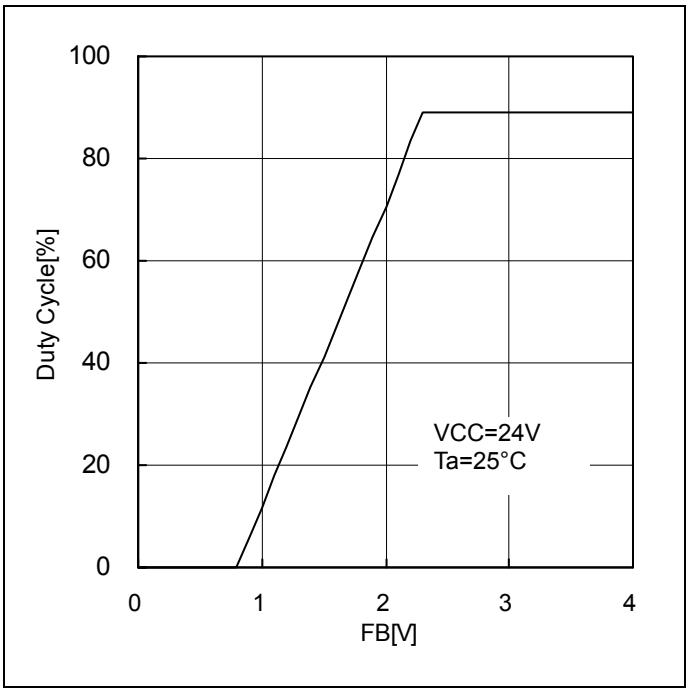


Figure 7. Duty Cycle vs FB character

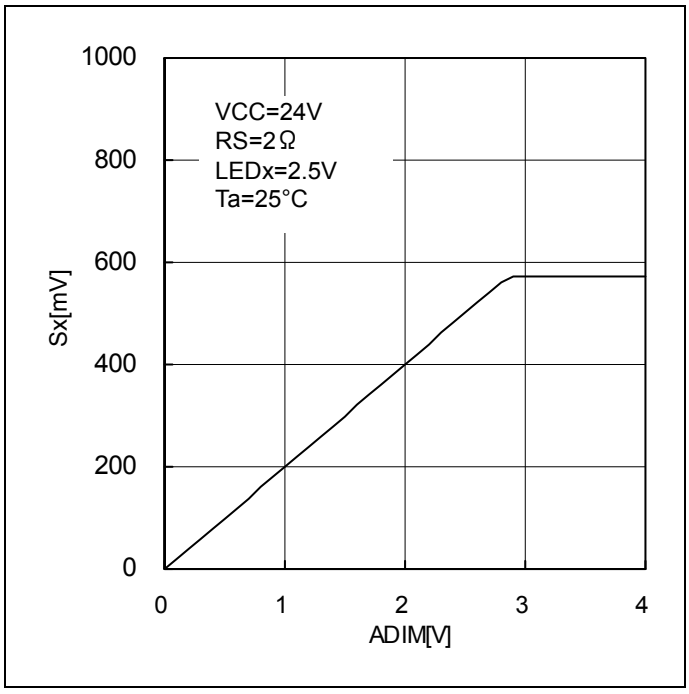


Figure 8. Sx vs ADIM character

1.10 Operating range

Parameter	Symbol	Range	Unit
VCC power supply voltage	VCC	9 to 35	V
DVDD power supply voltage	VDD	2.7 to 3.6	V
Boost-up oscillation frequency	FCT	50 to 1250(Note1)	kHz
ADIM input voltage	VADIM	0.2 to 2.5	V
ADIM_P input frequency	FADIM_P	to 20k	Hz
LSP pin input voltage	VLSP	0.8 to 3	V
LED_LV pin input voltage	VLED_LV	0.3 to 1.8	V
FB pin output voltage	VFB	0 to 5.0	V
PWM pin input frequency (With DVDD)	FPWM	0, 100 to 25k	Hz
PWM pin input Low width (With DVDD)	TLPWM	from 157ns	ns
SCL Clock frequency	FSCL	to 400	kHz

(Note1) When driving the external FET with high frequency, it may increase FET heat generation, therefore please do the setting carefully.

1.11 Recommendation range of external parts

Parameter	Symbol	Range	Unit
VCC pin connection capacitance	CVCC	1.0 to 10	μF
DVDD pin connection capacitance	CDVDD	0.047 to 1.0	μF
Soft start setting capacitance	CSS	0.001 to 1.0	μF
Timer latch setting capacitance	CCP	0.001 to 2.7	μF
Boost-up frequency setting resistor	RRT	12 to 150(Note2)	kΩ
REG9V pin connection capacitance	CREG9V	1.0 to 10	μF

(Note2) It depends on FOSC[4:0] register value, but please do the setting that make the oscillation frequency within the specification written in section 1.10.
The operating condition described above is for single IC constants. Adequate attention must be paid when setting the constants at actual set.

1.12 I2C command interface

1.12.1 Overview and condition

BD9423EF are using host CPU and Command Interface by I2C bus system. BD9423EFV register setting from 00h to 08h range is possible not only Write but also can Read. Besides, other than slave address, this IC also can perform to design 1bit Select Address and then do the Write and Read.
I2C bus slave mode format is shown as below.

	MSB LSB		MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	Data	A	P

S: Start Condition
Slave Address: After the set Slave Address (7bit) by ADDR, there is one more bit of Read Mode (H") or Write Mode (L") and the data will be sent in total of 8bit. (MSB format)
BD9423EFV slave address is 46h.
A: The acknowledge send and receive data is added by Acknowledge Bit as byte per byte.
When the send and receive data is correctly done, "L" will be sent and received.
When it is "H", acknowledge will be gone.
Select Address: BD9423EFV will use 1 byte of select address. (MSB format)
Data: Data Byte, send and receive data. (MSB format)
P: Stop Condition

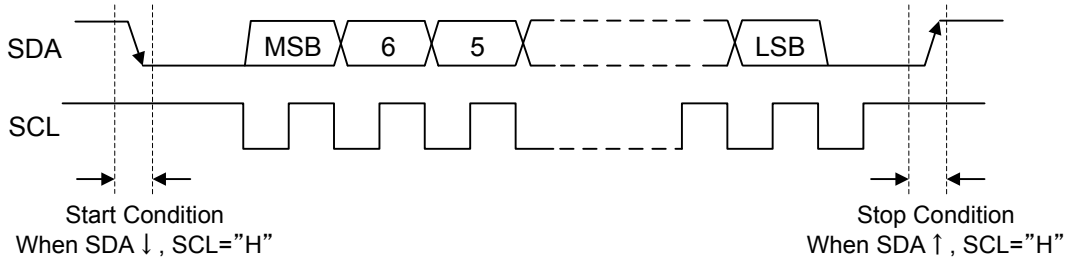


Figure 9. Command Interface

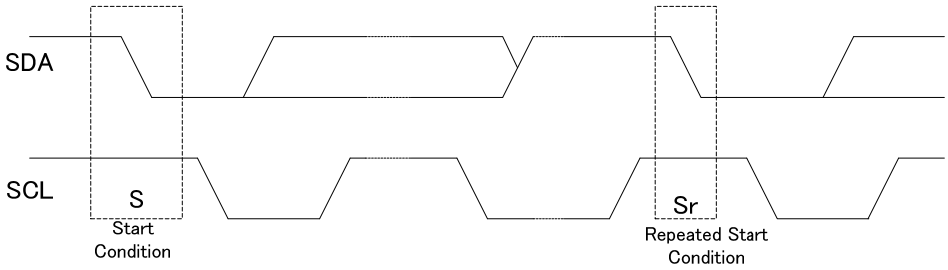


Figure 10. Repeated Start Condition

1.12.2 Data format

1byte Write format

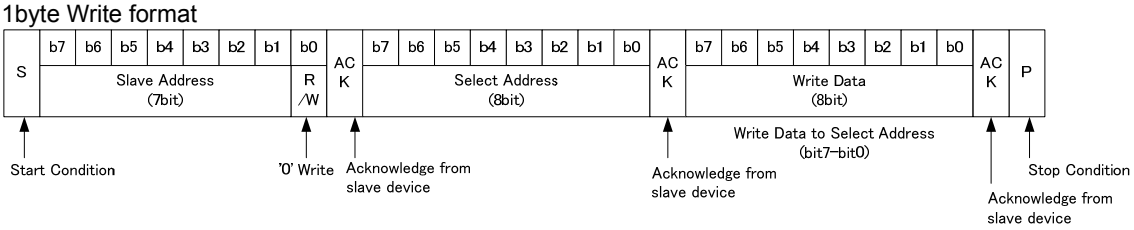


Figure 11. 1byte Write Data Format

1byte Read format (Read from select address=00h)

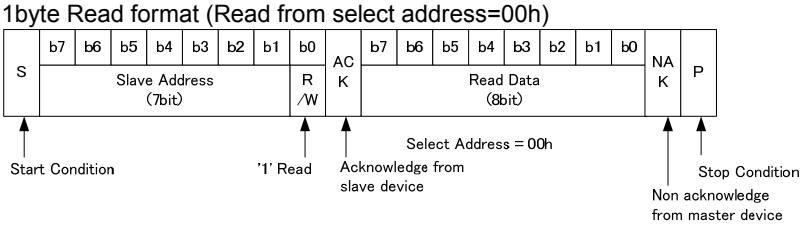


Figure 12. 1byte Read Data Format (Select Address=00h)

1byte Read format (Read from specific Select Address)

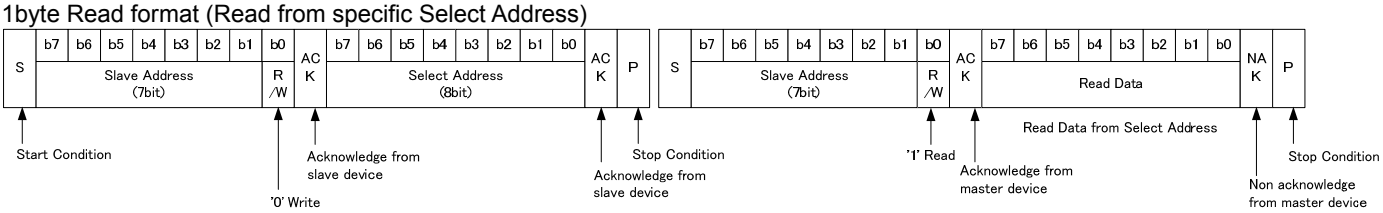


Figure 13. 1byte Read Data Format (specified select address)

Consecutive Write format

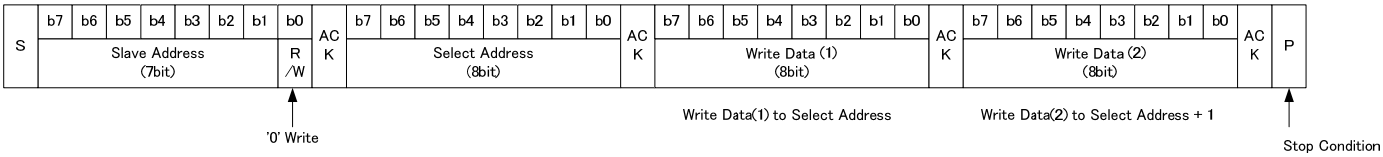


Figure 14. Consecutive Write Data Format

Consecutive Read format (Read from specific Select Address)

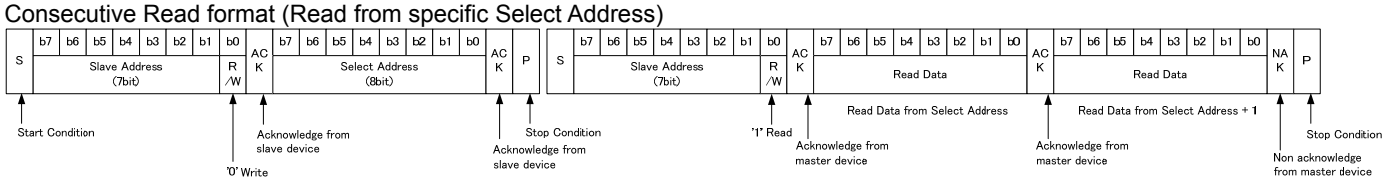


Figure 15. Consecutive Read Data Format

1.12.3 Signal control specification

Bus Line and I/O stage electrical specification and timing

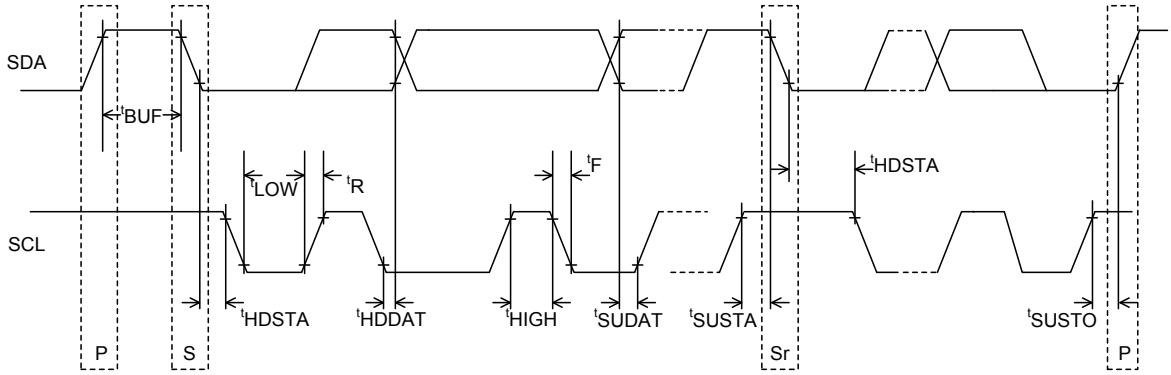


Figure 16. Timing chart

Table 1. SDA and SCL Bus Line characteristic (Unless otherwise stated Ta=25°C, DVDD=3.0V)

Parameter		Symbol	High speed mode		Unit
			Min.	Max.	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus Free Time between “Stop” Condition and “Start” Condition.	tBUF	1.3	—	μs
3	Hold Time (Resend) “Start” Condition. After this period, the first Clock Pulse will be generated.	tHDSTA	0.6	—	μs
4	SCL clock LOW state Hold Time	tLOW	1.3	—	μs
5	SCL clock HIGH state Hold Time	tHIGH	0.6	—	μs
6	Resend “Start” Condition set-up time	tSUSTA	0.6	—	μs
7	Data Hold Time	tHDDAT	0(Note1)	—	μs
8	Data Set-up Time	tSUDAT	100	—	ns
9	SDA and SCL signal rising time	tR	20+0.1Cb	300	ns
10	SDA and SCL signal falling time	tF	20+0.1Cb	300	ns
11	“Stop” Condition set-up time	tSUSTO	0.6	—	μs
12	Each Bus Line capacitive load	Cb	—	400	pF

Above values are all $V_{IH\,min}$ and $V_{IL\,max}$ level supported.

(Note1) Please note that the master device has uncertain interval maximum 300ns for the negative edge of SLC, therefore SDA is necessary at least 300ns hold time.

1.13 Register map and description

Slave address (Device address) for BD9423EFV is 46h. Please refer to section 1.12 I2C command interface for I2C details.

Update timing for each register is as follows.
(1) Data will reflect immediately after register is written.
(2) Data will reflect at next PWM rise after register is written (Refer to Section 1.14 PWM Phase shift setting)
(3) Data will reflect as PWM=Low after register is written.

Sequence that is assumed for each register will be as follow. (Please refer to 3.8.1 start up and shut down sequences). Writing is possible at any timing, however it is classified by the consideration of register function.
(A) Initial command: Please input the command before input the STB pin. It is assumed to set a condition for the application.
(B) Dimming command: It is possible to input the command before or after STB pin.

Address	R/W	Initial value	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	R/W	00h	SOFTRST	-	-	-	-	-		FAILSORST	PHASERST
			Update timing	-	-	-	-	-	-	(1)	(1)
			Write sequence	-	-	-	-	-	-	(B)	(B)
01h	R/W	00h	LEDDIS	-	-	LED6DIS	LED5DIS	LED4DIS	LED3DIS	LED2DIS	LED1DIS
			Update timing	-	-	(3)	(3)	(3)	(3)	(3)	(3)
			Write sequence	-	-	(A)	(A)	(A)	(A)	(A)	(A)
02h	R/W	00h	LEDPHASE	FOSC4	FOSC3	FOSC2	FOSC1	FOSC0	LEDPHASE2	LEDPHASE1	LEDPHASE0
			Update timing	(1)	(1)	(1)	(1)	(1)	(2)	(2)	(2)
			Write sequence	(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
03h	R/W	00h	ADIMGAIN	CPADJ1	CPADJ0	SSADJ1	SSADJ0	ADIM GAIN3	ADIM GAIN2	ADIM GAIN1	ADIM GAIN0
			Update timing	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
04h	R/W	00h	OVPSET	OVPSET3	OVPSET2	OVPSET1	OVPSET0	LSPSET3	LSPSET2	LSPSET1	LSPSET0
			Update timing	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
05h	R/W	00h	SFTONOFF	-	-	MSTSLVSFT	MSTSLVSEL	SFTONT1	SFTONT0	SFTOFFT1	SFTOFFT0
			Update timing	-	-	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	-	-	(A)	(A)	(B)	(B)	(B)	(B)
06h	R/W	00h	LOPMSK	SCPMSK	OVPMSK	LOPMSK6	LOPMSK5	LOPMSK4	LOPMSK3	LOPMSK2	LOPMSK1
			Update timing	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	(B)	(B)	(B)	(B)	(B)	(B)	(B)	(B)
07h	R/W	00h	LSPMSK	-	-	LSPMSK6	LSPMSK5	LSPMSK4	LSPMSK3	LSPMSK2	LSPMSK1
			Update timing	-	-	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	-	-	(B)	(B)	(B)	(B)	(B)	(B)
08h	R/W	00h	LEDLVSET	-	-	IFBSET1	IFBSET0	LEDLVSET3	LEDLVSET2	LEDLVSET1	LEDLVSET0
			Update timing	-	-	(1)	(1)	(1)	(1)	(1)	(1)
			Write sequence	-	-	(A)	(A)	(A)	(A)	(A)	(A)

Note) "-" : Invalid during Write, "0" during Read
Please do not write register other than 00h-08h. Besides, Read value from register other than 00h-08h is disabled.

●**ADDR=00h**

SOFTRST (SoftRESET control register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	-	-	-		FAILSO RST	PHASERST
Initial Value	-	-	-	-	-	-	0	0

FAILSORST	RESET setting
0	Normal
1	Latch OFF release, Protection operation mask

When FAILSORST is set as 1 (FAILSORST=1), protection circuit and FAIL are reset.
It is same with the operation when FAIL_RST pin=High.
During FAILSORST=1, latch OFF protection operation is masked.

PHASERST	RESET setting
0	Normal
1	Counter clear

When PHASERST=1, logics other than Phase shift part register are reset. Register values shown in the section 1.13 will not be reset. In order to release reset, please write PHASERST=0, it will return to normal condition.

●**ADDR=01h**

LEDDIS (LED driver disable setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register name	-	-	LED6DIS	LED5DIS	LED4DIS	LED3DIS	LED2DIS	LED1DIS
Initial Value	-	-	0	0	0	0	0	0

LEDDIS	Disable Control
0	Enable (LED driver operates when PWM=H)
1	Disable (LED driver is not used)

Unused channel will be set. The unused channel will not detect the abnormality (Short, Open).

●**ADDR=02h**

LEDPHASE (Phase shift setting, FCT setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register name	FOSC4	FOSC3	FOSC2	FOSC1	FOSC0	LEDPHASE2	LEDPHASE1	LEDPHASE0
Initial Value	0	0	0	0	0	0	0	0

FOSC[4:0]	FOSC setting	FCT default=200kHz
00000	1.000 time	200kHz
00001	0.250 time	50 kHz
00010	0.375 time	75 kHz
00011	0.500 time	100 kHz
00100	0.625 time	125 kHz
00101	0.750 time	150 kHz
00110	0.875 time	175 kHz
00111	1.000 time	200 kHz
01000	1.125 times	225 kHz
01001	1.250 times	250 kHz
01010	1.375 times	275 kHz
01011	1.500 times	300 kHz
01100	1.625 times	325 kHz
01101	1.750 times	350 kHz
01110	1.875 times	375 kHz
01111	2.000 times	400 kHz
10000	2.125 times	425 kHz
10001	2.250 times	450 kHz
10010	2.375 times	475 kHz
10011	2.500 times	500 kHz
10100	2.625 times	525 kHz
10101	2.750 times	550 kHz
10110	2.875 times	575 kHz
10111	3.000 times	600 kHz
11000	3.125 times	625 kHz
11001	3.250 times	650 kHz
11010	3.375 times	675 kHz
11011	3.500 times	700 kHz
11100	3.625 times	725 kHz
11101	3.750 times	750 kHz
11110	3.875 times	775 kHz
11111	4.000 times	800 kHz

Oscillating frequency FCT will be set.
When RT=100kΩ, default frequency is 200kHz, frequency will be set as the values shown in above table.
Register is setting based on how many times of frequency base, therefore, please always connect a resistor at RT terminal.

LEDPHASE[2:0]	LEDPHASE control
000	Phase1 setting (0 shift)
001	
010	Phase2 setting (1/2T shift)
011	Phase3 setting (1/3T shift)
100	Phase4 setting (1/4T shift)
101	Phase5 setting (1/5T shift)
110	Phase6 setting (1/6T shift)
111	

Phase shift setting will be done. Please refer to section 1.14 "PWM phase shift setting" for each phase shift timing.

●**ADDR=03h**

ADIMGAIN (ADIM GAIN Setting, CP and SS time setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register name	CPADJ1	CPADJ0	SSADJ1	SSADJ0	ADIMGAIN3	ADIMGAIN2	ADIMGAIN1	ADIMGAIN0
Initial value	0	0	0	0	0	0	0	0

CPADJ[1:0]	CP time setting
00	1time
01	2times
10	1/2time
11	1/4time

CP timer time, Tcp can be set.
CP timer time can be decided by, Tcp[s] = (Ccp[F]×3V×CPADJ) / 3μA.

SSADJ[1:0]	SS time setting
00	1time
01	2times
10	1/2time
11	1/4time

SS release time, Tss can be set.
SS release time can be decided by, Tss[s] = (Css[F]×4V×SSADJ) / 3μA.

ADIMGAIN[3:0]	ADIMGAIN setting
0000	0.200 time
0001	0.194 time
0010	0.188 time
0011	0.181 time
0100	0.175 time
0101	0.169 time
0110	0.163 time
0111	0.156 time
1000	0.150 time
1001	0.144 time
1010	0.138 time
1011	0.131 time
1100	0.125 time
1101	0.119 time
1110	0.113 time
1111	0.106 time

ADIM gain will be set. ADIM pin voltage × ADIMGAIN=Sx pin voltage.

●**ADDR=04h**

OVPSET (OVP voltage, LSP voltage setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register name	OVPSET3	OVPSET2	OVPSET1	OVPSET0	LSPSET3	LSPSET2	LSPSET1	LSPSET0
Initial value	0	0	0	0	0	0	0	0

OVPSET[3:0]	OVP voltage setting	OVP default=90V
0000	3.00V	90V
0001	0.90V	27V
0010	1.05V	32V
0011	1.20V	36V
0100	1.35V	41V
0101	1.50V	45V
0110	1.65V	50V
0111	1.80V	54V
1000	1.95V	59V
1001	2.10V	63V
1010	2.25V	68V
1011	2.40V	72V
1100	2.55V	77V
1101	2.70V	81V
1110	2.85V	86V
1111	3.00V	90V

OVP voltage will be set. When setting the OVP detection resistor 30 times (OVP upper side resistor : OVP lower side resistor=29 : 1), the setting shown in above table can be done.

LSPSET[3:0]	LSP voltage setting	LSP detection voltage value
0000	LSP pin input	4V to 15V
0001	0.8V	4V
0010	0.8V	4V
0011	0.8V	4V
0100	0.8V	4V
0101	1.0V	5V
0110	1.2V	6V
0111	1.4V	7V
1000	1.6V	8V
1001	1.8V	9V
1010	2.0V	10V
1011	2.2V	11V
1100	2.4V	12V
1101	2.6V	13V
1110	2.8V	14V
1111	3.0V	15V

LSP voltage will be set. When LSPSET[3:0]=0000, LSP pin voltage will be used as LSP detection reference voltage.
Other than LSPSET[3:0]=0000, IC internal reference voltage will be used, therefore external bias setting can be removed.
If you set the LSP by this register, it will be the priority rather than LSP pin voltage.

●**ADDR=05h**

SFTONOFF (SOFT ON, SOFT OFF setting register, Master/Slave setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	MSTSLV SFT	MSTSLV SEL	SFTONT1	SFTONT0	SFTOFFT1	SFTOFFT0
Initial Value	-	-	0	0	0	0	0	0

MSTSLVSFT	Master/Slave software setting
0	Master mode
1	Slave mode

(Note) Valid when MSTSLVSEL =1

MSTSLVSEL	Master/Slave selection setting
0	Hardware recognition (CSDET output detection)
1	MSTSLVSEL register control

Master/Slave setting is possible when MSTSLVSEL=1. This setting means for when CS pin is set to open. Please separately connect the SUMPWM pin between the IC.

SFTONT[1:0]	Soft ON time setting
00	Soft ON function stop
01	2time
10	1time (correspond to fsw 10CLK)
11	1/2time

Set Soft ON time when PWM＝L→H. CLK when N pin is operating in MAX duty.

SFTOFFT[1:0]	Soft OFF time setting
00	1time (correspond to fsw 15CLK) However, when Soft ON is 1/2time (SFTONT[1:0]=11), it will become 1/2time.
01	2times However, when Soft ON is 1time (SFTONT[1:0]=10), it will become 1time, when Soft On is 1/2time (SFTONT[1:0]=11), it will become 1/2time.
10	1/2time
11	-

Set Soft OFF time when PWM＝H→L. CLK when N pin is operating in MAX duty.

●ADDR=06h

LOPMSK (SCP, OVP, LOP Mask register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	SCPMSK	OVPMSK	LOPMSK6	LOPMSK5	LOPMSK4	LOPMSK3	LOPMSK2	LOPMSK1
Initial Value	0	0	0	0	0	0	0	0

SCPMSK	Short circuit protection (SCP) Mask control
0	Normal
1	SCP Mask

OVPMSK	Over voltage protection (OVP) Mask control
0	Normal
1	OVP Mask

Mask the SCP and OVP detection.

LOPMSK	LED Open protection (LOP) Mask control
0	Normal
1	LOP Mask

Mask LED open detection for each channel.

Example 1: When masking the OVP, ADDR=06h, DATA=40h
Example 2: When masking the SCP and OVP, ADR=06h and DATA=C0h
Example 3: When masking the LED1 LOP, ADDR=06h, DATA=01h

●ADDR=07h

LSPMSK (LSP Mask register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	LSPMSK6	LSPMSK5	LSPMSK4	LSPMSK3	LSPMSK2	LSPMSK1
Initial Value	-	-	0	0	0	0	0	0

LSPMSK	LED Short protection (LSP) Mask control
0	Normal
1	LSP Mask

Example 1: When masking the LED6 LSP, ADDR=07h, DATA=20h

●**ADDR=08h**

LEDLVSET (LED_LV voltage, FB current setting register: Read/Write)

Bit	7	6	5	4	3	2	1	0
Register Name	-	-	IFBSET1	IFBSET0	LEDLVSET3	LEDLVSET2	LEDLVSET1	LEDLVSET0
Initial Value	-	-	0	0	0	0	0	0

IFBSET[1:0]	FB current setting
00	1time
01	2times
10	1/2time
11	1/4time

Set the FB current.

LEDLVSET[3:0]	LED_LV voltage setting
0000	LED_LV pin input
0001	1.00V
0010	0.95V
0011	0.90V
0100	0.85V
0101	0.80V
0110	0.75V
0111	0.70V
1000	0.65V
1001	0.60V
1010	0.55V
1011	0.50V
1100	0.45V
1101	0.40V
1110	0.35V
1111	0.30V

Set the LED_LV voltage.
When LEDLVSET[3:0]=0000, LED_LV pin voltage will be used as reference for feedback voltage.
Other than LEDLVSET[3:0]=0000, IC internal reference voltage will be used, thus external bias setting can be removed.
If you set the LED_LV by this register, it will be the priority rather than LED_LV pin voltage.

1.14 PWM phase shift setting

Phase shifting for each channel is possible by setting the LEDPHASE register. In addition, by setting the LEDDIS register, unused channel also can be set. Therefore, various combinations of dimming can be performed.

1.14.1

(*1) When VCC and DVDD are supplied, STB becomes L→H, 15MHz oscillator for phase shift sampling will start operate.
(*2) Then, when PWM signal is supplied, counter will start at L→H edge as the starting point.
(*3) When PWM signal becomes H→L, PWM's ON width count-number N_{ON} will be decided.
(*4) PWM's period N_T will be decided at next PWM signal L→H edge when next PWM signal.

Period, duty and phase for each LED driver channel will be counted from ON width N_{ON}, period N_T and LEDPHASE register setting, then PWM signal will be reflected to each channel from next PWM signal.
Phase shift is possible for frequency within 100Hz to 20kHz.

This function operates during DVDD is being input and the cautions are as below. Please be noted that this function does not depend on phase shift amount.
(Caution 1) Possible phase shift frequency range is 100Hz to 25kHz.
(Caution 2) When input the signal around PWM=100%, please don't input the pulse lower than 157ns for Low interval. This is to correctly recognize the Low interval.

The following is the DUTY values which are not in the input range.
When PWM20kHz, above 99.68%, 100% and below (PWM=100% input is possible)
When PWM500Hz, above 99.992%, 100% and below (PWM=100% input is possible)

When there is no DVDD (during standalone), the PWM terminal will directly make the constant current driver goes ON/OFF, therefore above caution 1 and 2 are not applicable.

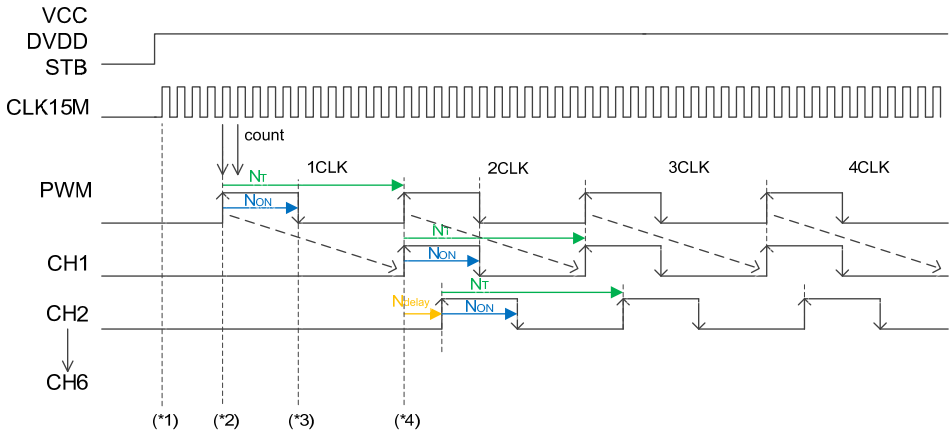


Figure 17. Timing chart for phase shift

1.14.2 Case when PWM is below 100Hz, PWM=H during overflow

When PWM signal's ON width and counter (period counting) is above 2^{18}=262144clk (correspond to frequency below 57Hz), it becomes overflow. If PWM's L→H edge is not input by this time, PWM signal's period can be decided. The operation at this condition is shown below.

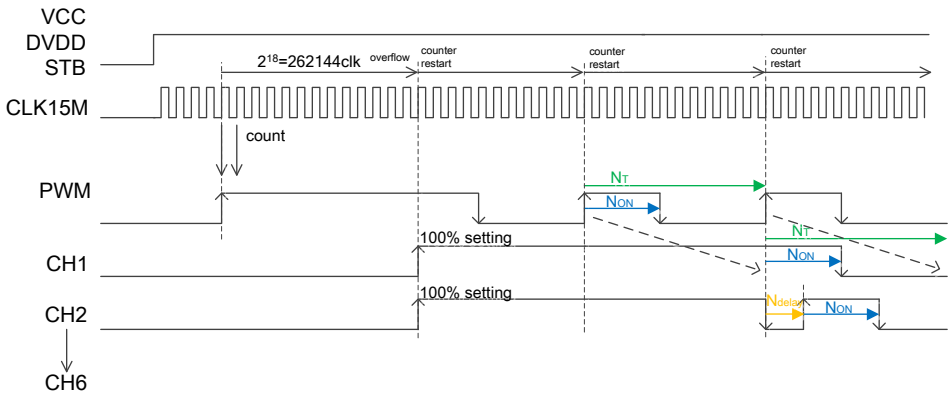


Figure 18. Timing chart for 100% duty overflow

PWM input is considered as High (Duty=100%), thus each LED driver channel will be set as Duty=100% same timing with counter restart.

1.14.3 Case when PWM is below 100Hz, PWM=L during overflow.

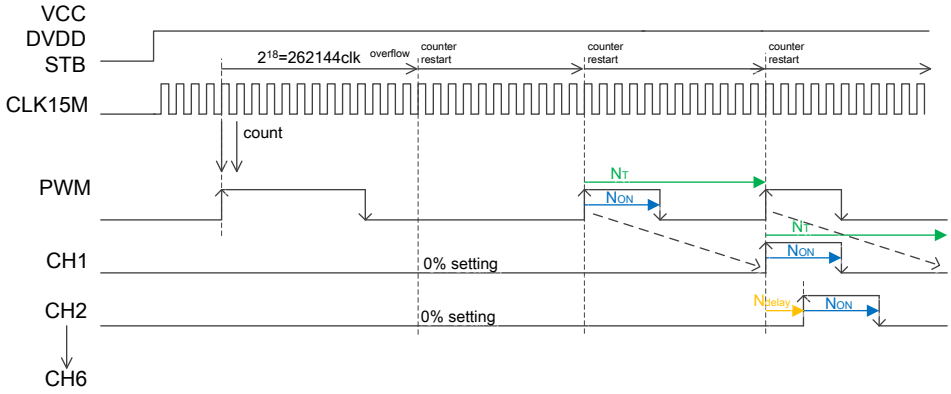
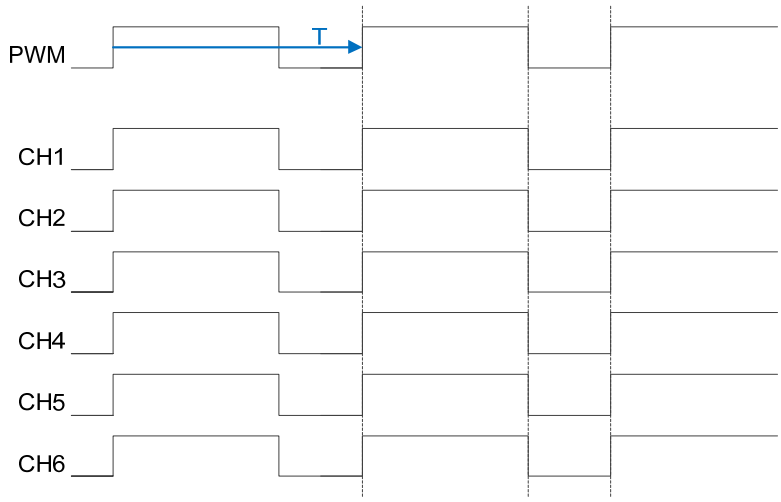


Figure 19. Timing chart for 0% duty overflow

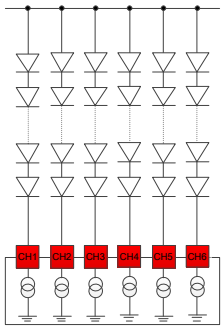
PWM input is considered as Low (Duty=0%), thus each LED driver channel will be set as Duty=0% same timing with counter restart.

1. Phase1 setting (0 shift)

□LEDDIS=00h[All ch ON], LEDPHASE=00h)

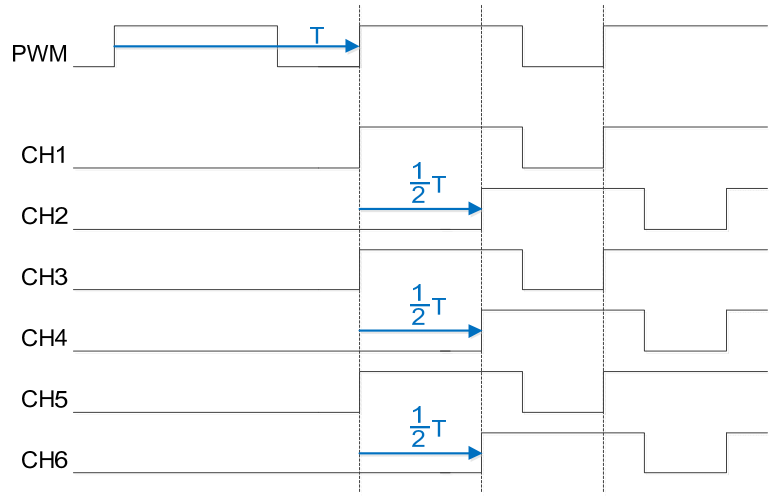


Signal from PWM pin is used as PWM signal for each channel. All channels will have same phase.

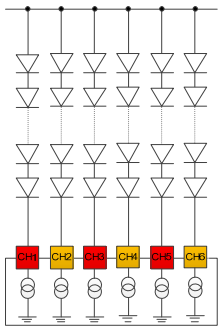


2.Phase2 setting (1/2T shift)

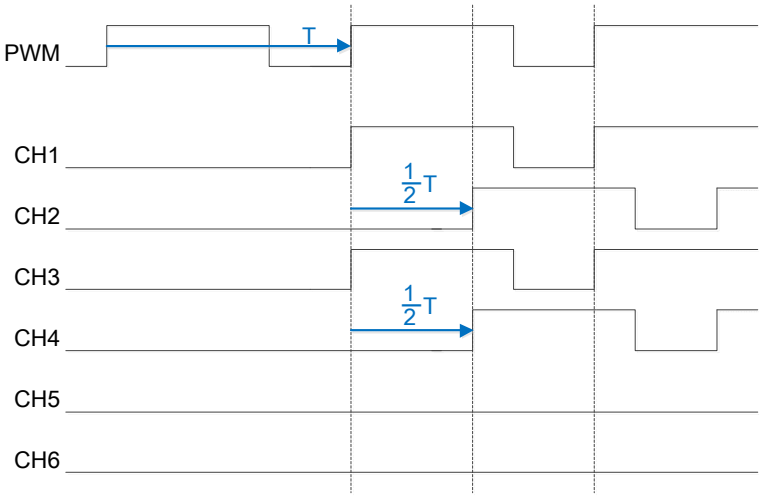
□LEDDIS=00h[All ch ON], LEDPHASE=02h



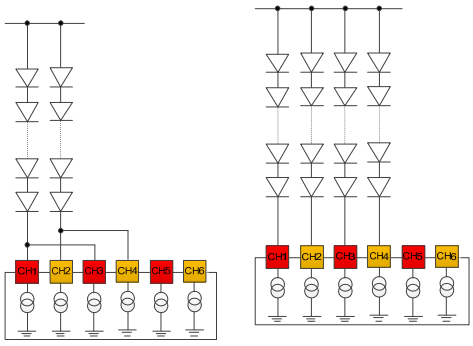
1/2T shift, mode which has 2 phases.



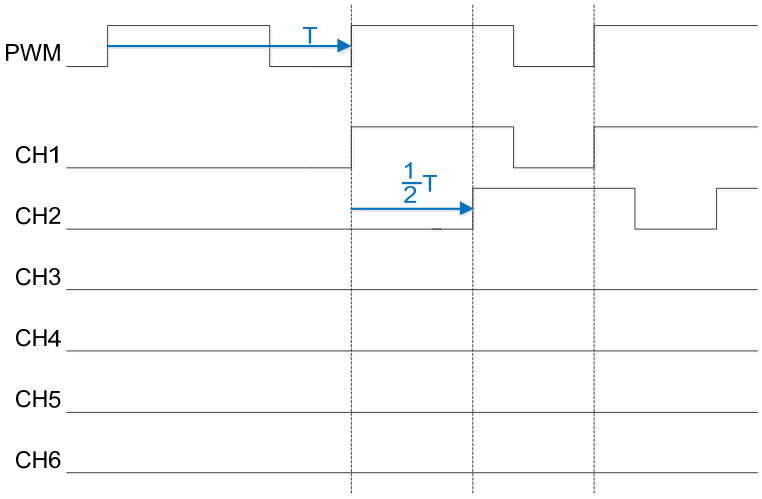
□LEDDIS=30h[CH5,6 OFF],LEDPHASE=02h



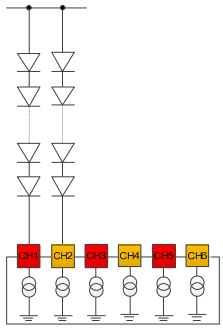
Case when CH5, CH6 are not in use.



・LEDDIS=3Ch[CH3-6 OFF], LEDPHASE=02h

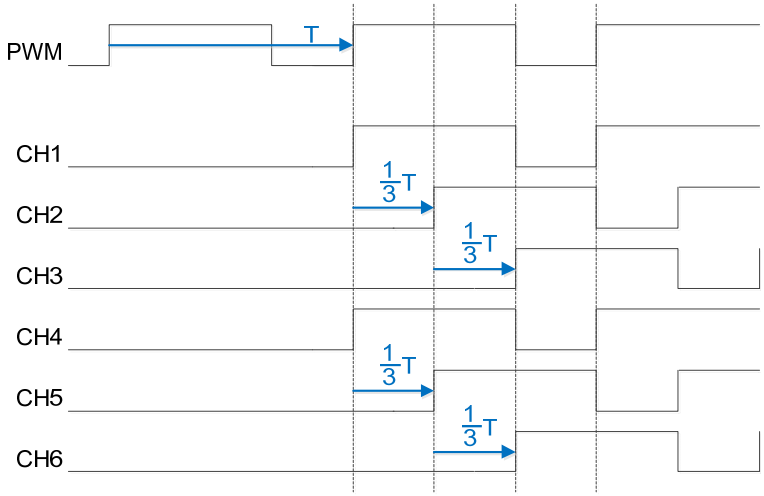


Case when CH3-6 are not in use.

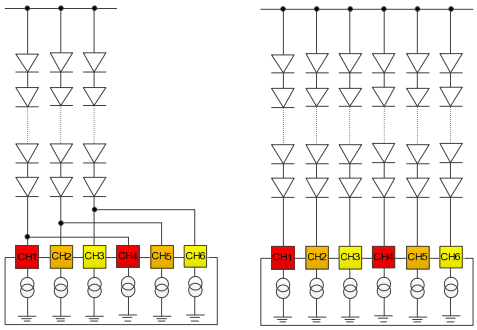


3. Phase3 setting (1/3T shift)

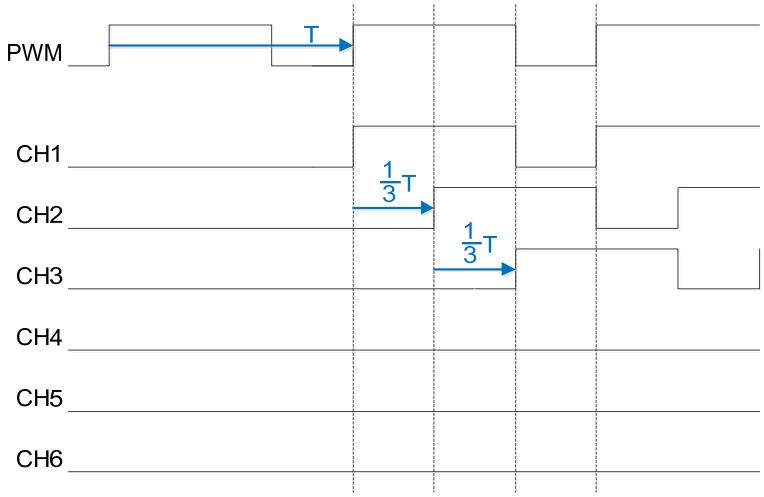
・LEDDIS=00h[All ch. ON]、LEDPHASE=03h



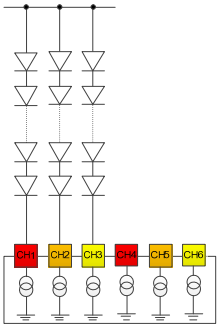
1/3T shift, mode which has 3 phases.



・LEDDIS=38h[CH4-6 OFF], LEDPHASE=03h

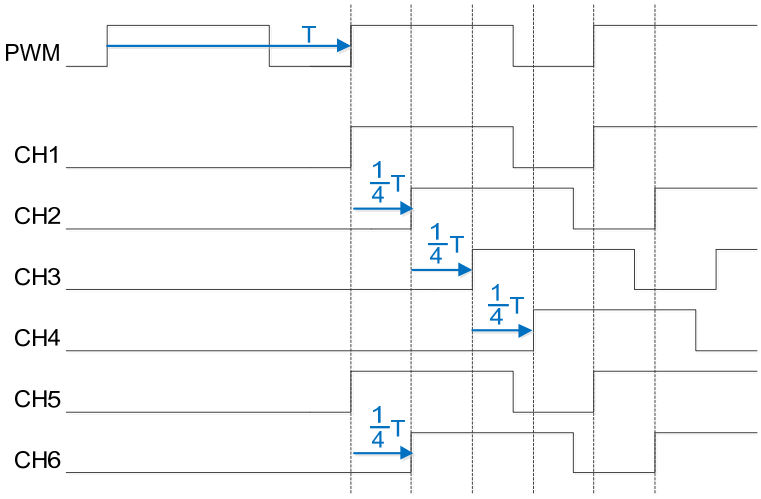


Case when CH4-6 are not in use.

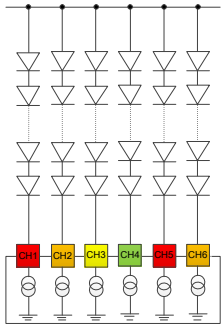


4.Phase4 setting (1/4T shift)

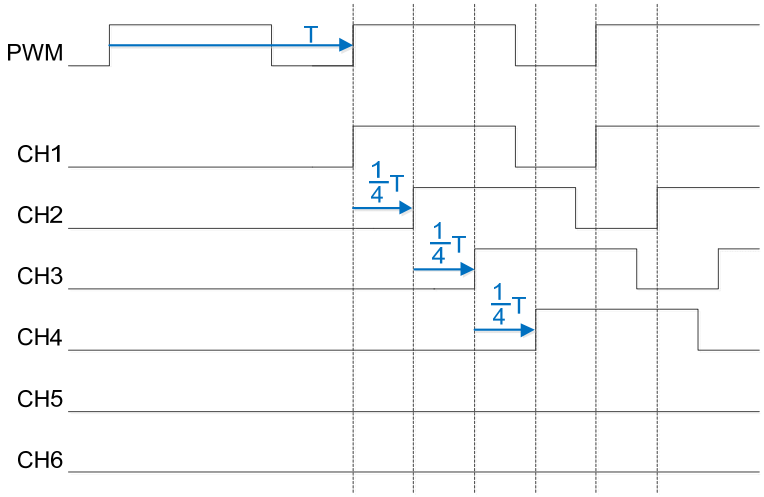
□LEDDIS=00h[All ch. ON], LEDPHASE=04h



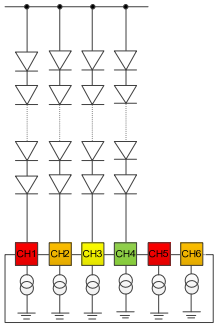
1/4T shift, mode which has 4 phases.



□LEDDIS=30h[LED5, 6 OFF], LEDPHASE=04h

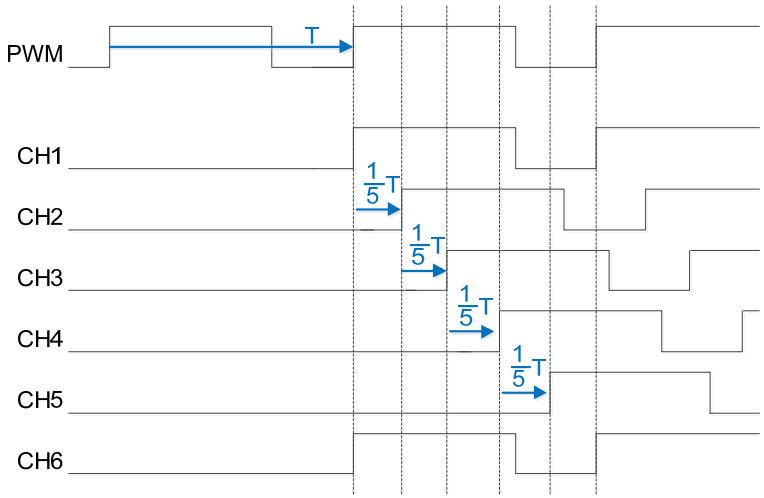


Case when CH5-6 are not in use.



5. Phase5 setting (1/5T shift)

□LEDDIS=00h[All ch. ON], LEDPHASE=05h



1/5T shift, mode which has 5 phases.