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Datasheet

LED Drivers for LCD Backlights

# 1ch Boost up type White LED Driver for large LCD

**BD9486F**

## 1.1 General Description

BD9486F is a high efficiency driver for white LEDs and is designed for large LCDs. BD9486F has a boost DCDC converter that employs an array of LEDs as the light source.
BD9486F has some protect functions against fault conditions, such as over-voltage protection (OVP), over current limit protection of DCDC (OCP), LED OCP protection, and Over boost protection (FBMAX). Therefore it is available for the fail-safe design over a wide range output voltage.

## Key Specifications

- Operating power supply voltage range:9.0V to 18.0V
- Oscillator frequency of DCDC: 150kHz (RT=100kΩ)
- Operating Current: 2.6mA(Typ.)
- Operating temperature range: -40°C to +85°C

## 1.2 Package(s)

| Package | W(Typ) x D(Typ) x H(Max) |
|---|---|
| SOP16 | 10.00mm x 6.20mm x 1.71mm |
| | Pin pitch 1.27mm |


Figure 1. SOP16

## Features

- DCDC converter with current mode
- VOUT discharge function at shutdown
- LED protection circuit (Over boost protection, LED OCP protection)
- Over-voltage protection (OVP) for the output voltage Vout
- Adjustable soft start
- Adjustable oscillation frequency of DCDC
- Wide range of analog dimming 0.2V to 3.0V
- UVLO detection for the input voltage of the power stage

## Applications

- TV, Computer Display, LCD Backlighting

## 1.3 Typical Application Circuit(s)

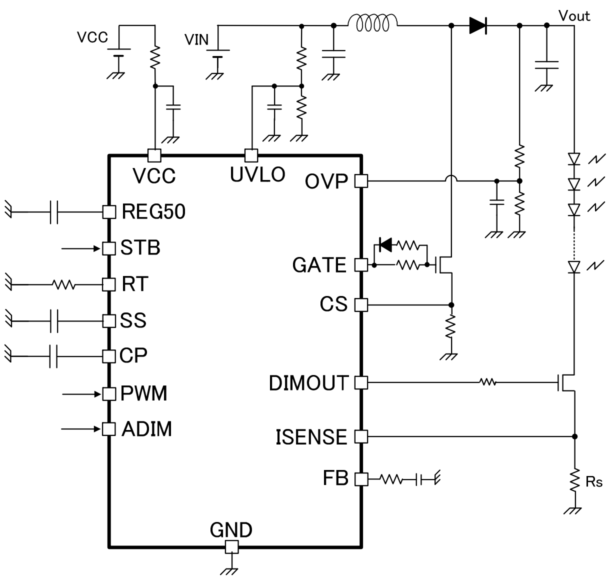



Figure 2. Typical Application Circuit

○Product structure：Silicon monolithic integrated circuit ○This product has not designed protection against radioactive rays

## ●1.4 Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Power Supply Voltage | Vccmax | 20 | V |
| STB, OVP, UVLO, PWM, ADIM Terminal Voltage | STB, OVP, UVLO, PWM, ADIM | 20 | V |
| SS, RT, ISENSE, FB, CS, CP, REG50 Terminal Voltage | SS, RT, ISENSE, FB, CS, CP, REG50 | 7 | V |
| DIMOUT, GATE Terminal Voltage | DIMOUT, GATE | VCC | V |
| Power Dissipation | Pd | 625 (Note 1) | mW |
| Operating Temperature Range | Topr | -40 to +85 | °C |
| Junction Temperature | Tjmax | 150 | °C |
| Storage Temperature Range | Tstg | -55 to +150 | °C |

(Note 1) In the case of mounting 1 layer glass epoxy base-plate of 70mm×70mm×1.6mm, derate by 5.0mW/°C when operating above Ta=25°C.

## ●1.5 Operating Ratings

| Parameter | Symbol | Range | Unit |
|---|---|---|---|
| Power Supply Voltage | VCC | 9.0 to 18.0 | V |
| DC/DC Oscillation Frequency | fsw | 50 to 800 | kHz |
| Effective Range of ADIM Signal | VADIM | 0.2 to 3.0 | V |
| PWM Input Frequency | FPWM | 90 to 2000 | Hz |

## ●1.6 External Components Recommended Range

| Parameter | Symbol | Range | Unit |
|---|---|---|---|
| REG50 Connection Capacitance | $C_{REG50}$ | 0.5 to 10 (Note 2) | μF |
| SS Connection Capacitance | $C_{SS}$ | 0.001 to 2.2 (Note 2) | μF |
| RT Connection Resistance | $R_{RT}$ | 15 to 300 | kΩ |
| GATE Drive Capacitance | $C_{GATE}$ | to 1000 | pF |

(Note 2) Please set connection capacitance above Min value of Recommended Range according to temperature characteristic and DC bias characteristic.

## ●1.7 Pin Configuration

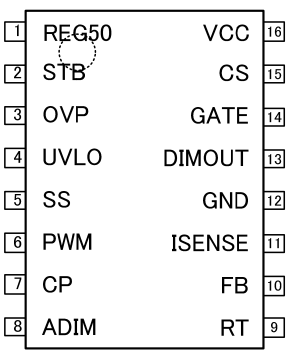



Figure 3. Pin Configuration

## ●1.8 Physical Dimension and Marking Diagram

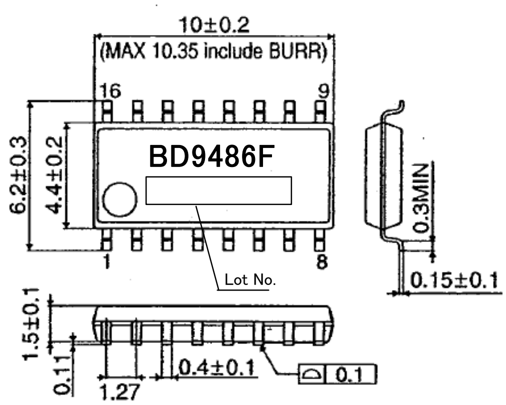



Figure4. Physical Dimension and Marking Diagram of SOP16

●**1.9 Electrical Characteristics** (Unless otherwise specified, Ta=25°C, VCC=12V)

| Parameter | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **【Total Current Consumption】** | | | | | | |
| Circuit Current | Icc | － | 2.6 | 5.2 | mA | VSTB=3.0V, PWM=3.0V, GATE=L,IREG50=0mA |
| Circuit Current (standby) | IST | － | 40 | 80 | μA | VSTB=0V |
| **【UVLO Block】** | | | | | | |
| Operation Voltage（VCC） | VUVLO_VCC | 6.5 | 7.5 | 8.5 | V | VCC=SWEEP UP |
| Hysteresis Voltage（VCC） | VUHYS_VCC | 150 | 300 | 600 | mV | VCC=SWEEP DOWN |
| UVLO Release Voltage | VUVLO | 2.88 | 3.00 | 3.12 | V | VUVLO=SWEEP UP |
| UVLO Hysteresis Voltage | VUHYS | 250 | 300 | 350 | mV | VUVLO=SWEEP DOWN |
| UVLO Pin Leak Current | UVLO_LK | -2 | 0 | 2 | μA | VUVLO=4.0V |
| **【DC/DC Block】** | | | | | | |
| ISENSE Threshold Voltage 1 | VLED1 | 0.225 | 0.233 | 0.242 | V | VADIM=0.7V |
| ISENSE Threshold Voltage 2 | VLED2 | 0.656 | 0.667 | 0.677 | V | VADIM=2.0V |
| ISENSE Threshold Voltage 3 | VLED3 | 0.988 | 1.000 | 1.012 | V | VADIM=3.0V |
| ISENSE Clamp Voltage | VLED4 | 0.989 | 1.015 | 1.040 | V | VADIM=3.3V (at masked analog dimming) |
| Oscillation Frequency | FCT | 142.5 | 150 | 157.5 | KHz | RT=100kΩ |
| RT Short Protection Range | RT_DET | -0.3 | - | VRT ×90% | V | RT=SWEEP DOWN |
| RT Terminal Voltage | VRT | 1.6 | 2.0 | 2.4 | V | RT=100kΩ |
| RT Pin ON Resistance at OFF | RRT_L | - | 2.0 | 4.0 | kΩ | At latch off |
| GATE Pin MAX DUTY Output | MAX_DUTY | 90 | 95 | 99 | % | RT=100kΩ |
| GATE Pin ON Resistance (as source) | RONSO | 2.5 | 5.0 | 10.0 | Ω | |
| GATE Pin ON Resistance (as sink) | RONSI | 2.0 | 4.0 | 8.0 | Ω | |
| SS Pin Source Current | ISSSO | -3.75 | -3.0 | -2.25 | μA | VSS=2.0V |
| SS Pin ON Resistance at OFF | RSS_L | - | 3.0 | 5.0 | kΩ | |
| Soft Start Ended Voltage | VSS_END | 3.52 | 3.70 | 3.88 | V | SS=SWEEP UP |
| FB Source Current | IFBSO | -115 | -100 | -85 | μA | VISENSE=0.2V, VADIM=3.0V, VFB=1.0V |
| FB Sink Current | IFBSI | 85 | 100 | 115 | μA | VISENSE=2.0V, VADIM=3.0V, VFB=1.0V |
| OCP Detect Voltage | VCS | 360 | 400 | 440 | mV | CS=SWEEP UP |
| OCP Latch Off Detect Voltage | VCS | 0.85 | 1.00 | 1.15 | V | CS=SWEEP UP |
| **【DC/DC Protection Block】** | | | | | | |
| OVP Detect Voltage | VOVP | 2.88 | 3.00 | 3.12 | V | VOVP SWEEP UP |
| OVP Detect Hysteresis | VOVP_HYS | 150 | 200 | 250 | mV | VOVP SWEEP DOWN |
| OVP Pin Leak Current | OVP_LK | -2 | 0 | 2 | μA | VOVP=4.0V, VSTB=3.0V |

●**1.9 Electrical Characteristics** (Unless otherwise specified, Ta=25°C, VCC=12V)

| Parameter | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **【LED Protection Block】** | | | | | | |
| LED OCP Detect Voltage | VLEDOCP | 2.88 | 3.0 | 3.12 | V | VISENSE=SWEEP UP |
| Over Boost Detection Voltage | VFBH | 3.84 | 4.00 | 4.16 | V | VFB=SWEEP UP |
| **【Dimming Block】** | | | | | | |
| ADIM Pin Leak Current | ILADIM | -2 | 0 | 2 | μA | VADIM=2.0V |
| ISENSE Pin Leak Current | IL_ISENSE | -2 | 0 | 2 | μA | VISENSE=4.0V |
| DIMOUT Source ON Resistance | RONSO | 5.0 | 10 | 20 | Ω | |
| DIMOUT Sink ON Resistance | RONSI | 4.0 | 8.0 | 16 | Ω | |
| **【REG50 Block】** | | | | | | |
| REG50 Output Voltage 1 | REG50_1 | 4.95 | 5.00 | 5.05 | V | IO=0mA |
| REG50 Output Voltage 2 | REG50_2 | 4.925 | 5.00 | 5.075 | V | IO=-5mA |
| REG50 Available Current | \| IREG50 \| | 5 | - | - | mA | |
| REG50_UVLO Detect Voltage | REG50_TH | 2.0 | 2.3 | 2.6 | V | VREG50=SWEEP DOWN VSTB=0V |
| REG50 Discharge Current | REG50_DIS | 3.0 | 5.0 | 7.0 | μA | STB=ON->OFF, REG50=4.0V, PWM=L |
| **【STB Block】** | | | | | | |
| STB Pin HIGH Voltage | STBH | 2.0 | - | 18 | V | |
| STB Pin LOW Voltage | STBL | -0.3 | - | 0.8 | V | |
| STB Pull Down Resistance | RSTB | 600 | 1000 | 1400 | kΩ | VSTB=3.0V |
| **【PWM Block】** | | | | | | |
| PWM Pin HIGH Voltage | PWM_H | 1.5 | - | 18 | V | |
| PWM Pin LOW Voltage | PWM_L | -0.3 | - | 0.8 | V | |
| PWM Pin Pull Down Resistance | RPWM | 600 | 1000 | 1400 | kΩ | VPWM=3.0V |
| **【FAIL Block 】** | | | | | | |
| CP Detect Voltage | VCP | 2.85 | 3.0 | 3.15 | V | VCP=SWEEP UP |
| CP Charge Current | ICP | 2.7 | 3.0 | 3.3 | μA | |

●**2.1 Pin Function**

| No. | Pin Name | IN/OUT | Function | Rating [V] |
|---|---|---|---|---|
| 1 | REG50 | Out | 5.0V output voltage pin and shutdown timer pin | -0.3 to 7 |
| 2 | STB | In | IC ON/OFF pin | -0.3 to 20 |
| 3 | OVP | In | Over voltage protection detection pin | -0.3 to 20 |
| 4 | UVLO | In | Under voltage lock out detection pin | -0.3 to 20 |
| 5 | SS | Out | Slow start setting pin | -0.3 to 7 |
| 6 | PWM | In | External PWM dimming signal input pin | -0.3 to 20 |
| 7 | CP | Out | Charge timer for abnormal state | -0.3 to 7 |
| 8 | ADIM | In | ADIM signal input pin | -0.3 to 20 |
| 9 | RT | Out | DC/DC switching frequency setting pin | -0.3 to 7 |
| 10 | FB | Out | Error amplifier output pin | -0.3 to 7 |
| 11 | ISENSE | In | LED current detection input pin | -0.3 to 7 |
| 12 | GND | - | - | |
| 13 | DIMOUT | Out | Dimming signal output for NMOS | -0.3 to VCC |
| 14 | GATE | Out | DC/DC switching output pin | -0.3 to VCC |
| 15 | CS | In | DC/DC output current detect pin, OCP input pin | -0.3 to 7 |
| 16 | VCC | In | Power supply pin | -0.3 to 20 |

●2.2 Pin ESD Type

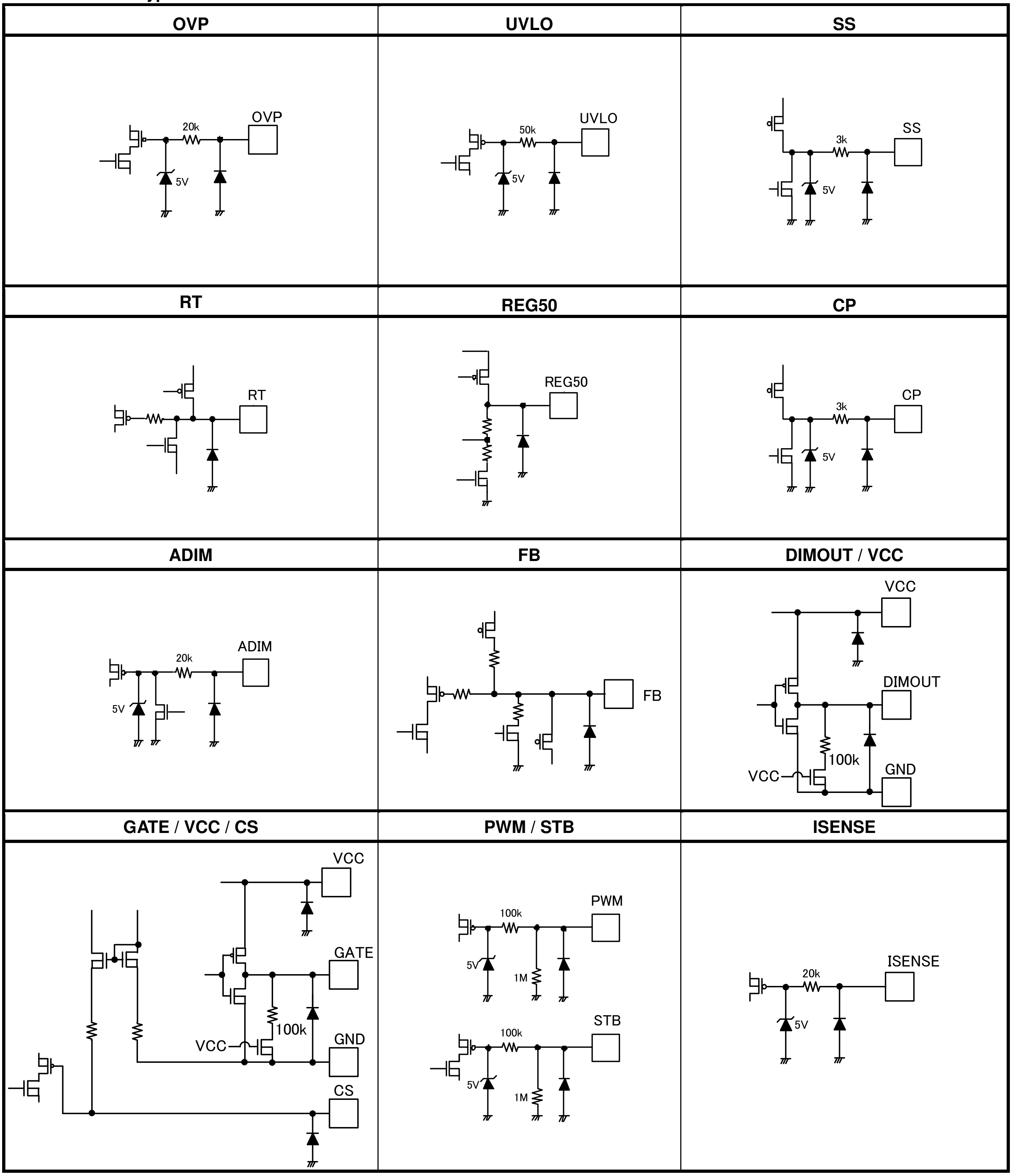



Figure 5. Pin ESD Type

●2.3 Block Diagram

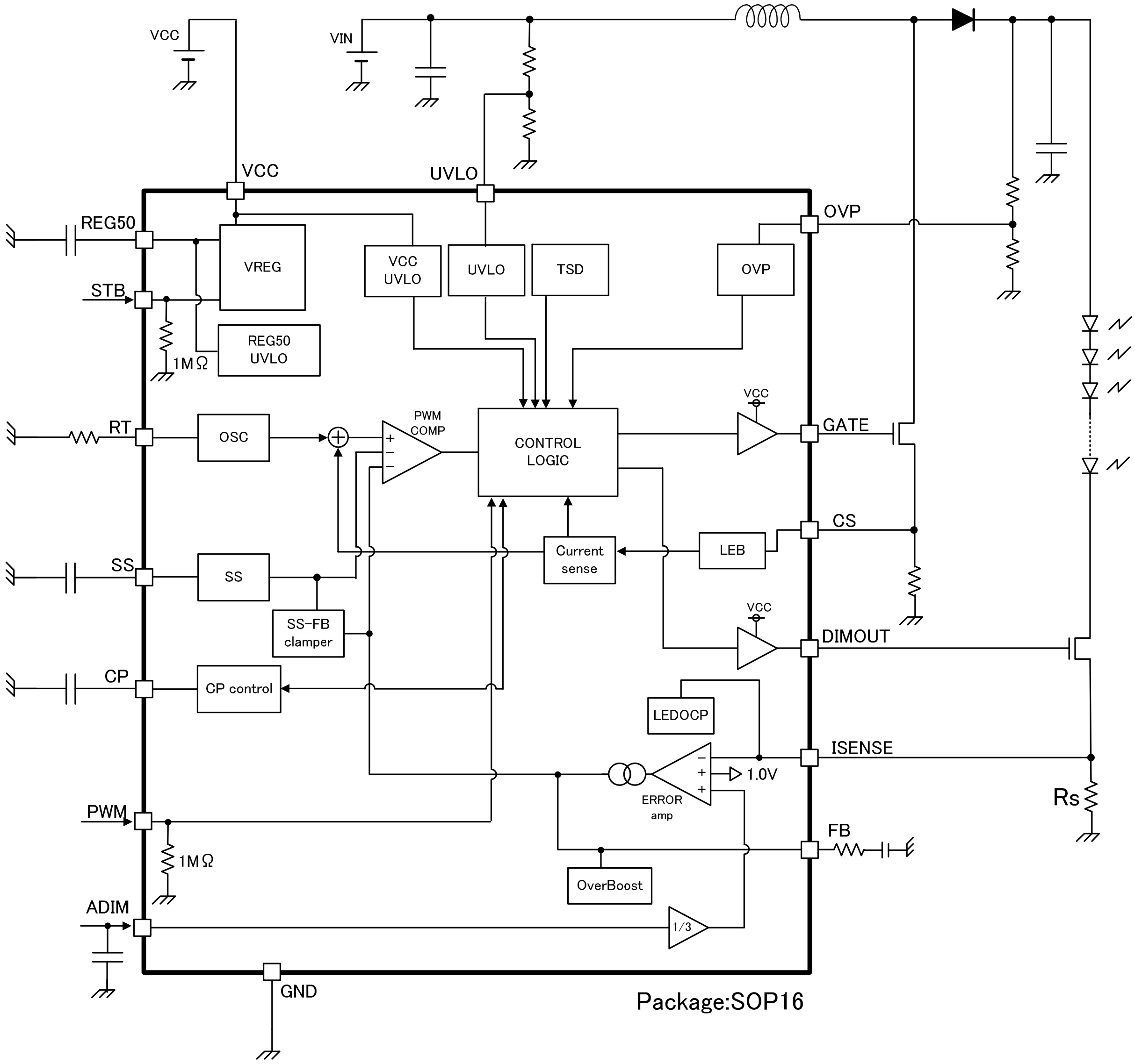



Figure 6. Block Diagram

●2.4 Typical Performance Curves (Reference data)

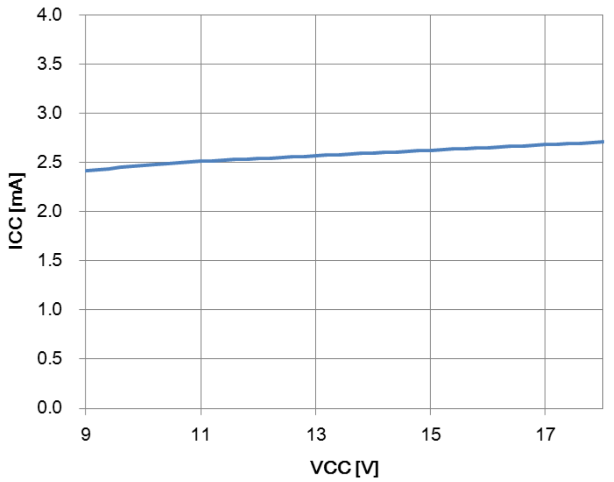



Figure 7. Circuit current (active)

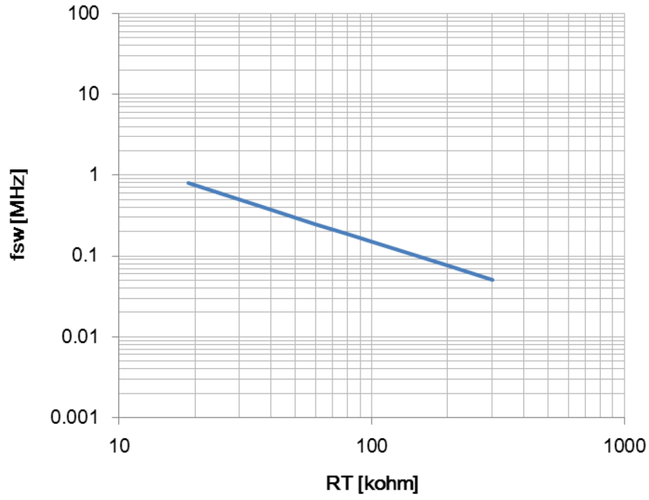



Figure 8. Fsw vs RT characteristic

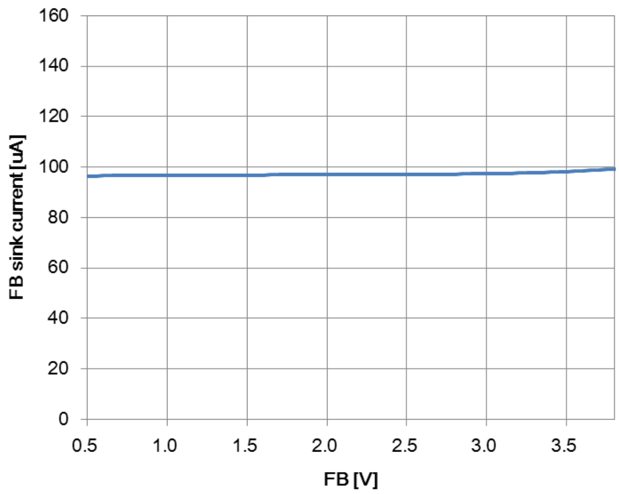



Figure 9. FB sink current vs FB voltage characteristic

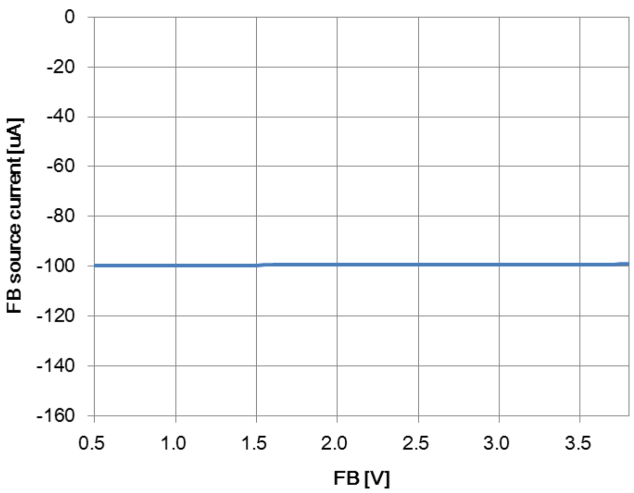



Figure 10. FB source current vs FB voltage characteristic

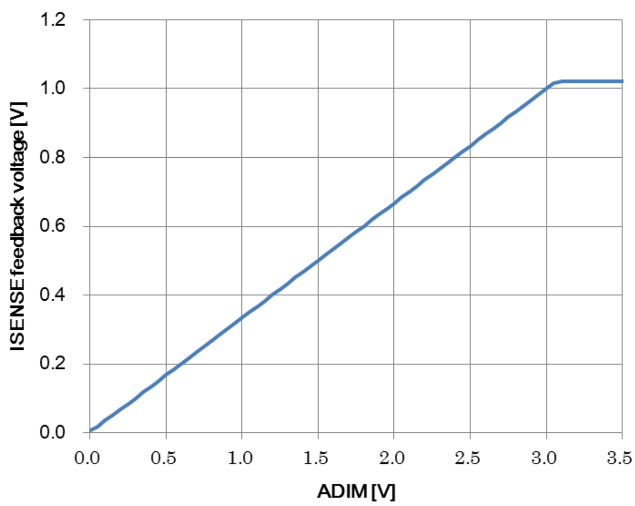



Figure 11. ISENSE feedback voltage vs ADIM voltage characteristic

## ●2.5 Pin Description

### ○Pin 1: REG50

This is the 5.0V(typ.) output pin. Available current is 5mA (min).
And this terminal is also used as timer for discharging DCDC output capacitor.
Please refer to section "3.2.2 Shutdown Method and REG50 Capacitance Setting", for detailed explanation.

### ○Pin 2: STB

This is the ON/OFF setting terminal of the IC. Input reset-signal to this terminal to reset IC from latch-off.
At startup, internal bias starts at high level, and then PWM DCDC boost starts after PWM rise edge inputs.
Note: IC status (IC ON/OFF) transits depending on the voltage inputted to STB terminal. Avoid the use of intermediate level (from 0.8V to 2.0V).
In order to discharge output voltage while STB=L and REG50UVLO=H, DIMOUT can assert High, depending on PWM logic. About discharge behavior at end, please refer to section "3.5.3 Timing Chart" or section "3.2.2 Shutdown Method and REG50 Capacitance Setting".

### ○Pin 3: OVP

The OVP terminal is the input for over-voltage protection. If OVP is more than 3.0V(typ), the over-voltage protection (OVP) will work. At the moment of these detections, it sets GATE=L, DIMOUT=L and starts to count up the abnormal interval. If OVP detection continued to count four GATE clocks, IC reaches latch off. (Please refer to "3.5.5 Timing Chart")
The OVP pin is high impedance, because the internal resistance is not connected to a certain bias.
Even if OVP function is not used, pin bias is still required because the open connection of this pin is not a fixed potential.
The setting example is separately described in the section "3.2.7 OVP Setting".
As PWM=L interval, IC operates to keep the OVP pin voltage therefore the output voltage. Please refer the section "TBD the Retaining Function of The Output Voltage".

### ○Pin 4: UVLO

Under Voltage Lock Out pin is the input voltage of the power stage. , IC starts the boost operation if UVLO is more than 3.0V(typ) and stops if lower than 2.7V(typ).
The UVLO pin is high impedance, because the internal resistance is not connected to a certain bias.
Even if UVLO function is not used, pin bias is still required because the open connection of this pin is not a fixed potential.
The setting example is separately described in the section "3.2.6 UVLO Setting"

### ○Pin 5: SS

This is the pin which sets the soft start interval of DC/DC converter. It performs the constant current charge of 3.0 μA to external capacitance Css. The switching duty of GATE output will be limited during 0V to 3.7V of the SS voltage.
So the soft start interval Tss can be expressed as follows

**$Tss = 1.23*10^6*Css$ Css: the external capacitance of the SS pin**.

The logic of SS pin asserts low is defined as the latch-off state or PWM is not input high level after STB reset release. When SS capacitance is under 1nF, take note if the in-rush current during startup is too large, or if over boost detection (FBMAXI) mask timing is too short.
Please refer to soft start behavior in the section "3.5.4 Timing Chart ".

### ○Pin 6: PWM

This is the PWM dimming signal input terminal. The high / low level of PWM pins are the following.

| State | PWM input voltage |
|---|---|
| PWM=H | PWM=1.5V to 18.0V |
| PWM=L | PWM=-0.3V to 0.8V |

### ○Pin 7: CP

Timer pin for counting the abnormal state of the over boost protection (FBMAX). If the abnormal state is detected, the CP pin starts charging the external capacitance by 3μA. As the CP voltage reaches 3.0V, IC will be latched off. (GATE=L, DIMOUT=L).
Please refer to section "3.2.8 Interval Until Latch Off Setting", for detailed explanation.

### ○Pin 8: ADIM

This is the input pin for analog dimming signal. The ISENSE feedback point is set as 1/3 of this pin bias. If more than 3.0V is input, ISENSE feedback voltage is clamped to limit to flow LED large current. In this condition, the input current is caused. Please refer to <ISENSE> terminal explanation.

### ○Pin 9: RT

This is the DC/DC switching frequency setting pin. DCDC frequency is decided by connected resistor.

○<u>The relationship between the frequency and RT resistance value **(ideal)**</u>

$$R_{RT} = \frac{15000}{f_{SW}\,[\text{kHz}]} \quad [\text{k}\Omega]$$

The oscillation setting ranges from 50kHz to 800kHz.
The setting example is separately described in the section ”3.2.5 DCDC Oscillation Frequency Setting”

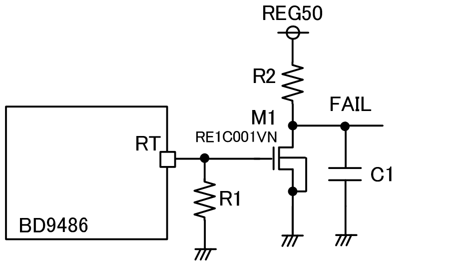
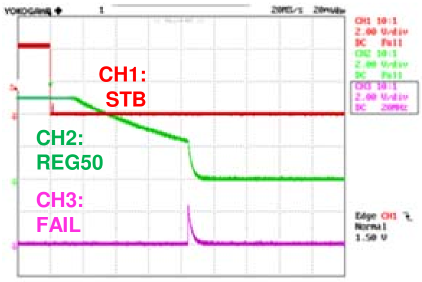



Figure 12. RT terminal circuit example

The fail logic indicating the abnormal state can be obtained by using the right circuit example. The gate capacitor is limited to 200pF. We recommend RE1C001VN for M1.The RT pin output the 2.0V(typ.) in the normal state and drops to 0V in the latch off state. When REG50 reaches to 0V,there is a point that FAIL output voltage is unstable, if this is a problem, please add C1 capacitor. Please refer to section “2.7 Behavior List of the Protect Functions” or “3.5 Timing Chart”.




### ○Pin 10: FB

This is the output terminal of error amplifier.
FB pin rises with the same slope as the SS pin during the soft-start period.
After soft -start completion (SS>3.7V), it operates as follows.

When PWM=H, it detects ISENSE terminal voltage and outputs error signal compared to analog dimming signal (ADIM).

It detects over boost (FBMAX) over FB=4.0V(typ). After the SS completion, if FB>4.0V and PWM=H continues 4clk GATE, the CP charge starts. After that, only the FB>4.0V is monitored, if CP charge continues to the CP=3.0V, IC will be latched off. (Please refer to section “3.5.6 Timing Chart”.)

The loop compensation setting is described in section "3.4 Loop Compensation".

### ○Pin 11: ISENSE

This is the input terminal for the current detection. Error amplifier compares the lower one among 1/3 of the voltage terminal ADIM analog dimming and 1.0V(typ). And it detects abnormal LED overcurrent at ISENSE=3.0V(typ) over. If GATE terminal continues during four CLKs (equivalent to 40μs at fosc = 100kHz), it becomes latch-off. (Please refer to section “3.5.7 Timing Chart”.)

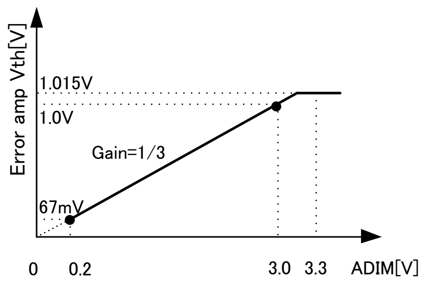



Figure 13. Relationship of the feedback voltage and ADIM

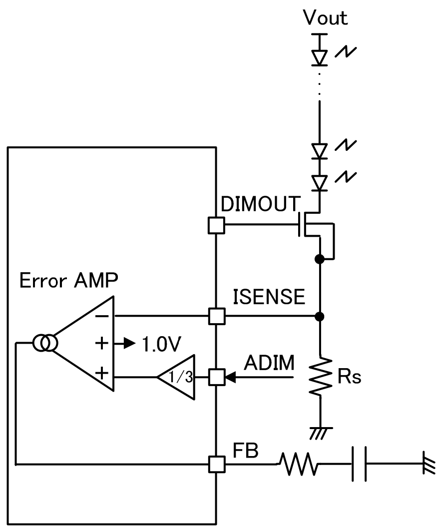



Figure 14. ISENSE terminal circuit example

### ○Pin 12: GND

This is the GND pin of the IC.

**○Pin 13: DIMOUT**

This is the output pin for external dimming NMOS. The table below shows the rough output logic of each operation state, and the output H level is VCC. Please refer to “3.5 Timing Chart” for detailed explanations, because DIMOUT logic has an exceptional behavior. Please insert the resistor $R_{DIM}$ between the dimming MOS gate to improve the over shoot of LED current, as PWM turns from low to high.

| Status | DIMOUT output |
|---|---|
| Normal | Same logic to PWM |
| Abnormal | GND Level |

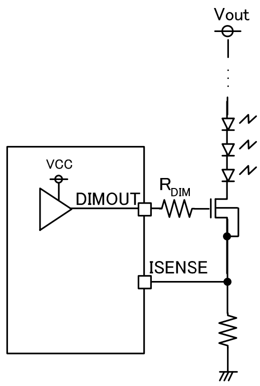


Figure 15. DIMOUT terminal circuit example

**○Pin 14: GATE**

This is the output terminal for driving the gate of the boost MOSFET. The high level is VCC. Frequency can be set by the resistor connected to RT. Refer to <RT> pin description for the frequency setting.

**○Pin 15: CS**

The CS pin has two functions.

<u>1. DC / DC current mode Feedback terminal</u>
The inductor current is converted to the CS pin voltage by the sense resistor $R_{CS}$. This voltage compared to the voltage set by error amplifier controls the output pulse.

<u>2. Inductor current limit (OCP) terminal</u>
The CS terminal also has an over current protection (OCP). If the voltage is more than 0.4V(typ.), the switching operation will be stopped compulsorily. And the next boost pulse will be restarted to normal frequency.
In addition, the CS voltage is more than 1.0V(typ.) during four GATE clocks, IC will be latch off. As above OCP operation, if the current continues to flow nevertheless GATE=L because of the destruction of the boost MOS, IC will stops the operation completely.

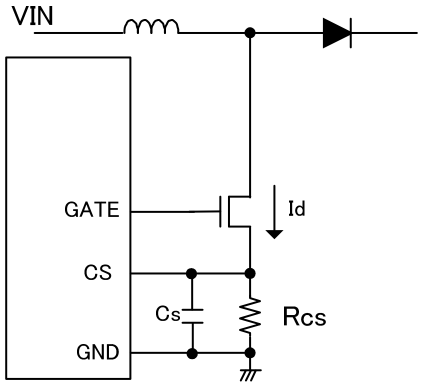


Figure 16. CS terminal circuit example

Both of the above functions are enabled after 300ns (typ) when GATE pin asserts high, because the Leading Edge Blanking function (LEB) is included into this IC to prevent the effect of noise.
Please refer to section “3.3.1 OCP Setting / Calculation Method for the Current Rating of DCDC Parts”, for detailed explanation.
If the capacitance Cs in the right figure is increased to a micro order, please be careful that the limited value of NMOS drain current Id is more than the simple calculation. Because the current Id flows not only through Rcs but also through Cs, as the CS pin voltage moves according to Id.

**○Pin 16: VCC**

This is the power supply pin of the IC. Input range is from 9V to 18V.
The operation starts at more than 7.5V(typ) and shuts down at less than 7.2V(typ)

### ●2.6 Detection Condition List of the Protect Functions (TYP Condition)

| Protect Function | Detection Pin | Detect Condition | | | Release Condition | Timer Operation | Protection Type |
|---|---|---|---|---|---|---|---|
| | | Detection Condition | PWM | SS | | | |
| **FBMAX** | FB | FB > 4.0V | H(4clk) | SS>3.7V | FB < 4.0V | CP charge | Latch off |
| **LED OCP** | ISENSE | ISENSE > 3.0V | - | - | ISENSE < 3.0V | 4clk | Latch off |
| **RT GND SHORT** | RT | RT<VRT×90% | - | - | Release RT=GND | NO | Restart by release |
| **UVLO** | UVLO | UVLO<2.7V | - | - | UVLO>3.0V | NO | Restart by release |
| **REG50UVLO** | REG50 | REG50<2.3V | - | - | REG50>2.6V | NO | Restart by release |
| **VCC UVLO** | VCC | VCC<7.2V | - | - | VCC>7.5V | NO | Restart by release |
| **OVP** | OVP | OVP>3.0V | - | - | OVP<2.8V | 4clk | Latch off |
| **OCP** | CS | CS>0.4V | - | - | - | NO | Pulse by Pulse |
| **OCP LATCH** | CS | CS>1.0V | - | - | CS<1.0V | 4clk | Latch off |

To reset the latch type protection, please set STB logic to 'L' once. Otherwise the detection of VCCUVLO, REG50UVLO is required.

The clock number of timer operation corresponds to the boost pulse clock.

### ●2.7 Behavior List of the Protect Function

| Protect Function | Operation of the Protect Function | | | |
|---|---|---|---|---|
| | DC/DC Gate Output | Dimming Transistor (DIMOUT) Logic | SS Pin | RT pin (FAILB logic) |
| **FBMAX** | Stops after latch | L after latch | discharge after latch | L after latch |
| **LED OCP** | Stops immediately | H immediately, L after latch | discharge after latch | L after latch |
| **RT GND SHORT** | Stops immediately | immediately L | Not discharge | - |
| **STB** | Stops immediately | L after REG50UVLO detects | discharge immediately | L after REG50UVLO detects |
| **UVLO** | Stops immediately | immediately L | discharge immediately | H (2.0V) |
| **REG50UVLO** | Stops immediately | immediately L | discharge immediately | H (2.0V) |
| **VCC UVLO** | Stops immediately | immediately L | discharge immediately | H (2.0V) |
| **OVP** | Stops immediately | immediately L | discharge after latch | L after latch |
| **OCP** | Stops immediately | Normal operation | Not discharge | H (2.0V) |
| **OCP LATCH** | Stops after latch | L after latch | discharge after latch | L after latch |

Please refer to section "3.5 Timing Chart" for details.

## ●3.1 Application Circuit Example

Introduce an example application using the BD9486F.

### 3.1.1 Basic Application Example

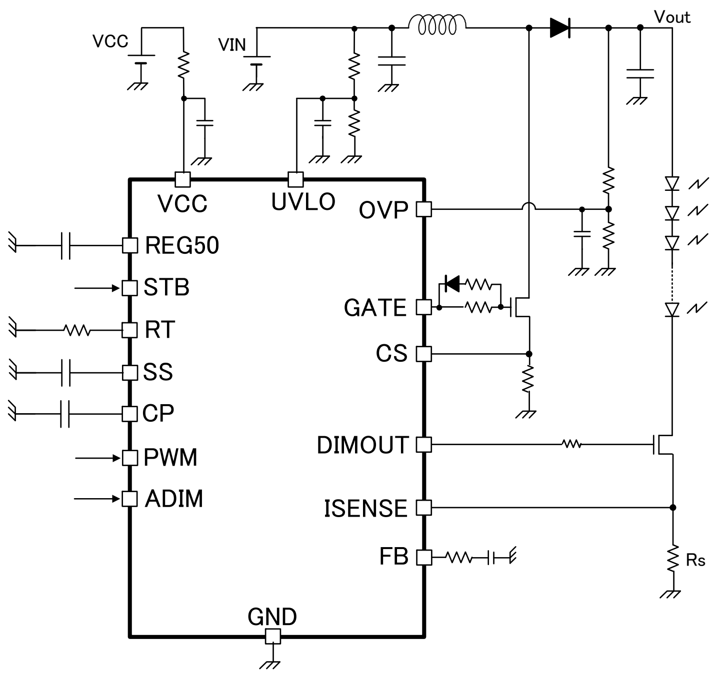



Figure 17. Basic application example

### ・3.1.2 Analog Dimming or PWM Dimming Examples

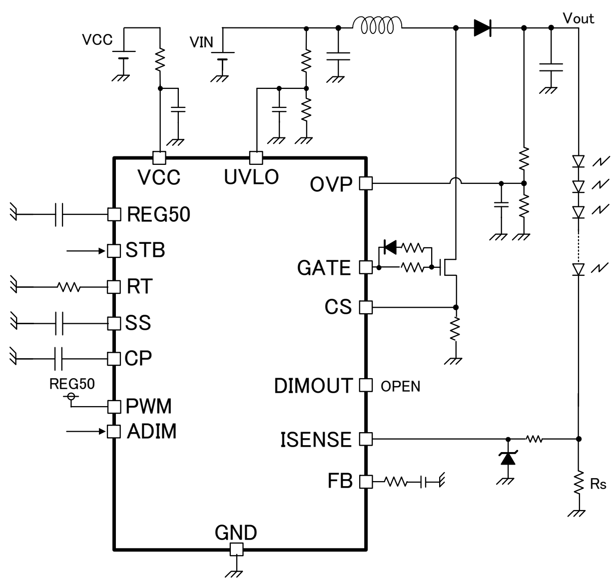



Figure 18. Example circuit for analog dimming

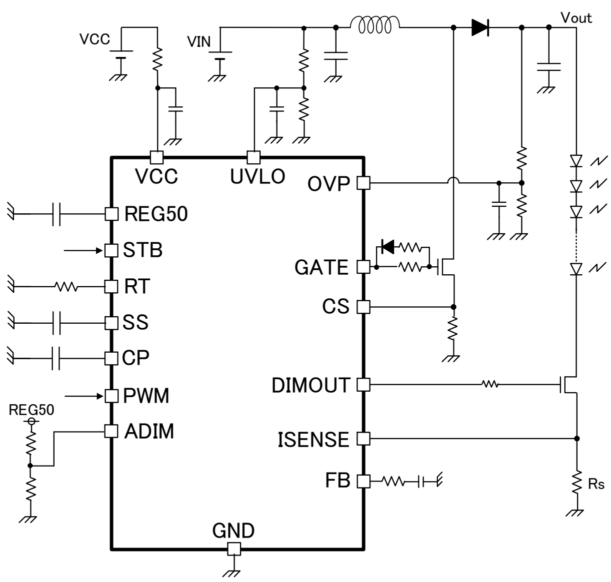



Figure 19. Example circuit for PWM dimming

## ●3.2 External Components Selection

### ●3.2.1 Start Up Operation and Soft Start External Capacitance Setting

The below explanation is the start up sequence of this IC

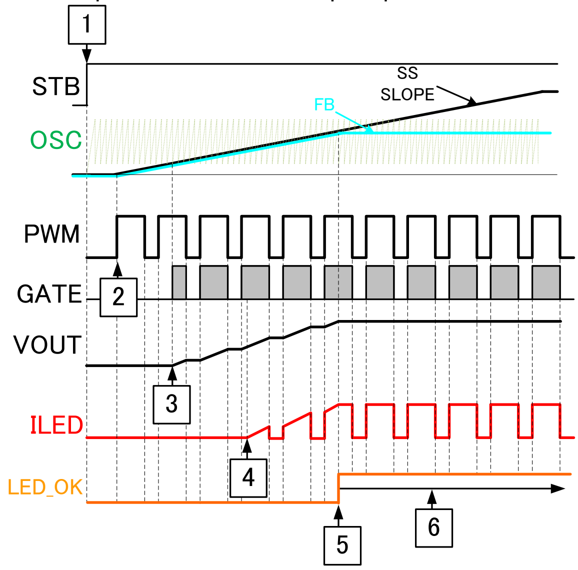



Figure 20. Startup waveform

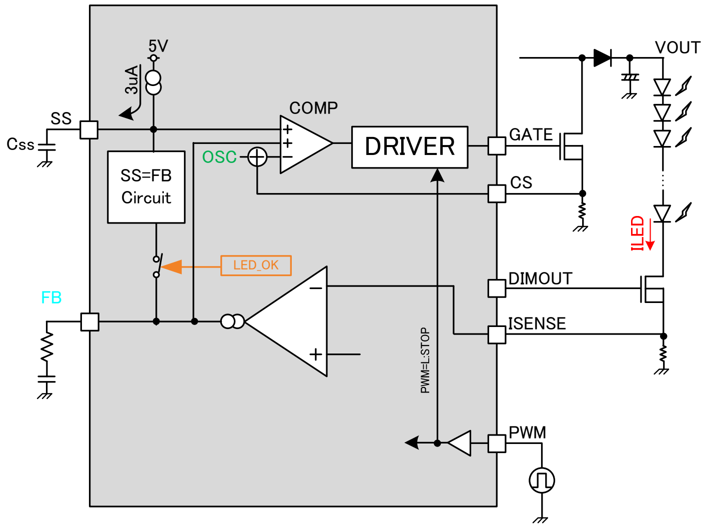



Figure 21. Circuit behavior at startup

**○Explanation of start up sequence**

1. Reference voltage REF50 starts by STB=H.
2. SS starts to charge at the time of first PWM=H. At this moment, the SS voltage of slow-start starts to equal FB voltage,and the circuit becomes FB=SS regardless of PWM logic.
3. When FB=SS reaches the lower point of internal sawtooth waveform, GATE terminal outputs pulse and starts to boost VOUT.
4. It boosts VOUT and VOUT reaches the voltage to be able to flow LED current.
5. If LED current flows over decided level, FB=SS circuit disconnects and startup behavior completes.
6. Then it works normal operation by feedback of ISENSE terminal. If LED current doesn't flow when SS becomes over 3.7V, SS=FF circuit completes forcibly and FBMAX protection starts.

**○Method of setting SS external capacitance**

According to the sequence described above, start time Tss that startup completes with FB=SS condition is the time that FB voltage reaches the feedback point.
The capacitance of SS terminal is defined as Css and the feedback voltage of FB terminal is defined as VFB. The equality on $T_{FB}$ is as follows.

$$T_{SS} = \frac{C_{SS}[\mu F] \times VFB[V]}{3[\mu A]} \quad [sec]$$

If Css is set to a very small value, rush current flows into the inductor at startup.
On the contrary, if Css is enlarged too much, LED will light up gradually.
Since Css differs in the constant set up with the characteristic searched for and differs also by factors, such as a voltage rise ratio, an output capacitance, DCDC frequency, and LED current, please confirm with the system.

**【Setting example】**

When Css=0.1μF,Iss=3μA,and startup completes at VFB=3.7V, SS setting time is as follows.

$$T_{SS} = \frac{0.1 \times 10^{-6}[F] \times 3.7[V]}{3 \times 10^{-6}[A]} = 0.123 \quad [sec]$$

## ●3.2.2 Shutdown Method and REG50 Capacitance Setting

When this IC shuts down, VOUT discharge function works. Indicated below is the sequence.

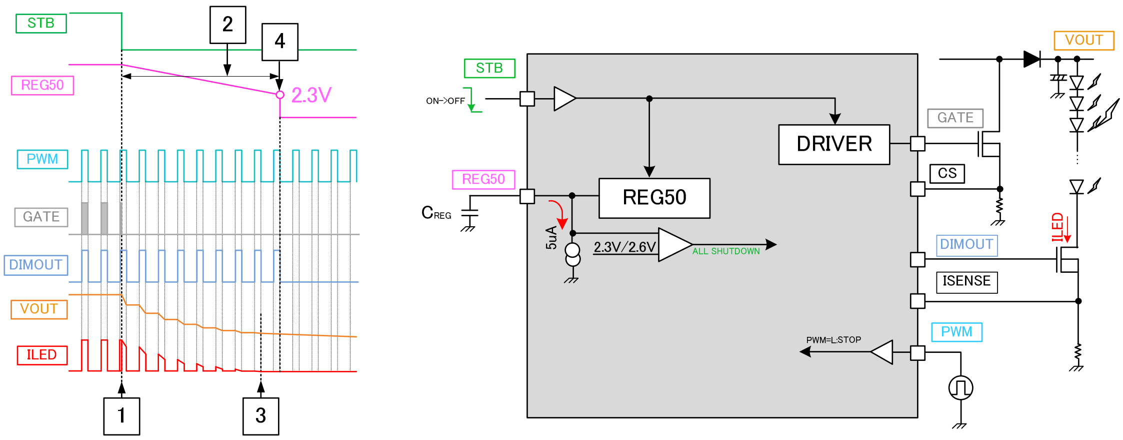



Figure 22. The waveform and diagram at shutdown

### ○Sequence explanation of shutdown

1. When STB=L, GATE and REG50 stop.
2. While STB=L and REG50UVLO=H, DIMOUT asserts the same logic of PWM. And VOUT is discharged until REG50=5.0V reaches 2.3V by -5µA(typ.).
3. When VOUT is discharged enough by ILED, ILED doesn’t get to flow.
4. When REG50 voltage reaches under 2.3V(typ), whole system is shutdown.

### ○Setting method of REG50 capacitance

When REG50 terminal capacitance is defined as $C_{REG}$ , shutdown time $T_{OFF}$ is decided by the following equation.

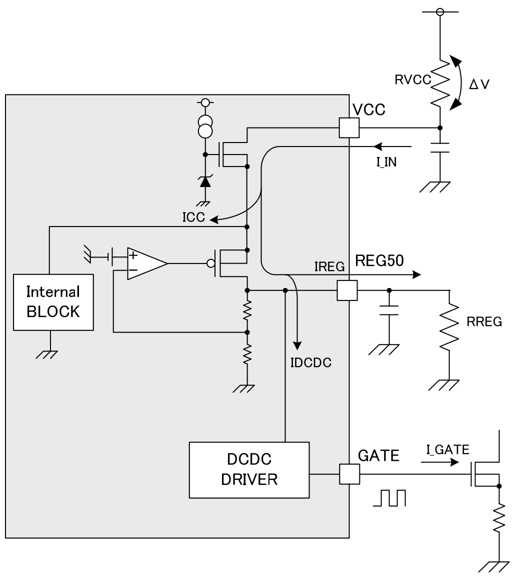
$$T_{OFF} = \frac{C_{REG}[\mu F] \times (5.0 - 2.3)\,[V]}{5\,[\mu A]} \quad [\mathrm{sec}]$$

When discharge function is used, PWM signal must be continuously inputted after STB=L.
VOUT discharge time is longest when PWM is set on mininum DUTY.
Please set $C_{REG}$ capacitance value with margin so that the system is shutdown after VOUT is discharged enough.
Please refer “1.6External Components Recommended Range” when setting $C_{REG}$ capacitance.

## ●3.2.3 VCC Series Resistance Setting

Here are the following effects of inserting series resistor Rvcc into VCC line.
(i) In order to drop the voltage VCC, it is possible to suppress the heat generation of the IC.
(ii) It can limit the inflow current to VCC line.
However, if resistance RVCC is set bigger, VCC voltage becomes under minimum operation voltage (VCC<9V). RVCC must be set to an appropriate series resistance.
Especially, after STB is set to High, IREG may become large and VCC may fall greatly in the section charged to the capacitor of REG50 terminal depending on the external circuit of a VCC terminal.
Even in such a case, please set up to be set to VCC>9V in an operating condition.

IC’s inflow current line I_IN has the following inflow lines.
・IC’s circuit current···ICC
・Current of RREG connected to REG50···IREG
・Current to drive FET’s Gate···I_GATE
These decide the voltage ΔV at RVCC.
VCC terminal voltage at that time can be expressed as follows.




$$VCC[V] = VIN[V] - (ICC[A] + IDCDC[A] + IREG[A]) \times RVCC[\Omega] \quad > \quad 9[V]$$

Figure 23. VCC series resistance circuit example

Here, judgement is the 9V minimum operation voltage.
Please consider a sufficient margin when setting the series resistor of VCC.

【setting example】

Above equation is translated as follows.

$$RVCC[\Omega] < \frac{VIN[V]-9[V]}{ICC[A]+IDCDC[A]+IREG[A]}$$

When VIN=12V, ICC=2.0mA, IREG=50mA and IDCDC=2mA, RVCC's value is calculated as follows.

$$RVCC[\Omega] < \frac{12[V]-9[V]}{0.002[A]+0.002[A]+0.050[A]} = 56\ [\Omega]$$

(ICC is 2.6mA(typ.)) . Please set each values with tolerance and margin.

●3.2.4 LED current setting

LED current can be adjusted by setting the resistance $R_S$ [Ω] which connects to ISENSE pin and ADIM[V].

**Relationship between $R_S$ and $I_{LED}$ current**

With DC dimming (ADIM<3.0V)

$$R_{ISENSE} = \frac{1}{3} \cdot \frac{ADIM[V]}{I_{LED}[A]} [\Omega]$$

Without DC dimming (ADIM>3.0V)

$$R_{ISENSE} = \frac{1.015[V]}{I_{LED}[A]} [\Omega]$$

【setting example】

If $I_{LED}$ current is 200mA and ADIM is 2.0V, we can calculate $R_{ISENSE}$ as below.

$$R_{ISENSE} = \frac{1}{3} \cdot \frac{ADIM[V]}{I_{LED}[A]} = \frac{1}{3} \frac{2.0[V]}{0.2[A]} = 3.33[\Omega]$$

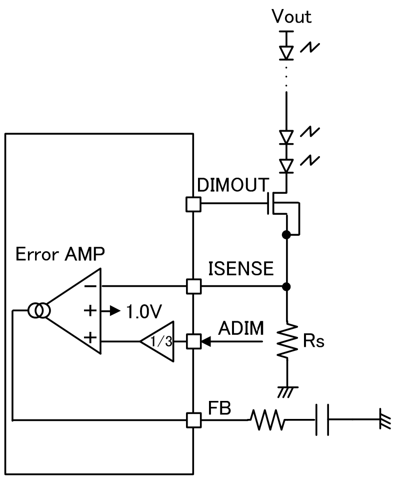



Figure 24. LED current setting example

●3.2.5 DCDC Oscillation Frequency Setting

$R_{RT}$ which connects to RT pin sets the oscillation frequency $f_{SW}$ of DCDC.

○**Relationship between frequency $f_{SW}$ and RT resistance (ideal)**

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

【setting example】

When DCDC frequency fsw is set to 200kHz, $R_{RT}$ is as follows.

$$R_{RT} = \frac{15000}{f_{sw}[kHz]} = \frac{15000}{200[kHz]} = 75 \quad [k\Omega]$$

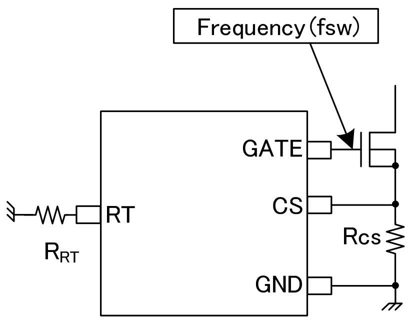



Figure 25. RT terminal setting example

●**3.2.6 UVLO Setting**

Under Voltage Lock Out pin is the input voltage of the power stage. IC starts boost operation if UVLO is more than 3.0V(typ.) and stops if lower than 2.7V(typ.).
The UVLO pin is high impedance, because the internal resistance is not connected to a certain bias.
So, the bias by the external components is required, because the open connection of this pin is not a fixed potential.

Detection voltage is set by dividing resistors R1 and R2. The resistor values can be calculated by the formula below.

○**UVLO detection equation**

As VIN decreases, R1 and R2 values are set in the following formula by the $VIN_{DET}$ that UVLO detects.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.7[V])}{2.7[V]} \quad [k\Omega]$$

○**UVLO release equation**

R1 and R2 setting is decided by the equation above. The equation of UVLO release voltage is as follows.

$$VIN_{CAN} = 3.0V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

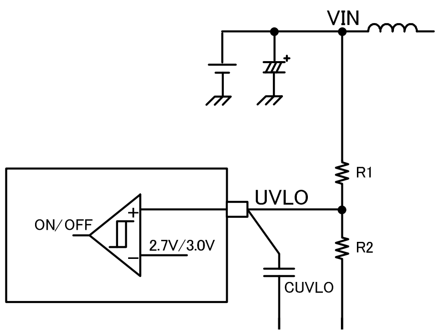


Figure 26. UVLO setting example

【**setting example**】

If the normal input voltage, VIN is 24V, the detect voltage of UVLO is 18V, R2 is 30kΩ, R1 is calculated as follows.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.7[V])}{2.7[V]} = 30[k\Omega] \times \frac{(18[V] - 2.7[V])}{2.7[V]} = 170.0 \quad [k\Omega]$$

By using these R1 and R2, the release voltage of UVLO, $VIN_{CAN}$, can be calculated too as follows.

$$VIN_{CAN} = 3.0[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 3.0[V] \times \frac{170[k\Omega] + 30[k\Omega]}{30[k\Omega]}[V] = 20.0 \quad [V]$$

### ●3.2.7 OVP Setting

The OVP terminal is the input for over-voltage protection of output voltage.
The OVP pin is high impedance, because the internal resistance is not connected to a certain bias.

Detection voltage of VOUT is set by dividing resistors R1 and R2. The resistor values can be calculated by the formula below.

**○OVP detection equation**

If VOUT is boosted abnormally, $VOVP_{DET}$, the detect voltage of OVP, R1, R2 can be expressed by the following formula.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} \quad [k\Omega]$$

**○OVP release equation**

By using R1 and R2 in the above equation, the release voltage of OVP, $VOVP_{CAN}$ can be expressed as follows.

$$VOVP_{CAN} = 2.8V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

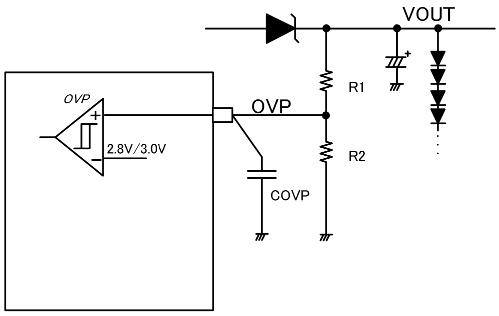



Figure 27. OVP setting example

**【setting example】**

If the normal output voltage, VOUT is 40V, the detect voltage of OVP is 48V, R2 is 10k ohm, R1 is calculated as follows.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} = 10[k\Omega] \times \frac{(48[V] - 3[V])}{3[V]} = 150[k\Omega]$$

By using these R1 and R2, the release voltage of OVP, $VOVP_{CAN}$ can be calculated as follows.

$$VOVP_{CAN} = 2.8[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 2.8[V] \times \frac{10[k\Omega] + 150[k\Omega]}{10[k\Omega]}[V] = 44.8[V]$$

### ●3.2.8 Interval Until Latch Off Setting

About over boost protection (FBMAX), the capacitance value of CP terminal can set the time of latch-off. About the behavior from abnormal detection to latch-off, please refer to the section “3.5.6 Timing Chart”.

The condition FB>4.0V(typ.) and PWM=H continues more than four GATE clocks, the CP terminal charge is started by 3µA. After that, only the FB voltage is monitored. As the CP voltage reaches to 3.0V(typ.), IC will be latched off.
The time $LATCH_{TIME}$ to reach to latch-off is set by CP terminal capacitance as follows.

$$LATCH_{TIME} = \frac{C_{CP}[\mu F] \cdot 3.0[V]}{3.0[\mu A]} \ [sec]$$

**【setting example】**

If the capacitor of CP pin is 0.47µF, the timer latch interval is as follows.

$$LATCH_{TIME} = \frac{0.47[\mu F] \cdot 3.0[V]}{3.0[\mu A]} = 470[msec]$$

## ●3.3 DCDC Parts Selection

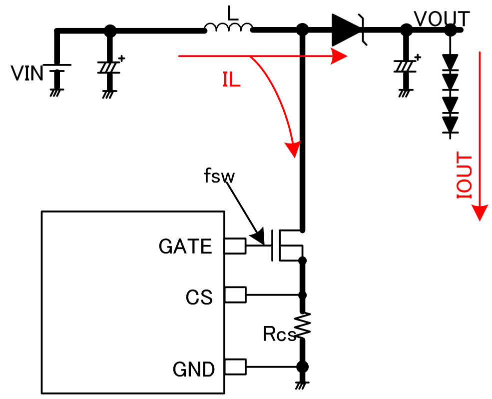
### 3.3.1. OCP Setting / Calculation Method for the Current Rating of DCDC Parts

OCP detection stops the switching when the CS pin voltage is more than 0.4V. The resistor value of CS pin, $R_{CS}$ needs to be considered by the coil L current. And the current rating of DCDC external parts is required more than the peak current of the coil.
Shown below are the calculation method of the coil peak current, the selection method of Rcs (the resistor value of CS pin) and the current rating of the external DCDC parts at Continuous Current Mode.

**(the calculation method of the coil peak current, Ipeak at Continuous Current Mode)**

At first, since the ripple voltage at CS pin depends on the application condition of DCDC, the following variables are used.
Vout voltage=VOUT[V]
LED total current=IOUT[A]
DCDC input voltage of the power stage =VIN[V]
Efficiency of DCDC =η[%]
And then, the average input current IIN is calculated by the following equation.

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$




And the ripple current of the inductor L (ΔIL[A]) can be calculated by using DCDC the switching frequency, fsw, as follows.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

On the other hand, the peak current of the inductor Ipeak can be expressed as follows.

$$\boxed{Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} \quad [A]} \quad \cdots (1)$$

Therefore, the bottom of the ripple current Imin is

$$Imin = I_{IN}[A] - \frac{\Delta IL[A]}{2} \quad \text{or } 0$$

If Imin>0, the operation mode is CCM (Continuous Current Mode), otherwise the mode is DCM (Discontinuous Current Mode).

**(the selection method of Rcs at Continuous Current Mode)**

Ipeak flows into Rcs and that causes the voltage signal to CS pin. (Please refer to the timing chart at the right)
Peak voltage VCSpeak is as follows.

$$VCS_{peak} = Rcs \times Ipeak \quad [V]$$

As this VCSpeak reaches 0.4V, the DCDC output stops the switching.
Therefore, Rcs value is necessary to meet the condition below.

$$\boxed{Rcs \times Ipeak\,[V] << 0.4[V]}$$

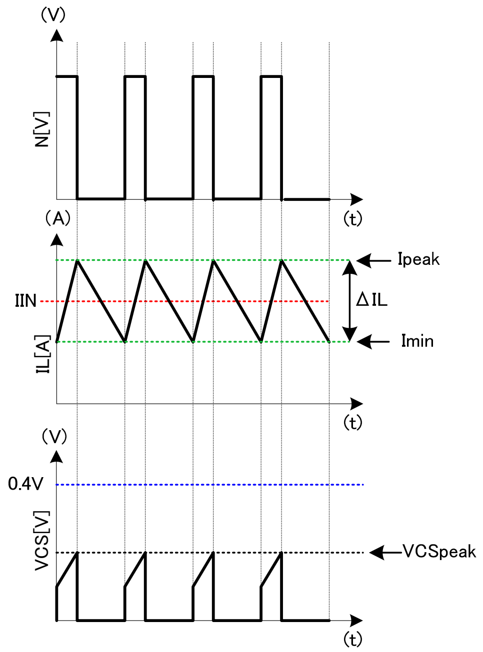



Figure 28. Coil current waveform

**(the current rating of the external DCDC parts)**

The peak current as the CS voltage reaches OCP level (0.4V) is defined as Ipeak_det.

$$I_{peak\_det} = \frac{0.4[V]}{Rcs[\Omega]} \quad [A] \quad \cdots (2)$$

The relationship among Ipeak (equation (1)), Ipeak_det (equation (2)) and the current rating of parts is required to meet the following

$$I_{peak} << I_{peak\_det} << \text{The current rating of parts}$$

Please make the selection of the external parts such as FET, Inductor, diode meet the above condition.

**[setting example]**
Output voltage = VOUT [V] = 40V
LED total current = IOUT [A] = 0.48V
DCDC input voltage of the power stage = VIN [V] = 24V
Efficiency of DCDC =η[%] = 90%
Averaged input current IIN is calculated as follows.

$$I_{IN}[A] = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} = \frac{40[V] \times 0.48[A]}{24[V] \times 90[\%]} = 0.89 \quad [A]$$

If the switching frequency, $f_{SW}$ = 200kHz, and the inductor, L=100μH, the ripple current of the inductor L (ΔIL[A]) can be calculated as follows.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} = \frac{(40[V] - 24[V]) \times 24[V]}{100 \times 10^{-6}[H] \times 40[V] \times 200 \times 10^{3}[Hz]} = 0.48 \quad [A]$$

Therefore the inductor peak current, Ipeak is

$$\boxed{Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2}[A] = 0.89[A] + \frac{0.48[A]}{2} = 1.13 \quad [A]}$$ …calculation result of the peak current

If Rcs is assumed to be 0.3Ω

$$\boxed{VCS_{peak} = Rcs \times Ipeak = 0.3[\Omega] \times 1.13[A] = 0.339 \quad [V] << 0.4V}$$ …Rcs value confirmation

The above condition is met.
And Ipeak_det, the current OCP works, is

$$I_{peak\_det} = \frac{0.4[V]}{0.3[\Omega]} = 1.33 \quad [A]$$

If the current rating of the used parts is 2A,

$I_{peak} << I_{peak\_det} <<$ The current rating $\boxed{= 1.13[A] << 1.33[A] << 2.0[A]}$ …current rating confirmation of DCDC parts

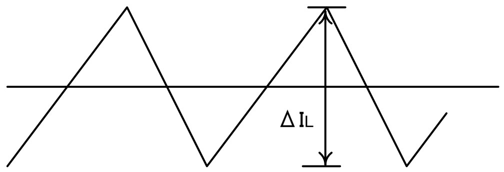
This inequality meets the above relationship. The parts selection is proper.
And $I_{MIN}$, the bottom of the IL ripple current, can be calculated as follows.

$$I_{MIN} = I_{IN}[A] - \frac{\Delta IL[A]}{2}[A] = 1.13[A] - 0.48[A] = 0.65[A] >> 0$$

This inequality implies that the operation is continuous current mode.

### 3.3.2. Inductor Selection

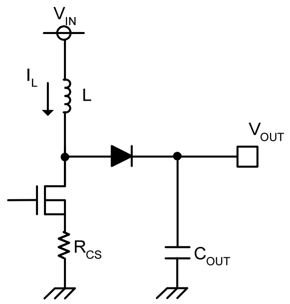
The inductor value affects the input ripple current. As shown in section 3.3.1,




$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$

$$Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} \quad [A]$$




Where
L: coil inductance [H] $V_{OUT}$: DCDC output voltage [V]
$V_{IN}$: input voltage [V]
$I_{OUT}$: output load current (the summation of LED current) [A]
$I_{IN}$: input current [A] $f_{SW}$: oscillation frequency [Hz]

Figure 29. Inductor current waveform and diagram

In continuous current mode, ⊿IL is set to 30% to 50% of the output load current in many cases.
In using smaller inductor, the boost is operated by the discontinuous current mode in which the coil current returns to zero at every period.

*The current exceeding the rated current value of inductor flown through the coil causes magnetic saturation, results in decreasing in efficiency. Inductor needs to be selected to have such adequate margin that peak current does not exceed the rated current value of the inductor.
*To reduce inductor loss and improve efficiency, inductor with low resistance components (DCR, ACR) needs to be selected

### 3.3.3. Output Capacitance Cout Selection

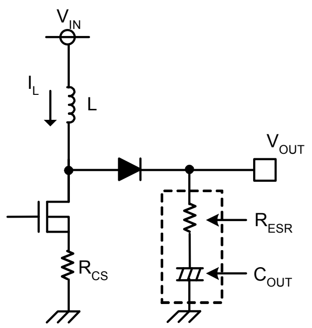



Figure 30. Output capacitor diagram

Output capacitor needs to be selected in consideration of equivalent series resistance required to even the stable area of output voltage or ripple voltage. Be aware that set LED current may not be flown due to decrease in LED terminal voltage if output ripple component is high.
Output ripple voltage □$V_{OUT}$ is determined by Equation (4):

$$\Delta Vout = \Delta IL \times R_{ESR}[V] \quad \cdot \cdot \cdot \cdot \cdot \quad (4)$$

When the coil current is charged to the output capacitor as MOS turns off, much output ripple is caused. Much ripple voltage of the output capacitor may cause the LED current ripple.

* Rating of capacitor needs to be selected to have adequate margin against output voltage.
*To use an electrolytic capacitor, adequate margin against allowable current is also necessary. Be aware that the LED current is larger than the set value transitionally in case that LED is provided with PWM dimming especially.

### 3.3.4. MOSFET Selection

There is no problem if the absolute maximum rating is larger than the rated current of the inductor L, or is larger than the sum of the tolerance voltage of $C_{OUT}$ and the rectifying diode $V_F$. The product with small gate capacitance (injected charge) needs to be selected to achieve high-speed switching.
* One with over current protection setting or higher is recommended.
* The selection of one with small on resistance results in high efficiency.

### 3.3.5. Rectifying Diode Selection

A schottky barrier diode which has current ability higher than the rated current of L, reverse voltage larger than the tolerance voltage of $C_{OUT}$, and low forward voltage VF especially needs to be selected.

### ●3.4.Loop Compensation

A current mode DCDC converter has each one pole (phase lag) $f_p$ due to CR filter composed of the output capacitor and the output resistance (= LED current) and zero (phase lead) $f_Z$ by the output capacitor and the ESR of the capacitor. Moreover, a step-up DCDC converter has RHP zero (right-half plane zero point) $f_{ZRHP}$ which is unique with the boost converter. This zero may cause the unstable feedback. To avoid this by RHP zero, the loop compensation that the cross-over frequency $f_c$, set as follows, is suggested.

**fc = $f_{ZRHP}$ /5 ($f_{ZRHP}$: RHP zero frequency)**

Considering the response speed, the calculated constant below is not always optimized completely. It needs to be adequately verified with an actual device.

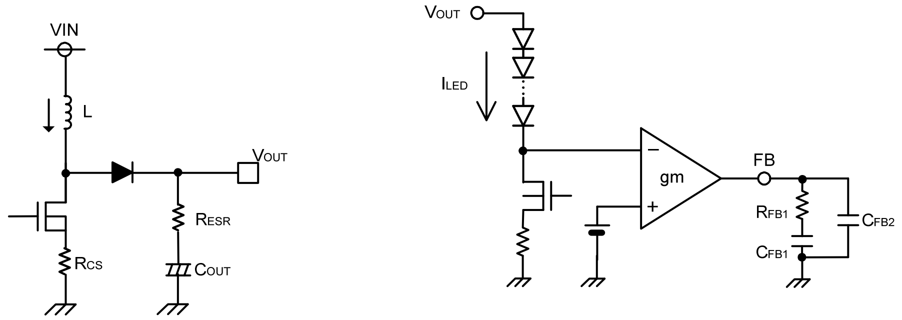



Figure 31. Output stage and error amplifier diagram

i. Calculate the pole frequency fp and the RHP zero frequency $f_{ZRHP}$ of DC/DC converter

$$f_p = \frac{I_{LED}}{2\pi \times V_{OUT} \times C_{OUT}} \text{ [Hz]} \qquad f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi \times L \times I_{LED}} \text{ [Hz]}$$

Where $I_{LED}$ = the summation of LED current, $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$ (Continuous Current Mode)

ii. Calculate the phase compensation of the error amp output ($f_c$ = $f_{ZRHP}$/5)

$$R_{FB1} = \frac{f_{RHZP} \times R_{CS} \times I_{LED}}{5 \times f_p \times gm \times V_{OUT} \times (1-D)} \text{ [}\Omega\text{]}$$

$$C_{FB1} = \frac{1}{2\pi \times R_{FB1} \times f_c} = \frac{5}{2\pi \times R_{FB1} \times f_{ZRHP}} \text{[F]}$$

$$gm = 4.0 \times 10^{-4} \text{[S]}$$

Above equation is described for lighting LED without the oscillation. The value may cause much error if the quick response for the abrupt change of dimming signal is required.
To improve the transient response, $R_{FB1}$ needs to be increased, and $C_{FB1}$ needs to be decreased. It needs to be adequately verified with an actual device in consideration of variation from parts to parts since phase margin is decreased.

## ●3.5.Timing Chart

### 3.5.1 PWM Start up 1 (Input PWM Signal After Input STB Signal)

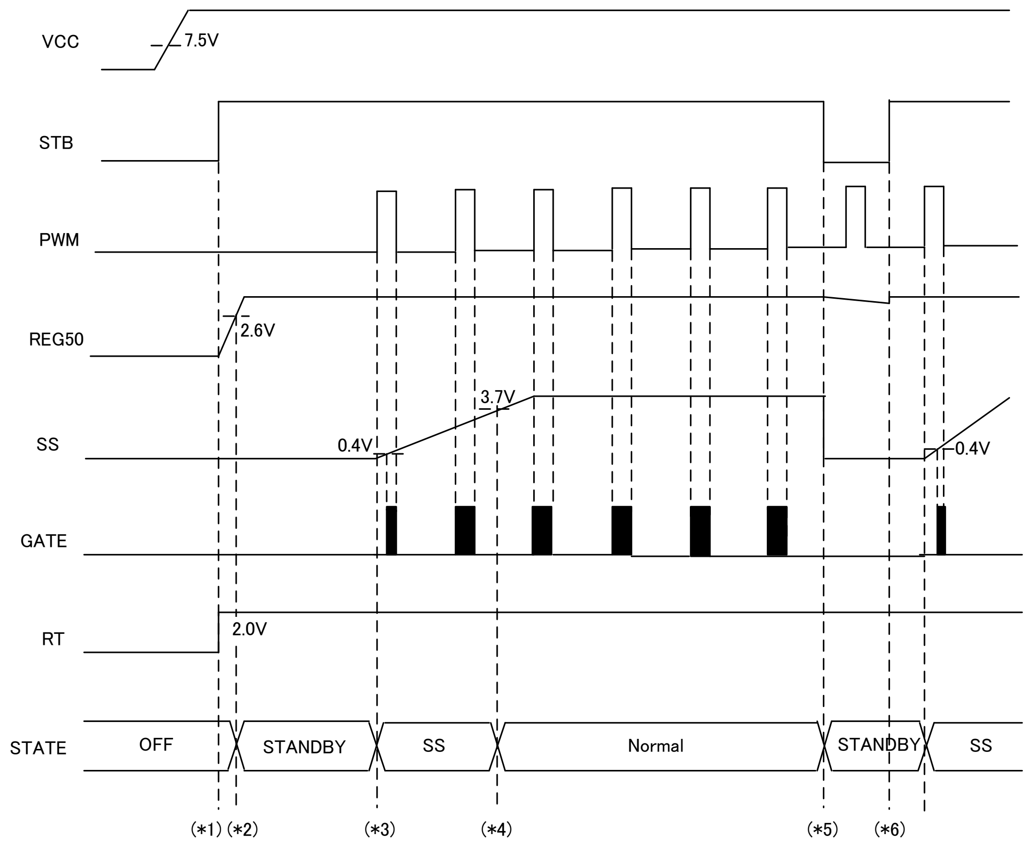



Figure 32. PWM Start up 1 (Input PWM Signal After Input STB Signal)

(*1)…REG50 starts up when STB is changed from Low to High. In the state where the PWM signal is not inputted, SS terminal is not charged and DCDC doesn't start to boost, either.

(*2)…When REG50 is more than 2.6V, the reset signal is released.

(*3)…The charge of the pin SS starts at the positive edge of PWM=L to H, and the soft start starts. The GATE pulse outputs only during the corresponding PWM=H. And while the SS is less than 0.4V, the pulse does not output. The pin SS continues charging in spite of the assertion of PWM or OVP level.

(*4)…The soft start interval will end if the voltage of the pin SS, Vss reaches 3.7V. By this time, it boosts $V_{OUT}$ to the voltage where the set LED current flows. The abnormal detection of FBMAX starts to be monitored.

(*5)…As STB=L, the boost operation is stopped instantaneously. (Discharge operation continues in the state of STB=L and REGUVLO=L. Please refer to section 3.5.3)

(*6)…In this diagram, before the charge period is completed, STB is changed to High again. As STB=H again, the boost operation restarts the next PWM=H. It is the same operation as the timing of (*2). (For capacitance setting of SS terminal, please refer to section 3.2.1.

### 3.5.2 PWM Start Up 2 (Input STB Signal after Inputted PWM Signal)

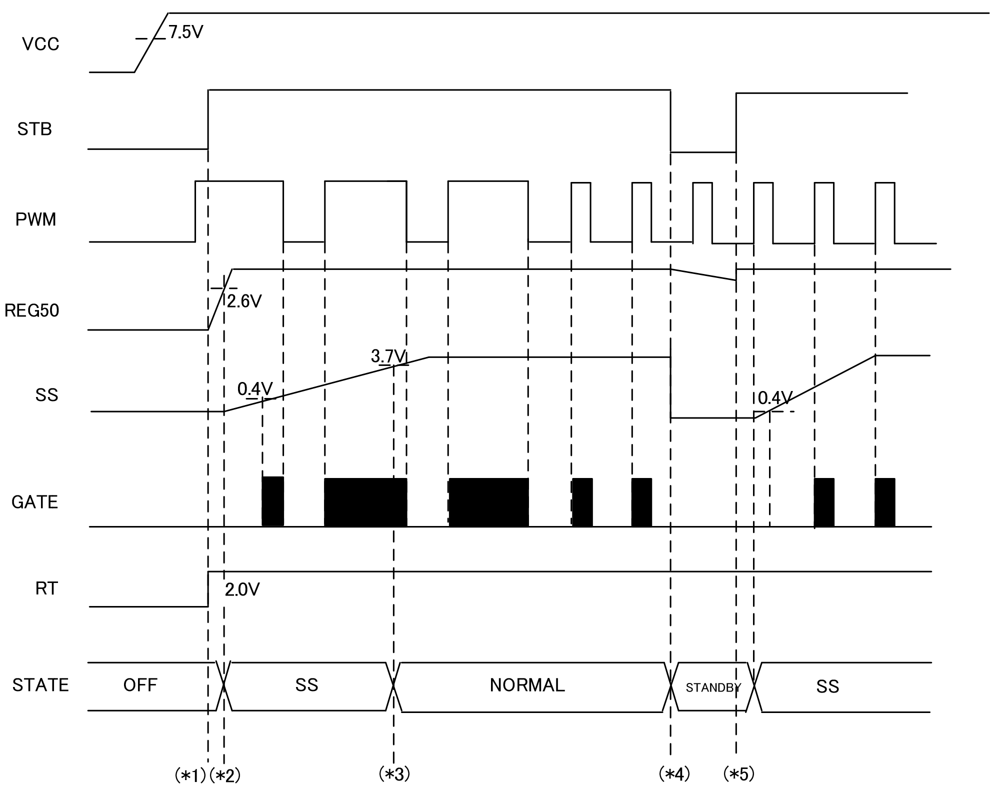



Figure 33. PWM Start Up 2 (Input STB Signal after Inputted PWM Signal)

(*1)…REG50 starts up when STB=H.

(*2)…When REG50UVLO releases or PWM is inputted to the edge of PWM=L→H, SS charge starts and soft start period is started. The GATE pulse outputs only during the corresponding PWM=H. And while the SS is less than 0.4V, the pulse does not output. The pin SS continues charging in spite of the assertion of PWM or OVP level.

(*3)…The soft start interval will end if the voltage of the pin SS, Vss reaches 3.7V. By this time, it boosts $V_{OUT}$ to the point where the set LED current flows. The abnormal detection of FBMAX starts to be monitored.

(*4)…As STB=L, the boost operation is stopped instantaneously (GATE=L, SS=L). (Discharge operation works in the state of STB=L and REG50UVLO=H. Please refer to section 3.5.3)

(*5)…In this diagram, before the discharge period is completed, STB is changed to High again. As STB=H again, operation will be the same as the timing of (*1).

### 3.5.3 Turn Off

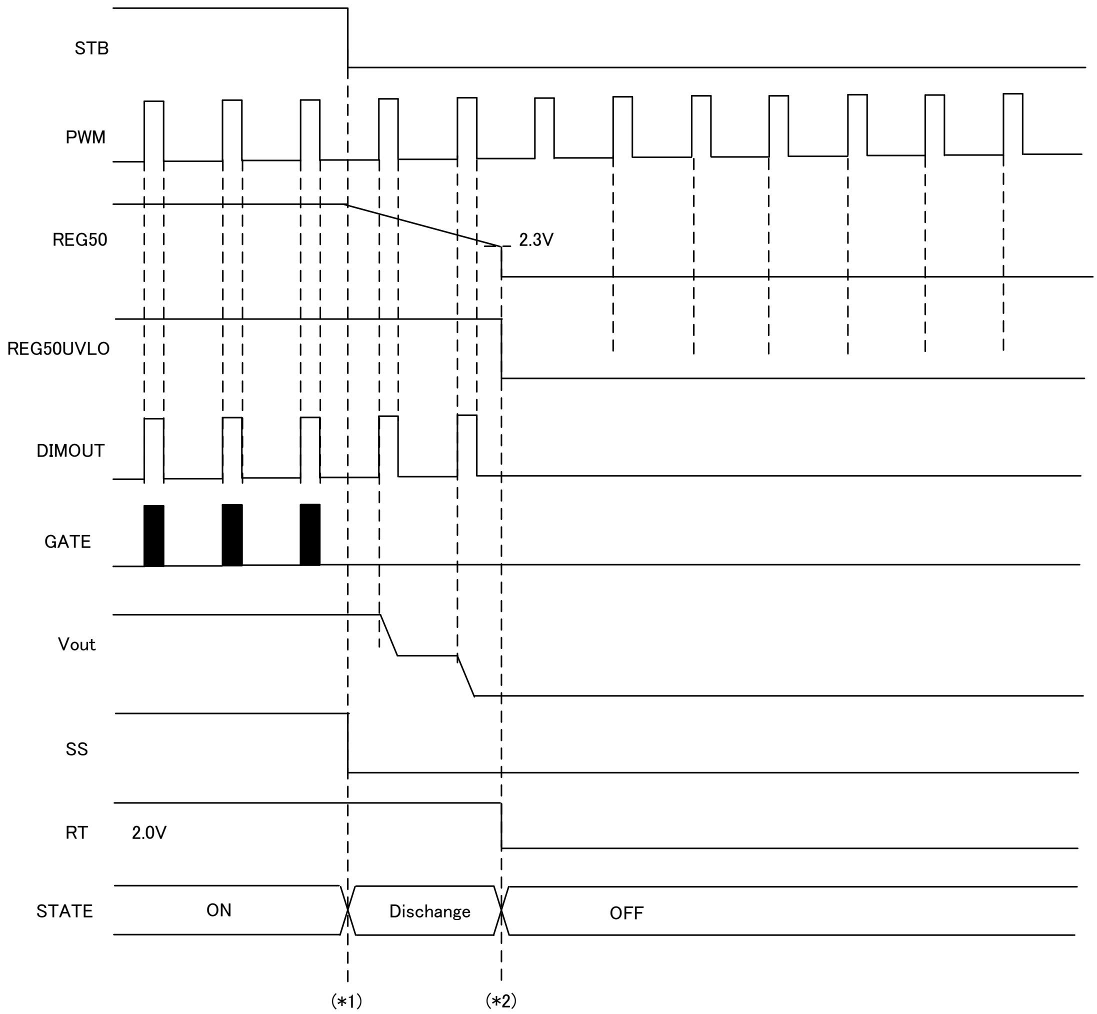



Figure 34. Turn Off

(*1)…As STB=H→L、boost operation stops and REG50 starts to discharge.
(*2)…While STB=L, REG50UVLO=H, DIMOUT becomes same as PWM. REG50=5.0V is discharged by -5μA until REG50=2.3V,and then IC becomes OFF state. REG50 is discharged rapidly and RT becomes 0V at the same time. $V_{OUT}$ is discharged completely until this time. It should be set to avoid a sudden brightness.
About capacitance value setting of REG50, please refer to the section 3.2.2.