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Datasheet

Boost 1channel white LED driver For large LCDs

BD9488F

●General Description

BD9488F is a high efficiency driver for white LEDs and designed for large LCDs. This IC is built-in a boost DCDC converters that employ an array of LEDs as the light source. BD9488F has some protect function against fault conditions, such as the over-voltage protection (OVP), the over current limit protection of DCDC (OCP), LED over current protection (LEDOCP), the open detection of LED string. Therefore BD9488F is available for the fail-safe design over a wide range output voltage.

●Key Specifications

- Input voltage range: 9.0V to 18.0V
- DCDC oscillation frequency: 150kHz (RT=100kΩ)
- Active current consumption: 1.2mA(Typ.)
- Operating temperature range: -40℃ to +85℃

●Package(s)

	W(Typ.) x D(Typ.) x H(Max.)
SOP18	11.20mm x 7.80mm x 2.01mm
	Pin pitch 1.27mm

Figure 1. SOP18

●Features

- Current mode DCDC converter
- Vout discharge circuit as shutdown
- LED protection circuit (OPEN protection, LED OCP protection)
- LED protect detection as small PWM dimming signal
- Over-voltage protection (OVP) for the output voltage.
- Adjustable soft start time constant
- The wide range of analog dimming 0.2V-3.5V
- The built-in transformation circuit from pulse to DC
- 2 PWM dimming signal
- The UVLO detection for the input voltage of the power stage
- FAIL logic output

●Applications

- TV, PC display and other LCD backlight system.

●Typical Application Circuit(s)

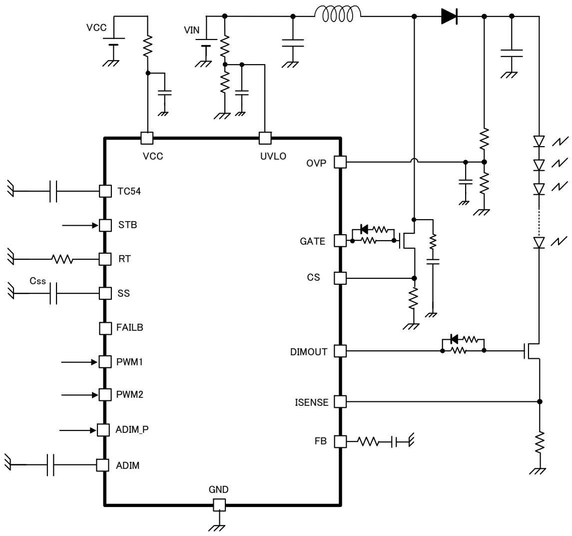


Figure 2. Typical application circuit

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Input voltage	Vccmax	20	V
STB pin voltage	STB	VCC	V
OVP, UVLO, SS, RT, ISENSE, FB, CS, TC54 pin voltage	OVP, UVLO, SS, RT, ISENSE, FB, CS, TC54	7	V
PWM1, PWM2, FAILB, ADIM, ADIM_P pin voltage	PWM1, PWM2, FAILB, ADIM, ADIM_P	20	V
DIMOUT, GATE pin voltage	DIMOUT, GATE	VCC	V
Power Dissipation	Pd	687 (*1)	mW
Operating Temperature Range	Topr	-40 to +85	℃
Junction Temperature	Tjmax	150	℃
Storage Temperature Range	Tstg	-55 to +150	℃

*1 Pd derated at 5.5 mW/℃ for temperature above Ta=25℃,
mounted on 70mm×70mm×1.6mm 1 layer glass-epoxy PCB.

●Operation range

Parameter	Symbol	Range	Unit
VCC Power source voltage	VCC	9.0 to 18.0	V
DC/DC oscillation frequency	fsw	50 to 800	kHz
The effective range of ADIM signal	VADIM	0.2 to 3.5	V
PWM input frequency range	FPWM	90 to 100k	Hz

●Pin Configuration

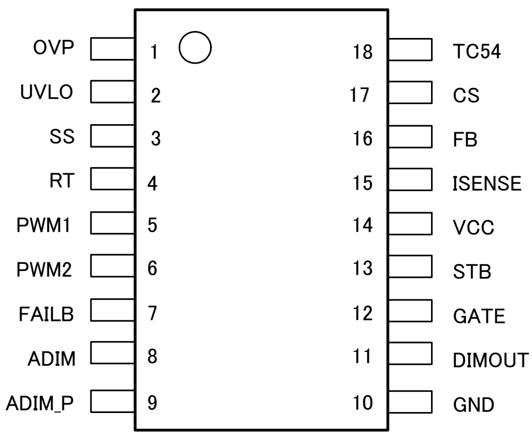


Figure 3-1. Pin configuration

●Package dimension, marking diagram

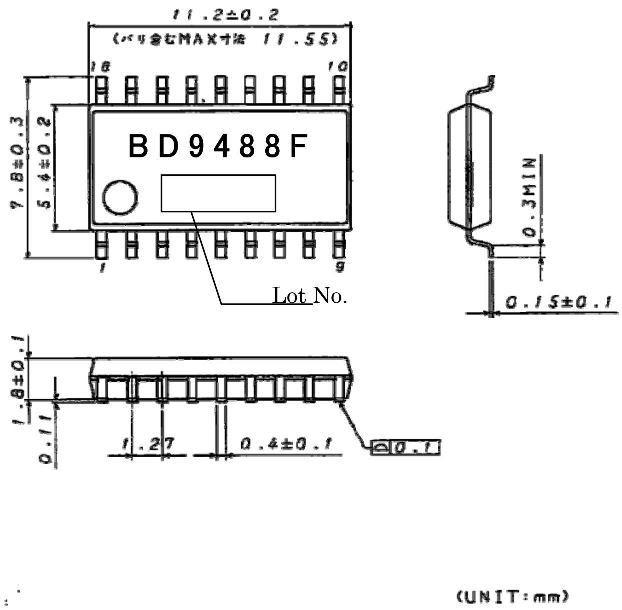


Figure 3-2. Package dimension

●1.1 Electrical character (Unless otherwise specified Ta=25℃, VCC=12V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
【Total current consumption】						
Circuit current	Icc	―	1.2	1.8	mA	VSTB=3V, PWM1=PWM2=0V
Standby current	IST	―	0	3	μA	VSTB=0V
【UVLO block】						
Operation voltage（VCC）	VUVLO_VCC	6.5	7.5	8.5	V	VCC=SWEEP UP
Hysteresis Voltage（VCC）	VUHYS_VCC	150	300	600	mV	VCC=SWEEP DOWN
UVLO release voltage	VUVLO	2.88	3.00	3.12	V	VUVLO=SWEEP UP
UVLO hysteresis voltage	VUHYS	250	300	350	mV	VUVLO=SWEEP DOWN
UVLO pin leak current	UVLO_LK	-2	0	2	μA	VUVLO=4V
【DC/DC block】						
ISENSE threshold voltage 1	VLED1	1.47	1.50	1.53	V	VADIM=1.5V
ISENSE threshold voltage 2	VLED2	3.33	3.50	3.67	V	VADIM=5.0V (as mask analog dimming)
ISENSE threshold voltage 3	VLED3	-2	-	+2	%	VADIM=0.7V
Oscillation frequency	FCT	142.5	150	157. 5	KHz	RT=100kohm
GATE pin MAX DUTY output	NMAX_DUTY	90	95	99	%	RT=100kohm
GATE pin ON resistance (as source)	RONSO	3.0	6.0	12.0	Ω	ION=-10mA
GATE pin ON resistance (as sink)	RONSI	1.2	2.5	5.0	Ω	ION=10mA
RT pin voltage	VRT	1.0	1.5	2.0	V	RT=100kohm
SS pin source current	ISSSO	-4.20	-3.0	-2.14	μA	VSS=2V
SS pin Low output voltage	VSS_L	-	0.20	0.50	V	VSTB=0V, Ioss=50uA
Soft start ended voltage	VSS_END	2.7	3.0	3.3	V	SS=SWEEP UP
FB source current	IFBSO	-140	-100	-60	μA	VISENSE=0.2V, VADIM=1.0V, VFB=1.0V
FB sink current	IFBSI	60	100	140	μA	VISENSE=2.0V, VADIM=1.0V, VFB=1.0V
OCP detect voltage	VCS	360	400	440	mV	CS=SWEEP UP
【DC/DC protection block】						
OVP detect voltage	VOVP	2.88	3.00	3.12	V	VOVP SWEEP UP
OVP detect hysteresis	VOVP_HYS	50	100	150	mV	VOVP SWEEP DOWN
OVP pin leak current	OVP_LK	-2	0	2	μA	VOVP=4V

●1.2 Electrical character (Unless otherwise specified Ta=25℃, VCC=12V)

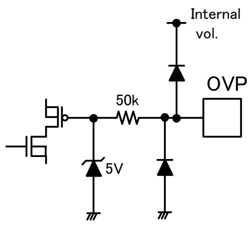
Parameter	Symbol	Limit Min.	Limit Typ.	Limit Max.	Unit	Condition
【LED protection block】						
LED OCP detect voltage	VLEDOCP	3.8	4.0	4.2	V	VISENSE=SWEEP UP
LED OPEN detect voltage	VOPEN	0.05	0.10	0.15	V	VISENSE=SWEEP DOWN
【Analog dimming block】						
ADIM_P pin HIGH voltage	ADIM_PH	2.0	-	3.8	V	
ADIM_P pin LOW voltage	ADIM_PL	-0.3	-	0.8	V	
ADIM_P pin input mask voltage	ADIM_PPU	4.2	-	18	V	
ADIM_P pin pull-down resistance	RADIM_P	130	200	300	kΩ	VADIM_P=3.0V
ADIM pin output voltage H	ADIMH	3.201	3.30	3.399	V	ADIM_P=3.3V
ADIM pin output voltage L	ADIML	-	0.0	0.05	V	ADIM_P=0.0V
ADIM pin output resistance	ADIMR	6.6	10	15	kΩ	
ADIM pin leak current	ILADIM	-2	0	2	μA	VADIM=4V, ADIM_P=5.0V
ISENSE pin leak current	IL_ISENSE	-2	0	2	μA	VISENSE=4V
【Dimming signal output block】						
DIMOUT source on-resistance	RONSO	6.0	12.0	24.0	Ω	ION=-10mA
DIMOUT sink on-resistance	RONSI	1.7	3.5	7.0	Ω	ION=10mA
【TC54 block】						
TC54 output voltage	VTC54	5.2	5.4	5.6	V	IO=0mA
TC54 available current	|ITC54|	100	-	-	μA	
TC54_UVLO detect voltage	TC54_TH	2.232	2.4	2.568	V	VSTB=H, TC54=SWEEP DOWN
TC54_UVLO hysteresis	TC54_HYS	50	100	200	mV	VSTB=H->L, TC54=SWEEP UP
TC54 discharge current	TC54_DIS	5	10	15	μA	VSTB=H->L, TC54=4V
【STB block】						
STB pin HIGH voltage	STBH	2.2	-	19	V	VSTB=SWEEP UP
STB pin LOW voltage	STBL	-0.3	-	0.8	V	VSTB=SWEEP DOWN
STB pin input current	ISTB	2.0	3.0	4.5	μA	VSTB=3.0V
【PWM block】						
PWMx pin HIGH Voltage	PWM_H	2.0	-	18	V	VPWMx=SWEEP UP
PWMx pin LOW Voltage	PWM_L	-0.3	-	0.8	V	VPWMx=SWEEP DOWN
PWMx pin Pull Down resistance	RPWM	130	200	300	kΩ	VPWMx=3.0V
【FAIL block (OPEN DRAIN)】						
FAILB pin on-resistance	RFAIL	0.75	1.5	3.0	kΩ	VFAIL=1.0V
FAILB pin leak current	ILFAIL	-2	0	2	μA	VFAIL=15V

●1.3 Pin number, pin name, pin function

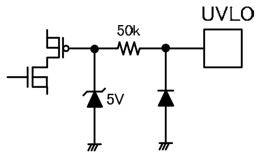
No.	name	IN/OUT	function	rating[V]
1	OVP	In	Over voltage protection detection pin	-0.3 to 7
2	UVLO	In	Under voltage lock out detection pin	-0.3 to 7
3	SS	Out	Slow start setting pin	-0.3 to 7
4	RT	Out	For DC/DC switching frequency setting pin	-0.3 to 7
5	PWM1	In	External PWM dimming signal input pin1	-0.3 to 20
6	PWM2	In	External PWM dimming signal input pin2	-0.3 to 20
7	FAILB	Out	Abnormality detection output pin	-0.3 to 20
8	ADIM	In/Out	ADIM signal input-output pin	-0.3 to 20
9	ADIM_P	In	ADIM pulse signal input pin	-0.3 to 20
10	GND	-	-	
11	DIMOUT	Out	Dimming signal pin for driving MOSFET	-0.3 to VCC
12	GATE	Out	DC/DC switching output pin	-0.3 to VCC
13	STB	In	IC On/OFF pin	-0.3 to VCC
14	VCC	-	Power supply pin	-0.3 to 20
15	ISENSE	In	Current detection input pin	-0.3 to 7
16	FB	In/Out	Error amplifier output pin	-0.3 to 7
17	CS	In	DC/DC output current detect pin, OCP input pin	-0.3 to 7
18	TC54	Out	5.4V output pin, shutdown timer pin	-0.3 to 7

●2.1.1 Pin ESD Type

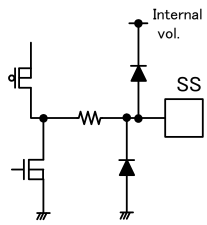
OVP



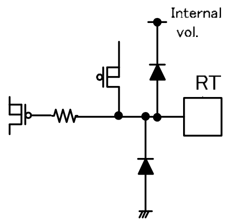
UVLO



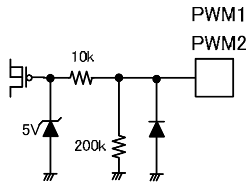
SS



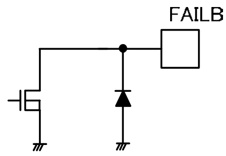
RT



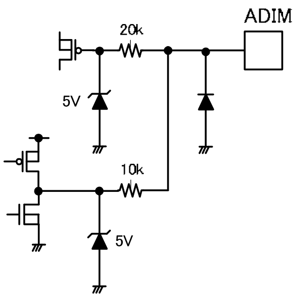
PWM1, PWM2



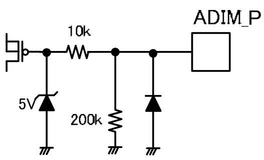
FAILB



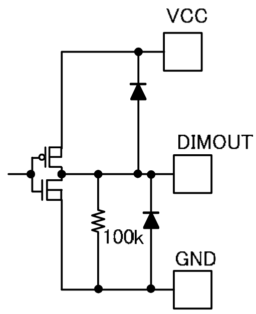
ADIM



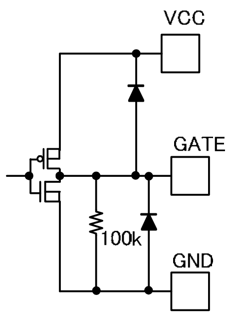
ADIM_P



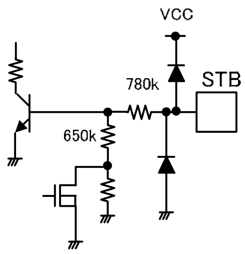
DIMOUT



GATE



STB



ISENSE

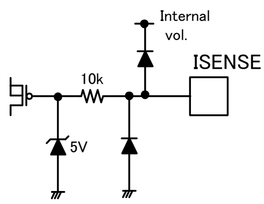


Figure 4-1. Internal equivalent circuit

●2.1.2 Pin ESD Type

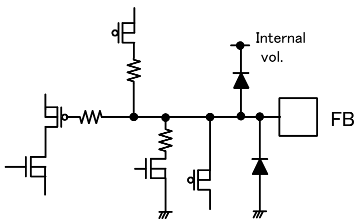
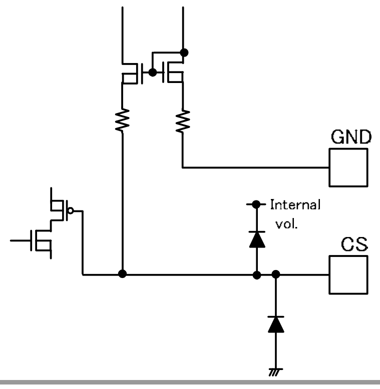
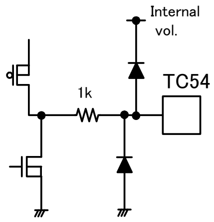
FB	CS	TC54
		

Figure 4-2. Internal equivalent circuit

●2.2 Block diagram

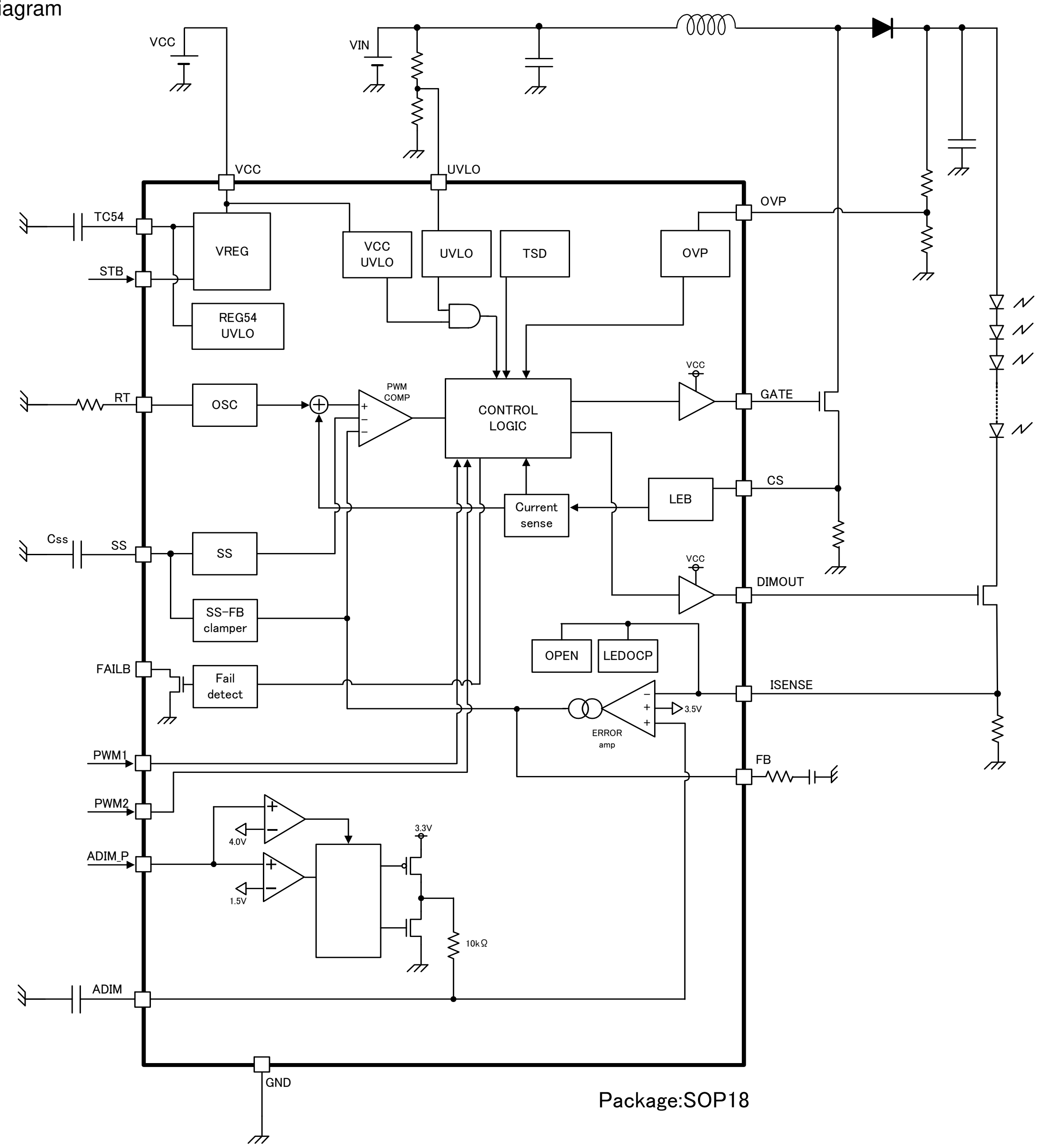


Figure 5. Block diagram

●2.3 Typical performance Curves

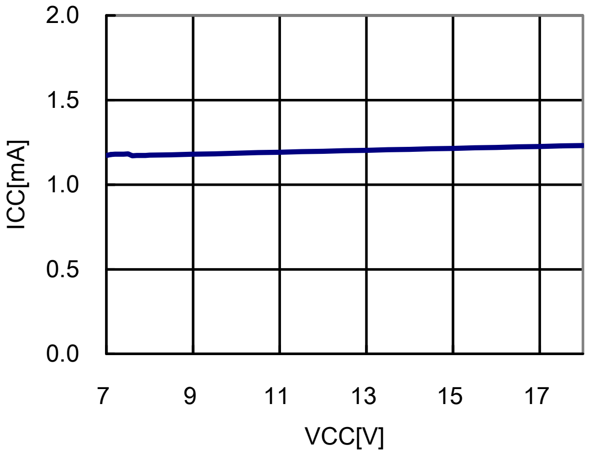


Figure 6. Operating current (ICC) vs VCC

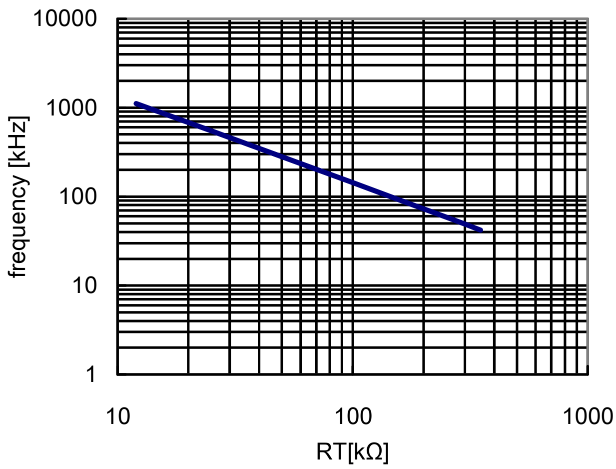


Figure 7. GATE frequency vs RT

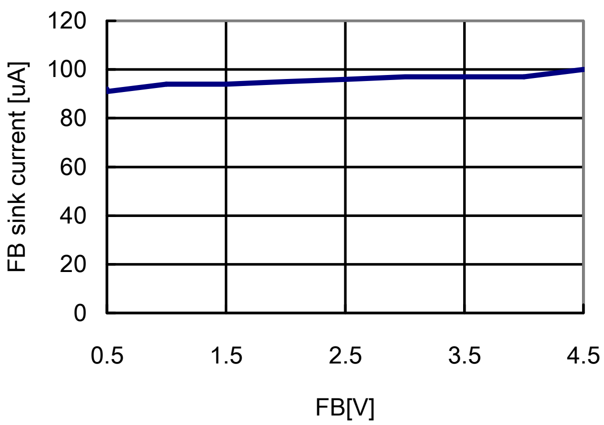


Figure 8. FB sink current vs FB voltage

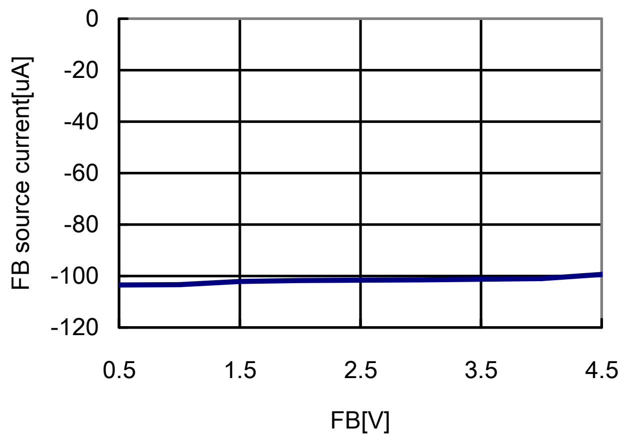


Figure 9. FB source current vs FB voltage

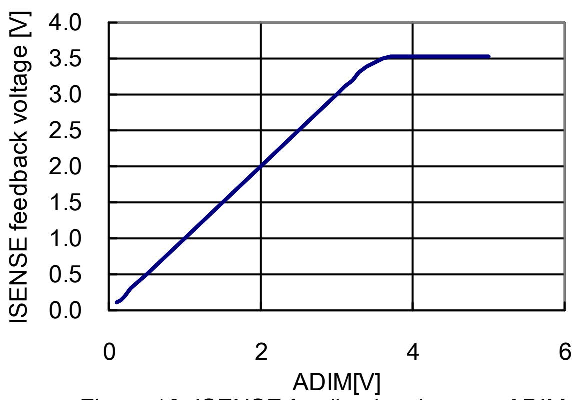


Figure 10. ISENSE feedback voltage vs ADIM

●2.4 Pin function description

○Pin1: OVP

The OVP terminal is the input for over-voltage protection of output voltage. As OVP is more than 3.0V, the over-voltage protection (OVP) will work. At the moment of this detection, the BD9488 stops the switching of the output GATE and starts to count up the abnormal interval, but IC doesn't reach latch off state instantaneously until the detection continues up to the number of counts of GATE terminals, which depend on the kind of abnormality. (Please refer to the time chart in the section 3.5.7)

The OVP pin is high impedance, because the internal resistance to a certain bias is not connected.

So, the bias by the external components is required, even if OVP function is not used, because the open connection of this pin is not fixed the potential.

The setting examples is separately described in the section 3.4.6, "external components selection, how to set OVP"

○Pin2: UVLO

Under voltage lock out pin for the input voltage of the power stage. More than 3.0V(typ.), IC starts the boost operation and stops lower than 2.7V(typ.).

The UVLO pin is high impedance, because the internal resistance to a certain bias is not connected.

So, the bias by the external components is required, even if UVLO function is not used, because the open connection of this pin is not fixed the potential.

The setting examples is separately described in the section 3.4.5, "external components selection, how to set UVLO"

○Pin3: SS

The pin which sets soft start interval of DC/DC converter. It performs the constant current charge of 3.0 μA to external capacitance Css(OPEN to 4.7μF). The switching duty of GATE output will be limited during 0V to 3.0V of the SS voltage. So the equality of the soft start interval can be expressed as following

$Tss = 1.0*10^6*Css$ Css: the external capacitance of the SS pin.

Regarding of the logic of SS=L

(SS=L) = (PWM1andPWM2 have not asserted H since ResetB=L->H) or (latch off state)

where ResetB = (STB=H) and (VCCUVLO=H) and (UVLO=H) and (TC54UVLO=H)

As the capacitor of SS pin is smaller than about 1nF, it is necessary to notice if the inrush current I(Vin) as turning-on is too large, and if the masking interval of OPEN detection is too short.

Please refer to the time chart on soft start behavior in the section 3.7.4

○Pin4: RT

DC/DC switching frequency setting pin. RT set the oscillation frequency inside IC.

○<u>The relationship between the frequency and RT resistance value **(ideal)**</u>

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

The oscillation setting range from 50kHz to 800kHz.

The setting examples is separately described in the section 3.4.4, "external components selection, how to set DCDC oscillation frequency"

○Pin5, Pin6: PWM1, PWM2

The ON / OFF terminal of the LED driver. LED lights when both PWM signal are high (DIMOUT = H). The Duty signal of this pin can control the PWM dimming.

The high / low level of PWM pins are following.

State	PWM input voltage
PWM1=H or PWM2=H	PWM=2.0V to 18.0V
PWM1=L or PWM2=L	PWM=-0.3V to 0.8V

PWM1 and PWM2 have the functional difference, and GATE pin outputs only by the logic of PWM1.

This is why only boost operation continues while PWM1=H, PWM2=L. In this case, the adequate confirmation is required not to be over voltage of the output voltage Vout.

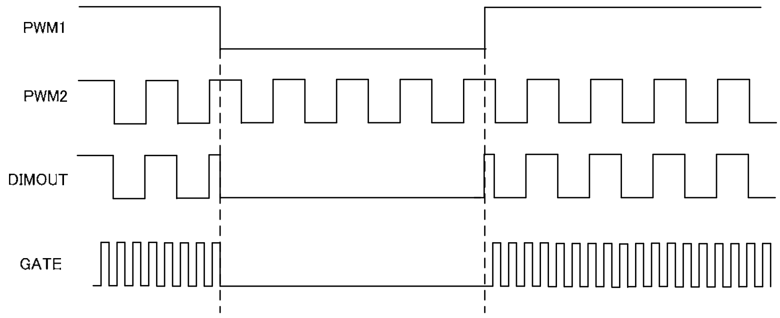


Figure 11. PWM pin function

○Pin7: FAILB

FAIL signal output pin (open drain). As abnormal, the internal NMOS turn on.

Status	FAILB output
Normal	OPEN
Abnormal	GND Level

○Pin8: ADIM

ADIM_P input level	ADIM_P pin function	ADIM pin function	Required signal to IC
-0.3V<ADIM_P<3.8V	Pulse signal input for analog dimming	DC output signal for analog dimming	DUTY signal for analog dimming
4.2V <ADIM_P<18V	ADIM_P pin function is masked.	DC input signal for analog dimming	DC signal for analog dimming

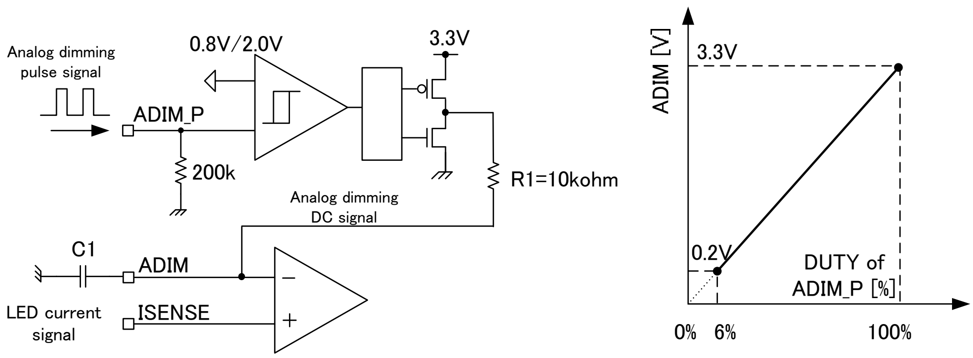


Figure 12. Analog dimming function and character

Above functions enable BD9488 use both of the duty and DC signal for analog dimming.

○When the duty signal is used, that input to the pin ADIM_P with the amplitude about 3.3V. The input duty of ADIM_P needs to be larger than 6% so that the output ADIM is larger than 0.2V. In the case of the normal feedback with analog dimming, The ADIM pin voltage is equal to the ISENSE pin voltage. Therefore, please be careful that the lower ADIM voltage than 0.1V causes the OPEN abnormal detection.

○When the DC signal is used, ADIM_P will be pulled up more than 4.2V, and the signal input to the pin ADIM.
In the driver module with more than two BD9488, and the analog dimming is performed by the duty signal, the architecture will be shown in the right figure. That can reduce the LED current error between the channels, because the common circuit of the pulse DC transform is used.
The pulse DC transform circuit outputs DC signal to the ADIM pin with the time constant of R1, C1 in the above diagram. More C1 value, the ripple components of the ADIM pin is decreased, on the other hand, the transient response is delayed.
And please keep in mind the error voltage if the pull down resistor of ADIM pin will be connected.

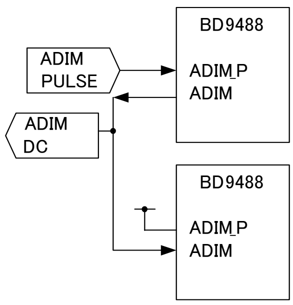


Figure 13. the analog dimming circuit as two BD9488 are used.

○Pin9: ADIM_P

The pulse signal input pin for analog dimming. Please pull up the voltage level more than 4.2V(typ.), when DC signal is

used for the analog dimming. In normal operation, please set the input voltage under 18.0V. For more details, please refer to <ADIM> pin descriptions.
The input frequency of this pin assumed from 2kHz to 100kHz. Please keep in mind that the capacitor of ADIM pin is small considering of this input frequency, the error of LED current can be cause.

○Pin10: GND
GND pin of IC.

○Pin11: DIMOUT
This is the output pin for external NMOS of dimming. The below table shows the rough output logic of each operation state, and the output H level is VCC. Please refer to the time chart in the section 3.7 for detail explanations, because The DIMOUT logic has the exceptional behavior. Please insert the resistance between the dimming MOS gate to improve the over shoot of LED current, as PWM turns from low to high.

Status	DIMOUT output
Normal	PWM1 and PWM2
Abnormal	GND Level

○Pin12: GATE
This is the output terminal for driving the gate of the boost MOSFET. The high level is VCC of IC. Frequency can be set by the resistor connected to RT. Please refer to the <RT> pin description for the frequency setting.

○Pin13: STB
ON/OFF setting terminal for IC, which can be used to perform a reset at shutdown. Please reset this pin after latch off.
Regarding of the sequence of turning on, if the input logic STB turns from low to high, the internal power supply is activated. After the positive edge of PWM is input , BD9488 starts the boost operation.

○ The input voltage of STB pin toggles the IC state(IC ON/OFF). Please avoid the use of the intermediate level (from 0.8V to 2.2V).

Regarding of the power down sequence, while STB=L and TC54UVLO=H, in order to discharge the output voltage, DIMOUT logic can assert high, depending on the PWM logic. This discharge behavior is separately described in the time chart in the section 3.7.3, or in the section 3.4.2, "how to shutdown and set TC54 capacitance"

○Pin14: VCC
Power supply pin of IC. Input range is from 9V to 18.0V.

The operation starts more than 7.5 V(TYP.) and shuts down less than 7.2 V(TYP.).

○Pin15: ISENSE
This is the input terminal for the current detection. The error amplifier compares the lower voltage the analog dimming pin ADIM and 3.5V. The abnormal voltage of this pin activates the protection function of LED, such as LEDOCP, OPEN.

[LED OCP Protection Function]
More than ISENSE = 4.0V (typ.), the over current of LED (LEDOCP) will be detected. If that states continues 130k clock of GATE pin, IC will latch off. (Please refer to the time chart in the section 3.7.7.)

[LED OPEN Protection Function]
If OPEN state (ISENSE<0.1V) continues during 4 clocks interval of GATE terminal, BD9488 starts to count the interval of the abnormal state. If the abnormal condition continues by the completion of counting, BD9488 will be latched off. (Please refer to the time chart in the section 3.7.6.)
Exceptionally the OPEN protect detection are masked in the following conditions,
<u>CASE1.</u> When PWM = L. ISENSE is less than 0.1V even in normally, because DIMOUT = L.
<u>CASE2.</u> In the soft-start interval. ISENSE is less than 0.1V, because of the insufficient output voltage Vout.

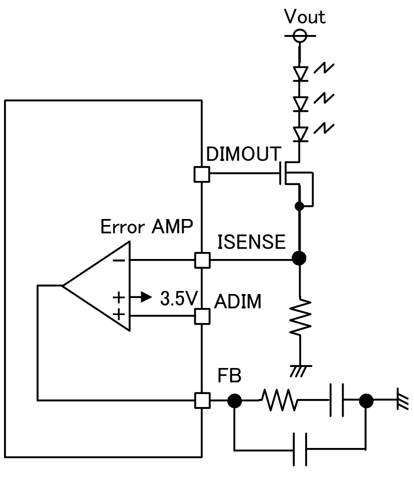


Figure 14. ISENSE pin circuit

○Pin16: FB
This is the output terminal of error amplifier. Monitoring the ISENSE terminal voltage, this pin outputs the error signal with the analog dimming signal (pin ADIM) or 3.5V.
After the completion of the SS, this pin outputs high impedance as the logic "PWM1 and PWM2" asserts low. FB voltage is hold to the external capacitance.
(For more detail on the compensation setting is described in the section " 3.6 loop compensation".)

○Pin17: CS

The CS pin has two functions.

1. DC / DC current mode Feedback terminal

The inductor current is converted to the CS pin voltage by the sense resistor R_{CS} and this CS pin voltage controls the output voltage by compared with the error amp output.

2. Inductor current limit (OCP) terminal

The CS terminal also has a over current protection (OCP), if it voltage is more than 0.4V, the switching operation will be stopped compulsorily.

Both of above functions are enable after 300ns (typ.) when GATE pin asserts high, because the leading Edge Blanking function is included into this IC to prevent the affect noise. Please refer to the section 3.5.1 “DCDC parts selection / how to set OCP”, for detail explanation.

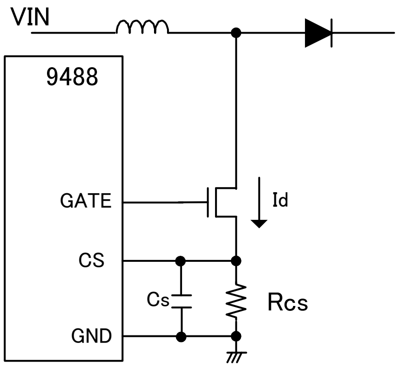


Figure 15. CS pin circuit

If the capacitance Cs in the right figure is increased to a micro orders, please be careful that the limited value of NMOS drain current Id is much than the simple calculation. Because the current Id flow not only Rcs but also Cs, as the CS pin voltage move according to Id.

○Pin18: TC54

This is the 5.4V (TYP.) output pin that is used for internal power supply. Available current is 100uA.

TC54 can be used as a timer for the discharge of output capacitance DCDC. For detailed instructions, please refer the section 3.4.2 “how to shutdown and set TC54 capacitance”

●3.1 Application circuit example
The bellows are example circuits of using BD9488F.

・The basic application circuit example

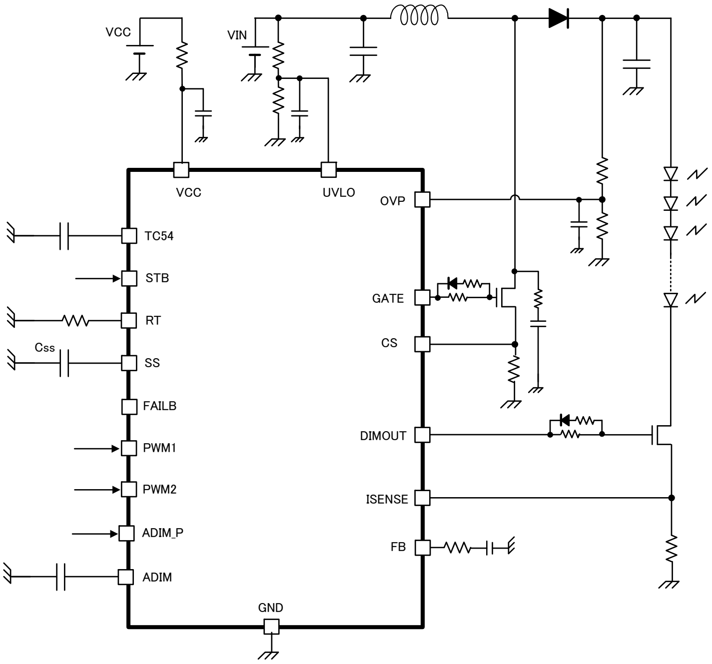
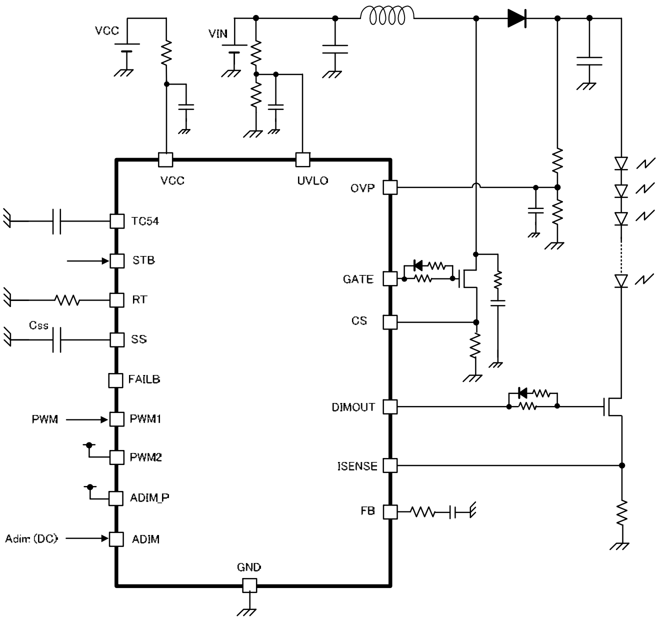
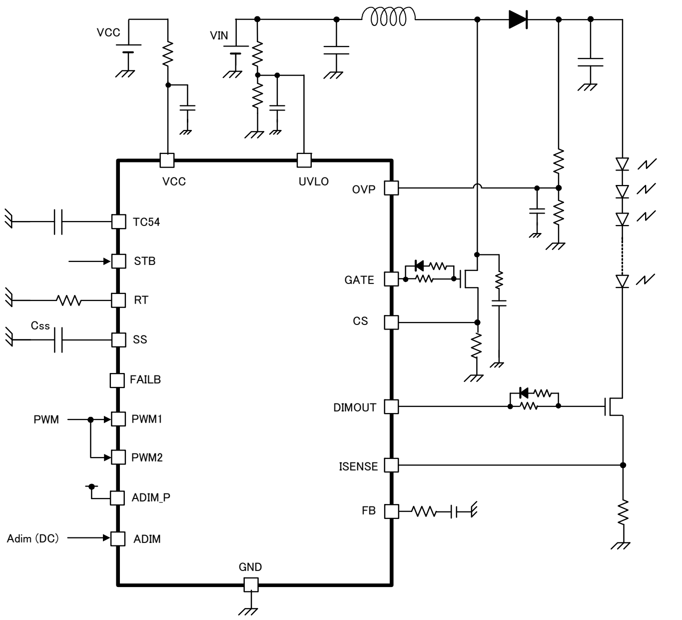


Figure 16. The basic application circuit example

・As for the dimming signal, the single PWM and the DC for analog dimming





PWM1 pin and PWM2 pin are shorted.

Figure 17. the circuit example with single PWM (1)

Figure 18. the circuit example with single PWM (2)

・Only analog dimming

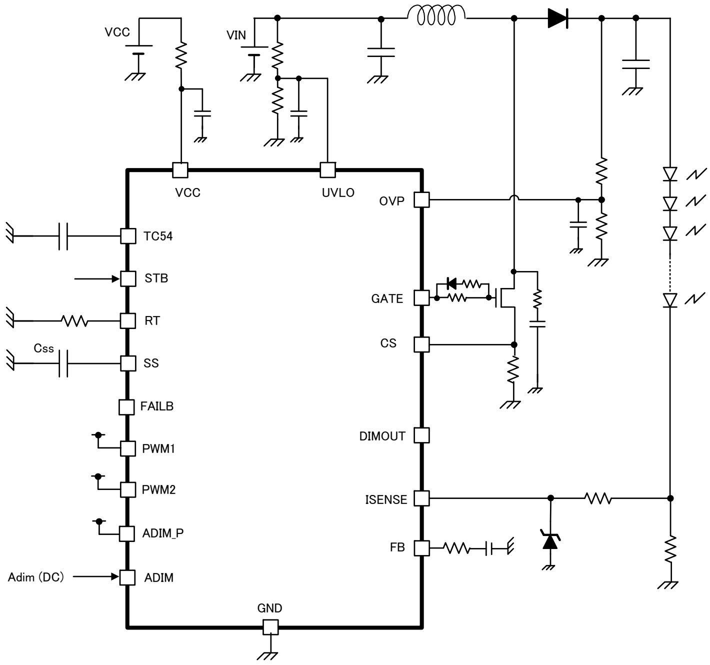


Figure 19. the circuit example of analog dimming only

・Application example when use numerous IC

The application circuit of analog dimming by external duty signal.

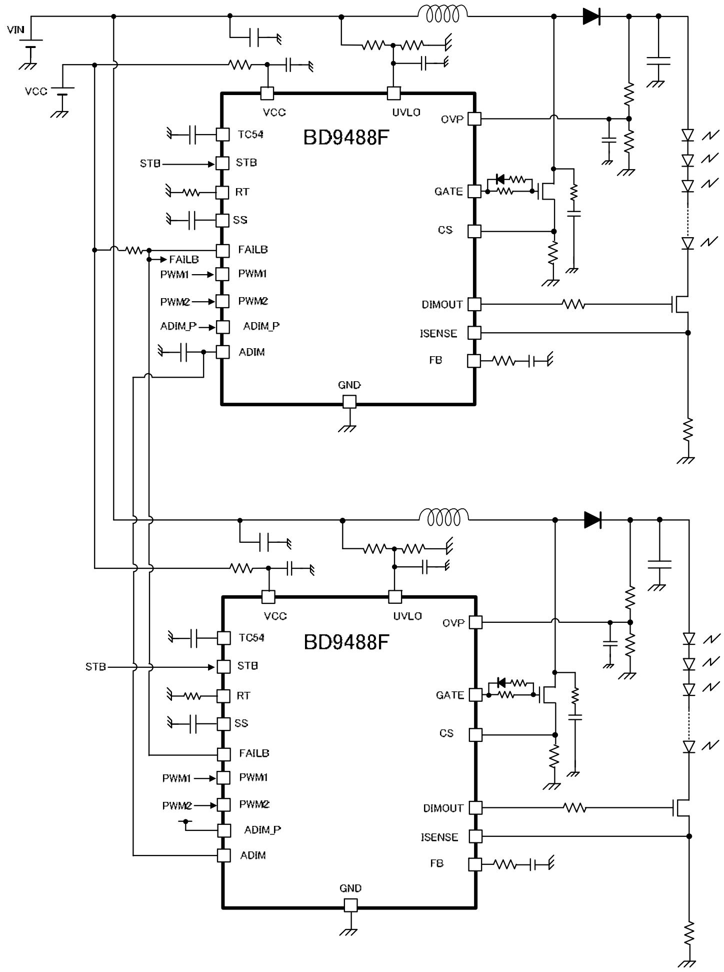


Figure 20. the circuit example of when plural IC is used.

●3.2 **The detection condition list of the protection (TYP. Condition)**

Protection	Detection pin	Detect condition			Release condition	Timer operation	Protection type
		pin condition	PWM1 and PWM2	SS			
LED OPEN	ISENSE	ISENSE < 0.1V	H(4count)	SS>3.0V	ISENSE > 0.1V	130k count	Latch off
LED OCP	ISENSE	ISENSE > 4.0V	-	-	ISENSE < 4.0V	130k count	Latch off
UVLO	UVLO	UVLO<2.7V	-	-	UVLO>3.0V	NO	Auto recovery
TC54 UVLO	TC54	TC54<2.4V	-	-	TC54>2.5V	NO	Auto recovery
VCC UVLO	VCC	VCC<7.2V	-	-	VCC>7.5V	NO	Auto recovery
OVP	OVP	OVP>3.0V	-	-	OVP<2.9V	4 count	Latch off
OCP	CS	CS>0.4V	-	-	-	NO	Pulse by Pulse

To reset the latch type protection, please input of STB logic to 'L' once. Otherwise the detection of VCCUVLO, TC54UVLO is required.

The count number in the table suggests the oscillation frequency of DCDC converter.

●3.3 **The behavior list of the protection**

Protect Function	The operation of the protection			
	DC/DC Gate output	Dimming transistor (DIMOUT) logic	Soft Start	FAILB pin
LED OPEN	Stops after latch	L after latch	discharge after latch	L after latch
LED OCP	Stops immediately	H immediately, L after latch	discharge after latch	L after latch
STB	Stops immediately	L if TC54<2.4V	discharge immediately	OPEN
UVLO	Stops immediately	immediately L	discharge immediately	immediately L
TC54 UVLO	Stops immediately	immediately L	discharge immediately	immediately L
VCC UVLO	Stops immediately	immediately L	discharge immediately	immediately L
OVP	Stops immediately	immediately L	discharge after latch	L after latch
OCP	Stops immediately	Normal operation	Not discharge	OPEN

Please refer to the timing chart in the section 3.7 for the detail.

●3.4 External components selection

●3.4.1 The start up operation and the setting of Soft Start external capacitance

The below explanations are the start up sequency of BD9488.

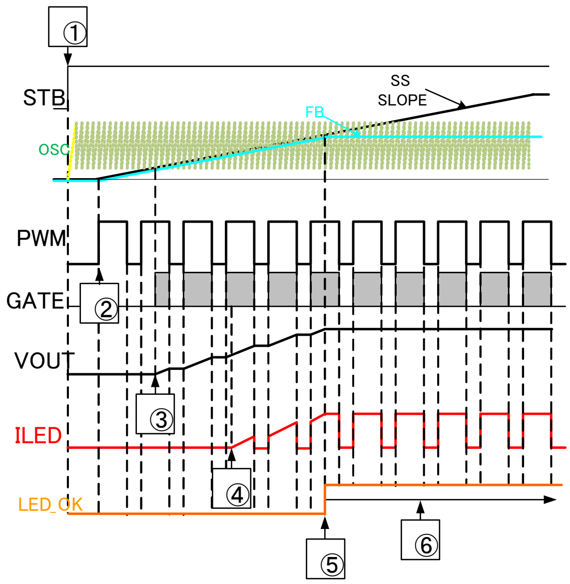


Figure 21. the turn-on waveform

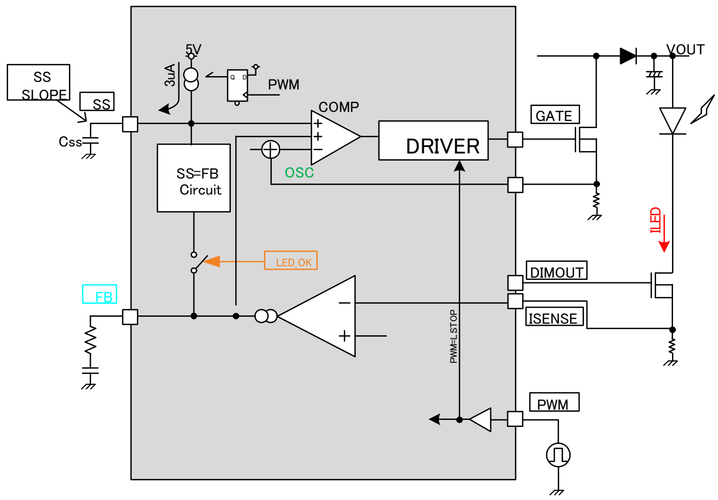


Figure 22. the turn-on circuit

○The explanation of start up sequency

①When STB is H, the internal bias voltage of TC54 rising.

②With the first PWM=H, BD9488 enables output the boost pulse, and the SS start to charge to the external capacitance. At this moment, the voltage of FB will be the same as SS voltage internally regardless of the PWM logic.

③The FB=SS voltage reach the bottom voltage of saw-toothed wave and the DC/DC start to output the pulse signal. Therefore the boost of VOUT is started.

④VOUT is boosted to fixed level, and the LED current is rising.

⑤When the LED current reached to fixed level, FB is removed from SS internally. The start up operation completed.

⑥IC start the normal operation by sensing the voltage of ISENSE pin. When SS is more than 3.0V, even if the LED current does not flows, the clamped circuit of SS and FB is off, and the protect detection of OPEN starts.

○The setting method of SS external capacitance

As above desribed, DC/DC stops when the PWM1=L. It means the boost operation only enabled within PWM1=H duration and SS time will be extented while boost with samll PWM duty. Also the SS time is affected by the output capacitance, the LED current and application conditions.

Tss is defined as the time for the SS voltage to reach to the FB feedback voltage. Please set the Tss longer than Trise_min, which is the start up time of the minimum PWM duty.

When the FB voltage during LED turns on is expressed VFB, the equality on Tss is the following.

$$T_{ss} = \frac{C_{ss}[F] \times VFB[V]}{3[\mu A]} \quad [\mu Sec]$$

So please set the external capacitance to meet the Tss>>Trise_min.

●3.4.2 **how to shutdown and set TC54 capacitance**

This IC is equipped the discharge function when shutdown is operated.

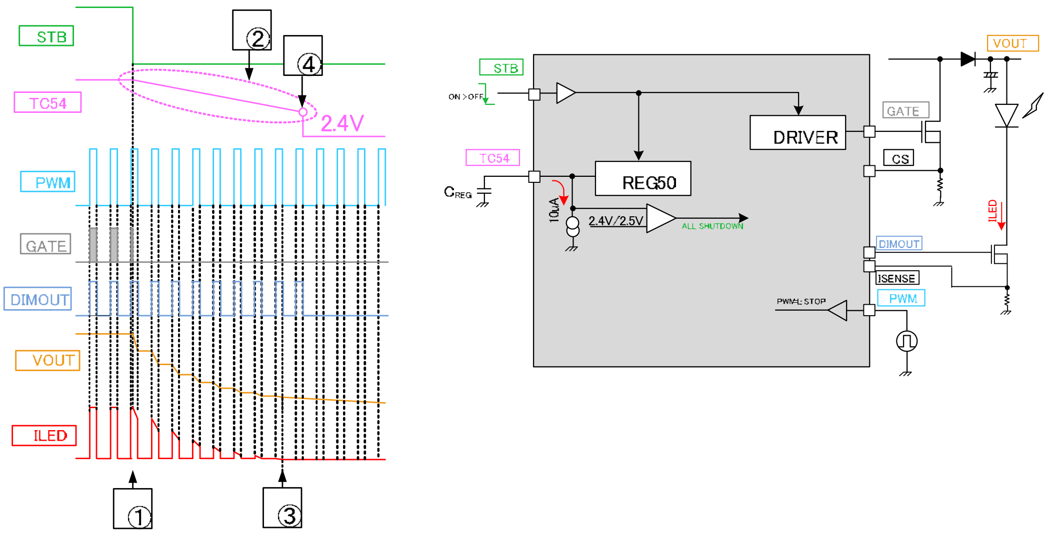


Figure 23. the shutdown waveform and circuit

○Explanation of shutdown sequence

①When STB=L, DC/DC and TC54 are stop.

②When STB=L, TC54UVLO=H, the DIMOUT logic asserts the PWM logic. The voltage of TC54 (5.4V) will decrease by the constant current -10uA and is discharged to 2.4V.

③VOUT will be discharged and ILED decresing.

④When the voltage of TC54 pin is under 2.4V(typ.), the IC will shutdown.

○The setting method of TC54 external capacitance

Please use below formula to calculate the shutdown time TOFF.

$$T_{OFF} = \frac{C_{REG}[F] \times 3.0[V]}{10[\mu A]} \quad [\mu Sec]$$

As shown the above, the PWM signal is required even after STB=L.
The discharge interval of VOUT is the longest in the minimum PWM duty. Please set the Creg value with a enough timing margin from the end of the VOUT discharge to shutdown.

●3.4.3 The LED current setting

LED current can be adjusted by setting the resistance R_{ISENSE} which connects to ISENSE pin.

○the relationship between RISET and ILED current

With DC dimming

$$R_{ISENSE} = \frac{ADIM[V]}{I_{LED}[A]}[\Omega]$$

Without DC dimming

$$R_{ISENSE} = \frac{3.5[V]}{I_{LED}[A]}[\Omega]$$

[setting example]

If ILED current is 400mA as ADIM is 1.5V, we can calculate R_{ISENSE} as below.

$$R_{ISENSE} = \frac{ADIM[V]}{I_{LED}[A]} = \frac{1.5[V]}{0.4[A]} = 3.75[\Omega]$$

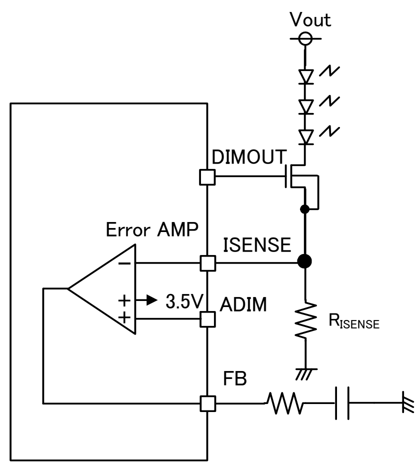


Figure 24. the example of LED current setting

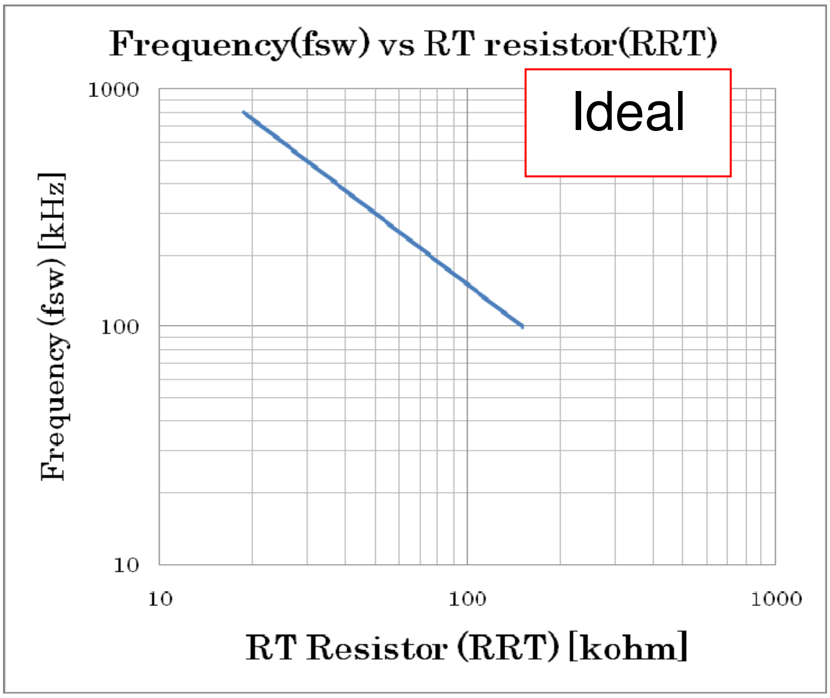
●3.4.4. how to set DCDC oscillation frequency

R_{RT} which connects to RT pin set the oscillation frequency of DCDC.

○ **the relationship between OSC and R_{RT} (ideal)**

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

where fsw is the oscillation frequency of DCDC [kHz]



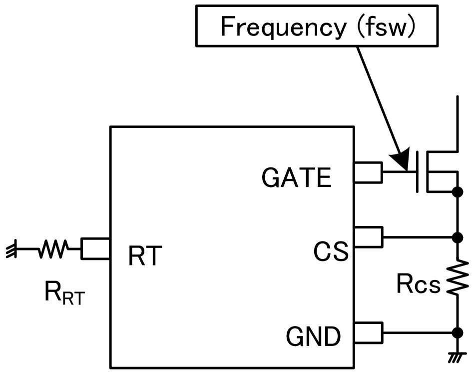


Figure 25. RT pin setting example

This equation is an ideal equation in which correction factors are not applied.
The adequate verification with an actual set needs to be performed to set frequency precisely.

[setting example]

If DCDC oscillation frequency is 200kHz, we can calculate the R_{RT} as below.

$$R_{RT} = \frac{15000}{f_{sw}[kHz]} = \frac{15000}{200[kHz]} = 75 \quad [k\Omega]$$

●3.4.5. how to set UVLO

Under voltage lock out pin for the input voltage of the power stage. More than 3.0V(typ.), IC starts boost operation and stops lower than 2.7V(typ.).

The UVLO pin is high impedance, because the internal resistance to a certain bias is not connected.

So, the bias by the external components is required, even if UVLO function is not used, because the open connection of this pin is not fixed the potential.

The resistor value can be calculated by the below formula, if the VIN voltage is monitored, and that is divided by the resistor R1, R2 like the below diagram.

○UVLO detection equality

If VIN decreases, R1, R2 value is expressed the following formula by the VINdet, the detect voltage of UVLO.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.7[V])}{2.7[V]} \quad [k\Omega]$$

○UVLO release equality

By using the R1, R2 in the above equality, the release voltage of UVLO can be expressed as following.

$$VIN_{CAN} = 3.0V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

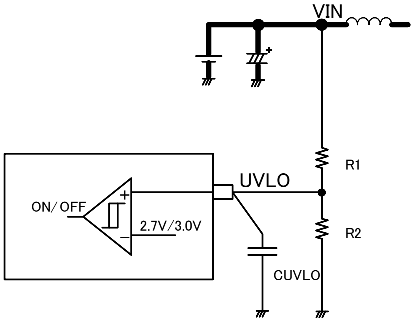


Figure 26. UVLO setting example

[setting example]

If the normal input voltage, VIN is 24V, the detect voltage of UVLO is 18V, R2 is 30k ohm, R1 is calculated as following.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.7[V])}{2.7[V]} = 30[k\Omega] \times \frac{(18[V] - 2.7[V])}{2.7[V]} = 170.0 \quad [k\Omega]$$

By using these R1, R2, the release voltage of UVLO, VINcan can be calculated as following.

$$VIN_{CAN} = 3.0[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 3.0[V] \times \frac{170.0[k\Omega] + 30[k\Omega]}{30[k\Omega]}[V] = 20.0 \quad [V]$$

●3.4.6. how to set OVP

The OVP terminal is the input for over-voltage protection of output voltage.
The OVP pin is high impedance, because the internal resistance to a certain bias is not connected.
So, the bias by the external components is required, even if OVP function is not used, because the open connection of this pin is not fixed the potential.
The resistor value can be calculated by the below formula, if the VOUT voltage is monitored, and that is divided by the resistor R1, R2 like the below diagram.

○OVP detection equality
If the VOUT is boosted abnormally, VOVPdet is the detect voltage of OVP, R1, R2 can be expressed by the following formula.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} \quad [k\Omega]$$

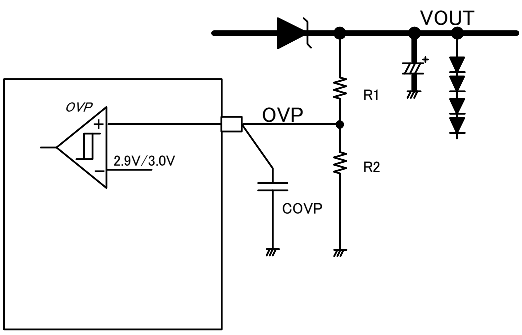


Figure 27. OVP setting example

○OVP release equality
By using the R1, R2 in the above equality, the release voltage of OVP, VOVPcan can be expressed as following.

$$VOVP_{CAN} = 2.9V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

[setting example]
If the normal output voltage, VOUT is 40V, the detect voltage of OVP is 48V, R2 is 10k ohm, R1 is calculated as following.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} = 10[k\Omega] \times \frac{(48[V] - 3[V])}{3[V]} = 150 \quad [k\Omega]$$

By using these R1, R2, the release voltage of OVP, VOVPcan can be calculated as following.

$$VOVP_{CAN} = 2.9[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 2.9[V] \times \frac{10[k\Omega] + 150[k\Omega]}{10[k\Omega]}[V] = 46.4 \quad [V]$$

●3.4.7. how to set the interval until latch off

BD9488 built in the counter by latch off time, that is performed by counting the oscillation clock which is set by the RT pin. Since the common oscillation circuit is used for counting, the interval until latch off is corresponding to the 130k clock, which the GATE pulse output continuously. Please refer the time chart of the operation from the detect abnormality to the latch off in the section 3.7.

○latch off time

BD9488 starts the counting up from the detection of each abnormal state, falls to the latch off state when the following interval has passed.
Only PWM=L input does not reset the timer counter, if the abnormal state continues.

$$LATCH_{TIME} = 2^{17} \times \frac{R_{RT}[\Omega]}{1.5\times10^{10}} = 130k \times \frac{R_{RT}[k\Omega]}{1.5\times10^{7}}[\sec]$$

Where $LATCH_{TIME}$ is the interval until latch off state
R_{RT} is the connected resistor of RT pin.

[setting example]

If the resistor of RT pin is 100k ohm, the timer latch interval is as following.

$$LATCH_{TIME} = 130k \times \frac{R_{RT}[k\Omega]}{1.5\times10^{7}} = 130k \times \frac{100[k\Omega]}{1.5\times10^{7}} = 866[m\sec]$$

●3.5. DCDC parts selection

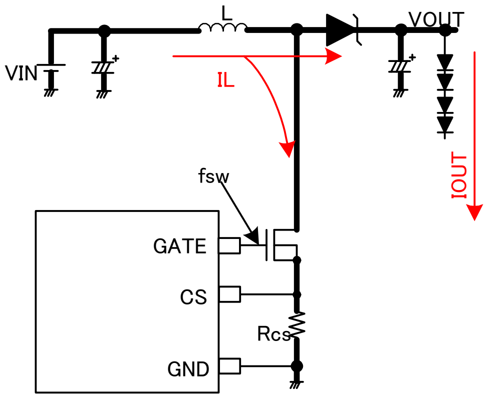
3.5.1. how to set OCP / the calculation method for the current rating of DCDC parts

BD9488 stops the switching by the OCP detect, when the CS pin voltage is more than 0.4V. The resistor value of CS pin, R_{CS} need to be considered by the coil L current. And the current rating of DCDC external parts is required more than the peak current of the coil.
It is shown below that the calculation method of the coil peak current, the selection method of Rcs (the resistor value of CS pin) and the current rating of the external DCDC parts.

(the calculation method of the coil peak current, Ipeak)

At first, since the ripple voltage at CS pin depend on the application condition of DCDC, those put onto the equality to calculate as following.
The output voltage = VOUT [V]
LED total current = IOUT [A]
The DCDC input voltage of the power stage = VIN [V]
The efficiency of DCDC = η [%]
And then, the averaged input current IIN is calculated by the following equality

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$



And the ripple current of the inductor L (ΔIL[A]) can be calculated by using DCDC the switching frequency, fsw, as following.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

On the other hand, the peak current of the inductor Ipeak can be expressed as the following equality.

$$\boxed{Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} \quad [A]} \quad \text{… (1)}$$

Therefore, the bottom of the ripple current Imin is

$$\mathrm{Im}\,in = I_{IN}[A] - \frac{\Delta IL[A]}{2} \quad \text{or 0}$$

As Imin>0, that operation mode is CCM (Continuous Current Mode), otherwise another mode is DCM (Discontinuous Current Mode).

(the selection method of Rcs)

Ipeak flows into Rcs and that cause the voltage signal to CS pin. (Please refer the right timing chart)
That peak voltage VCSpeak is as following.

$$VCS_{peak} = Rcs \times Ipeak \quad [V]$$

As this VCSpeak reaches to 0.4V, the DCDC output stops the switching.
Therefore, Rcs value is necessary to meet the under condition.

$$\boxed{Rcs \times Ipeak[V] << 0.4[V]}$$

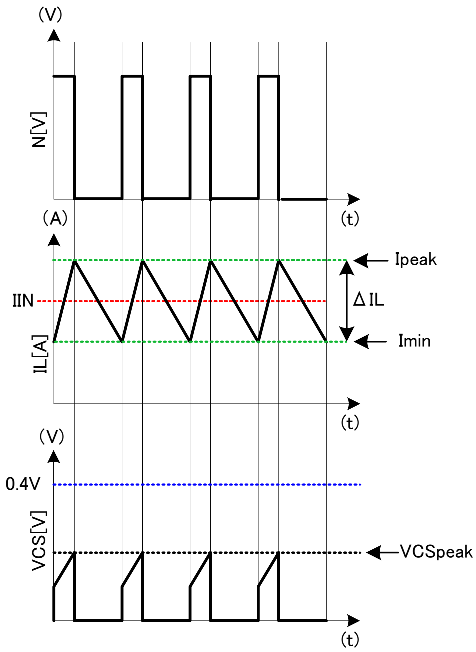


Figure 28. Coil current waveform

(the current rating of the external DCDC parts)

The peak current as the CS voltage reaches to OCP level (0.4V) is defined as Ipeak_det.

$$I_{peak\_det} = \frac{0.4[V]}{Rcs[\Omega]} \quad [A] \quad \text{… (2)}$$

The relation among Ipeak (equality (1)), Ipeak_det (equality (2)) and the current rating of parts is required to meet the following

$$\boxed{I_{peak} << I_{peak\_det} << \text{The current rating of parts}}$$

Please make the selection of the external parts to meet the above condition such as FET, Inductor, diode.

[setting example]

The output voltage = VOUT [V] = 40V
LED total current = IOUT [A] = 0.48V
The DCDC input voltage of the power stage = VIN [V] = 24V

The efficiency of DCDC = η [%] = 90%
The averaged input current IIN is calculated as the following.

$$I_{IN}[A] = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} = \frac{40[V] \times 0.48[A]}{24[V] \times 90[\%]} = 0.89 \quad [A]$$

And the ripple current of the inductor L (Δ IL[A]) can be calculated if the switching frequency, fsw = 200kHz, the inductor, L=100μH.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} = \frac{(40[V] - 24[V]) \times 24[V]}{100 \times 10^{-6}[H] \times 40[V] \times 200 \times 10^{3}[Hz]} = 0.48 \quad [A]$$

Therefore the inductor peak current, Ipeak is

$$Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2}[A] = 0.89[A] + \frac{0.48[A]}{2} = 1.13 \quad [A]$$

The calculation result of the peak current

If Rcs is assume to be 0.3 ohm

$$VCS_{peak} = Rcs \times Ipeak = 0.3[\Omega] \times 1.13[A] = 0.339 \quad [V] << 0.4V$$

The Rcs value confirmation

The above condition is met.
And Ipeak_det, the current OCP works is

$$I_{peak\_det} = \frac{0.4[V]}{0.3[\Omega]} = 1.33 \quad [A]$$

If the current rating of the used parts is 2A,

$I_{peak} << I_{peak\_det} <<$ The current rating $= 1.13[A] << 1.33[A] << 2.0[A]$

The current rating confirmation of DCDC parts

This inequality meets the above relationship. The parts selection is proper.
And Imin, the bottom of the IL ripple current can be calculated as following.

$$I_{MIN} = I_{IN}[A] - \frac{\Delta IL[A]}{2}[A] = 1.13[A] - 0.48[A] = 0.65[A] >> 0$$

This inequality implies the operation is the continuous current mode.

3.5.2. Inductor selection

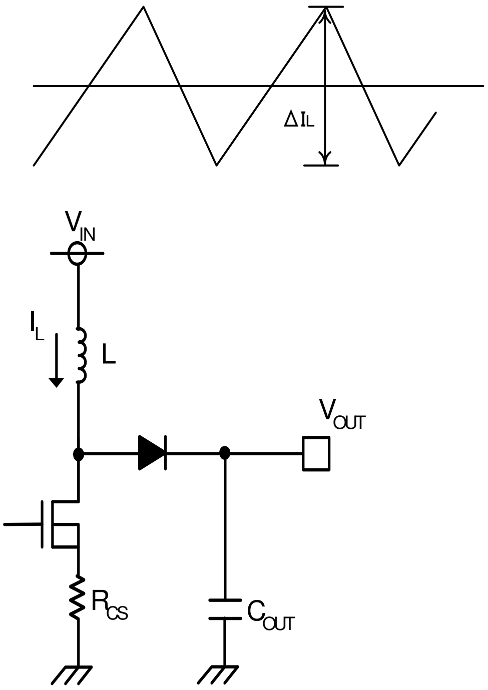


Figure 29. the waveform and the circuit of inductor current

The inductor value affects the input ripple current. The equality in the section 3.5.1 is as following.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$

$$Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} \quad [A]$$

Where
L: the coil inductance [H] Vout: the DCDC output voltage [V]
Vin: the input voltage [V]
Iout: the output load current (the summation of LED current) [A]
Iin: the input current [A] Fsw: the oscillation frequency [Hz]

If in the continuous current mode, Please set ⊿IL to 30% - 50% of the output load current.

* The current exceeding the rated current value of inductor flown through the coil causes magnetic saturation, results in decreasing in efficiency. Inductor needs to be selected to have such adequate margin that peak current does not exceed the rated current value of the inductor.

* To reduce inductor loss and improve efficiency, inductor with low resistance components (DCR, ACR) needs to be selected

3.5.3. Output capacitance Cout selection

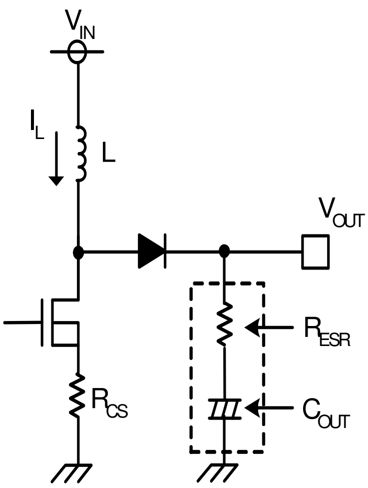


Figure 30. the circuit of the output capacitor

Output capacitor needs to be selected in consideration of equivalent series resistance required to even the stable area of output voltage or ripple voltage. Be aware that set LED current may not be flown due to decrease in LED terminal voltage if output ripple componet is high.
Output ripple voltage ΔV_{OUT} is determined by Equation (4):

$$\Delta V_{OUT} = ILMAX \times R_{ESR} + \frac{1}{C_{OUT}} \times \frac{I_{OUT}}{\eta} \times \frac{1}{f_{SW}} [V] \quad \cdots\cdots \quad (4)$$

where, R_{ESR} is the equivalent series resistance of Cout.

* Rating of capacitor needs to be selected to have adequate margin against output voltage.

* To use an electrolytic capacitor, adequate margin against allowable current is also necessary. Be aware that the LED current is larger than the set value transitionally in case that LED is provided with PWM dimming especially.

3.5.4. MOSFET selection

Though there is no problem if the absolute maximum rating is larger than the rated current of the inductor L, or is larger than the sum of the tolerance voltage of C_{OUT} and the rectifying diode V_F. The product with small gate capacitance (injected charge) needs to be selected to achieve high-speed switching.

* One with over current protection setting or higher is recommended.
* The selection of one with small on resistance results in high efficiency.

3.5.5. Rectifying diode selection

A schottky barrier diode which has current ability higher than the rated current of L, the reverse voltage larger than the tolerance voltage of C_{OUT}, and the low forward voltage VF especially needs to be selected.