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# 5.5V to 28V Input, 2ch Synchronous Buck DC/DC Controller

## BD9528AMUV

### General Description

BD9528AMUV is a dual buck regulator controller with adjustable output voltage from 1.0V to 5.5V and an input voltage range of 5.5 to 28V. High efficiency is achieved with an external synchronous Nch-MOSFET. H<sup>3</sup>Reg™, Rohm's advanced proprietary control method that uses constant on-time control to provide ultra high transient responses to load changes is used. SLLM(Simple Light Load Mode) technology is added to improve efficiency with light loads giving high efficiency over a wide load range. In addition to the dual buck regulator controllers, here are 2 LDO regulators included that are fixed output voltage of 3.3V and 5.0V. Other functions included are soft start, variable frequency, short circuit protection with timer latch, over voltage, and power good outputs. This buck regulator is optimal for high-current applications.

### Features

- Adjustable Simple Light Load Mode (SLLM), Quiet light Load Mode (QLLM), Forced continuous Mode.
- Multifunctional Protection Circuit
  - Settable Over Current Protection (OCP)
  - Thermal Shut down (TSD)
  - Under Voltage Lock Out (UVLO)
  - Over Voltage Protection (OVP)
  - Short Circuit Protection with Timer-Latch (SCP)
- 150kHz to 500kHz Switching frequency.
- Adjustable Soft Start.
- Power Good.
- Dual Linear Regulator (5V/3.3V (total 100mA)).
- Output Discharge.
- Reference voltage Circuit (0.7V).
- Boot diode

### Applications

- Industrial Equipment ,FPGA, POL Power Supply, Mobile PC, Desktop PC, LCD-TV, Digital Components, etc.

### Key Specifications

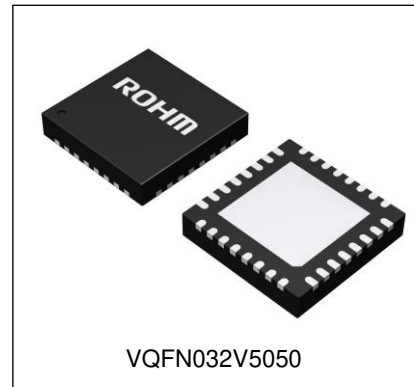
- Input Voltage Range: 5.5V to 28V
- Output Voltage Range: 1.0V to 5.5V
- Switching Frequency: 200k to 500kHz(Typ)
- Operating Temperature Range: -20°C to +100°C

### Package

VQFN032V5050

W(Typ) x D(Typ) x H(Max)

5.00mm x 5.00mm x 1.00mm



Typical Application Circuit

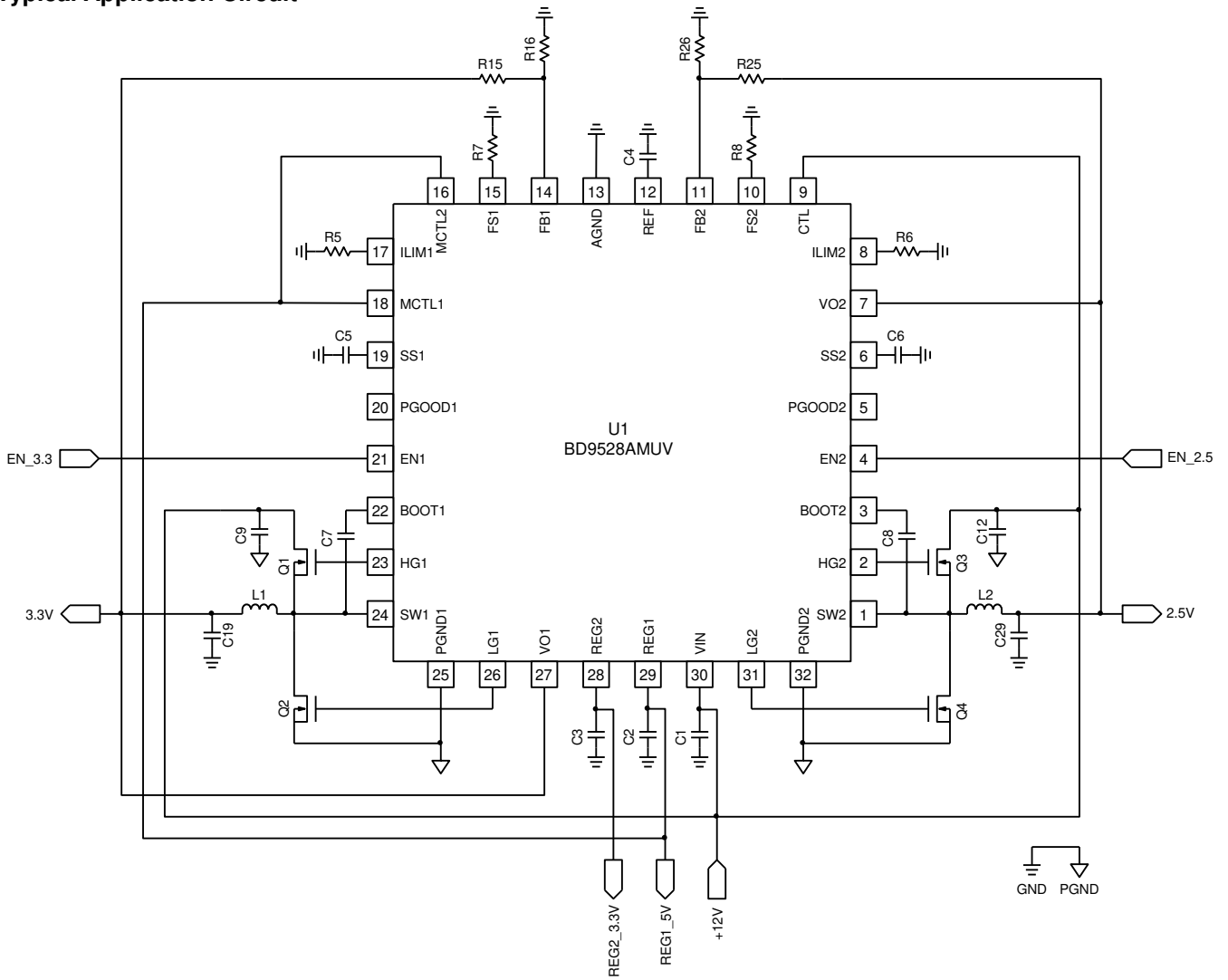


Figure 1. Application Circuit

Pin Configuration

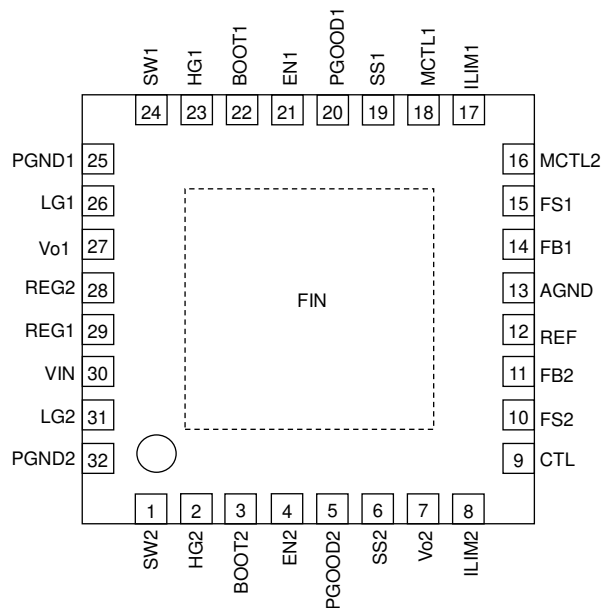


Figure 2. Pin Configuration

## Pin Descriptions

Pin No.	Pin Name	Function																	
1 24	SW2 SW1	Ground pin for High-side FET. The maximum voltage range of this pin is 30V.																	
2 23	HG2 HG1	High-side FET gate drive pin.																	
3 22	BOOT2 BOOT1	This is the power supply pin for High-side FET driver. The maximum voltage range to ground is to 35V, to SW pin is to 7V. In switching operations, the voltage swings from (VIN+REG1) to REG1 by BOOT pin operation.																	
4 21	EN2 EN1	When EN pin voltage is at least 2.3V, the status of the switching regulator becomes active. Conversely, the status switches off when EN pin voltage goes lower than 0.8V. This pin is pulled down to AGND with 1MΩ resistor.																	
5 20	PGOOD2 PGOOD1	If FB pin voltage is 15% or less of reference voltage, it will output low level. The output format is open drain, so please connect pull-up resistance.																	
6 19	SS2 SS1	This is the setting pin for soft start. The rising time is determined by the capacitor connected between SS and ground, and the fixed current inside IC after it is the status of low in standby mode. It controls the output voltage till SS voltage catch up the REF pin to become the SS terminal voltage.																	
7 27	VO2 VO1	This is the output discharge pin, and output voltage feedback pin for frequency setting.																	
8 17	ILIM2 ILIM1	This is the coil current limit setting pin. Set the resistor which is connected in between ground.																	
9	CTL	When CTL pin voltage is at least 2.3V, the status of the linear regulator REG1 and REG2 output becomes active. Conversely, the status switches off when CTL pin voltage goes lower than 0.8V. The switching regulator doesn't become active when the status of CTL pin is low, if the status of EN pin is high. This pin is pulled up to VIN with 1MΩ resistor.																	
10 15	FS2 FS1	Frequency input. A resistor to ground will set the switching frequency. Frequencies from 150kHz to 500kHz are possible.																	
11 14	FB2 FB1	This is the output voltage feedback pin. The IC controls reference voltage and FB terminal voltage are almost same.																	
12	REF	This is the output voltage setting pin. The IC controls reference voltage and FB terminal voltage are almost same.																	
13	AGND	Ground input for control circuit.																	
16 18	MCTL2 MCTL1	<p>This is the operation mode setting pin. If terminal voltage reaches less than 0.8V, it will be Low Level. If terminal voltage reaches more than 2.3V, it will be High Level. This pin is pulled down to AGND with 300kΩ resistor.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2">Input</th> <th rowspan="2">Control Mode</th> </tr> <tr> <th>MCTL1</th> <th>MCTL2</th> </tr> </thead> <tbody> <tr> <td>Low</td> <td>Low</td> <td>SLLM</td> </tr> <tr> <td>Low</td> <td>High</td> <td>QLLM</td> </tr> <tr> <td>High</td> <td>Low</td> <td>Continuous PWM Mode</td> </tr> <tr> <td>High</td> <td>High</td> <td>Continuous PWM Mode</td> </tr> </tbody> </table>	Input		Control Mode	MCTL1	MCTL2	Low	Low	SLLM	Low	High	QLLM	High	Low	Continuous PWM Mode	High	High	Continuous PWM Mode
Input		Control Mode																	
MCTL1	MCTL2																		
Low	Low	SLLM																	
Low	High	QLLM																	
High	Low	Continuous PWM Mode																	
High	High	Continuous PWM Mode																	
25 32	PGND1 PGND2	This is the ground pin for Low-side FET drive.																	
26 31	LG1 LG2	This is the Low-side FET gate drive pin. It is operated in switching between REG1 to PGND. ON resistance of output stage when High, it is 2Ω and when Low, it is 0.5Ω drive Low-side FET gate with the high pace.																	
28	REG2	This is the output pin for 3.3V/50mA linear regulator (5V/3.3V (total 100mA)). Please connect 10μF capacitor which characteristic is more than X5R near the pin.																	
29	REG1	This is the output pin for 5V/50mA linear regulator (5V/3.3V (total 100mA)). Please connect 10μF capacitor which characteristic is more than X5R near the pin.																	
30	VIN	Supply pin of H <sup>3</sup> Reg™ control circuit and linear regulator. Monitor input voltage and determine necessary on-time. As a result, this terminal voltage changes, and then the IC operation become unstable. Please connect 10μF capacitor which characteristic is more than X5R near the pin.																	
FIN	FIN	This is the thermal PAD. Please connect to the ground.																	

Output condition table

Input			Output			
CTL	EN1	EN2	REG1(5V)	REG2(3.3V)	DC/DC1	DC/DC2
Low	Low	Low	OFF	OFF	OFF	OFF
Low	Low	High	OFF	OFF	OFF	OFF
Low	High	Low	OFF	OFF	OFF	OFF
Low	High	High	OFF	OFF	OFF	OFF
High	Low	Low	ON	ON	OFF	OFF
High	Low	High	ON	ON	OFF	ON
High	High	Low	ON	ON	ON	OFF
High	High	High	ON	ON	ON	ON

\* CTL pin is connected to VIN pin with 1MΩ resistor(pull up) internal IC.  
 \* EN pin is connected to AGND pin with 1MΩ resistor(pull down) internal IC.

Block Diagram

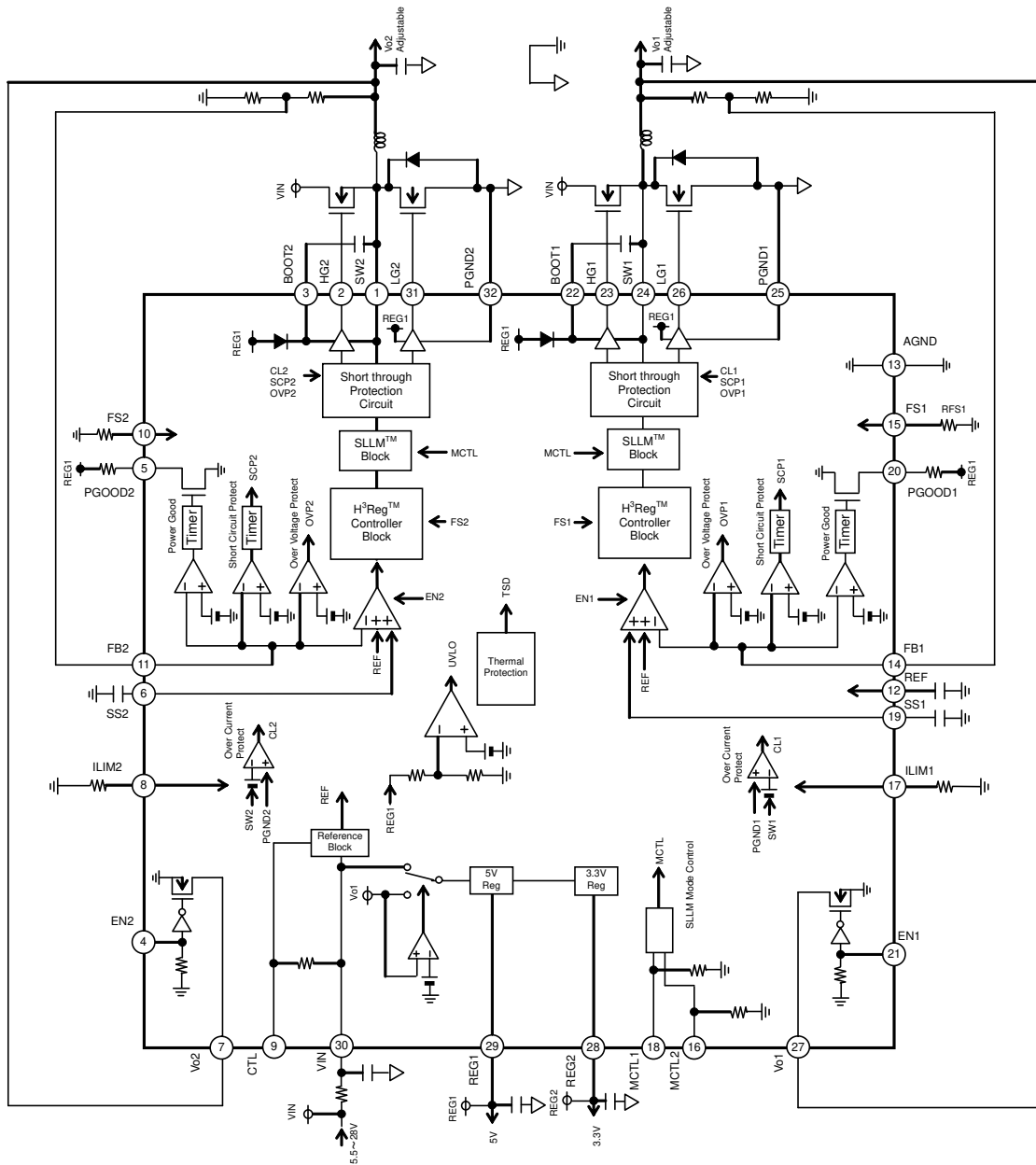


Figure 3. Block Diagram

## Absolute Maximum Ratings(Ta = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Terminal Voltage	VIN, CTL, SW1, SW2	30	V	Note 1
	EN1, EN2, PGOOD1, PGOOD2 Vo1, Vo2, MCTL1, MCTL2	6	V	Note 1, Note 2
	FS1, FS2, FB1, FB2, ILIM1, ILIM2, SS1, SS2, LG1, LG2, REF,REG2	REG1+0.3	V	Note 1
	BOOT1, BOOT2	35	V	Note 1, Note 2
	BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2	7	V	Note 1, Note 2
	HG1	BOOT1+0.3	V	Note 1, Note 2
	HG2	BOOT2+0.3	V	Note 1, Note 2
	PGND1, PGND2	AGND±0.3	V	Note 1, Note 2
Power Dissipation1	Pd1	0.38	W	Note 3
Power Dissipation2	Pd2	0.88	W	Note 4
Power Dissipation3	Pd3	3.26	W	Note 5
Power Dissipation4	Pd4	4.56	W	Note 6
Operating Temperature Range	Topr	-20 to +100	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Junction Temperature	Tjmax	+150	°C	

(Note 1) Not to exceed Pd.

(Note 2) Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.

(Note 3) Derating in done 3.0 mW/°C for operating above Ta ≥ 25°C (when don't mounted on a heat radiation board).

(Note 4) Derating in done 7.0 mW/°C for operating above Ta ≥ 25°C (Mount on 1-layer 74.2mm x 74.2mm x 1.6mm board).  
Surface heat dissipation copper foil:20.2mm<sup>2</sup>.

(Note 5) Derating in done 26.1 mW/°C for operating above Ta ≥ 25°C (Mount on 4-layer 74.2mm x 74.2mm x 1.6mm board  
Two sides heat dissipation copperfoil:20.2mm<sup>2</sup>. 2 or 3-layer : heat dissipation copper foil : 5505mm<sup>2</sup>).

(Note 6) Derating in done 36.5 mW/°C for operating above Ta ≥ 25°C (Mount on 4-layer 74.2mm x 74.2mm x 1.6mm board)  
All layers heat dissipation copper foil:5505mm<sup>2</sup>.

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Terminal Voltage	VIN	5.5	-	28	V	
	CTL	-0.3	-	28	V	
	EN1, EN2, MCTL1, MCTL2	-0.3	-	5.5	V	
	BOOT1, BOOT2	4.5	-	33	V	
	SW1, SW2	-0.3	-	28	V	
	BOOT1-SW1, BOOT2-SW2, HG1-SW1, HG2-SW2	-0.3	-	5.5	V	
	Vo1, Vo2, PGOOD1, PGOOD2	-0.3	-	5.5	V	
Minimum ON Time	TONMIN	-	-	150	nsec	
Soft Start time	Tss_max	-	-	100	ms	

This product should not be used in a radioactive environment.

**Electrical Characteristics** (Unless otherwise noted, Ta=25°C VIN=12V, CTL=OPEN, EN1=EN2=5V, FS1=FS2=51kΩ)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VIN Standby Current	I <sub>STB</sub>	70	150	250	μA	EN1= EN2= 0V, CTL= 5V
VIN Bias Current	I <sub>IN</sub>	60	130	230	μA	Vo1= 5V
VIN Shut Down Mode Current	I <sub>SHD</sub>	6	12	18	μA	CTL= 0V
CTL Low Voltage	V <sub>CTL</sub> L	-0.3	-	0.8	V	
CTL High Voltage	V <sub>CTL</sub> H	2.3	-	28	V	
CTL Bias Current	I <sub>CTL</sub>	-18	-12	-6	μA	CTL= 0V
EN Low Voltage	V <sub>EN</sub> L	-0.3	-	0.8	V	
EN High Voltage	V <sub>EN</sub> H	2.3	-	5.5	V	
EN Bias Current	I <sub>EN</sub>	-	3	6	μA	EN= 3V
5V Linear Regulator -VIN						
REG1 Output Voltage	V <sub>REG1</sub>	4.90	5.00	5.10	V	I <sub>REG1</sub> =1mA
Maximum Current	I <sub>REG1</sub>	100	-	-	mA	I <sub>REG2</sub> = 0mA, (Note 7)
Line Regulation	R <sub>REG1</sub>	-	90	180	mV	VIN= 5.5 to 28V
Load Regulation	R <sub>REG1</sub> L	-	30	50	mV	I <sub>REG1</sub> = 0 to 30mA
3.3V Linear Regulator						
REG2 Output Voltage	V <sub>REG2</sub>	3.27	3.30	3.33	V	I <sub>REG2</sub> = 1mA
Maximum Current	I <sub>REG2</sub>	100	-	-	mA	I <sub>REG1</sub> = 0mA, (Note 7)
Line Regulation	R <sub>REG2</sub>	-	-	20	mV	VIN= 5.5 to 28V
Load Regulation	R <sub>REG2</sub> L	-	-	30	mV	I <sub>REG2</sub> = 0 to 30mA
5V Linear Regulator -Vo1						
Input Threshold Voltage	R <sub>REG1</sub> th	4.1	4.4	4.7	V	Vo1: Sweep up
Input Delay Time	T <sub>REG1</sub>	1.5	3.0	6.0	ms	
Switch Resistance	R <sub>REG1</sub>	-	1.0	3.0	Ω	
Under Voltage Lock Out Block						
REG1 Threshold Voltage	R <sub>REG1</sub> _UVLO	3.9	4.2	4.5	V	REG1: Sweep up
Hysteresis Voltage	dV_ <sub>UVLO</sub>	50	100	200	mV	REG1: Sweep down
Output Voltage Sense Block						
Feedback Voltage1	V <sub>FB1</sub>	0.693	0.700	0.707	V	
FB1 Bias Current	I <sub>FB1</sub>	-	0	1	μA	FB1= REF
Output Discharge Resistance1	R <sub>DISOUT1</sub>	50	100	200	Ω	
Feedback Voltage2	V <sub>FB2</sub>	0.693	0.700	0.707	V	
FB2 Bias Current	I <sub>FB2</sub>	-	0	1	μA	FB2= REF
Output Discharge Resistance2	R <sub>DISOUT2</sub>	50	100	200	Ω	
H <sup>3</sup> REG™ Control Block						
On Time1	t <sub>ON1</sub>	0.760	0.910	1.060	μs	Vo1= 5V,FS1= 51kΩ
On Time2	t <sub>ON2</sub>	0.470	0.620	0.770	μs	Vo2= 3.3V ,FS2= 51kΩ
Maximum On Time 1	t <sub>ONMAX1</sub>	2.5	5	10	μs	Vo1= 5V
Maximum On Time 2	t <sub>ONMAX2</sub>	1.65	3.3	6.6	μs	Vo2= 3.3V
Minimum Off Time	t <sub>OFFMIN</sub>	-	0.2	0.4	μs	
FET Driver Block						
HG High Side ON Resistance	HGHON	-	3.0	6.0	Ω	
HG Low Side ON Resistance	HGLON	-	2.0	4.0	Ω	
LG High Side ON Resistance	LGHON	-	2.0	4.0	Ω	
LG Low Side ON Resistance	LGLON	-	0.5	1.0	Ω	

(Note 7) I<sub>REG1</sub>+I<sub>REG2</sub> ≤ 100mA.

**Electrical Characteristics** (Unless otherwise noted, Ta=25°C VIN=12V, CTL=OPEN, EN1=EN2=5V, FS1=FS2=51kΩ)

Over Voltage Protection Block						
OVP Threshold Voltage	VOVP	0.77 (+10%)	0.84 (+20%)	0.91 (+30%)	V	
OVP Hysteresis	dV_OVP	50	150	300	mV	
Output Short Protection Block						
SCP Threshold Voltage	VSCP	0.42 (-40%)	0.49 (-30%)	0.56 (-20%)	V	
Delay Time	TSCP	0.4	0.75	1.5	ms	
Over Current Protection Block						
Offset Voltage	dVS MAX	80	100	120	mV	ILIM= 100kΩ
Power Good Block						
Power Good Low Threshold	VPGTHL	0.525 (-25%)	0.595 (-15%)	0.665 (-5%)	V	
Power Good Low Voltage	VPGL	-	0.1	0.2	V	IPGOOD= 1mA
Delay Time	TPGOOD	0.4	0.75	1.5	ms	
Power Good Leakage Current	ILEAKPG	-2	0	2	μA	VPGOOD= 5V
Soft Start Block						
Charge Current	ISS	1.5	2.3	3.1	μA	
Standby Voltage	VSS_STB	-	-	50	mV	
Mode Control Block						
MCTL Low Voltage	VMCTL_L	-0.3	-	0.3	V	
MCTL High Voltage	VMCTL_H	2.3	-	REG1 +0.3	V	
MCTL Bias Current	IMCTL	8	16	24	μA	MCTL= 5V



Typical Performance Curves (Reference data)

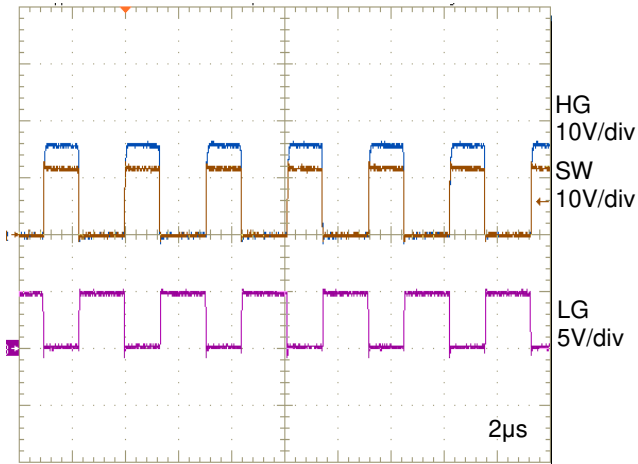


Figure 1. Switching Waveform  
( $V_o = 5V$ ,  $I_o = 0A$ , PWM)

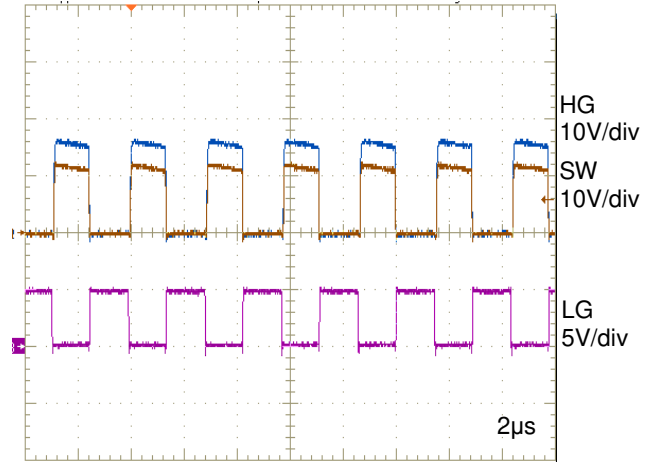


Figure 2. Switching Waveform  
( $V_o = 5V$ ,  $I_o = 8A$ , PWM)

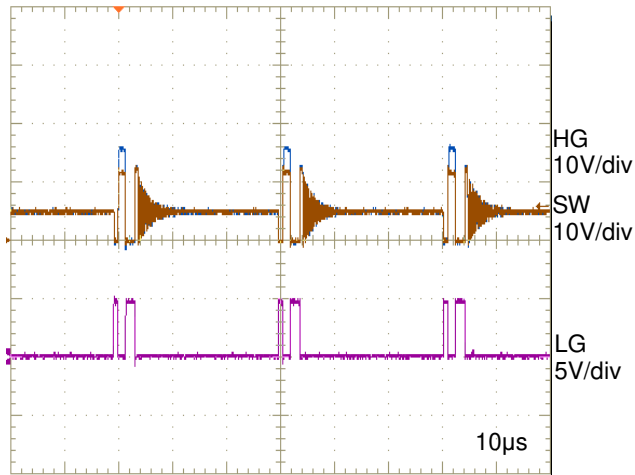


Figure 3. Switching Waveform  
( $V_o = 5V$ ,  $I_o = 0A$ , QLLM)

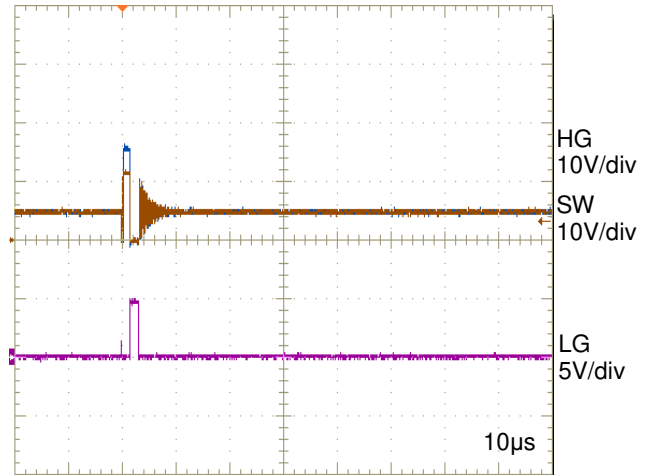


Figure 4. Switching Waveform  
( $V_o = 5V$ ,  $I_o = 0A$ , SLLM)

Typical Performance Curves - continued

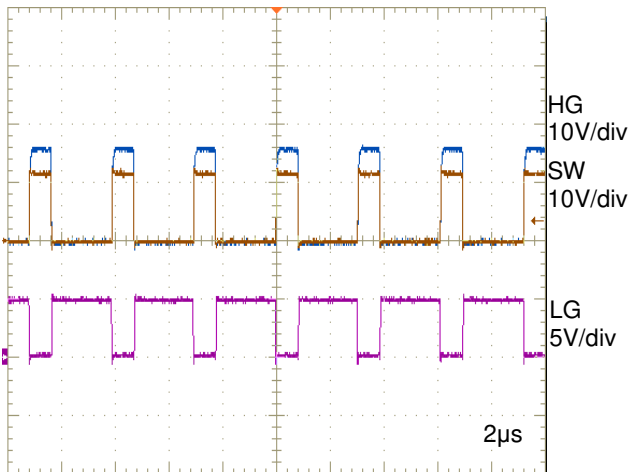


Figure 5. Switching Waveform  
( $V_o = 3.3V$ ,  $I_o = 0A$ , PWM)

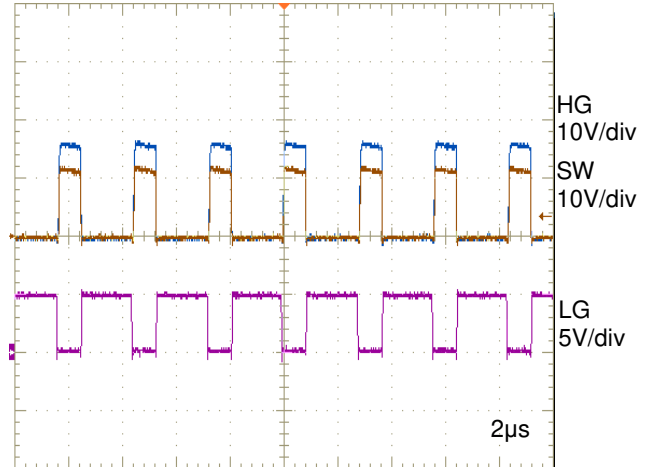


Figure 6. Switching Waveform  
( $V_o = 3.3V$ ,  $I_o = 8A$ , PWM)

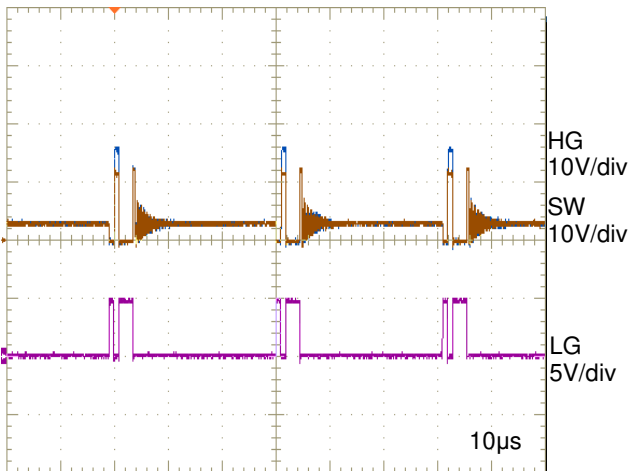


Figure 7. Switching Waveform  
( $V_o = 3.3V$ ,  $I_o = 0A$ , QLLM)

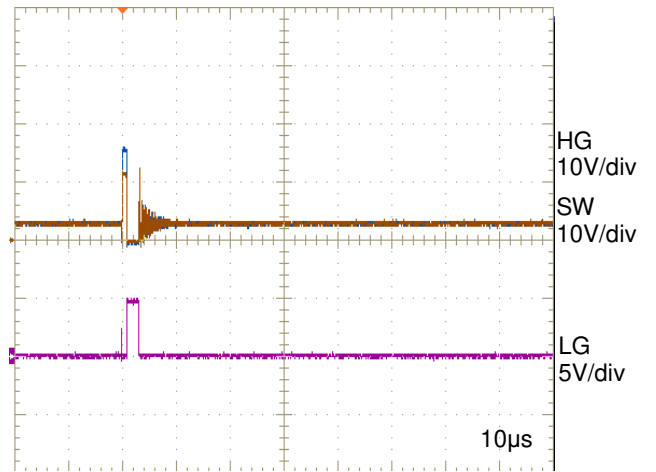


Figure 8. Switching Waveform  
( $V_o = 3.3V$ ,  $I_o = 0A$ , SLLM)

Typical Performance Curves - continued

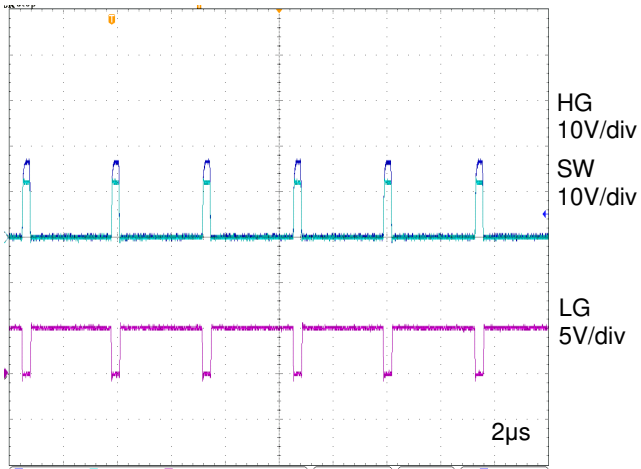


Figure 9. Switching Waveform  
( $V_o = 1V$ ,  $I_o = 0A$ , PWM)

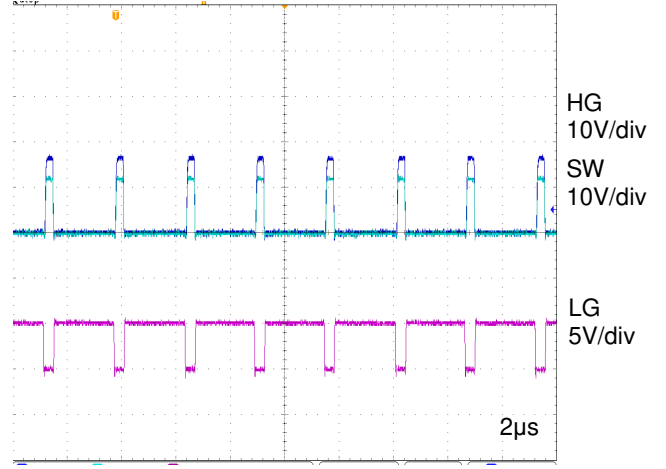


Figure 10. Switching Waveform  
( $V_o = 1V$ ,  $I_o = 8A$ , PWM)

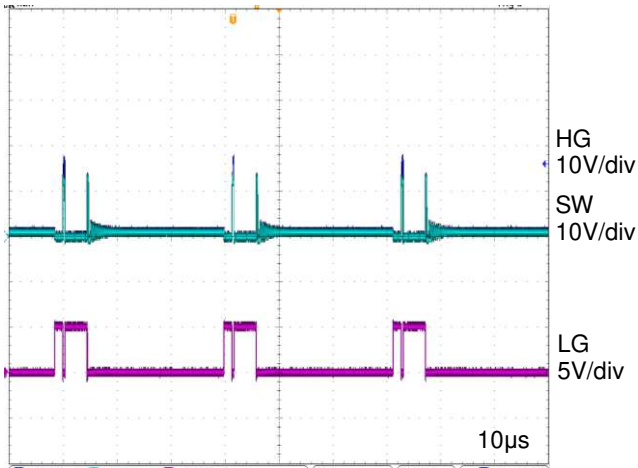


Figure 11. Switching Waveform  
( $V_o = 1V$ ,  $I_o = 0A$ , QLLM)

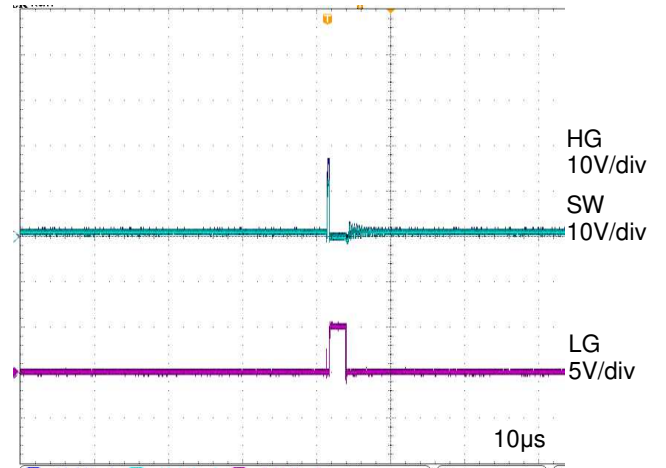


Figure 12. Switching Waveform  
( $V_o = 1V$ ,  $I_o = 0A$ , SLLM)

Typical Performance Curves - continued

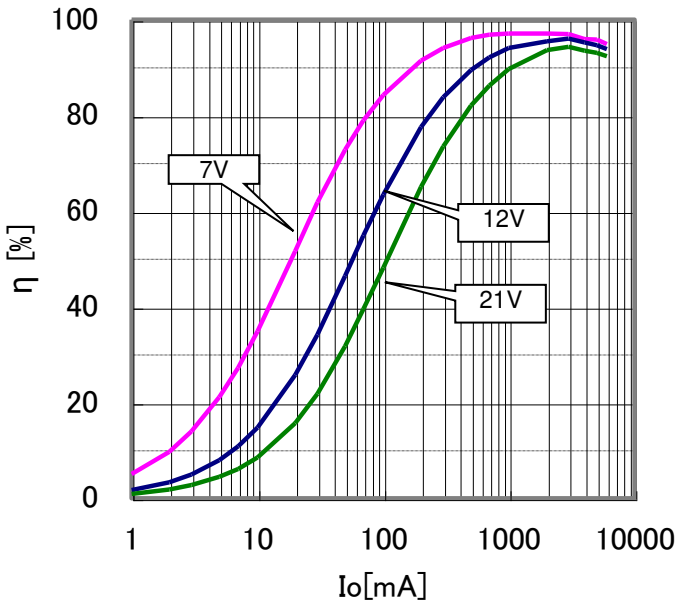


Figure 13. Efficiency  
(Vo= 5V, PWM)

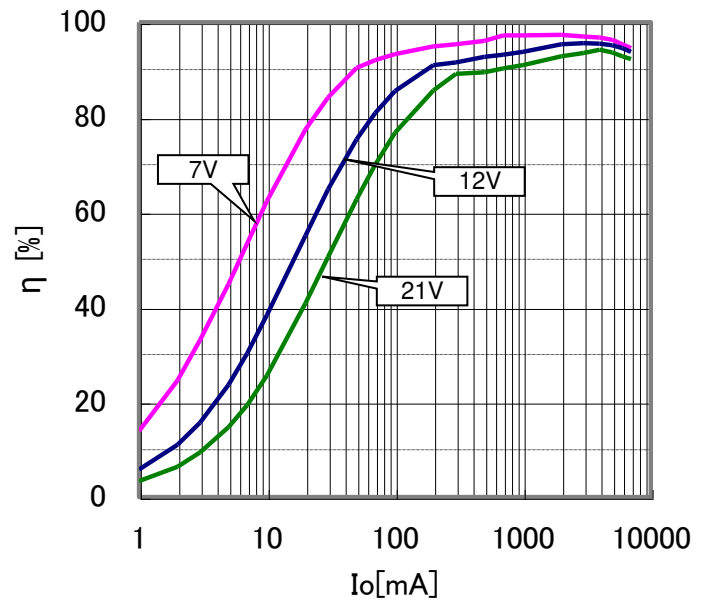


Figure 14. Efficiency  
(Vo= 5V, QLLM)

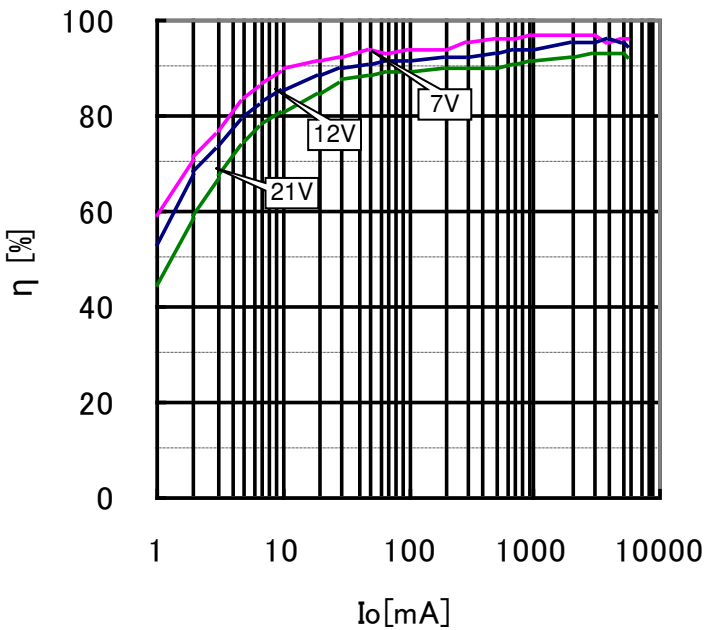


Figure 15. Efficiency  
(Vo= 5V, SLLM)

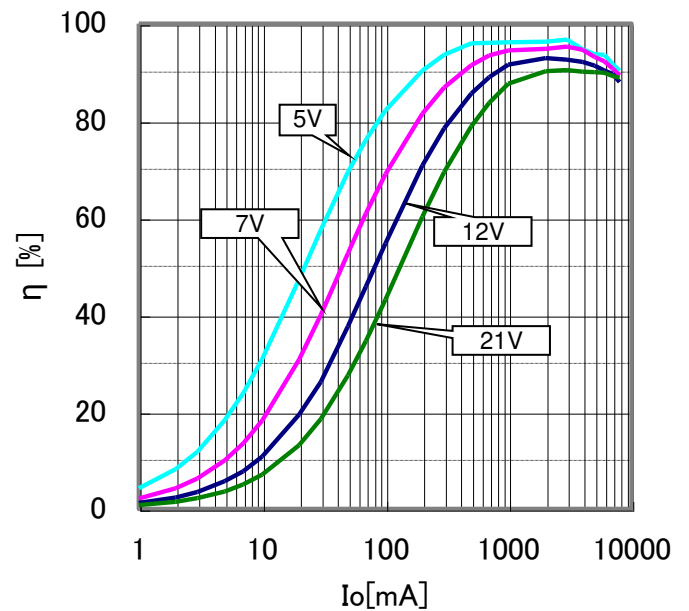


Figure 16. Efficiency  
(Vo= 3.3V, PWM)

Typical Performance Curves - continued

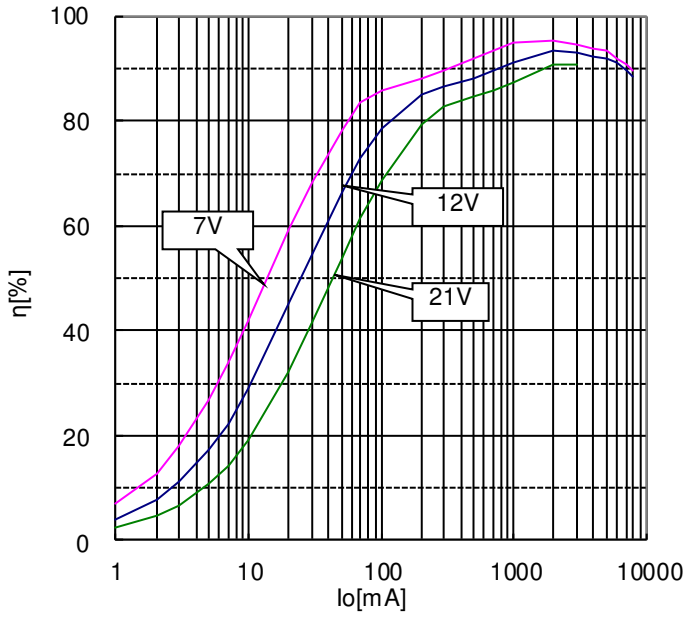


Figure 17. Efficiency  
(Vo= 3.3V, QLLM)

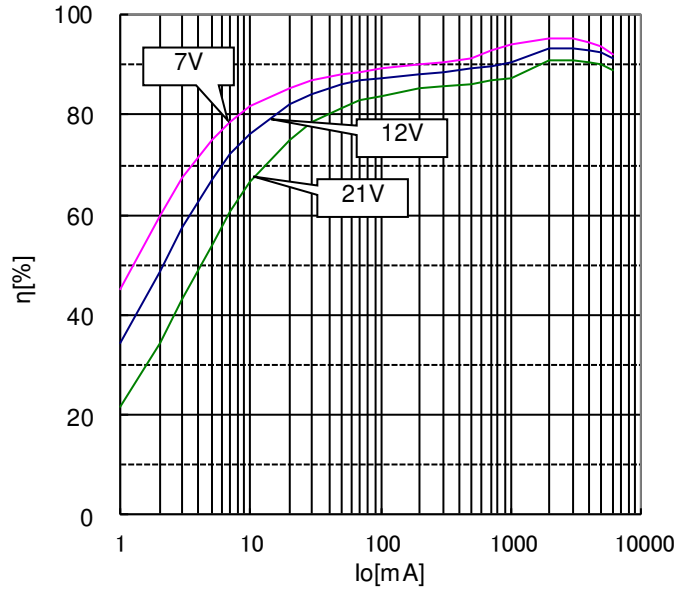


Figure 18. Efficiency  
(Vo= 3.3V, SLLM)

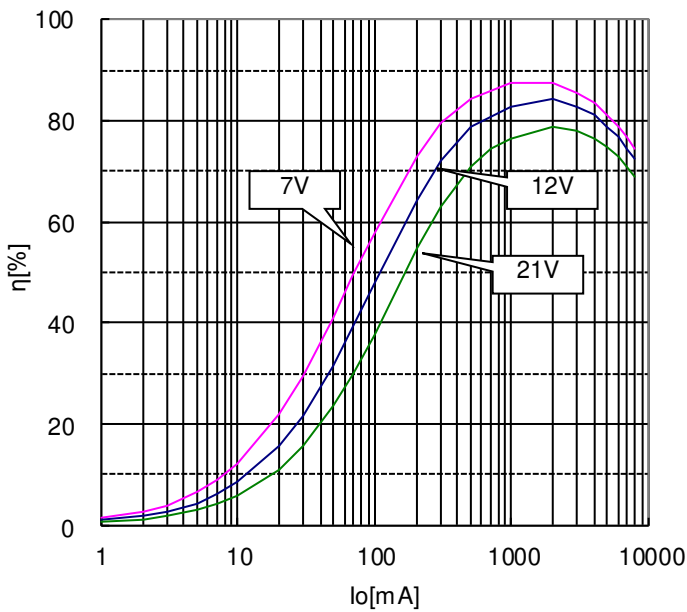


Figure 19. Efficiency  
(Vo= 1V, PWM)

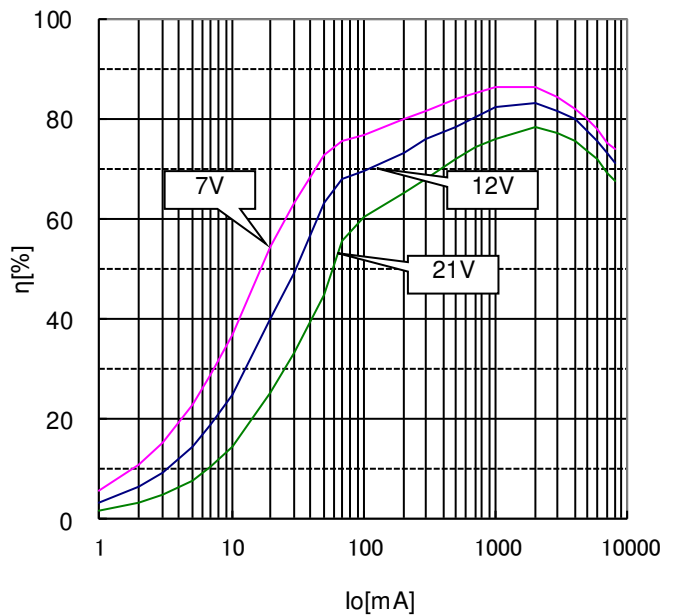


Figure 20. Efficiency  
(Vo= 1V, QLLM)

Typical Performance Curves - continued

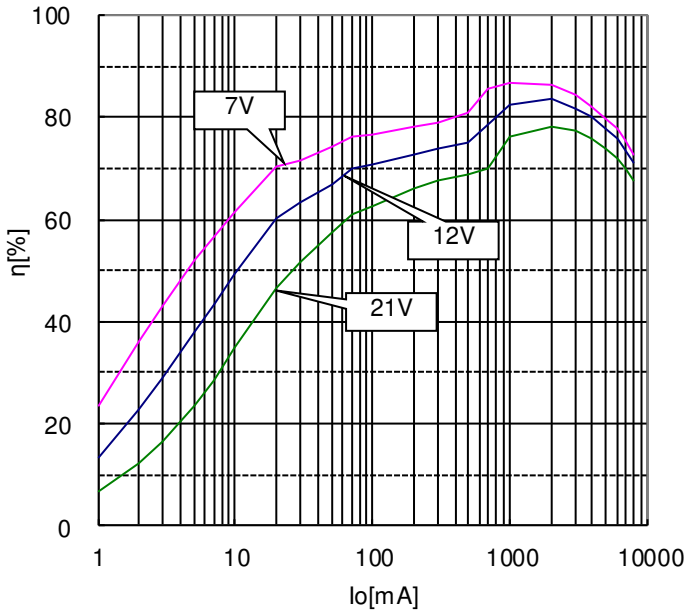


Figure 21. Efficiency  
( $V_o = 1V$ , SLLM)

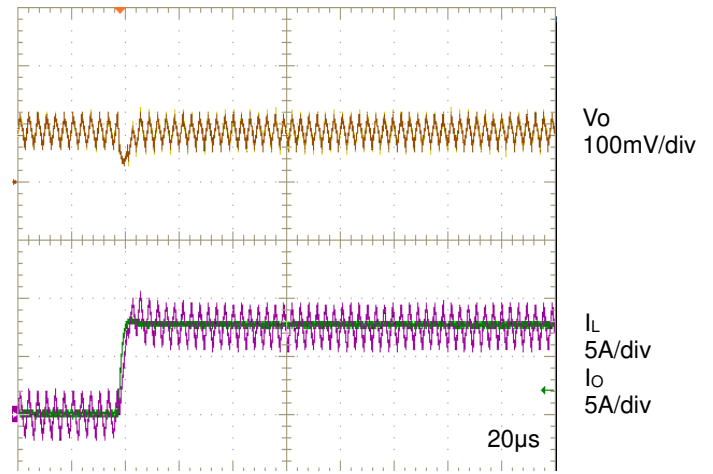


Figure 22. Transient Response  
( $V_o = 5V$ , PWM,  $I_o = 0A \rightarrow 8A$ )

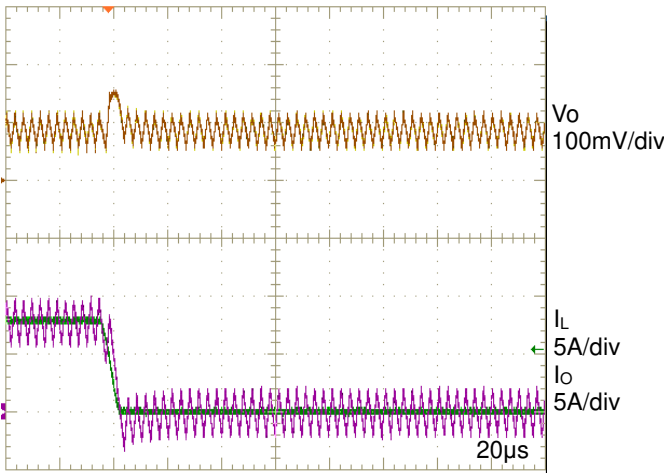


Figure 23. Transient Response  
( $V_o = 5V$ , PWM,  $I_o = 8A \rightarrow 0A$ )

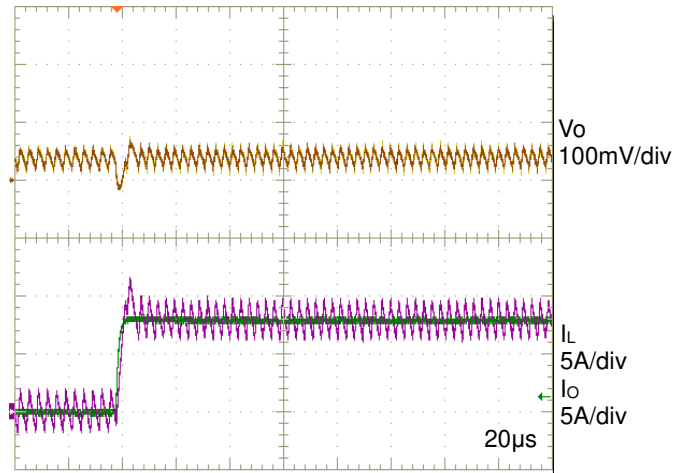


Figure 24. Transient Response  
( $V_o = 3.3V$ , PWM,  $I_o = 0A \rightarrow 8A$ )

Typical Performance Curves - continued

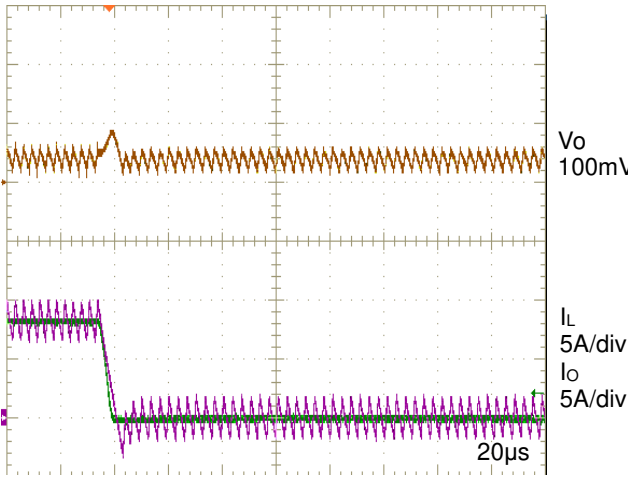


Figure 25. Transient Response  
( $V_o = 3.3V$ , PWM,  $I_o = 8A \rightarrow 0A$ )

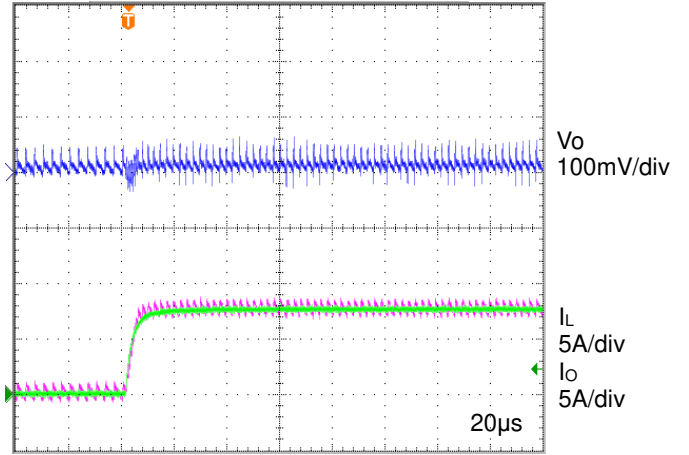


Figure 26. Transient Response  
( $V_o = 1V$ , PWM,  $I_o = 0A \rightarrow 8A$ )

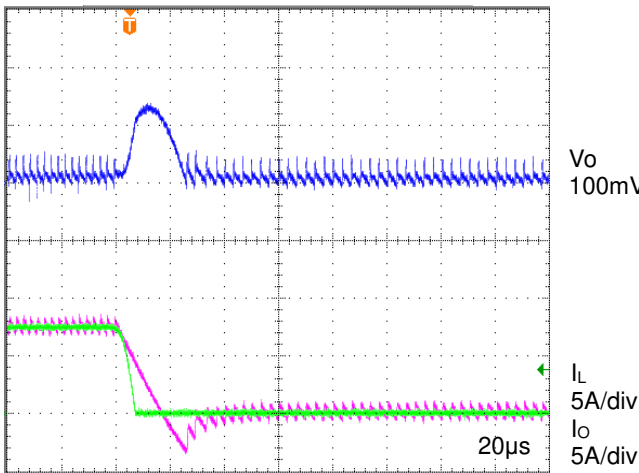


Figure 27. Transient Response  
( $V_o = 1V$ , PWM,  $I_o = 8A \rightarrow 0A$ )

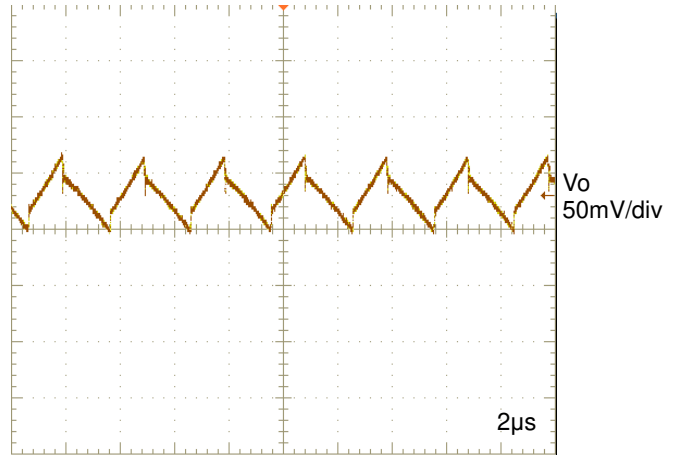


Figure 28. Output Voltage  
( $V_o = 5V$ , PWM,  $I_o = 0A$ )

Typical Performance Curves - continued

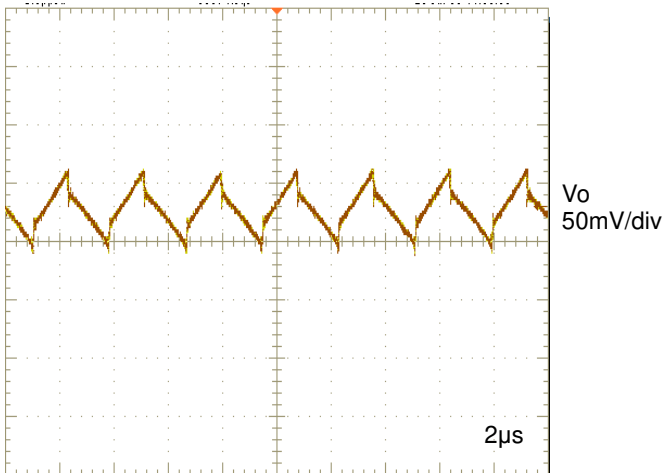


Figure 29. Output Voltage  
(Vo= 5V, PWM, Io= 8A)

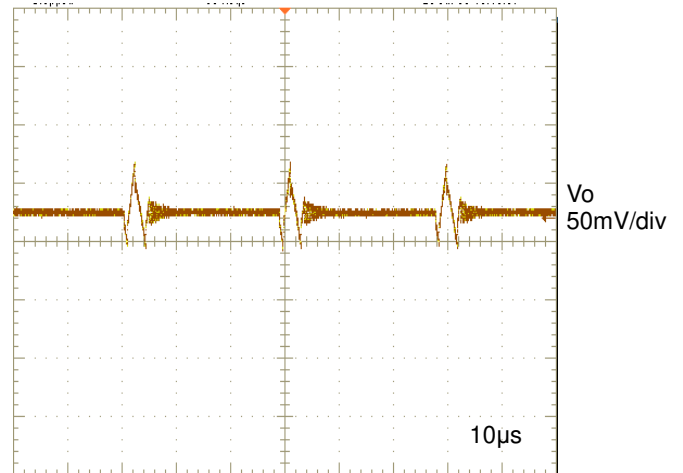


Figure 30. Output Voltage  
(Vo= 5V, QLLM, Io= 0A)

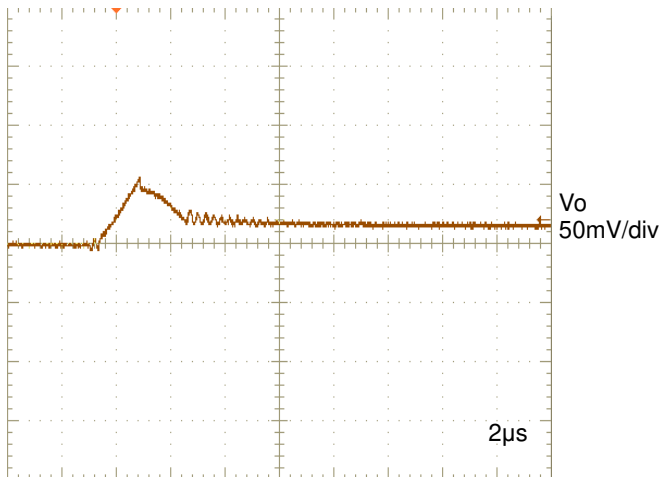


Figure 31. Output Voltage  
(Vo= 5V, SLLM, Io= 0A)

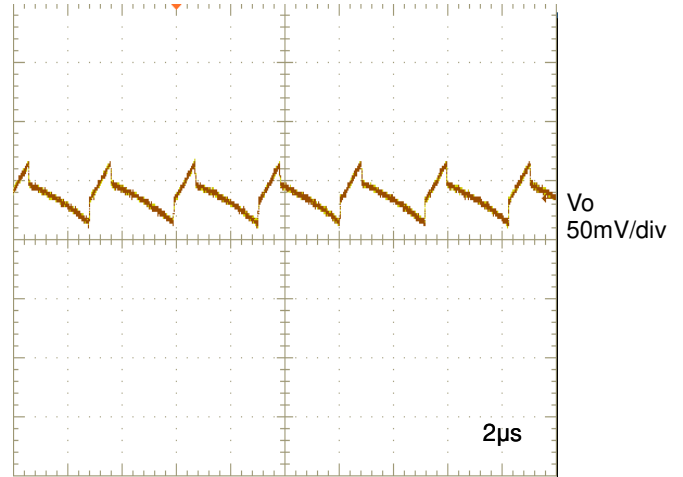


Figure 32. Output Voltage  
(Vo= 3.3V, PWM, Io= 0A)



Typical Performance Curves - continued

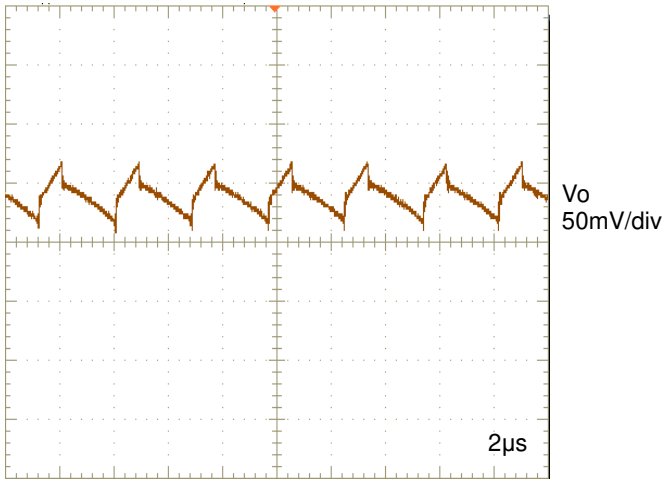


Figure 33. Output Voltage  
(Vo= 3.3V, PWM, Io= 8A)

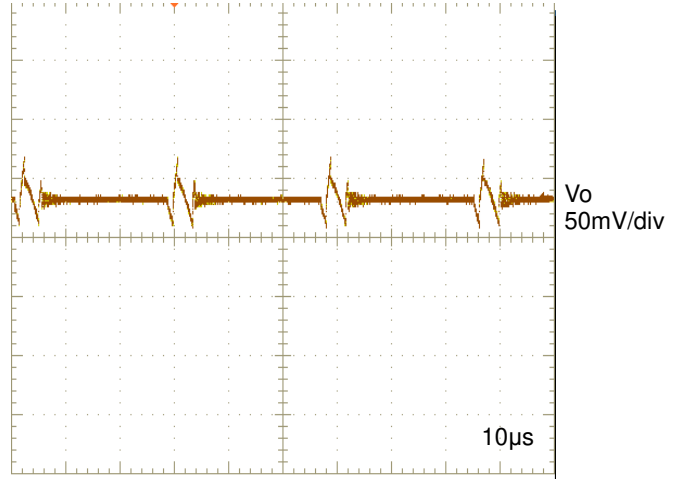


Figure 34. Output Voltage  
(Vo= 3.3V, QLLM, Io= 0A)

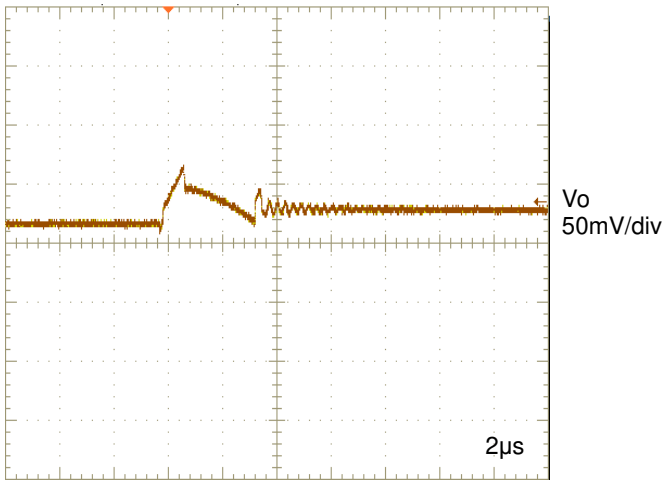


Figure 35. Output Voltage  
(Vo= 3.3V, SLLM, Io= 0A)

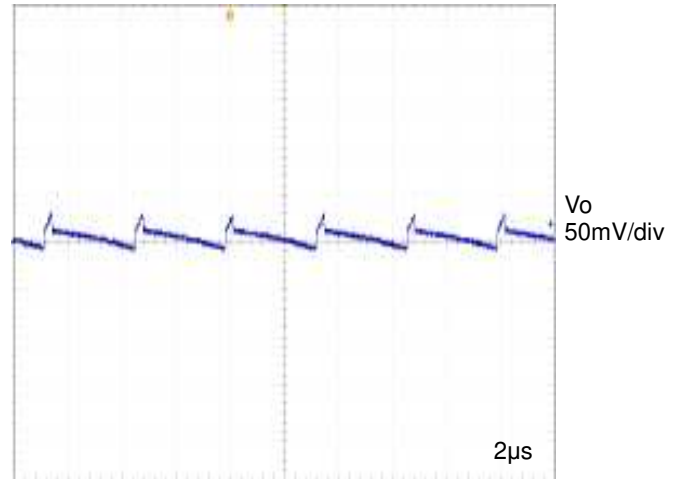


Figure 36. Output Voltage  
(Vo= 1V, PWM, Io= 0A)

Typical Performance Curves - continued

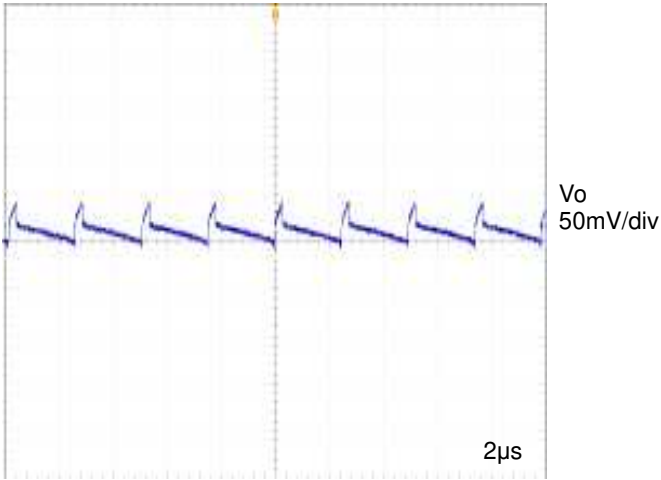


Figure 37. Output Voltage  
(Vo= 1V, PWM, Io= 8A)

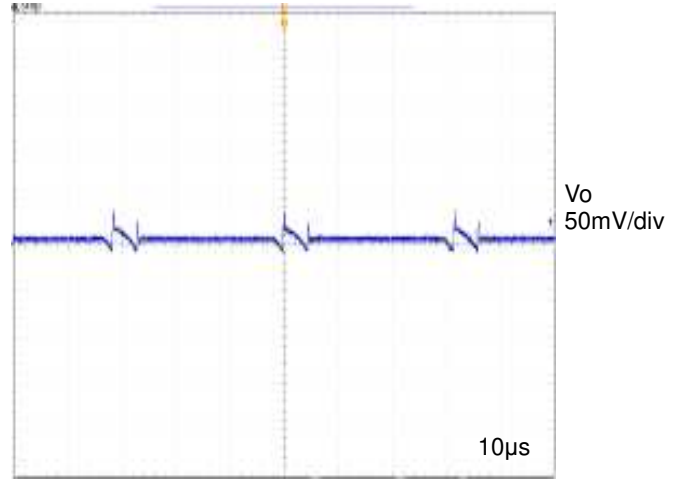


Figure 38. Output Voltage  
(Vo= 1V, QLLM, Io= 0A)

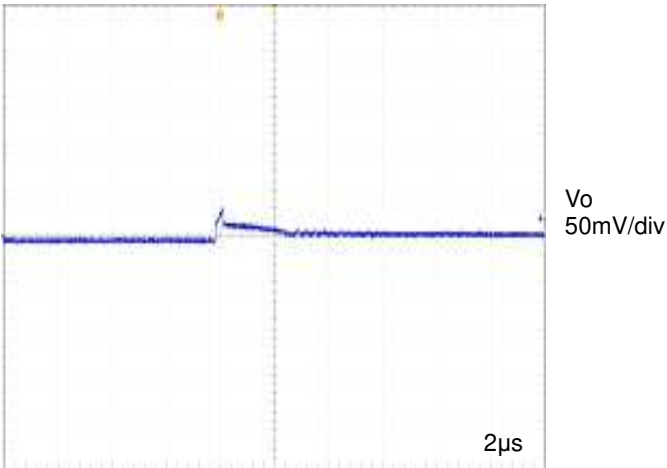


Figure 39. Output Voltage  
(Vo= 1V, SLLM, Io= 0A)

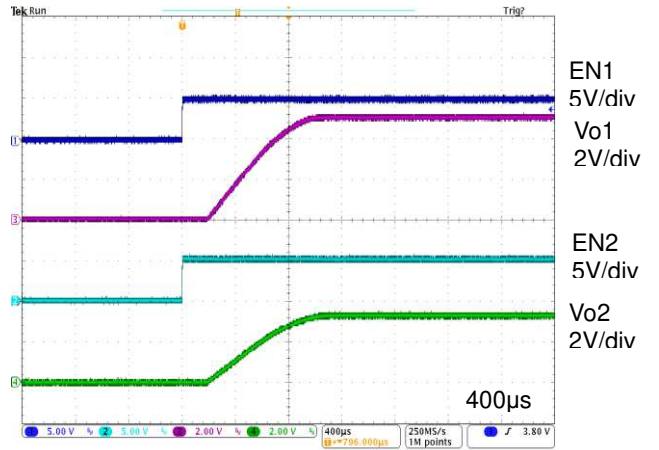


Figure 40. Start-up  
(EN1= EN2)

Typical Performance Curves - continued

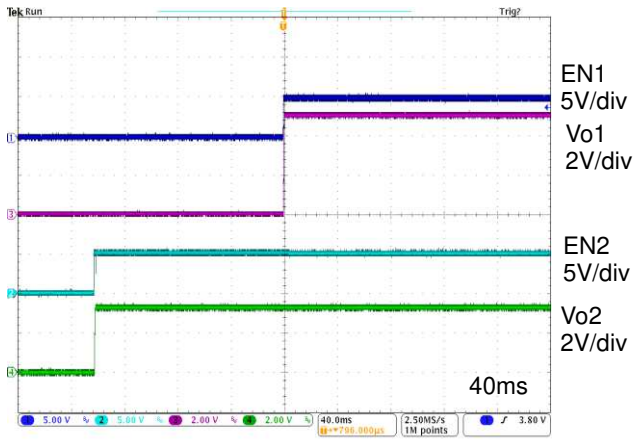


Figure 41. Start-up (EN2→EN1)

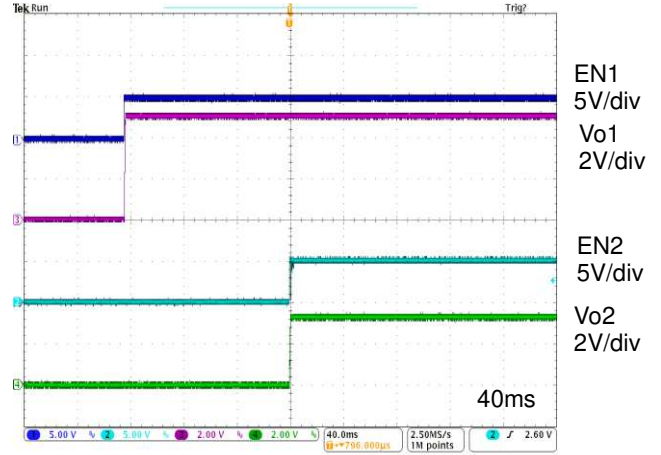


Figure 42. Start-up (EN1→EN2)

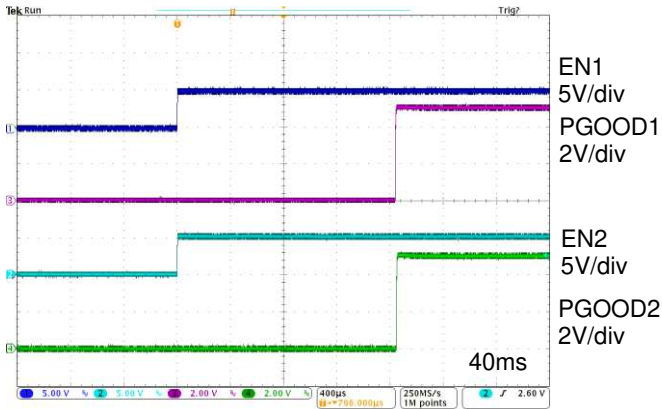


Figure 43. Start-up (EN1/2→PGOOD1/2)

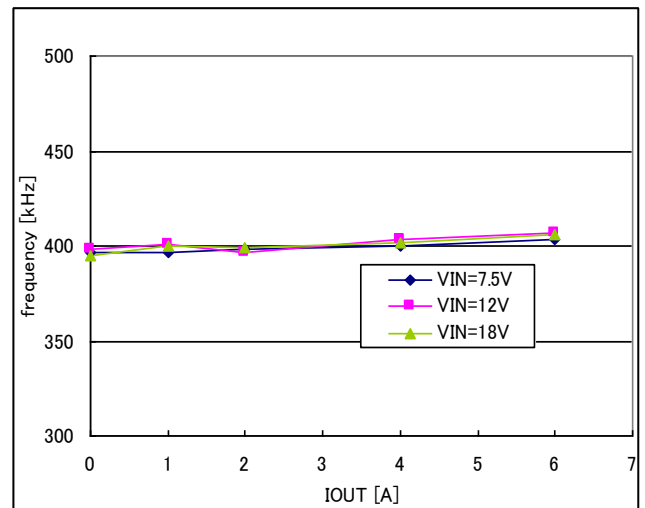


Figure 44. Io-frequency (Vo= 5V, PWM, RFS= 68kΩ)

Typical Performance Curves - continued

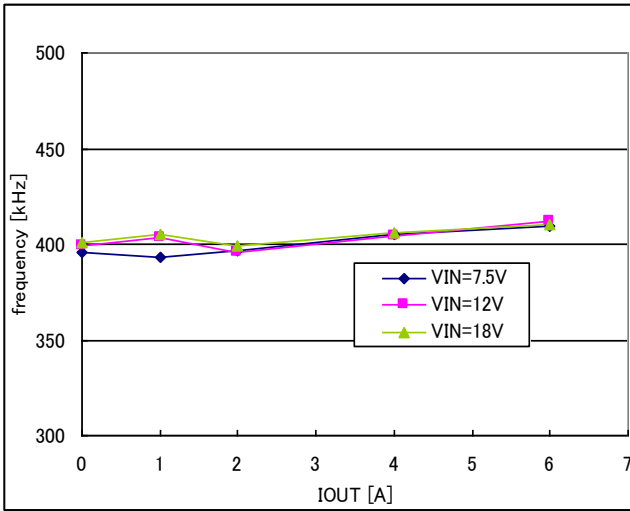


Figure 45. lo-frequency  
(Vo= 3.3V, PWM, RFS= 68kΩ)

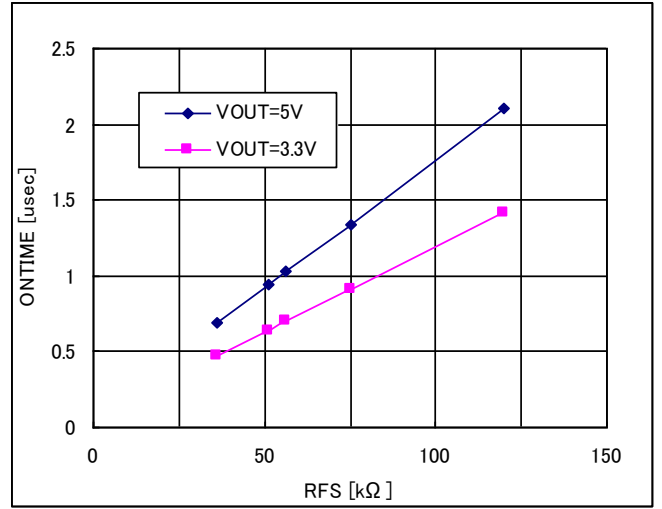


Figure 46. On time-RFS

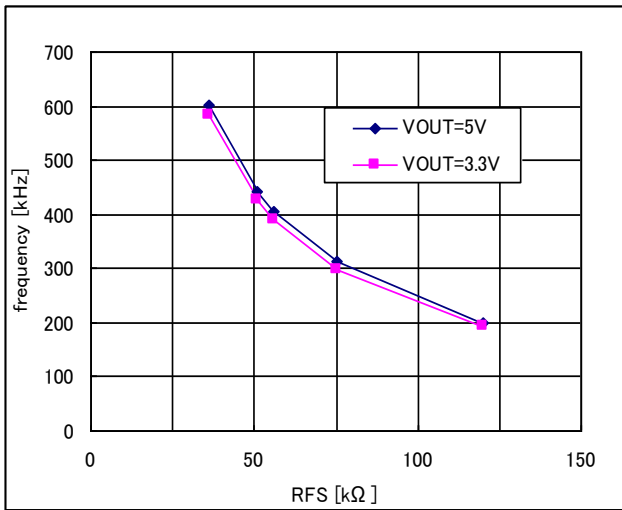


Figure 47. SW Frequency-RFS

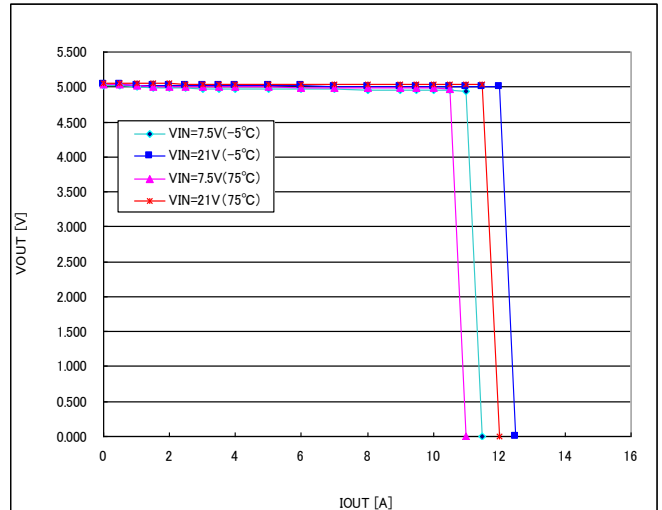


Figure 48. Current Limit  
(Vo= 5V)

Typical Performance Curves - continued

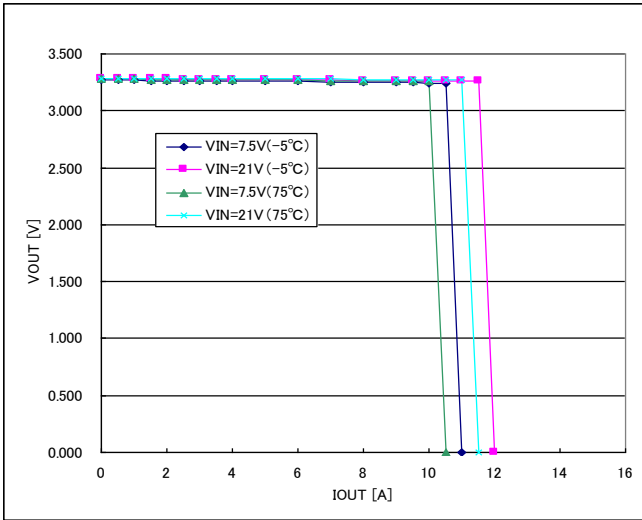


Figure 49. Current Limit (Vo= 3.3V)

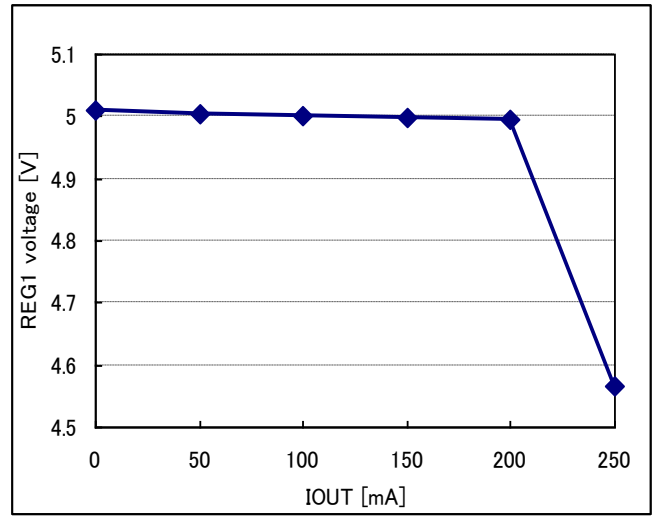


Figure 50. REG1 Load Regulation

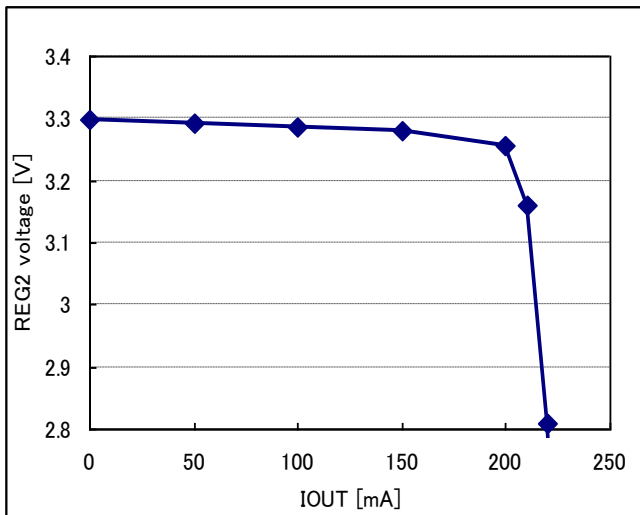
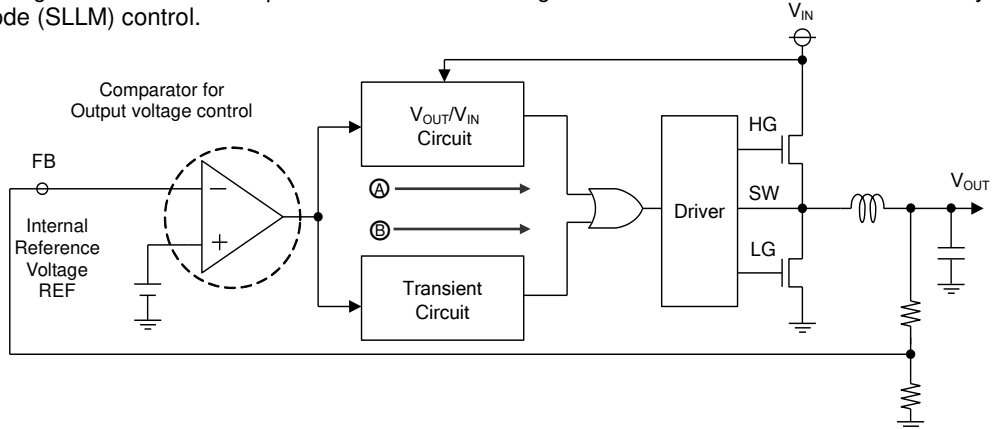


Figure 51. REG2 Load Regulation

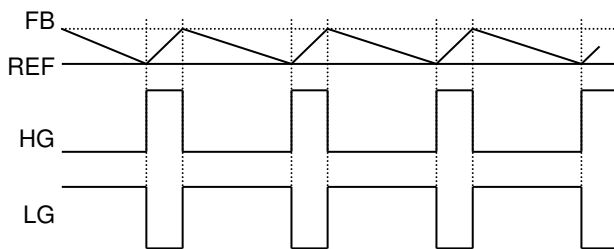
**Description of Block**

BD9528AMUV is a dual channel synchronous buck regulator using H<sup>3</sup>Reg™, Rohm's latest constant on-time controller technology. Fast load response is achieved by controlling the output voltage using a comparator without relying on the switching frequency. When V<sub>OUT</sub> drops due to a rapid load change, the system quickly restores V<sub>OUT</sub> by extending the t<sub>ON</sub> time interval. Thus, it serves to improve the regulator's transient response. Activation of the light load mode further increases efficiency by using Simple Light Load Mode (SLLM) control.

**H<sup>3</sup>Reg™ Control**



(Normal operation)



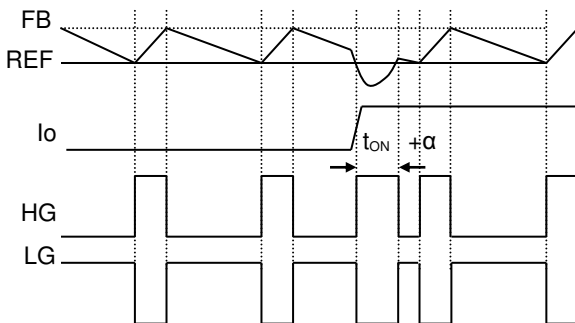
When FB falls to a reference voltage (REF), the drop is detected, activating the H<sup>3</sup>Reg™ control system

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \text{ [sec]} \dots (1)$$

HG output on-time is determined by the formula (1). When HG is off, LG is on until the output voltage becomes FB= REF.

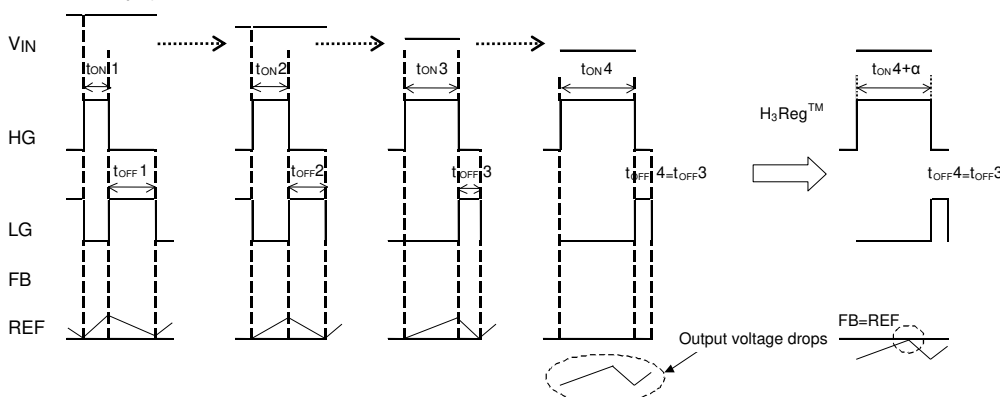
After the status of HG is off, LG go on outputting until output voltage become FB= REF.

(V<sub>OUT</sub> drops due to a rapid load change)



When V<sub>OUT</sub> drops due to a rapid load change, and the voltage remains below the output setting following the programmed t<sub>ON</sub> time, the system quickly restores V<sub>OUT</sub> by extending the t<sub>ON</sub> time, thus improving the transient response. Once V<sub>OUT</sub> is restored, the controller continues normal operation.

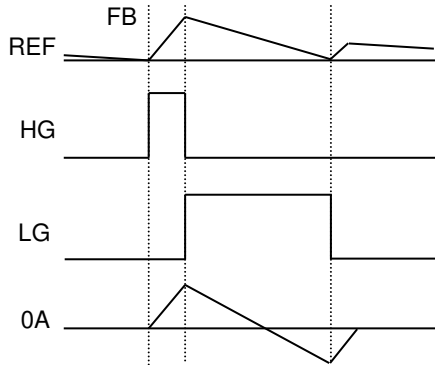
(When V<sub>IN</sub> drops)



Based on the value of V<sub>IN</sub>, the on-time t<sub>ON</sub> and off-time t<sub>OFF</sub> are determined by t<sub>ON</sub>= V<sub>OUT</sub> / V<sub>IN</sub> x 1/f and t<sub>OFF</sub>= (V<sub>IN</sub>- V<sub>OUT</sub>)/V<sub>IN</sub>. As the V<sub>IN</sub> voltage drops, in order to maintain the output voltage, t<sub>ON</sub> becomes longer and t<sub>OFF</sub> is shorter. However, for normal operation, if V<sub>IN</sub> drops further, t<sub>ON</sub> is longer and t<sub>OFF</sub>= t<sub>minoff</sub> (minimum off- time is defined internally), the output voltage will decrease because t<sub>OFF</sub> cannot be any shorter than the minimum off-time. With H<sup>3</sup>Reg™, if V<sub>IN</sub> goes even lower, the output voltage is maintained as the t<sub>ON</sub> time is extended. (t<sub>ON</sub> time is extended until FB>REF). In this case, the switching frequency is lowered so that the t<sub>ON</sub> time can be extended.

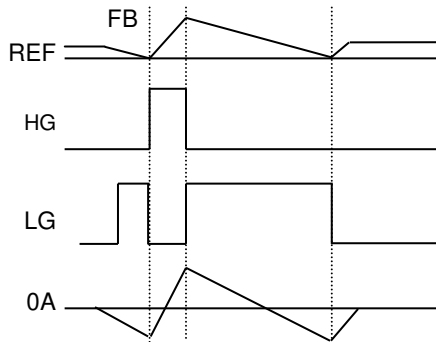
Description of Block - continued

Light Load Control (SLLM)



SLLM will activate when the LG pin is off and the coil current is near 0A (current flows from  $V_{OUT}$  to SW). When the FB input is lower than the REF voltage again, HG will be enabled once again.

(QLLM)

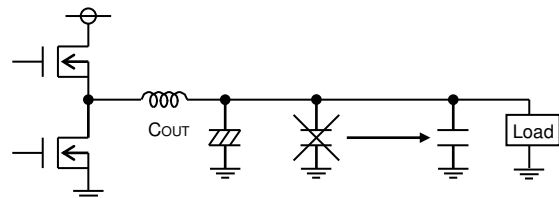


QLLM will activate when the LG pin is off and the coil current is near 0A (current flows from  $V_{OUT}$  to SW). In this case, the next HG is prevented. Then, when FB falls below the output programmed voltage within the programmed time (Typ= 40 $\mu$ s), HG will resume. In the case where FB doesn't fall in the programmed time, LG is forced on causing  $V_{OUT}$  to fall. As a result, the next HG is on.

MCTL1	MCTL2	Control Mode	Start-up
L	L	SLLM	PWM
L	H	QLLM	PWM
H	X	PWM	PWM

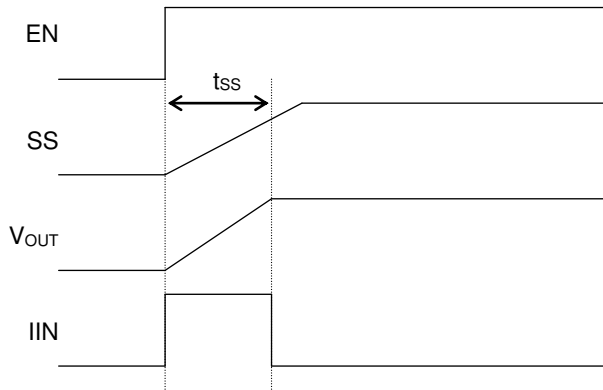
The BD9528AMUV operates in PWM mode until the SS input reaches the clamp voltage (2.5V), regardless of the control mode setting, this assures stable operation while the during soft start.

\*Attention: To effect the rapid transient response, the H<sup>3</sup>Reg™ control monitors the current from the output capacitor to the load using the ESR of the output capacitor. Do not use ceramic capacitors on  $C_{OUT}$  side of power supply. Ceramic bypass capacitors can be used near the individual loads if desired.



Timing Chart

- Soft Start Function



Soft start is exercised with the EN pin set high. Current control takes effect at startup, enabling a moderate output voltage “ramping start.” Soft start timing and incoming current are calculated with formulas (2) and (3) below.

- Soft start time

$$t_{ss} = \frac{0.7(\text{Typ}) \times C_{ss}}{2.3\mu\text{A}(\text{Typ})} < 100\text{m [sec]} \dots (2)$$

C <sub>SS</sub> (pF)	Soft start time(ms)
18000	5
33000	10
68000	20

- Inrush current

$$I_{in} = \frac{C_o \times V_{OUT}}{t_{ss}} \times \frac{V_{OUT}}{V_{IN}} \text{ [A]} \dots (3)$$

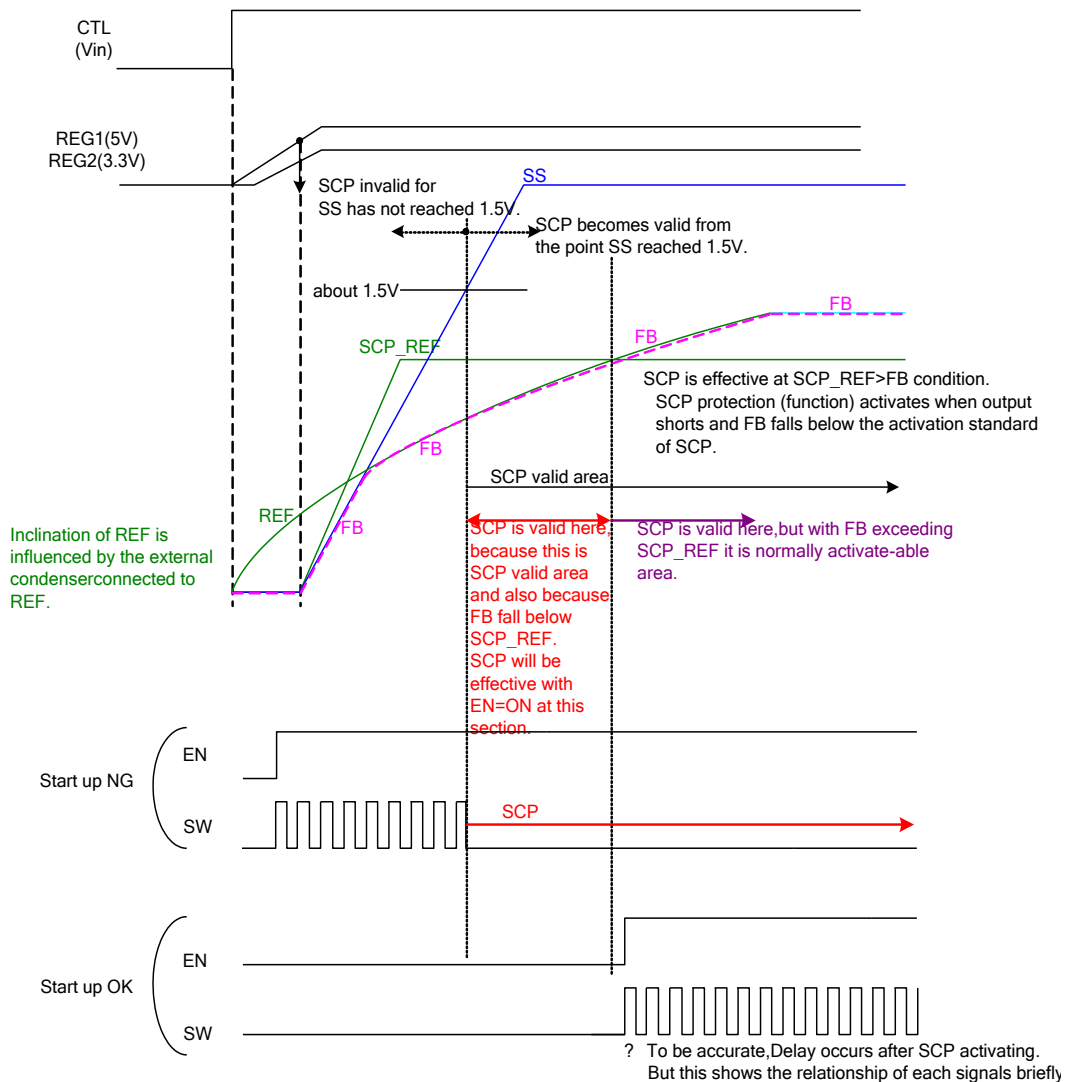
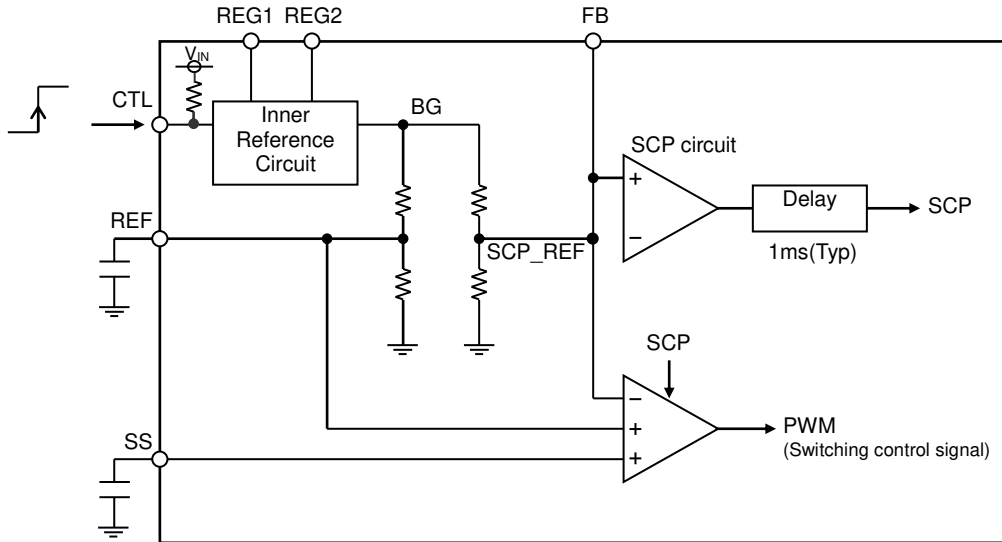
(C<sub>ss</sub>: Soft start capacitor C<sub>o</sub>: Output capacitor)

\*Notice : Max ontime function is disable by SS voltage reach to 2.5V.

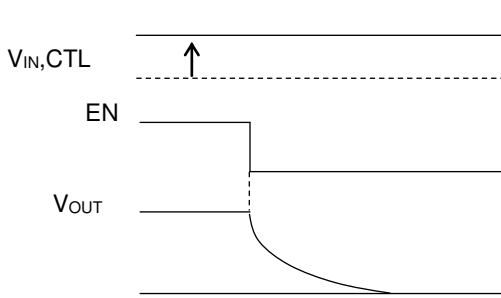


Timing Chart - continued

- Notes when waking up with CTL pin or  $V_{IN}$  pin  
 If EN pin is high or short (or pull up resistor) to REG1 pin, IC starts up by switching CTL pin, the IC might fail to start up (SCP function) with the reason below, please be careful of SS pin and REF pin capacitor capacity.

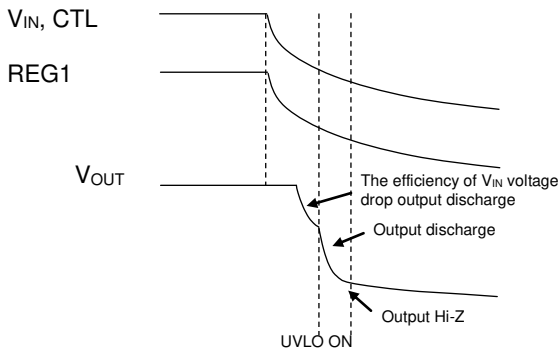


Output Discharge



It will be available to use if connecting  $V_{OUT}$  pin to DC/DC output. (about  $100\Omega$ ). Discharge function operates when <1> EN='L', <2> UVLO= ON (If input voltage is low) <3> SCP latch <4> TSD= ON. The function at output discharge time is shown as left.

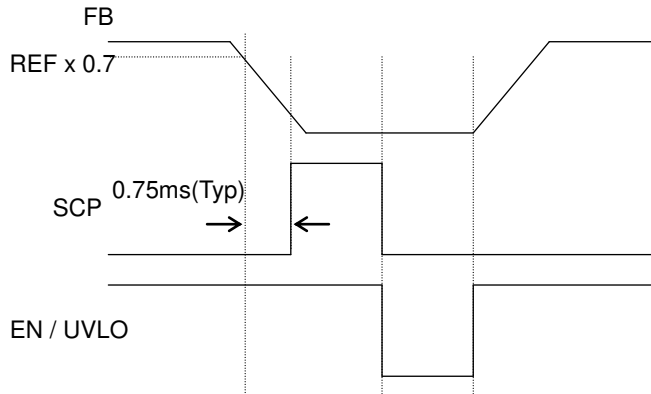
[1] When switch to low from high with EN pin.  
If EN pin voltage is below than EN threshold voltage, output discharge function is operated, and discharge output capacitor charge.



[2] When switch to low from high with EN pin

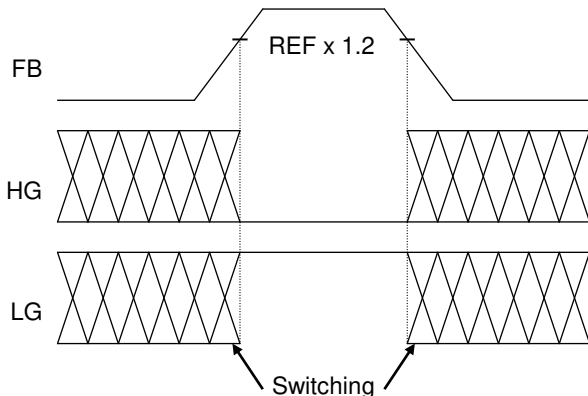
- 1) IC is in normal operation until REG1 voltage becomes lower than UVLO voltage. However, because  $V_{IN}$  voltage also becomes low, output voltage will drop, too.
- 2) If REG1 voltage reaches the UVLO voltage, output discharge function is operated, and discharge output capacitor charge.
- 3) In addition, if REG1 voltage drops, inner IC logic cannot operate, so that output discharge function does not work, and becomes output Hi-z. (In case, FB has resistor against ground, discharge at the resistor.)

• Timer Latch Type Output Short Circuit Protection



Short protection is enabled when the output voltage falls to or below  $REF \times 0.7$ . Once the programmed time period has elapsed, the output is latched off to prevent destruction of the circuit. (HG= Low, LG= Low) Output voltage can be restored either by cycling the EN pin or disabling UVLO.

• Over Voltage Protection



When the output voltage increases to or above  $REF \times 1.2$  (Typ), output over voltage protection is enabled, and the Low-side FET turns on to reduce the output. (LG= High, HG= Low). When the output falls to within normal operation, the function is restored to normal operation.