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Hi-performance Regulator IC Series for PCs

2ch Switching Regulators for Desktop PC

BD9540EFV

No.09030EBT07

●Description

BD9540EFV is a 2ch switching regulator synchronous controller that can generate low output voltages (0.75V to 5.5V). High efficiency for the switching regulator can be achieved due to its external N-MOSFET power transistor. The IC also incorporates a new technology called H^{3}Reg^{TM}, a Rohm proprietary control method which facilitates ultra-high transient response against changes in load. For protection and ease of use, the IC also incorporates soft start, and short circuit protection with timer latch functions. This switching regulator is designed for DRAM and power supplies for graphics chips.

●Features

1) 2ch H^{3}Reg^{TM} DC/DC converter synchronous controller
2) Thermal Shut Down (TSD), Under-Voltage Lock-Out (UVLO),
   Adjustable Over Current Protection (OCP) : detected Low side FET Ron, Over Voltage Protection (OVP),
   Short Circuit Protection (SCP) built-in
3) Soft start function to minimize rush current during startup
4) HTSSOP-B28 package
5) Built-in 5V power supply for FET driver
6) Integrated bootstrap diode

●Applications

LCD-TV, Game Consoles, Desktop PCs

●Maximum Absolute Ratings (Ta=25℃)

Parameter	Symbol	Limit	Unit
Input Voltage	VIN	24*1	V
BOOT Voltage	BOOT1,BOOT2	30*1	V
BOOT-SW Voltage	BOOT1-SW1, BOOT2-SW2	7*1	V
HG-SW Voltage	HG1-SW1, HG2-SW2	7*1	V
LG Voltage	LG1, LG2	5VReg	V
Output Voltage	VOUT1, VOUT2	7*1	V
Output Feedback Voltage	FB1, FB2	5VReg	V
5VReg Voltage	5VReg	7*1	V
Current Limit Setting Voltage	ILIM1, ILIM2	5VReg	V
Logic Input Voltage 1	EN1, EN2	24*1	V
Logic Input Voltage 2	CTL1, CTL2	7*1	V
Power dissipation 1	Pd1	1.45*2	W
Power dissipation 2	Pd2	1.85*3	W
Power dissipation 3	Pd3	3.30*4	W
Power dissipation 4	Pd4	4.70*5	W
Operating Temperature Range	Topr	-20～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd.
*2 Reduced by 11.6mW for each increase in Ta of 1℃ over 25℃
(when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB, 1layer, no copper foil area.)
*3 Reduced by 14.8mW for increase in Ta of 1℃ over 25℃.
(when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB, 2layers, copper foil area : 15mm×15mm.)
*4 Reduced by 26.4mW for increase in Ta of 1℃ over 25℃.
(when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB, 2layers, copper foil area : 70mm×70mm.)
*5 Reduced by 37.6mW for increase in Ta of 1℃ over 25℃.
(when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB, 4layers, copper foil area : 70mm×70mm.)

●Operating Conditions (Ta=25℃)

Parameter	Symbol	Min.	Max.	Unit
Input voltage	VIN	7.5	20	V
BOOT voltage	BOOT1, BOOT2	4.5	25	V
SW Voltage	SW1, SW2	-0.7	20	V
BOOT-SW voltage	BOOT1-SW1, BOOT2-SW2	4.5	5.5	V
Logic Input Voltage 1	EN1, EN2	0	20	V
Logic Input Voltage 2	CTL1, CTL2	0	5.5	V
Output Voltage	VOUT1, VOUT2	0.7	5.5	V
MIN ON Time	tonmin	-	100	ns

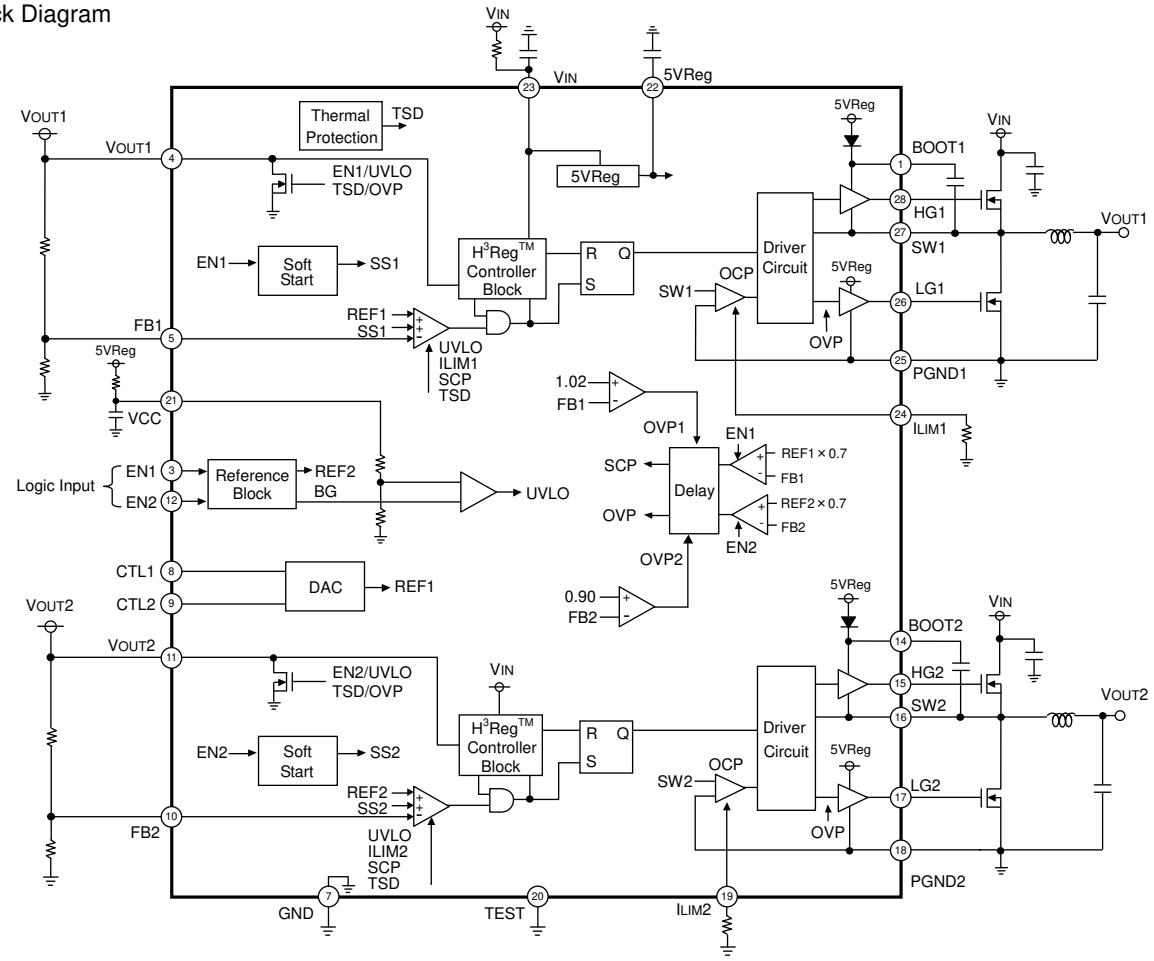
*This product should not be used in a radioactive environment.
*The range of the VOUT is limited by the voltage between VIN and VOUT.

●Electrical characteristics

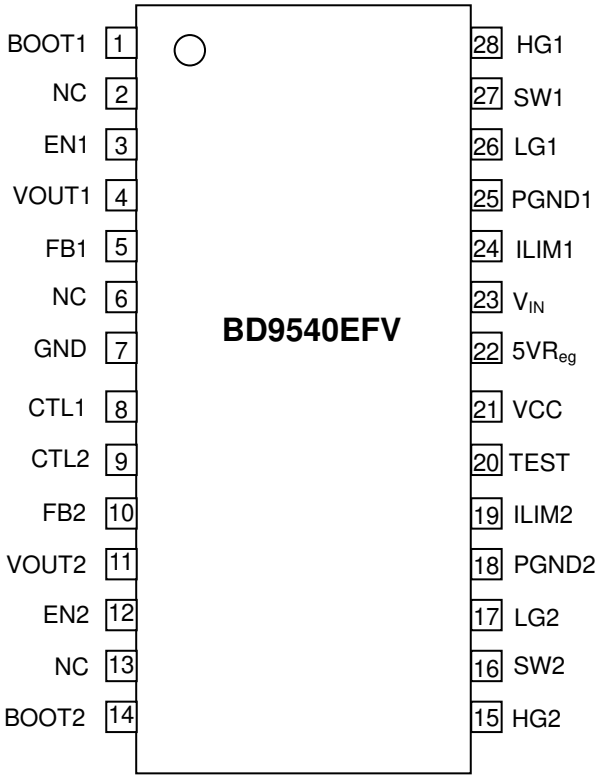
(Unless otherwise noted, Ta=25℃ VCC=5V, VIN=12V, VEN1=VEN2=3V, Vout1=1.5V, Vout2=1.05V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[General]						
VIN Bias Current	IIN	-	1.6	2.5	mA	
VIN Standby Current	IIN_stb	-	0	10	μA	VEN1=VEN2=0V
EN Low Voltage 1,2	VEN_low1,2	GND	-	0.3	V	
EN High Voltage 1,2	VEN_high1,2	2.2	-	20	V	
EN Bias Current 1,2	IEN1,2	-	1.5	5.0	μA	VEN1=VEN2=3V
[5V Linear Regulator]						
5VReg Standby Voltage	5Vreg_stb	-	-	0.1	V	VEN1=VEN2=0V
5VReg Output Voltage	5VReg	4.8	5.0	5.2	V	VIN=7.5V to 20V Ireg=0mA to 10mA
Maximum Current	IReg	50	-	-	mA	
[Under-Voltage Lock-Out]						
5VReg Threshold Voltage	5Vreg_UVLO	3.75	4.20	4.65	V	5VReg:Sweep up
5VReg Hysteresis Voltage	d5Vreg_UVLO	100	160	220	mV	5VReg:Sweep down
[OVP Block]						
FB Threshold Voltage 1	FB_OVP1	0.92	1.02	1.12	V	
FB Threshold Voltage 2	FB_OVP2	0.80	0.90	1.00	V	
OVP delay time	tOVP	-	1.7	-	μs	
[H^3Reg^{TM} Control Block]						
ON Time1	ton1	290	390	490	ns	
MIN OFF Time 1	toffmin1	200	380	-	ns	
ON Time 2	ton2	110	210	310	ns	
MIN OFF Time 2	toffmin2	200	380	-	ns	
[FET Block]						
HG High side ON Resistance 1,2	RHGhon1,2	-	5.5	11	Ω	
HG Low side ON Resistance 1,2	RHGlon1,2	-	2.5	5	Ω	
LG High side ON Resistance 1,2	RLGhon1,2	-	4	8	Ω	
LG Low side ON Resistance 1,2	RLGlon1,2	-	2	4	Ω	
[Over Current Protection Block]						
Current Limit Threshold Voltage 1,2	Vilim1,2	80	100	120	mV	RILIM=100kΩ
[Output Voltage Detection Block]						
FB1 threshold(REF1) Voltage1	FB1-1	0.769	0.781	0.793	V	CTL1=0V, CTL2=0V
FB1 threshold(REF1) Voltage2	FB1-2	0.802	0.814	0.826	V	CTL1=5V, CTL2=0V
FB1 threshold(REF1) Voltage3	FB1-3	0.839	0.851	0.863	V	CTL1=0V, CTL2=5V
FB1 threshold(REF1) Voltage4	FB1-4	0.738	0.750	0.762	V	CTL1=5V, CTL2=5V
FB2 threshold(REF2) Voltage	FB2	0.738	0.750	0.762	V	
CTL Low Voltage 1,2	VCTL_low1,2	GND	-	0.5	V	
CTL High Voltage 1,2	VCTL_high1,2	VCC-0.5	-	VCC	V	
FB1/2 Input Current	IFB1,2	-1	-	1	μA	
VOUT Discharge Current	IVOUT1,2	5	10	-	mA	VOUT=1V, EN=0V
[SCP Block]						
Threshold Voltage 1,2	Vthscp1,2	REF1,2×0.60	REF1,2×0.70	REF1,2×0.80	V	
SCP delay time	tSVP	-	28	-	μs	

●Block Diagram



●Pin Configuration



●Pin Function

PIN No.	PIN name	PIN Function
1	BOOT1	HG Driver Power Supply Pin 1
2	NC	Non connection Pin
3	EN1	Enable Input Pin 1 (0～0.3V:OFF, 2.2～20V:ON)
4	VOUT1	Output Voltage Sence Pin 1
5	FB1	Output Voltage Feedback Pin 1
6	NC	Non connection Pin
7	GND	Sense GND
8	CTL1	1ch Reference Voltage Setting Control Pin 1:See P12/17
9	CTL2	1ch Reference Voltage Setting Control Pin 2:See P12/17
10	FB2	Output Voltage Feedback Pin 2
11	VOUT2	Output Voltage Sense Pin 2
12	EN2	Enable Input Pin 2 (0～0.3V:OFF, 2.2～20V:ON)
13	NC	Non connection Pin
14	BOOT2	HG Driver Power Supply Pin 2
15	HG2	High side FET Gate Driver Pin 2
16	SW2	High side FET Source Pin 2
17	LG2	Low side FET Gate Driver Pin 2
18	PGND2	Power GND for 2ch
19	ILIM2	2ch OCP Setting Pin
20	TEST	Connect to GND Pin
21	VCC	Power Supply Input Pin
22	5VReg	Reference Voltage Inside IC (5V Voltage Output)
23	VIN	Battery Voltage Sense Pin
24	ILIM1	1ch OCP Setting Pin
25	PGND1	Power GND for 1ch
26	LG1	Low side FET Gate Driver Pin 1
27	SW1	High side FET Source Pin 1
28	HG1	High side FET Gate Driver Pin 1
reverse	FIN	Exposed Pad, Connect to GND

●Reference Data

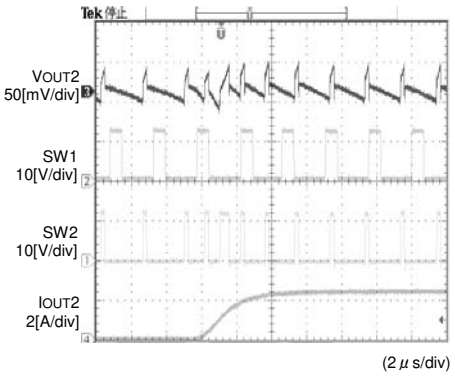


Fig.1 Transient Respnse
(VIN=12V VOUT2=1.05V)

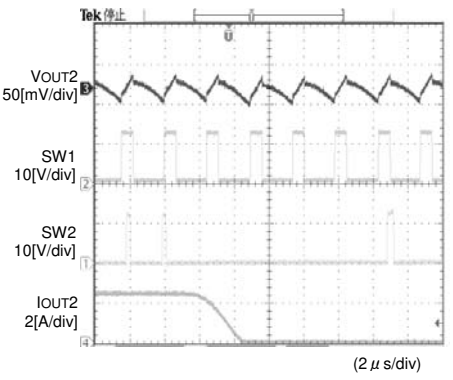


Fig.2 Transient Respnse
(VIN=12V VOUT2=1.05V)

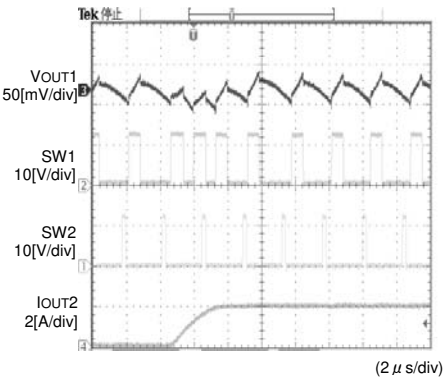


Fig.3 Transient Respnse
(VIN=12V VOUT1=3.3V)

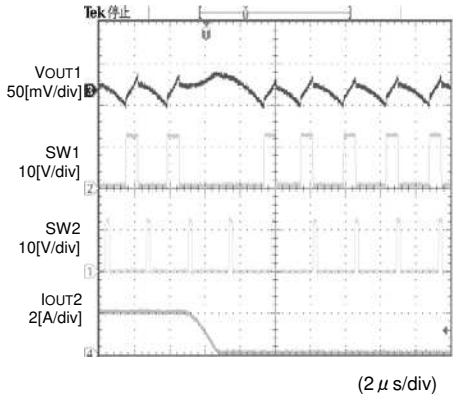


Fig.4 Transient Respnse
(VIN=12V VOUT1=3.3V)

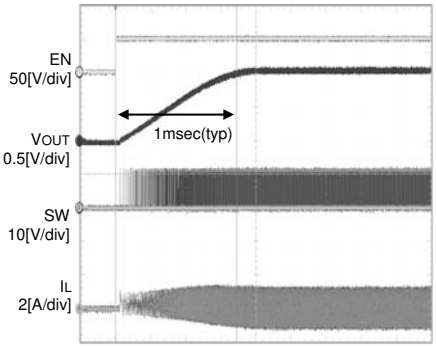


Fig.5 VOUT wake up
(Io=0A)

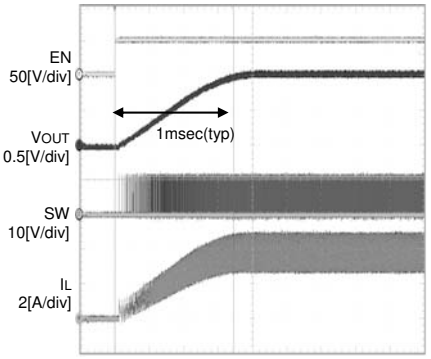


Fig.6 VOUT wake up
(Io=4A)

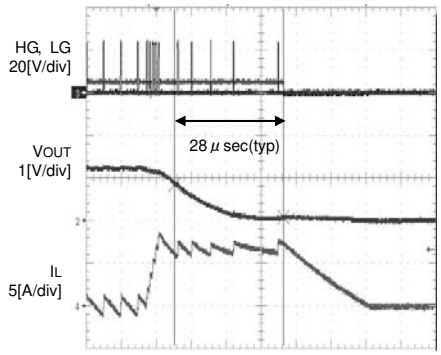


Fig.7 OCP and SCP

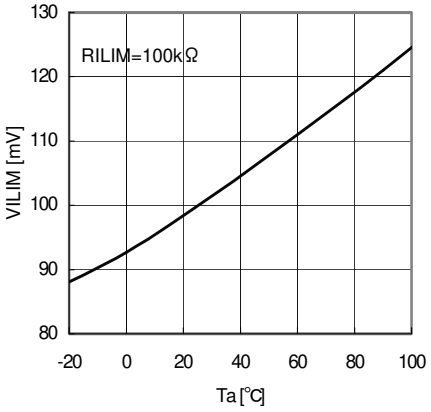


Fig.8 Ta-VILIM

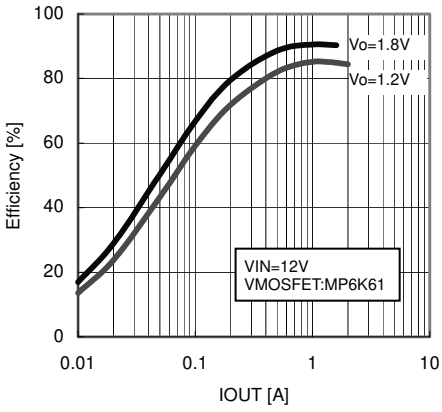


Fig.9 IOUT-Efficiency

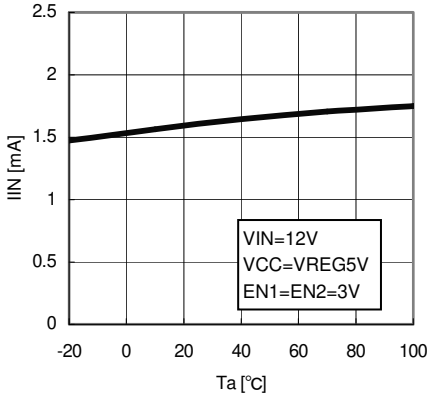


Fig.10 Ta-IIN

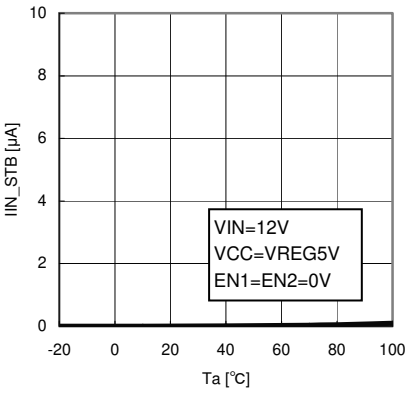


Fig.11 Ta-IIN_STB

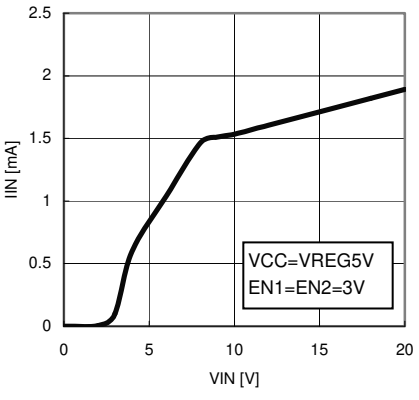


Fig.12 VIN-IIN

●Reference Data

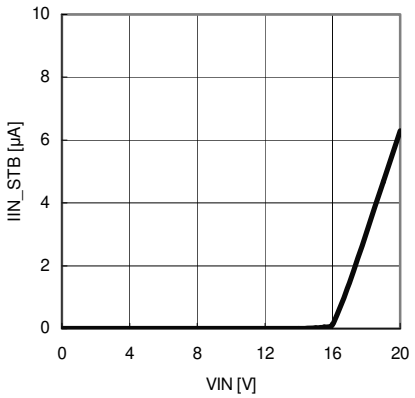


Fig.13 VIN-IIN_STB

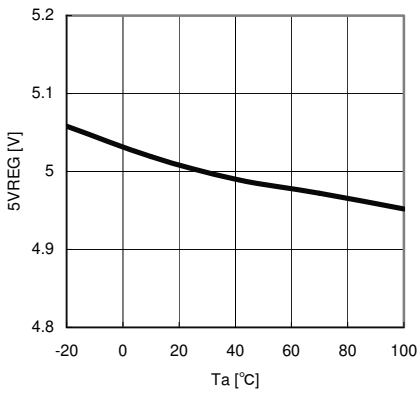


Fig.14 Ta-5VREG

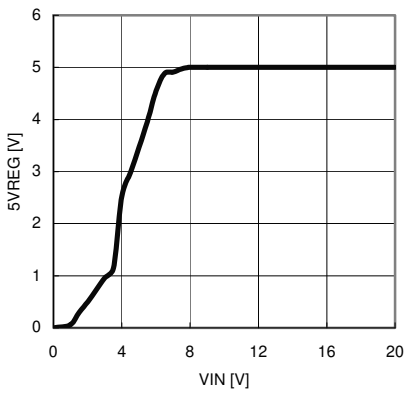


Fig.15 VIN-5VREG

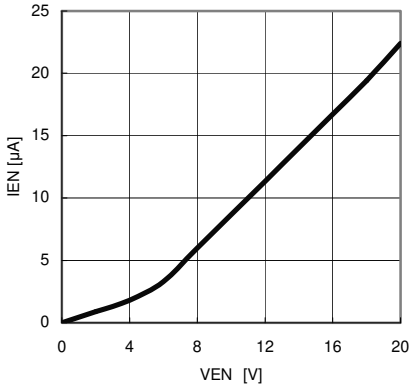


Fig.16 VEN-IEN

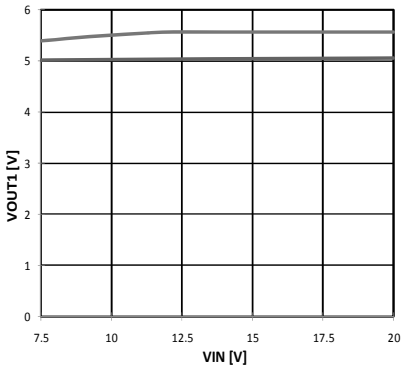


Fig.17 VIN-VOUT1

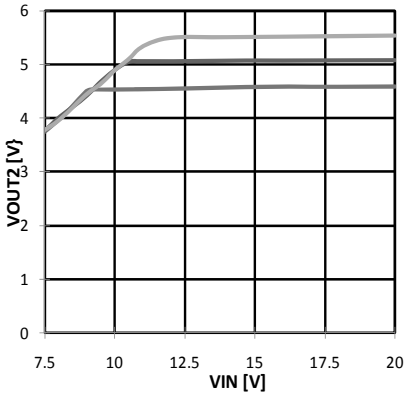


Fig.18 VIN-VOUT2

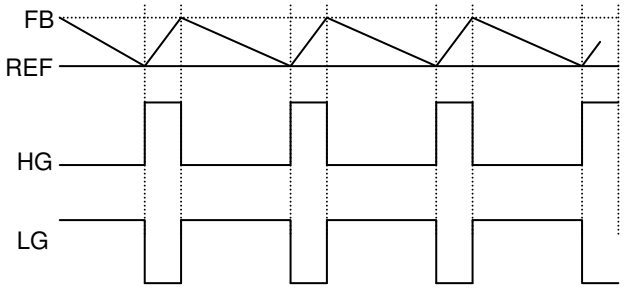
●Pin Descriptions

- EN1 (3 pin) / EN2 (12 pin)
  When the input voltage on the EN pin reaches at least 2.2V, the switching regulator becomes active.
  At voltages less than 0.3 V, the switching regulator becomes inactive, and the input current drops to 10μA or less.
  Thus the IC can be controlled from 2.5V, 3.3V or 5V power supplies.
- 5VReg (22 pin)
  5.0V reference voltage output pin. If at least 2.2V is supplied to either the EN1 or EN2 pin, the reference output is switched on. This pin supplies 5.0V at up to 10mA. Inserting a 4.7μF capacitor (with a X5R or X7R rating) between the 5VReg and GND pins is recommended.
- ILIM1 (24 pin) / ILIM2 (19 pin)
  The IC monitors the voltage between the SW pin and PGND pin as a control for the output current protection (OCP) mechanism. The voltage at which OCP engages is determined by the resistance value connected to the ILIM pin.
  This also allows for compatibility with FETs of various RON values.
- VIN (23 pin)
  The IC determines the duty cycles internally based upon the input voltage on this pin. Therefore, variations in voltage on this pin can lead to highly unstable operation. This pin also acts as the voltage input to the internal switching regulator block, and is sensitive to the impedance of the power supply. Attaching a bypass capacitor or RC filter on this pin as appropriate for the application is recommended.
- BOOT1 (1 pin) / BOOT2 (14 pin)
  This pin supplies voltage used for driving the high-side FET. Maximum absolute ratings are 25V from GND and 5.5V from SW. BOOT voltage swings between VIN + 5VReg and 5VReg during active operation.
- HG1 (28 pin) / HG2 (15 pin)
  This pin supplies voltage used for driving the gate of the high-side FET. This voltage swings between BOOT and SW. High-speed gate driving for the high side FET can be achieved due to its low on-resistance (5.5Ω when HG = high, 2.5Ω when HG = low) of the driver.
- SW1 (27 pin) / SW2 (16 pin)
  This pin acts as the source connection to the high-side FET. Maximum absolute rating is 20V from GND.
  SW voltage swings between VIN and GND.
- LG1 (26 pin) / LG2 (17 pin)
  This pin supplies voltage used for driving the gate of the low-side FET. This voltage swings between VDD and PGND. High-speed gate driving for the low-side FET can be achieved due to its low on-resistance (4Ω when LG = high, 2Ω when LG = low) of the driver.
- PGND1 (25 pin) / PGND2 (18 pin)
  This pin acts as the ground connection to the source of the low-side FET.
- GND (7 pin)
  This is the ground pin for all internal analog and digital power supplies.
- VOUT1 (4 pin) / VOUT2 (11 pin)
  This is the output voltage sense pin; this pin features an integrated discharge FET used to discharge the output capacitor when status is set to OFF.
- FB1 (5 pin) / FB2 (10 pin)
  This is the output feedback pin. While the internal reference voltage of channel 2 is fixed at 0.750V, the internal reference voltage of channel 1 is adjustable depending on the input conditions of the CTL1 and CTL2 pins.
- Vcc (21 pin)
  This is the power supply pin for all internal circuitry. This pin can be supplied directly by a 5V source, or via an RC filter (10 Ω, 0.01μF) from the 5VReg pin.
- CTL1 (8 pin) / CTL2 (9 pin)
  These pins allow for the adjustment of the internal voltage reference (REF1) for channel 1. The pins recognize logic High at VCC-0.5 V or above, and logic Low at 0.5 V or below. Refer to the voltage adjustment table for REF1 on page 12.

●Explanation of Operation

The BD9540EFV is a 2ch switching regulator controller incorporating ROHM's proprietary H^3Reg^{TM} CONTROLLA control system. When VOUT drops due to a rapid load change, the system quickly restores VOUT by extending the TON time interval.

H^3Reg^{TM} control
(Normal operation)

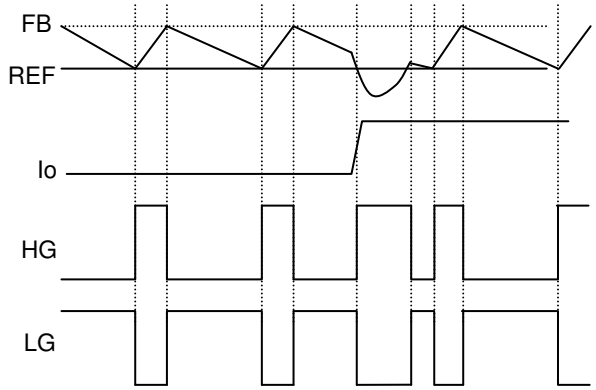


When FB falls below the threshold voltage (REF), a drop is detected, activating the H^3Reg^{TM} CONTROLLA system.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \text{ [sec]} \cdot \cdot \cdot (1)$$

HG output is determined by the formula above. (See P13)
LG output operates until FB voltage falls below REF voltage after HG becomes OFF.

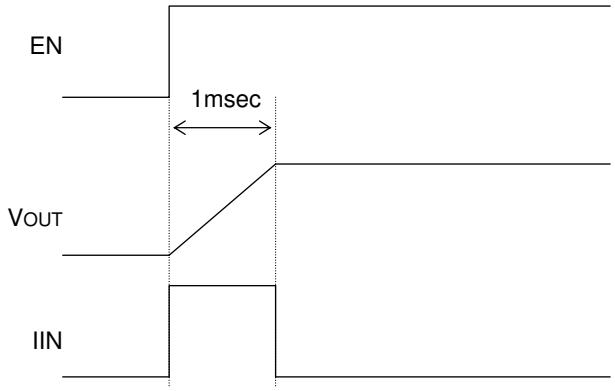
(VOUT drops due to a rapid load change)



When FB (V_{OUT}) drops due to a rapid load change, and the voltage remains below REF after the programmed t_{ON} time interval has elapsed, the system quickly restores V_{OUT} by extending the t_{ON} time, improving transient response.

●Timing Chart

・Soft Start Function



Soft start is utilized when the EN pin is set high. Current control takes effect at startup, enabling a moderate "ramping start" on the output voltage. Soft start time is 1msec. And input current is determined via formula (2) below.

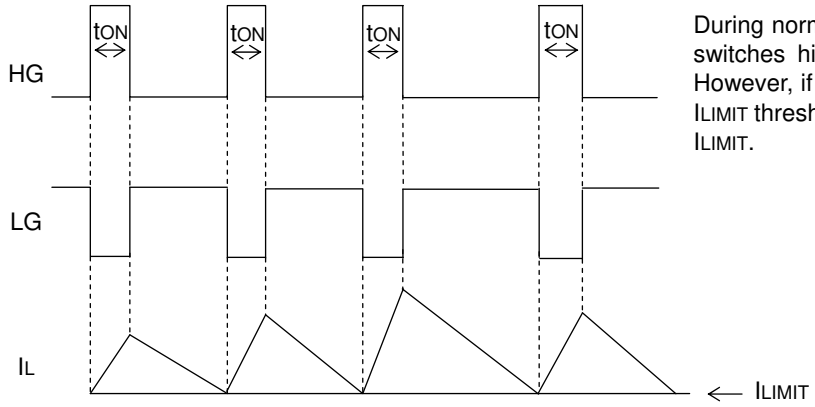
Rush current:

$$I_{IN} = \frac{Co \times V_{OUT}}{1ms} \text{ [A]} \cdot \cdot \cdot (2)$$

(Co: All capacitors connected with V_{OUT})

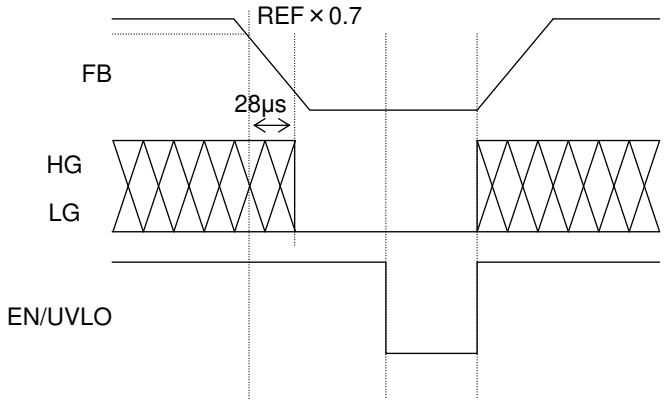
●Timing Chart

・Over current protection circuit



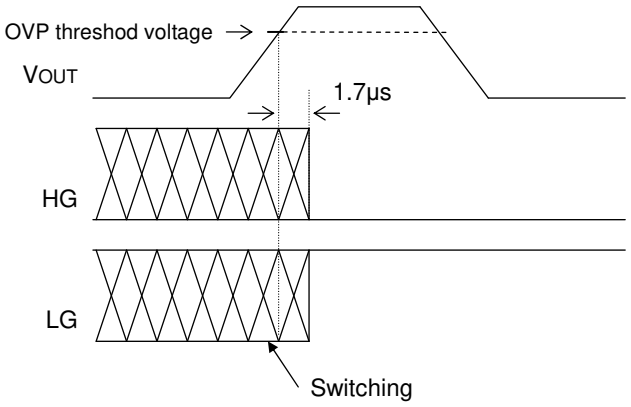
During normal operation, when FB falls below REF, HG switches high during for the period of time tON (P8). However, if the current of the low-side FET exceeds the ILIMIT threshold, HG will switch off until it becomes below ILIMIT.

・Timer Latch Type Short Circuit Protection



Short protection engages when output falls to or below REF × 0.7. When the programmed time period (28µs) elapses, output is latched off to prevent damage to the IC. Output voltage can be restored either by reconnecting the EN pin or disabling UVLO.

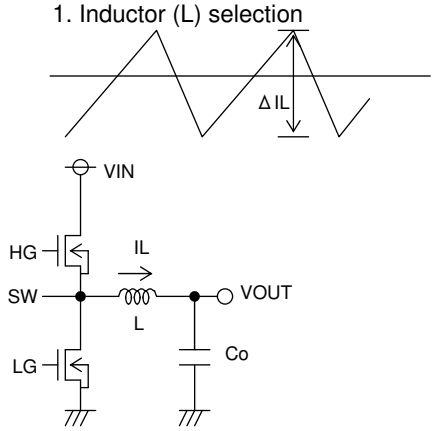
・Output Over Voltage Protection



When output voltage rises to or above the OVP threshold voltage (1ch:1.02V, 2ch:0.9V), output over-voltage protection engages after the set time (1.7µs) has elapsed. During this protection period, the low-side FET opens completely for maximum reduction of output voltage (LG = high, HG = low). Output voltage can be restored either by reconnecting the EN pin or disabling UVLO.

●External Component Selection

1. Inductor (L) selection



Output Ripple Current

The inductance value has a major influence on output ripple current. As formula (3) below indicates, the greater the inductance or switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \quad [A] \cdots (3)$$

The proper output ripple current setting is about 30% of maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT}max. \quad [A] \cdots (4)$$

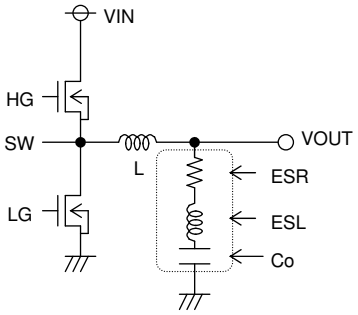
$$L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f} \quad [H] \cdots (5)$$

(ΔI_L: output ripple current; f: switch frequency)

※Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. When selecting an inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor's rated current value.

※To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.

2. Output Capacitor (CO) Selection



Output Capacitor

When determining a proper output capacitor, be sure to factor in the equivalent series resistance and equivalent series inductance required to set the output ripple voltage to 20mV or more. Also, make sure the capacitor's voltage rating is high enough for the set output voltage (including ripple).
Output ripple voltage is determined as in formula (6) below.

$$\Delta V_{OUT} = \Delta I_L \times ESR + ESL \times \Delta I_L / T_{ON} \cdots (6)$$

(ΔI_L: Output ripple current; ESR: C_O equivalent series resistance, ESL: equivalent series inductance)

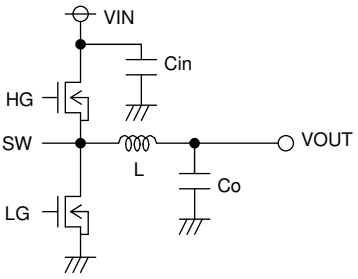
Also, give due consideration to the conditions in formula (7) below for output capacitance, bearing in mind that output rise time must be established within the soft start time frame:

$$Co \leqq \frac{1ms \times (Limit - I_{OUT})}{V_{OUT}} \cdots (7)$$

Tss: Soft start time
Limit: Over current detection
I_{OUT} : Output current

Note: an improper output capacitor may cause startup malfunctions.

3. Input Capacitor (Cin) Selection



Input Capacitor

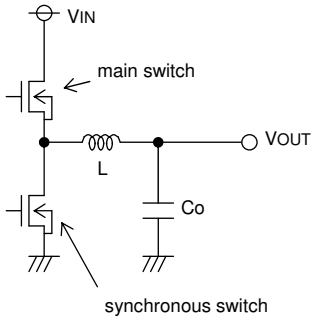
In order to prevent transient spikes in voltage, the input capacitor selected must have a low enough ESR resistance to fully support a large ripple current on the output. The formula for ripple current IRMS is given in equation (8) below:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN}-V_{OUT})}}{V_{IN}} \quad [A] \cdots (8)$$

Where $V_{IN} = 2 \times V_{OUT}$, $I_{RMS} = \frac{I_{OUT}}{2}$

A low-ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

4. MOSFET Selection



Main MOSFET power dissipation is computed as follows:

$$Pmain = P_{RON} + P_{GATE} + P_{TRAN}$$

$$= \frac{V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + Qg(High) \times f \times 5VReg + \frac{V_{IN}^2 \times Crss \times I_{OUT} \times f}{I_{DRIVE}} \quad \cdots (9)$$

(Ron: On-resistance of FET; Qg: FET gate capacitance;
f: Switching frequency; Crss: FET inverse transfer function;
I_{DRIVE}: Gate peak current)

Synchronous MOSFET power dissipation is computed as follows:

$$Psyn = P_{RON} + P_{GATE}$$

$$= \frac{V_{IN}-V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + 5VReg \times f \times V_{DD} \quad \cdots (10)$$

Qg loss is also incurred as internal power dissipation in the IC:

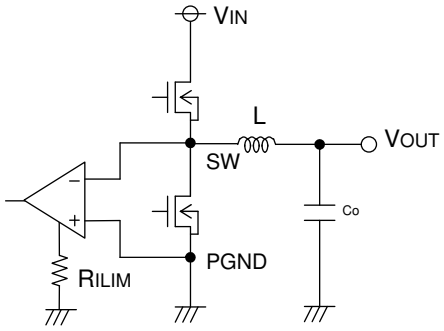
$$= P_{IC(DRIVE)} = \left\{Qg(High) \times f + Qg(Low) \times f\right\} \times (VIN-5VReg) \quad \cdots (11)$$

For example:
If Qg(High) = 20nq, Qg(Low) = 50nq, f = 300kHz,

$$P_{IC(DRIVE)} = \left\{ 20n \times 300k + 50n \times 300k \right\} \times (12\text{-}5)$$

$$= 0.147W$$

5. Determining Detection Resistance



The over-current protection function is controlled via the voltage detected between the SW and PGND pins – i.e., the ON-resistance of the synchronous FET. The current limit value is determined by formula (12) below:

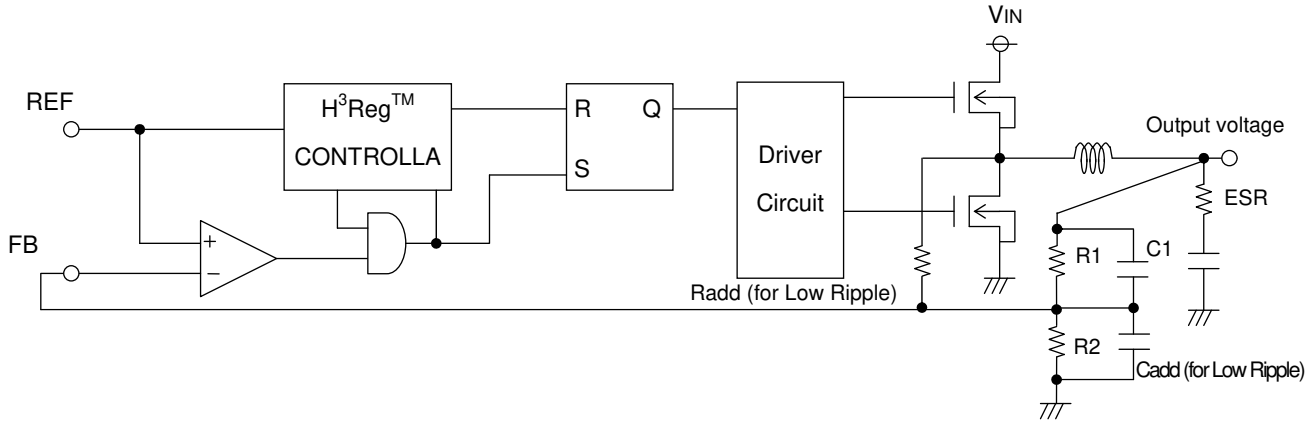
$$I_{LIM} = \frac{10k}{R_{ILIM} \times R_{ON}} \text{ [A]} \quad \cdots (12)$$

(R_{ILIM}: Resistance for setting over-current protection limit,
R_{ON}: Low side FET On-resistance)

6. Output Voltage Setting

The IC will try to maintain output voltage such that REF≒VFB.
However, the actual output voltage will also reflect the average ripple voltage value.
The output voltage is set via a resistive voltage divider between the output and the FB pin. The formula for output voltage is given in (13) below:

$$\text{Output voltage} = \frac{R1+R2}{R2} \times \text{REF} + \frac{1}{2} \times \Delta I_L \times \text{ESR} \cdots (13)$$



It is recommended that R1 and C1 be connected in parallel to the FB pin.
In low output ripple applications (ΔV < 20 mV), add Radd and Cadd as shown in the above application circuit.
For value settings, refer to the tool provided separately.

REF voltage (for 2ch) is fixed at 0.750 V; however, REF voltage (for 1ch) can be adjusted via the CTL input conditions.
REF1 voltage setting table

CTL1	CTL2	REF1
L	L	0.781V
H	L	0.814V
L	H	0.851V
H	H	0.750V

7. Relationship between output voltage and Ton duration

Both 1ch and 2ch of BD9540EFV are synchronous rectification type of switching controllers operated at fixed-frequency. The Ton duration for each channel depends on the output voltage settings, as described by the following formulas.

$$Ton1 = \frac{VOUT1}{VIN} \times 2\mu + 130n\ [ns] \cdots (14) \qquad (1ch)$$

$$Ton2 = \frac{VOUT2}{VIN} \times 0.9\mu + 130n\ [ns] \cdots (15) \qquad (2ch)$$

Thus from the above Ton duration, the frequency of the applied condition is

$$Frequency = \frac{VOUT}{VIN} \times \frac{1}{Ton}\ [kHz] \cdots (16)$$

However with actual applications, there exists a rising and falling time of the SW due to the gate capacitance of the external MOSFET and the switching speed, which may vary the above parameters. Thus please also verify those parameters experimentally.

8. Relationship between output current and frequency

BD9540EFV is a fixed-Ton type of switching controller. When the output current increases, the switching loss of the coil and MOSFET also increases and hence the switching frequency speeds up.
The loss of the coil and MOSFET is determined as

① Loss of coil = $IOUT^2 \times DCR$

② Loss of high-side MOSFET = $IOUT^2 \times Ronh \times \frac{VOUT}{VIN}$

③ Loss of low-side MOSFET = $IOUT^2 \times Ronn \times (1 - \frac{VOUT}{VIN})$

(Ronh : on-resistance of high-side MOSFET, Ronn : on resistance of low-side MOSFET)

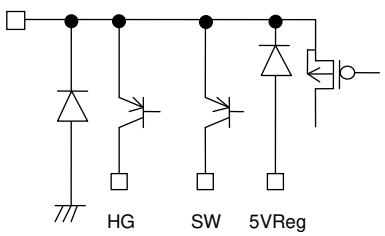
Taking the above losses into the frequency equation, then T (=1/Freq) becomes

$$T\ (=1/Freq) = \frac{VIN \times IOUT \times Ton}{VOUT \times IOUT + ① + ② + ③} \cdots (17)$$

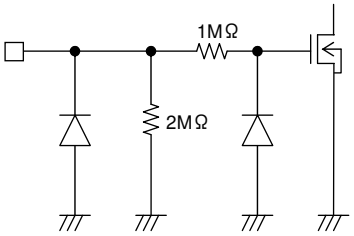
However since the parasitic resistance of the layout pattern exists in actual applications and affects the parameter, please also verify experimentally.

●I/O Equivalent Circuits

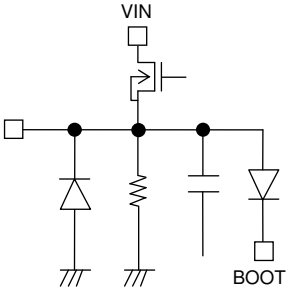
1pin, 14pin (BOOT1, BOOT2)



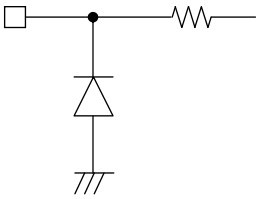
3pin, 12pin (EN1, EN2)



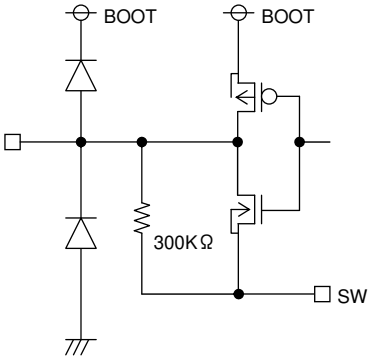
22pin (5VReg)



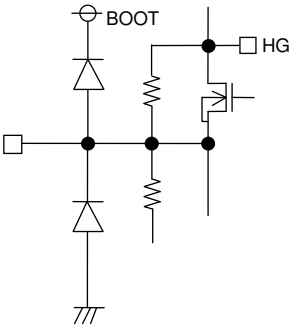
8pin 9pin (CTL1, CTL2)



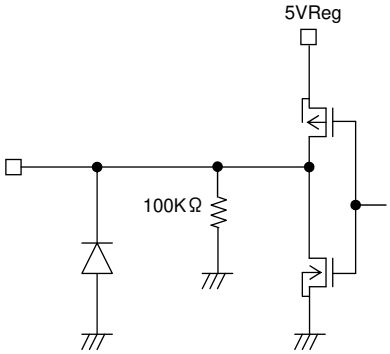
28pin, 15pin (HG1, HG2)



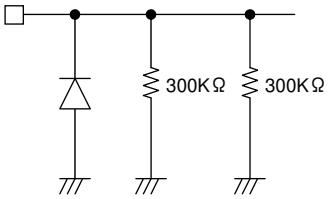
27pin, 16pin (SW1, SW2)



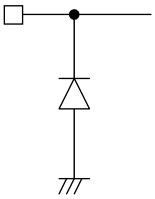
26pin, 17pin (LG1, LG2)



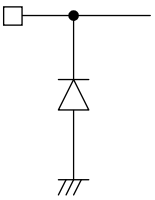
20pin (TEST)



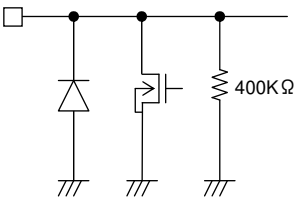
24pin, 19pin (ILIM1, ILIM2)
5pin, 10pin (FB1, FB2)



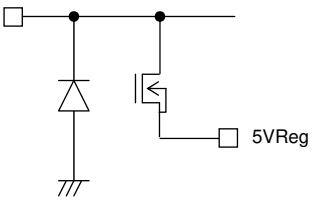
21pin (VCC)



4pin, 11pin (VOUT1, VOUT2)



23pin (VIN)



●Operation Notes

(1) Absolute Maximum Ratings

Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

(2) Power Supply Polarity

Connecting the power supply in reverse polarity can cause damage to the IC. Take precautions when connecting the power supply lines. An external power diode can be added.

(3) Power Supply Lines

In order to minimize noise, PCB layout should be designed such that separate, low-impedance power lines are routed to the digital and analog blocks. Additionally, a coupling capacitor should be inserted between all power input pins and the ground terminal. If electrolytic capacitors are used, keep in mind that their capacitance characteristics are reduced at low temperatures.

(4) GND voltage

The potential of the GND pin must be the minimum potential in the system in all operating conditions.

(5) Thermal design

Use a thermal design that allows for a sufficient margin for power dissipation (Pd) under actual operating conditions.

(6) Inter-pin Shorts and Mounting Errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by poor soldering or foreign objects may result in damage to the IC.

(7) Operation in Strong Electromagnetic Fields

Using this product in strong electromagnetic fields may cause IC malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.

(8) ASO - Area of Safe Operation

When using the IC, ensure that operating conditions do not exceed absolute maximum ratings or ASO of the output transistors.

(9) Thermal shutdown (TSD) circuit

The IC incorporates a built-in thermal shutdown circuit, which is designed to turn the IC off completely in the event of thermal overload. It is not designed to protect the IC from damage or guarantee its operation. ICs should not be used after this function has activated, or in applications where the operation of this circuit is assumed.

	TSD ON Temp. [°C] (typ.)	Hysteresis Temp. [°C] (typ.)
BD9540EFV	175	15

(10)Testing on application boards

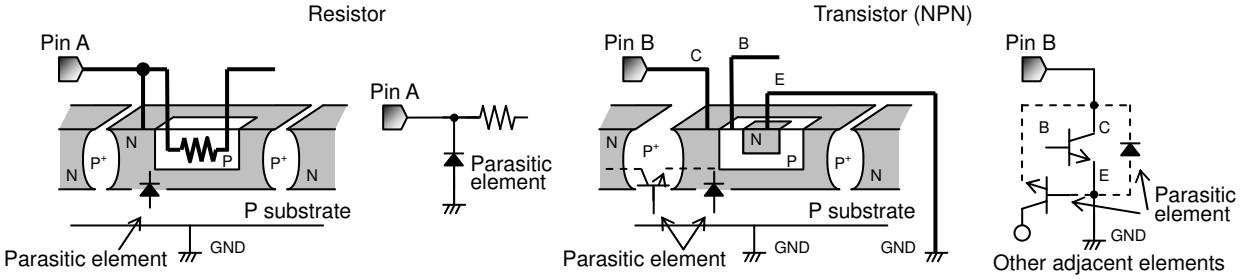
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(11) Regarding input pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):

- When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

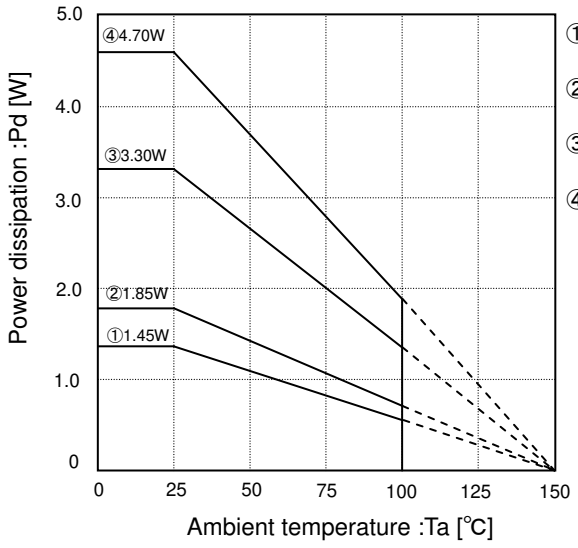


Example of IC structure

(12)Ground Wiring Pattern

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.

●Power Dissipation



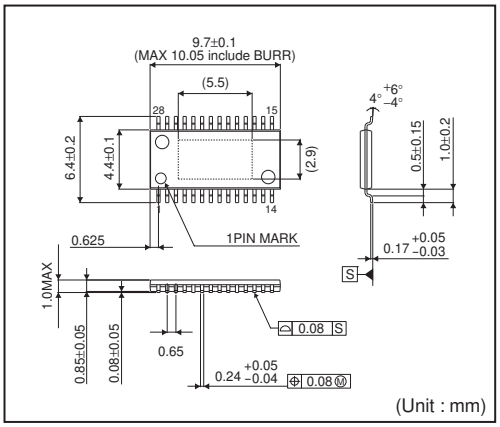
①Mounted on board 70mm × 70mm × 1.6mm glass-epoxy PCB, 1 layer
No copper foil area. θj-a=86.2℃/W
②Mounted on board 70mm × 70mm × 1.6mm glass-epoxy PCB, 2 layers,
Copper foil area : 15mm × 15mm, θj-a=67.6℃/W
③Mounted on board 70mm × 70mm × 1.6mm glass-epoxy PCB, 2 layers,
Copper foil area :: 70mm × 70mm, θj-a=37.9℃/W
④Mounted on board 70mm × 70mm × 1.6mm glass-epoxy PCB, 4 layers,
Copper foil area :: 70mm × 70mm, θj-a=26.6℃/W

●Ordering part number

B	D	9	5	4	0	E	F	V	-	E	2

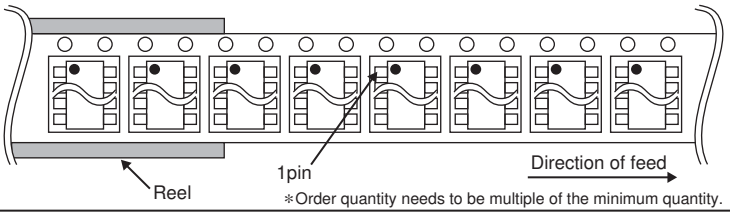
Part No. (BD) — Part No. (9540) — Package: EFV : HTSSOP-B28 — Packaging and forming specification: E2: Embossed tape and reel

HTSSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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