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High Performance Switching Regulator Series

60V Synchronous Step-down Switching Regulator(Controller type)

BD9610AMUV

●General Description

The BD9610AMUV is a family of high resistance and wide-input voltage (10V to 56V), synchronous, step-down switching regulator. BD9610AMUV offers design flexibility with a variety of user-programmable functions, including soft-start, operating frequency, high-side current limit, and loop compensation. BD9610AMUV uses the pulse-width modulation method of the voltage mode, and drives 2 external Nch-FETs. The externally programmable current limit provides pulse-by-pulse current limit, as well as hiccup mode operation utilizing an internal fault counter for longer duration overloads.BD9610AMUV is safe for pre-biased outputs, not turning on the synchronous rectifier until the high-side FET has already started switching

●Features

- High Resistance and Wide Range Input Voltage :VCC=10V~56V
- Internal Outside FET Gate Driver:REG10=10V
- 0.8V±1.0% Reference Voltage Accuracy
- Safe for Pre-biased Outputs
- Adjustable Oscillating Frequency and Soft-Start
- Master/Slave Synchronize Function
- Over Current Protection (OCP)
- Under Voltage Locked Output(UVLO)
- Thermal Shut-down(TSD)

●Key Specifications

Input Supply Voltage	10~56 [V]
Output Voltage	1.0~(Vin×0.8) [V]
Reference Voltage Accuracy	±1.0 [%]
Gate Drive Voltage(REG10)	9~11 [V]
Frequency	50~500 [kHz]

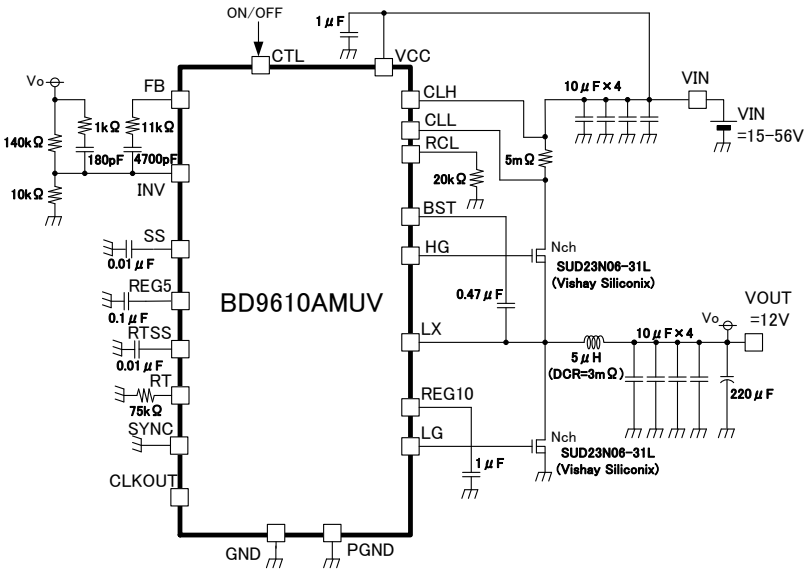
●Package

VQFN020V4040 4.00㎜×4.00㎜×1.00㎜

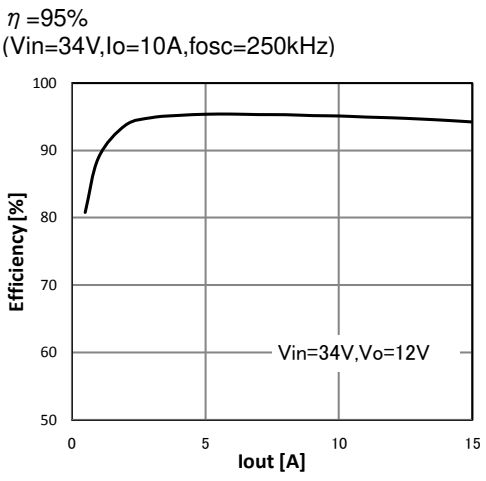
●Applications

- Amusement machines
- FA Equipments
- OA Equipments
- LED Lighting Equipments
- General Equipments used 24V,48V Bus line

●Typical Application Circuit

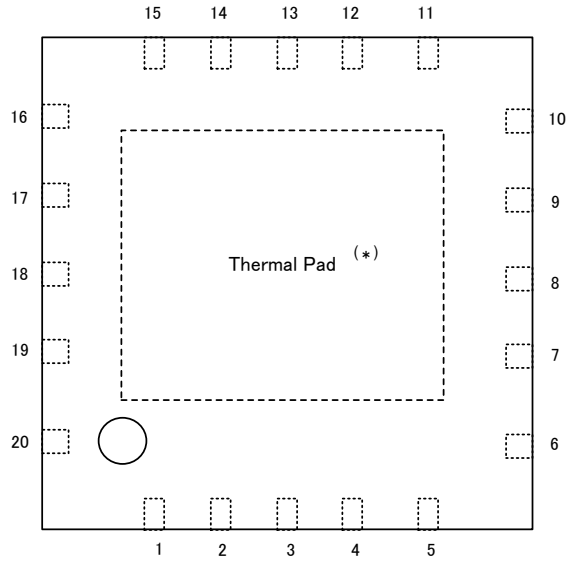


●A Type of Efficiency



○STRUCURE : Silicon Monolithic Integrated Circuit **○**Not designed to withstand radiation.

●Pin Configuration

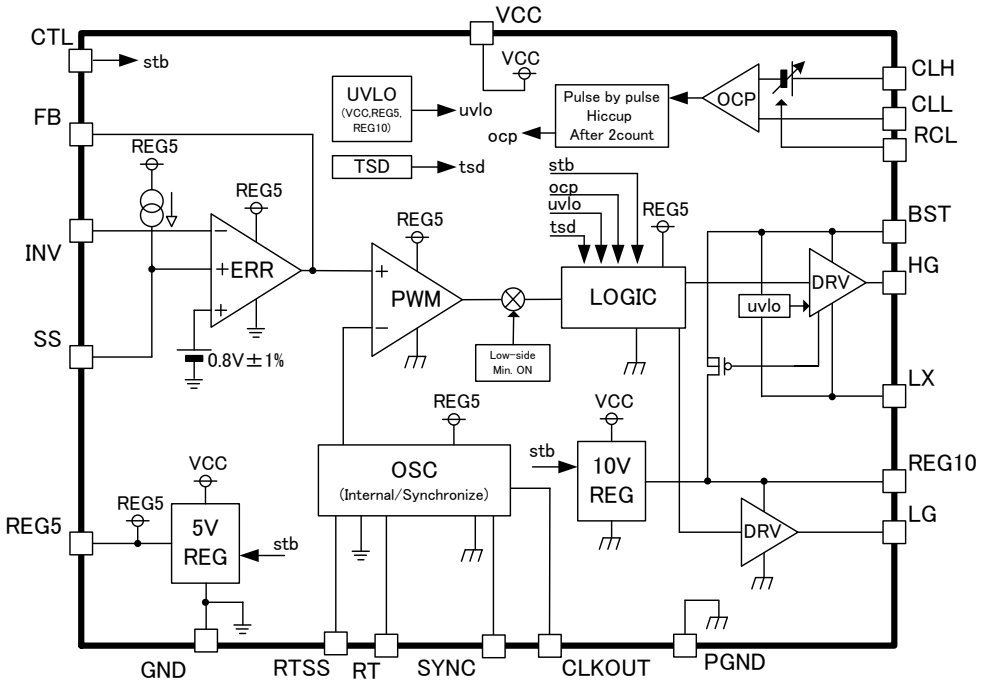


(＊) Recommend connecting Thermal Pad to GND for increasing radiation characteristic.

●Pin Description

Pin No.	Pin Name	Description
1	GND	GROUND
2	SS	Soft-start programming
3	INV	Inverting input to the error amplifier
4	FB	Output of the error amplifier
5	RCL	Current limit programming
6	RT	Frequency programming
7	RTSS	Reference of the RT voltage
8	CLKOUT	Output of Internal clock pulse
9	PGND	GROUND
10	SYNC	Syncronization input for the device
11	LG	Gate drive for low-side N-channel FET
12	REG10	Output of 10V regulator for gate drive
13	LX	This pin is connected to the switched node of the converter
14	HG	Gate drive for high-side N-channel FET
15	BST	Gate drive voltage for the high side N-channel FET
16	CLL	Inverting input to current detector
17	CLH	Input to current detector
18	VCC	Power supply
19	CTL	Shutdown pin
20	REG5	Output of 5V regulator for internal circuit

●Block Diagram



●Block Functional Description

1. 5VREG
   5V Regulator supplied voltage for Internal Circuits(5V±2%).
   It is available as external supply voltage for current ability (2mA Max) or less.

2. ERROR AMP
   Error amplifier output PWM control signal after detected output signal.
   Internal reference voltage is 0.8V(accuracy±1%).
   Connect capacitor and resistor between inverting pin (INV) and output pin (FB) as phase compensation elements.

3. Soft Start
   A Circuit that does Soft Start to the Output Voltage of DC / DC Comparator, and prevents Rush Current during start-up. The external capacitor of SS pin is charged with the internal source current (1uA), and That slope inputs to the error amplifier as the reference voltage of the start-up.

4. OSC
   This is a oscillator for the reference of the PWM modulation. The frequency of the internal triangle wave is programmed by RRT which connected to RT within 50kHz to 500kHz. RT pin is the output of the buffer of RTSS voltage. CLKOUT is the output of the internal oscillator as the square wave.
   Also this can be synchronized to an external clock through the SYNC pin.

5. PWMCOMP
   This is a comparator for PWM modulation comparing the output of error amplifier and ramp wave to decide switching duty. Switching duty is limited by HG min OFF time(350ns), because of charging of BST-LX capacitor.

6. DRV
   It drives the external FETs. Particularly, high side DRV is built in UVLO.

7. 10VREG
   10V Regulator supplied voltage for low-side driver and charged capacitor between BST and LX through internal switch.

8. UVLO
   This is a Low Voltage Error Prevention Circuit.
   This prevents internal circuit error during increase of Power supply Voltage and during decline of Power supply voltage. It monitors VCC, REG5 and REG10. This operation turns off both external FET and reset soft-start by detecting the monitoring voltage under each threshold.

9. TSD
   This is a heat protect (Thermal Shut Down) circuit.
   When it detects an abnormal temperature exceeding Maximum Junction Temperature (Tj=150℃), it turns off both external FET. It has with Hysteresis and automatically releases by becoming under the threshold temperature.

10. OCP
    This is a Over Current Protection circuit. It uses a two-tier approach. The first tier is a pulse-by-pulse protection scheme. Current limit is implemented on the high-side FET by sensing the CLH-CLL voltage when the gate is driven high. The CLH-CLL voltage is compared to the threshold voltage programmed by RCL resister. If the CLH-CLL voltage exceeds the threshold, the switching pulse is immediately terminated. The FET remains off until the next switching cycle is initiated. The second consists of a fault counter. The fault counter is incremented on an over-current pulse. When the counter reaches two within three pulse, both FETs, FB and SS are tuned off during the definite time. After the time both FET, FB and SS are released, and automatically re-start with soft-start.

11. CTL
    With the voltage applied to CTL, IC ON / OFF can be controlled.
    When a voltage of 2.8V or more is applied, it turns ON, at open or 0V application, it turns OFF.
    About 300kΩ pull-down resistance is contained within the pin.

●Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	VCC	60	V
CTL pin	VCTL	VCC	V
BST pin	VBST	70	V
LX pin	VLX	VCC	V
Between BST pin – LX pin	VBSTLX	15	V
HG pin	VHG	LX~BST	V
LG pin	VLG	0~VREG10	V
REG10 pin	VREG10	15	V
REG5 pin	VREG5	7	V
SYNC pin	VSYNC	7	V
INV pin	VINV	REG5	V
CLH pin	VCLH	LX	V
CLL pin	VCLL	LX	V
Power Dissipation	Pd	3.56[*1]	W
Operating Temperature Range	Topr	-40～+105	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	150	℃

*1 During mounting of 70×70×1.6t mm 4layer board (Copper area：70mm×70mm).
Reduce by 28.5mW for every 1℃ increase. (Above 25℃)

●Operating Ratings

Item	Symbol	Range	Unit
Power supply voltage	VCC	10~56	V
Configurable output voltage	VOUT	1.0~(Vin × 0.8V)	V
CTL input voltage	CTL	0~VCC	V
Frequency	FOSC	50~500	kHz
RT resister	RRT	33~470	kΩ
RTSS capacitor	CRTSS	0.001~1.0	uF
Synchronize frequency	SYNCFRQ	FOSC±10%	kHz
SYNC input duty	SYNCDTY	40~60	%
OCP program resister	RRCL	3.3~20	kΩ

●**Electrical Characteristics**

(Unless otherwise specified, Ta=25℃,VCC=CTL=24V,RT=200kΩ)

PARAMETER	SYMBOL	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
【OSCILLATOR】						
Frequency	FOSC	93	100	107	kHz	RT=200kΩ
RTSS maximum current (sink/source)	IRTSS	2.5	5	10	uA	VRTSS=0.48V/1.0V
RTSS pre-charge threshold	VRTSSTH	0.40	0.45	0.50	V	
RTSS pre-charge current	IRTSSP	50	100	200	uA	VRTSS=0.3V
【SOFT START】						
SS source current	ISSSO	0.7	1	1.3	μA	SS=1.0V
【UVLO】						
UVLO threshold (VCC)	VUTHVCC	8.5	9.0	9.5	V	VCC rise-up
UVLO threshold (REG10)	VUTHR10	7.9	8.7	9.5	V	REG10 rise-up
UVLO threshold (REG5)	VUTHR5	4.2	4.5	4.8	V	REG5 rise-up
UVLO hysteresis (VCC)	VUHSVCC	-	0.5	1.0	V	VCC pin
UVLO hysteresis (REG10)	VUHSR10	-	0.5	1.0	V	REG10 pin
UVLO hysteresis (REG5)	VUHSR5	-	0.2	0.4	V	REG5 pin
【ERROR AMPLIFIER】						
Reference voltage	VNON	0.792	0.8	0.808	V	INV=FB
INV input bias current	IBINV	-	0.01	1.0	μA	INV=0.8V
FB max. voltage	VFBH	REG5-0.5	-	REG5	V	
FB min. voltage	VFBL	-	0	0.5	V	
FB sink current	IFBSI	0.5	2	-	mA	FB=1.25V , INV=1.5V
FB source current	IFBSO	60	120	-	μA	FB=1.25V , INV=0V
【PWM COMPARATOR】						
Input threshold voltage	VT0	1.4	1.5	1.6	V	0% Duty ,FB pin vol.
HG min. OFF pulse width	HGmin	150	350	600	ns	FB=3V
【OUTPUT DRIVER】						
Output driver PchFET Ron	RONH	-	6	10	Ω	Iout=0.1A
Output driver NchFET Ron	RONL	-	1	3	Ω	Iout=0.1A

●**Electrical Characteristics**

(Unless otherwise specified, Ta=25℃,VCC=CTL=24V,RT=200kΩ)

PARAMETER	SYMBOL	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
【CURRENT LIMIT】						
OCP threshold voltage	VOCPTH	160	200	240	mV	Between CLH and CLL (RCL=7.5kΩ)
OCP propagation delay to output	TOCP	-	200	300	ns	
OCP counts to hiccup	NOCP	-	2	-	counts	series or every other cycles
OCP shut-down hold cycles	THICCUP	-	32768	-	cycles	T=1/FOSC, Hold time=T×THICCUP
【REGULATOR】						
REG10 output voltage	VREG10	9	10	11	V	
REG5 output voltage	VREG5	4.9	5.0	5.1	V	
REG5 current ability	IREG5	10	30	-	mA	V=VREG5＊0.95
【SYNCHRONIZE OSCILLATOR】						
SYNC input current	ISYNC	-	8	16	uA	SYNC=5V
SYNC input voltage H	VSYNCH	2.8	-	5.0	V	
SYNC input voltage L	VSYNCL	GND	-	0.3	V	
CLKOUT output range	VCLKOUT	REG5-0.5	REG5	REG5+0.5	V	
CLKOUT sink current	ICLKSI	1.5	3	-	mA	CLKOUT=0.5V
CLKOUT source current	ICLKSO	1.5	3	-	mA	CLKOUT=4.5V
【WHOLE DEVICE】						
CTL input current	ICTL	-	5	10	μA	CTL=5V
CTL input voltage H	VCTLH	2.8	-	VCC	V	
CTL input voltage L	VCTLL	GND	-	0.3	V	
Stand-by current	ISC	-	0	5.0	μA	CTL=0V
Quiescent current	ICC	1.5	3	4.5	mA	INV=5V

●**Typical Performance Curves**

(Unless otherwise specified, Ta=25℃,VCC=CTL=24V,RT=200kΩ)

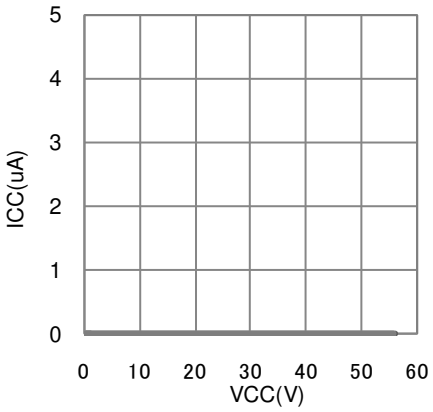


Fig.1. Stand-by current vs VCC (Ta=105℃)

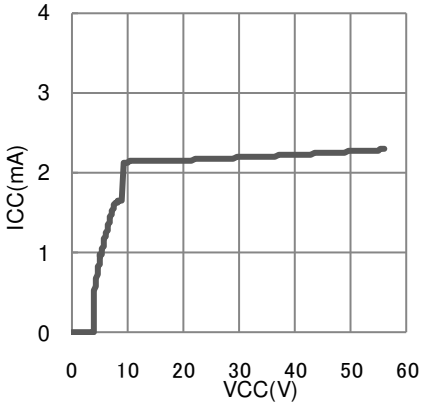


Fig.2. Quiescent current vs VCC

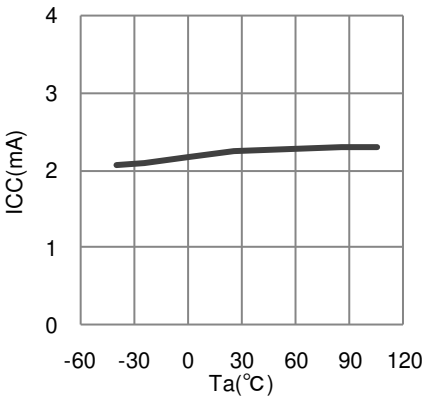


Fig.3. Quiescent current vs temp

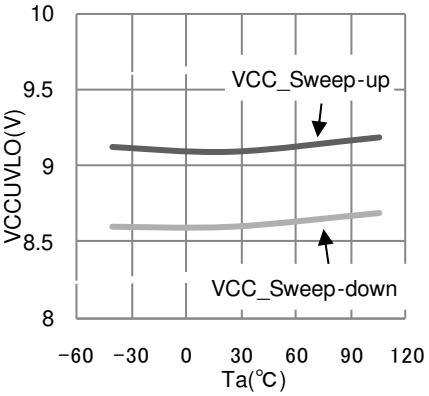


Fig.4. VCCUVLO vs temp

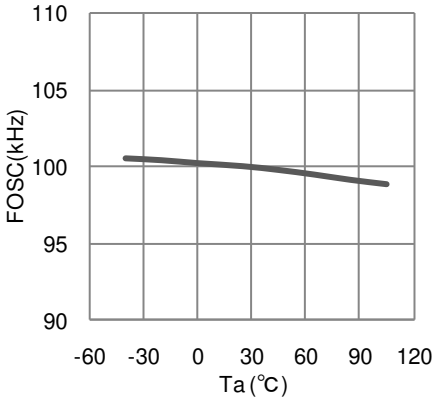


Fig.5. Frequency vs temp

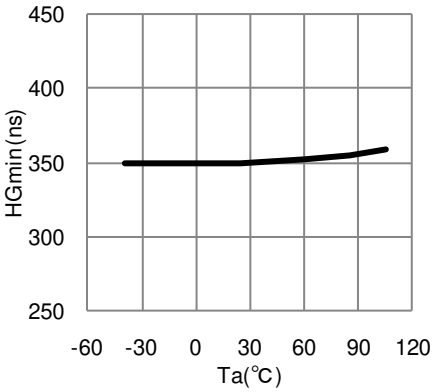


Fig.6. HG min off pulse vs temp

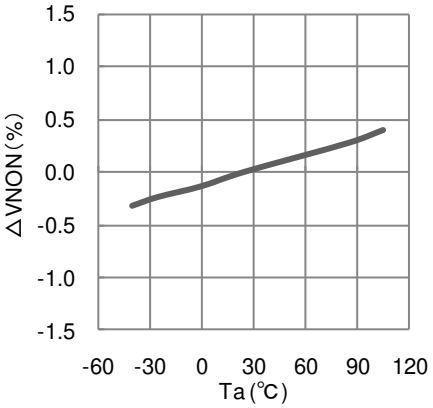


Fig.7. Reference Voltage vs temp

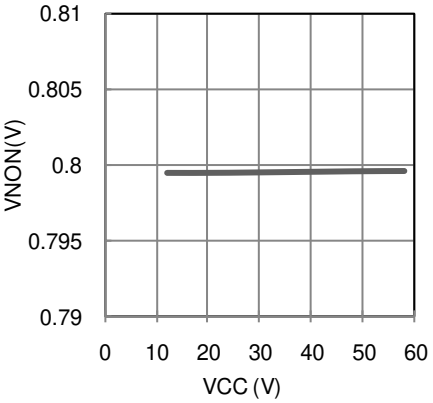


Fig.8. Reference Voltage vs VCC

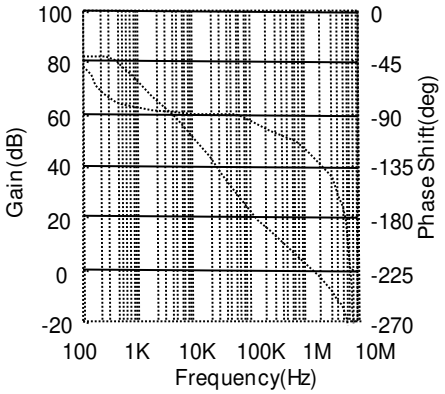


Fig.9.ERRAMP Closed loop gain

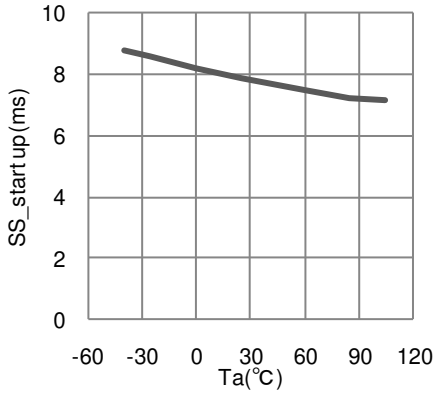


Fig.10. Soft start vs temp

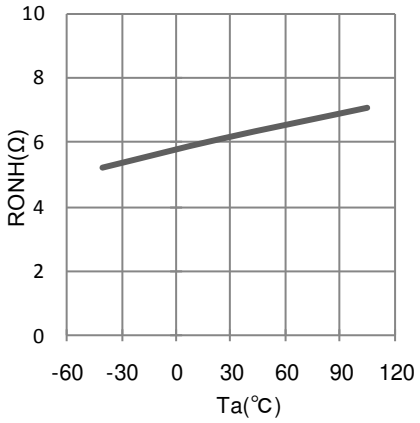


Fig.11. Pch-FET Ron vs temp.

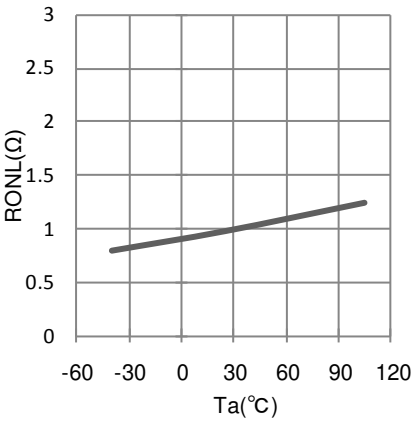


Fig.12. Nch-FET Ron vs temp

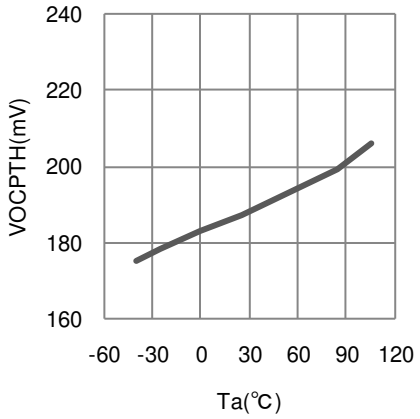


Fig.13 OCP threshold vs temp
(RCL=7.5kΩ)

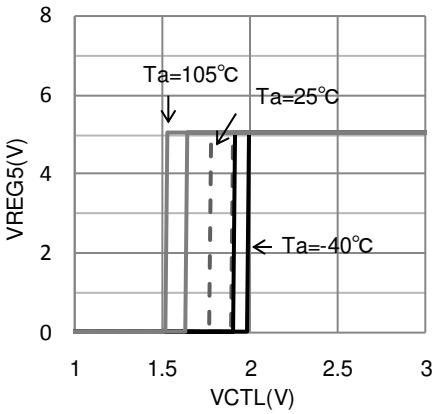


Fig.14. CTL threshold Voltage

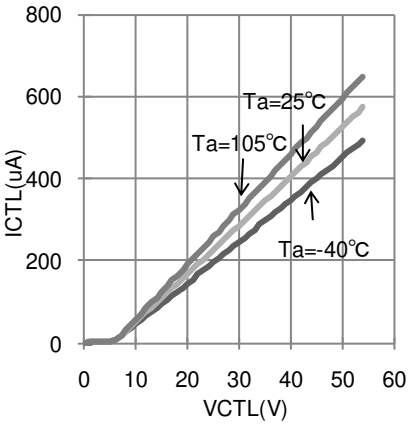


Fig.15. CTL input current

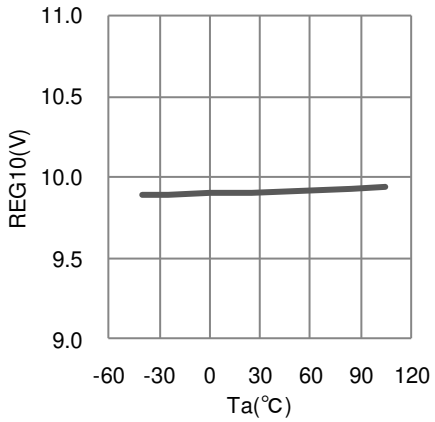


Fig.16 REG10 voltage vs temp

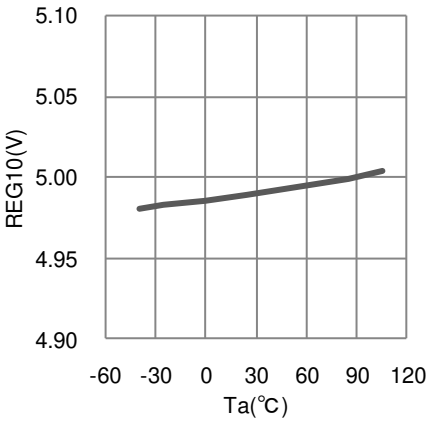


Fig.17. REG5 voltage vs temp

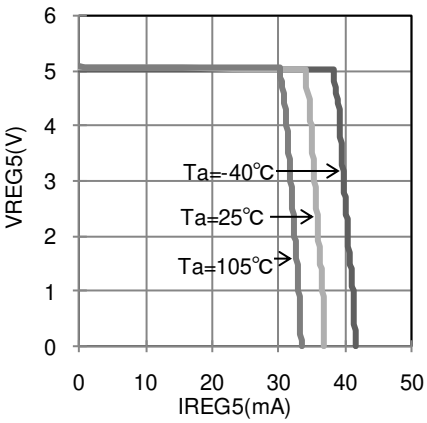
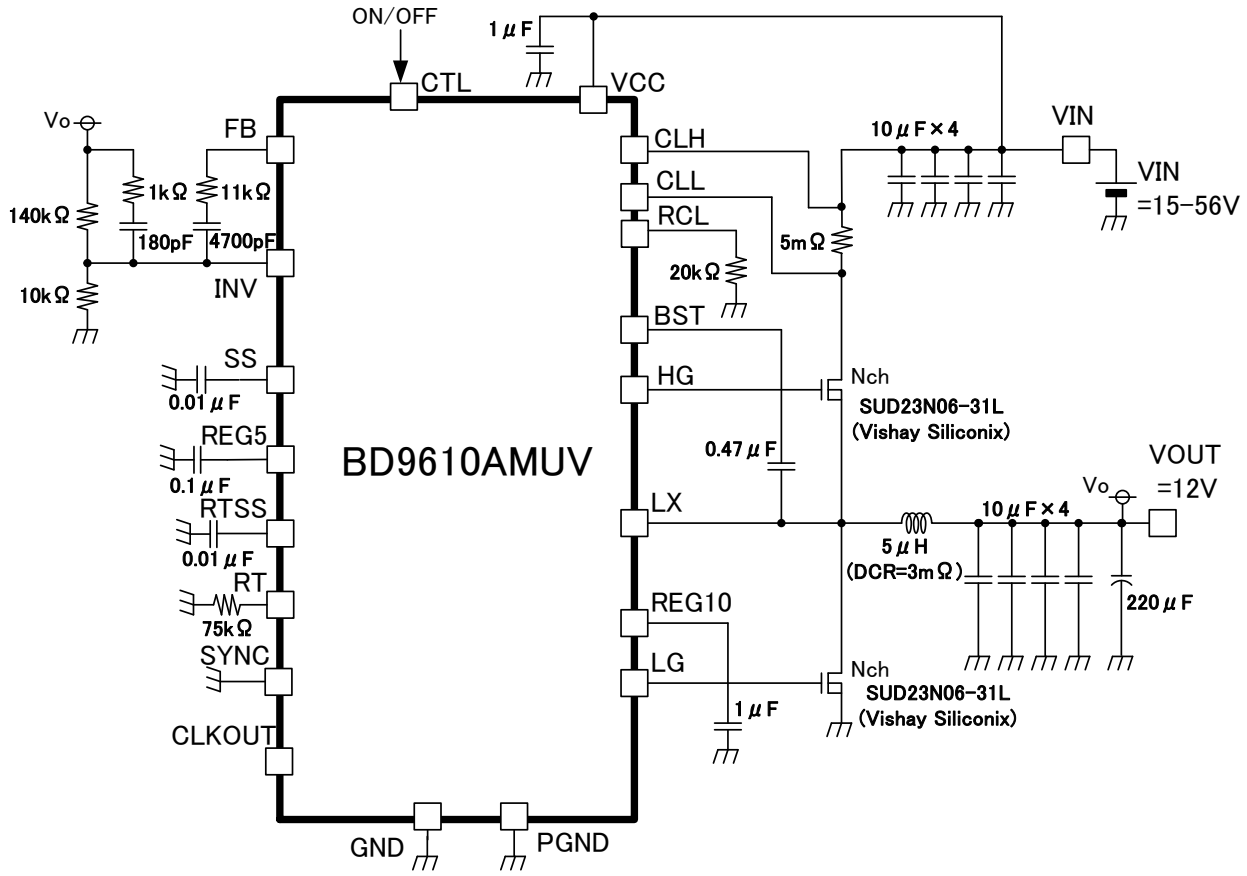


Fig.18. REG5 vs IREG5

●**Reference Application**



●**Reference Application data**

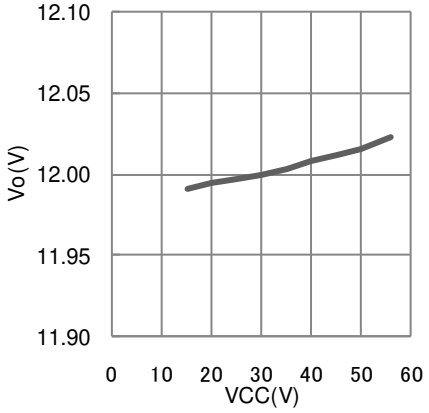


Fig.19 Line Regulation

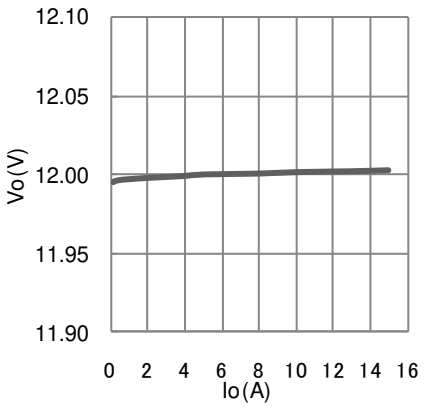


Fig.20 Load Regulation

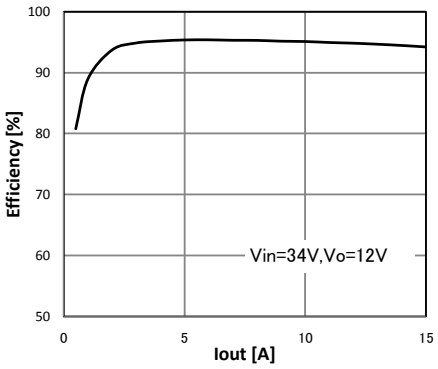


Fig.21 Efficiency

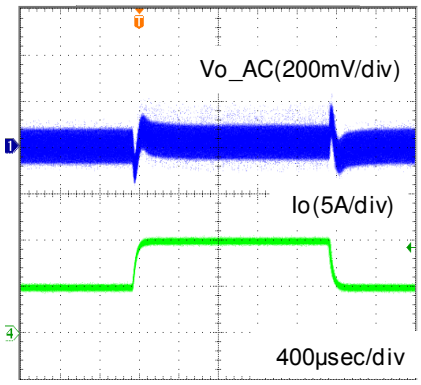


Fig.22 Load Response(Io=5A⇔10A)

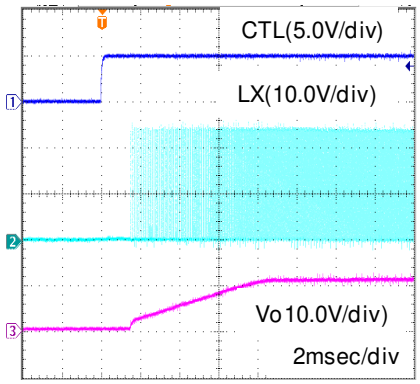


Fig.23 Start-up

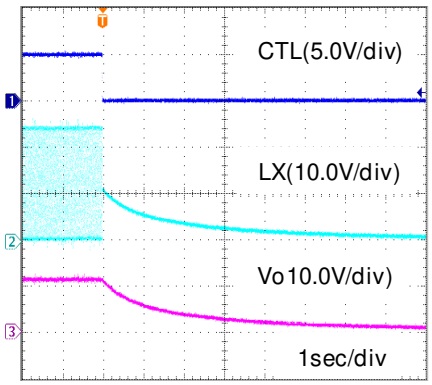


Fig.24 Stop (No Load)

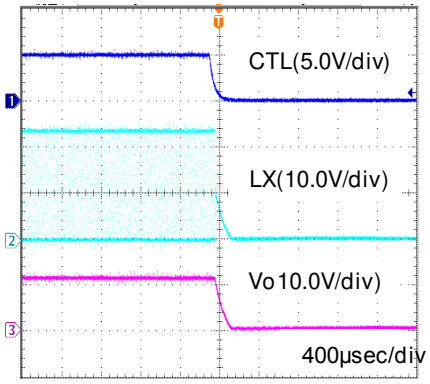


Fig.25 Stop (Rload=2.5Ω)

●Function Description

(1)REG5 REGULATOR

It is used for internal power supply and the reference voltage. It can load more less than 2mA.
Please connect a ceramic capacitor (CREG5=0.1uF) between REG5 and GND.

(2)REG10 REGULATOR

This is a regulator for a low side DRV and charge the BST-LX capacitor through the internal FET switch. Please connect a ceramic capacitor (CREG10=1.0uF) between REG10 and GND.
This regulator limites load current about 20mA, When REG10 pin short to GND. Because of this function,

(3)SOFT START

For preventing rush current or overshoot, The reference voltage should be ramped startup.
The reference voltage used for the startup is derived in the following manner. A capacitor (CSS) is connected to the SS pin. There is a ramped voltage generated at this pin be charging CSS with a source current (ISS=1uA).
The soft-start time is decided by the time to reach SS voltage to 0.8V.

$$tss = (CSS \times VNON) / ISS$$

(ex.)CSS=0.01uF $tss = (0.01u \times 0.8)/1u = 8$ [ms]

Before the beginning of soft start, It takes the start-up time for RTSS described next state.

(4)OSCILLATOR (RT、RTSS、CLKOUT)

The switching frequency of the oscillator is set by a single resistor RRT to ground.
The clock frequency is related to RRT by the following equation and the relationship is charted in fig.26
The amplitude of the triangle wave of the oscillator is 1.5V-2.0V.

$$FOSC = 1 / (50e\text{-}6 \times RRT) \text{ [kHz]}$$ （RRT: RT resister [kΩ]）

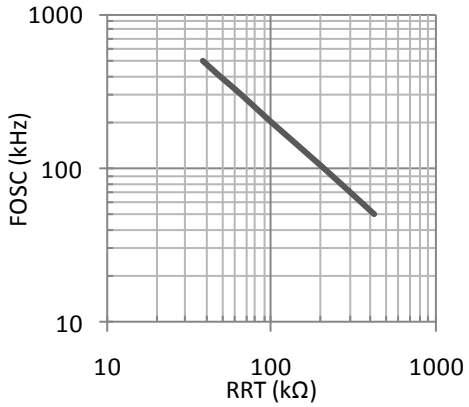


Fig.26 Switching frequency vs RRT resistance

The case of not using the synchronizing to an external supply, the RTSS terminal outputs the internal reference voltage (0.5V) through the internal voltage buffer. And the RT terminal is the buffer of the RTSS voltage. A 0.01uF ceramic capacitor should be connected from this RTSS to ground.

When the UVLO is going to be released, the RTSS pin is quickly charged up to VRTSS=0.45V by the source current (IRTSS=100uA) as a pre-charge function, because CRTSS is discharged during UVLO.
If the voltage of RTSS pin is reached to 0.45V, the UVLO is released and soft start function is started.
It takes this charging time for start-up of DC/DC to begin charging the CSS.

(ex.)CRTSS=0.01uF

$TRTSS = (0.01uF \times 0.50V) / 100uA = 50$ [us]

The CLKOUT pin outputs a square wave which synchronized to internal oscillator for a clock of master-slave synchronizing function.

(5)External synchronization(SYNC)

This IC can be synchronized to an external clock through the SYNC pin for noise management and can be used as a master IC to output clock through the CLKOUT terminal and as a slave IC to input clock through the SYNC terminal for synchronizing some ICs

SYNC pin is connected to GND when not in use for this function.

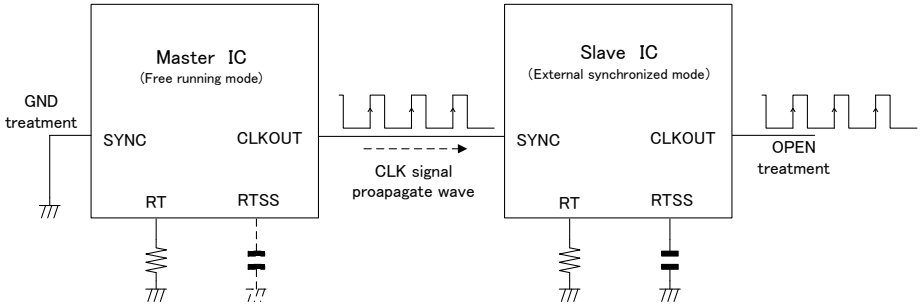


Fig.27 A type of External synchronization circuit

Synchronization occurs on the series three rising edges of the SYNC signal. The clock frequency at the SYNC pin replaces the master clock generated by the oscillator circuit. Pulling the SYNC pin low programs the BD961A0MUV to freely run at the frequency programmed by RRT.

◆Input wave conditions into SYNC pin SYNC

The synchronization frequency should be in the range of -10% to +10% equal to its programmed free-run frequency that is in the range of 50 to 500kHz. The input pulse should be more than 500ns and in the range of 2.8V to 5.0V needed in H level . The special sequence against VCC or CTL is nothing.
Refer to RRT vs Frequency on the previous page when decided RT resistor fixed input signal frequency into SYNC.

It recommended to decide if the BD9610AMUV is used at synchronizing function or not before start-up.
If it need to synchronize after start-up, please notice to the fluctuation of the Vout caused by the instability of oscillation for a while. When the SYNC pin become open, the oscillator state is changed by detecting no eight series pulses from synchronize mode to free-run mode. The BD9610AMUV freely run at the frequency programmed by RRT slowly. It depends on the speed to conclude the RTSS voltage equal to 0.5V by charging or discharging CRTSS with IRTSS (=5uA max.). The frequency changes with RTSS shift.

The RT voltage is fixed almost 0.5V at free-run mode. In synchronizing mode, the RT voltage adjusts freely to the voltage between 0.25V and 1.0V for the oscillator to be able to output the synchronized frequency. The movement of the RT voltage is smoothed by the CRTSS. When the capacitance of the CRTSS is too little, the frequency is fluctuated. But the capacitance is too large, It takes long time to synchronize the frequency. It should be adjusted by the behavior of your condition.

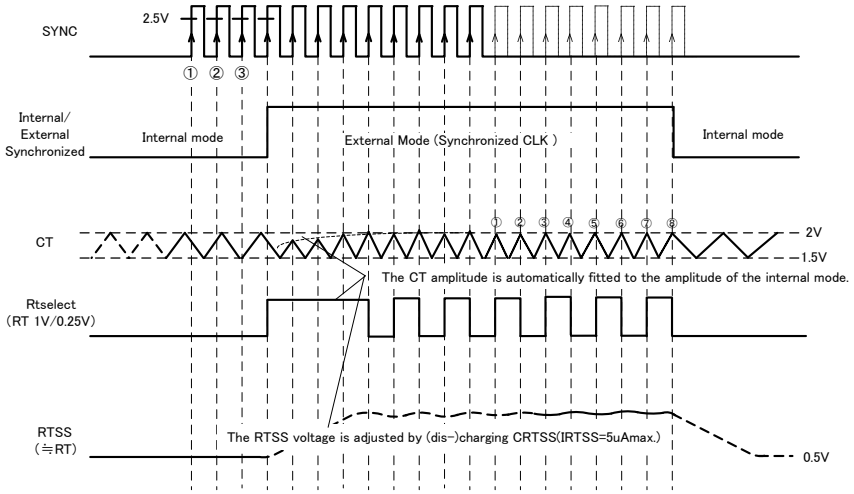


Fig.28 timing chart about External Mode

(6) PWM / BOOST (PRE-CHARGE MODE)

It should be needed to charge the CBST (BST-LX) for driving high-side N-channel FET
The CBST capacitor is charged to the voltage of REG10 by turning on the low side FET through the internal FET switch between REG10 and BST.
The maximum on duty does not reach to 100% because of the LG minimum on pulse. It makes possible to charge the CBST even if the voltage of the FB pin is over 2.0V (It is the high voltage of the internal ramp wave.) and the HG is always going to output the High. If the voltage of Vin and Vout are becoming close, the voltage of the Vout doesn't become equal to the voltage of the Vin.

※About Max Duty

The BD9610AMUV turns off for almost 350nsec in the every turn.(=High side minimum off pulse :HGmin)
This time (about 350ns) consists of the LG min pulse (about 100ns) and of the anti cross conduction time among the HG and the LG (each 100ns).
The Max ON Duty is calculated in the following equation.

$$D(on) = (T - Toff) / T$$ [T：Switching cycle(1/FOSC)、Toff：OFF time(≒350ns typ.)]

※PRE-CHARGE MODE

The BD9610AMUV operates in the pre-charge mode during the time for charging the CBST at the start-up, dropping the voltage of CBST and the releasing protect function (UVLO, TSD, OCP hiccup-mode) for charging the CBST in advance. In this mode, the CBST is charged by the LG on pulse that is limited to almost 300ns at every turn. This mode is switched to the normal switching mode by being detected to release the BSTUVLO.

(7)STAND-BY

It is possible to make the value of the quiescent current 0uA by turning off the CTL pin.
The all of the function is terminated for example REG5 and REG10 in this mode.

(8)UVLO

The UVLO circuits shut down HG, LG, SS and FB, when the voltage of VCC or REG10 or REG5 are under the each UVLO threshold (VCC<9V, REG10<8V, REG5<4.5V). And there are voltage hysteresis at VCC, REG10 and REG5 (VCC:0.5V, REG10:0.5V, REG5:0.2V). When the UVLO is released, soft-start starts after the voltage of RTSS is over 0.5V. Case of being needed the quick start-up, please adjust the capacitance of the CRTSS.
The BST_UVLO is also built t between BST and LX. When the BST_UVLO is detected, HG, SS and FB are shut down and the BD9610AMUV shift to the pre-charge mode. (CBST is charged by LG pulse(t≅ 300ns))

(9)TSD

The TSD is the protection for the IC chip against abnormal temperature (over Tjmax(150deg)). The TSD works at almost 175deg, so It doesn't work in the normal operating temperature range. If the chip is cool down, TSD is automatically released at almost 150deg. Under the TSD protection, HG, LG, SS and FB are shut down like the UVLO.

(10)LG short protection

When the LG pin short to GND, an exceptional large current flow in the BD9610AMUV. (The DC/DC is able to output as a diode rectifier mode by the body diode of the low side Nch-FET.)
For this case, the BD9610AMUV checks to turn LG on after the PWM low output in every cycle. If LG doesn't turn on, the DC/DC will be shut down.

(11)PROGRAMING OCP

This IC monitors the voltage between CLH and CLL for turning on High-side driver (HG=ON).When this voltage is over the threshold adjusted by RRCL, the output is turned off immediately. The switching current is detected by the current detect resistor Rs connected the high side FET drain side usually.

The value of the OCP current is decided by the following .

$$IOCP = VOCPTH / Rs \quad (8)$$

IOCP：OCP detect current
VOCPTH：Threshold voltage between CLH and CLL programmed using RCL.
Rs：Current detect resistor

The OCP threshold is set by a single resistor RCL to ground. Please refer the following graph.
Using RRCL>12.5kΩ, take into consideration the increase of OCP variability.

VOCPTH = (0.8 / RRCL) × 1850 [mV]　RRCL: RCL pin connected resistor [kΩ]

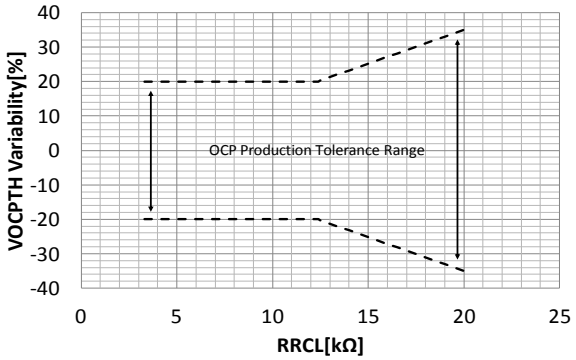


Fig.29 OCP Variability vs RRCL

Recommend to fix OCP threshold voltage using Rs connecting between VCC and Drain of hi side Nch-FET and CR filter between CLH and CLL.
It is available to response stability for control detected variation when connecting CLH and CLL trying not to are common impedance between large current pass line and Rs both ends, and inserting CR filter between CLH and CLL.
CR filter for CLH and CLL is consist of following figure, the impedance of Cocp the lowest possible around noise frequency(adjust noise frequency and self-resonant frequency) and fixed filter constant with Rocp.

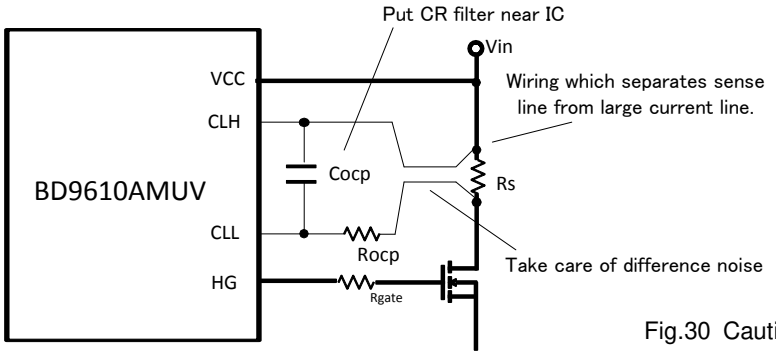


Fig.30 Caution for CLH,CLL filter

Please note that selecting FET and wiring pattern when OCP detection using Ron of FET.
Because of variable Ron and large switching noise false detection, it is false detection.

Please connect CLH and CLL to VCC or line became voltage LX when FET is ON.

Connect RCL to REG5 and CLH,CLL to VCC with shortest wiring not to be used

＜Pulse by pulse protection＞
The detection of OCP doesn't work for almost 60ns as the blanking time against to the ringing noise, also has the delay time for almost 140ns.
When the switching frequency is high and the ratio of Vin and Vout is high, this IC may not detect the OCP. Please take care for the min. pulse width and refer the graph of the item (13) About Output programmed voltage range on the following page graph.

＜Hiccup protection＞
When the OCP is detected in the two series pulse or every one pulse (two time detecting in the three series pulse), the outputs, FB and SS are turned off for a OCP shut-down hold cycles (32768 clock cycles).
(ex.) FOSC=300kHz

$$\text{OCP shut-down hold cycles (THICCUP)} = T(=1/FOSC) \times 32768$$
$$= (1/300k) \times 32768 = 108\ [ms]$$

At the end of the OCP shut-down hold cycles, the soft start begins automatically.

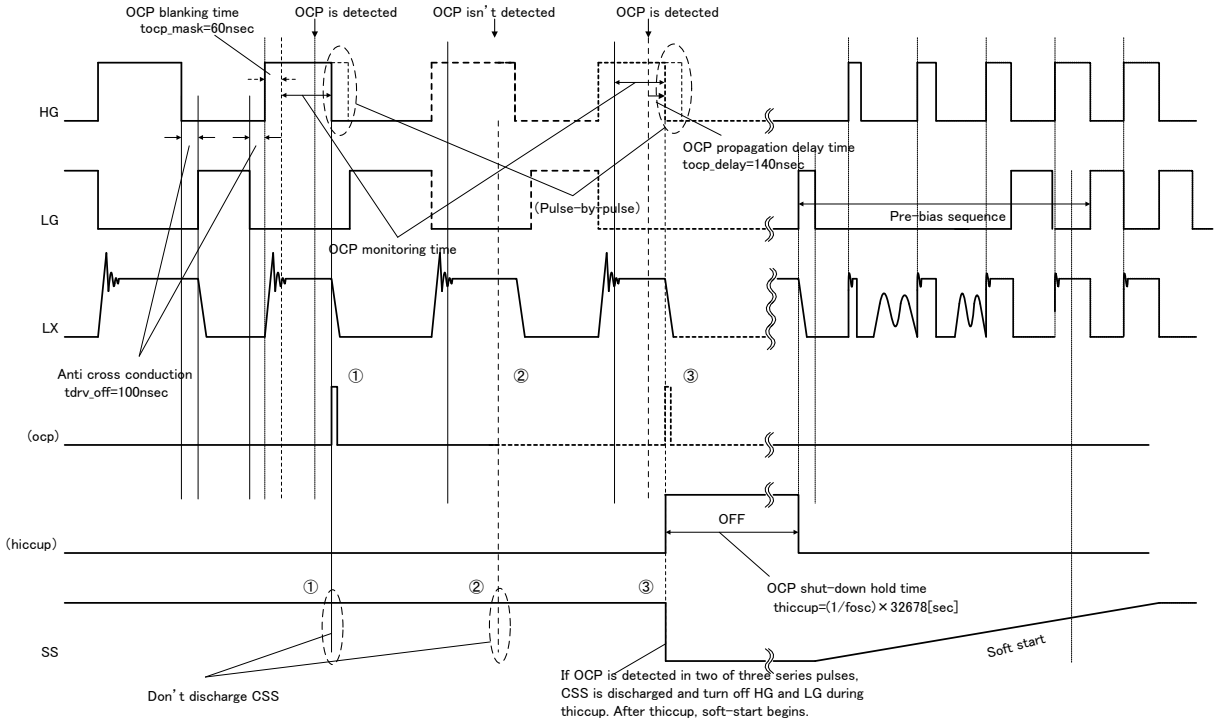


Fig.31 OCP TIMING CHART(※Because of explaining, this chart has ambiguity of time)

(12) PRE-BIAS

This IC is programmed not to sink the large current from Vout, when the Vout has been already biased high voltage at the starting up.

But there is the potential for an increase in output voltage through Body-Di of BST charge SW when output programmed voltage is under 10V.

So connect following resistance with feedback or discharge SW between Vo and PGND to use Vo<10V.

There is no problem as long as Vo≧10V.

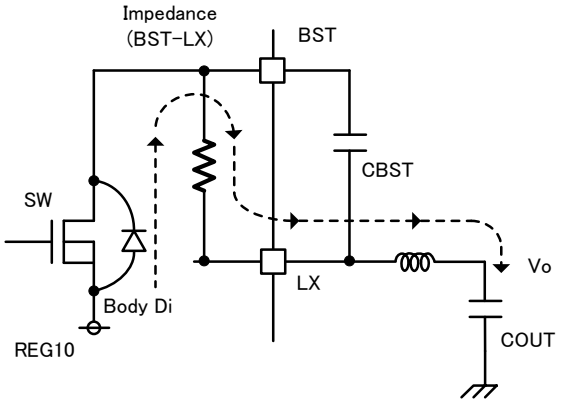
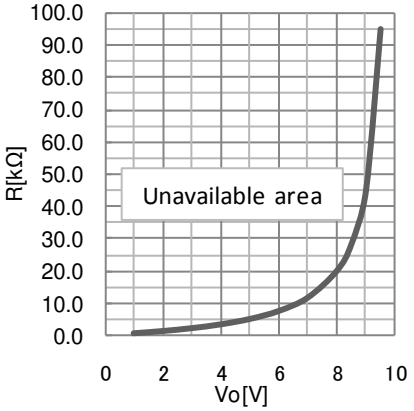


Fig.32 Current pass at PRE-BIAS and low setting output voltage



Vo[V]	R[kΩ]
1	0.56
2	1.25
3	2.14
4	3.33
5	5.00
6	7.50
7	11.67
8	20.00
8.5	28.33
9	45.00
9.5	95.00

Fig.33 setting output voltage vs load resistance

(13)About Output programmed voltage range

This IC's Output voltage available programmed area in the application is restricted on the following graph because of input-voltage, frequency, High-side minimum off pulse and load current.

◆About relation between frequency and input-output voltage ratio

This IC has limitation in output programmed voltage on the following graphs because of restriction of minimum pulse for available feedback control and programmed OCP detect voltage.

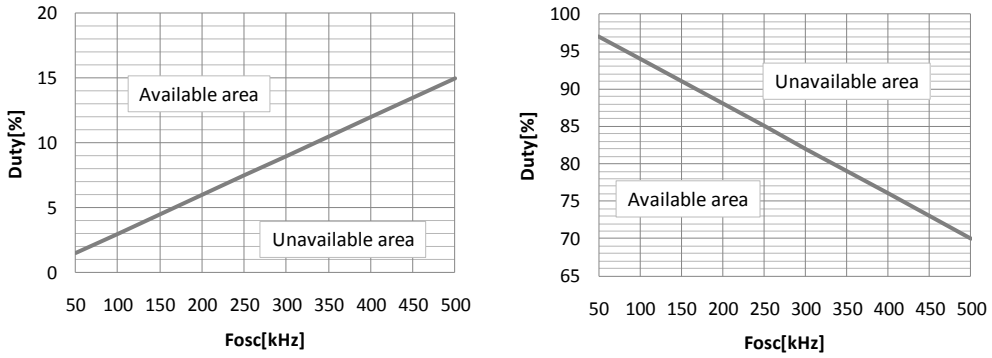


Fig.34 Frequency vs input-output voltage ratio(Duty)

◆About High-side(HG) minimum off pulse

This IC has limitation in output programmed voltage on Hi-side minimum off pulse for charged BST capacitor(CBST) because Bootstrap system is adopted.

Consider toff=600ns as OFF duty pulse.

In the case that input voltage is near output ,input voltage effects from this off pulse.

So take care of input reduced voltage limit when output programmed voltage is near input.

(ex.)Output programmed voltage Vo=12V、frequency f=250kHz (T = 1 / f = 4us)

OFF_Duty=1-Vo/Vin、minimum OFF pulse toff_min = T × OFF_Duty

Toff_min = T × (1 - Vo / Vin) = 4us × (1 - 12V / Vin) ≧ 600ns

It is necessary that Vin ≧ 14.12 [V] for holding Vo=12[V] with upper equation.

Actually consider additionally drop voltage of Ron of high-side FET, DCR of coil PCB pattern impedance.

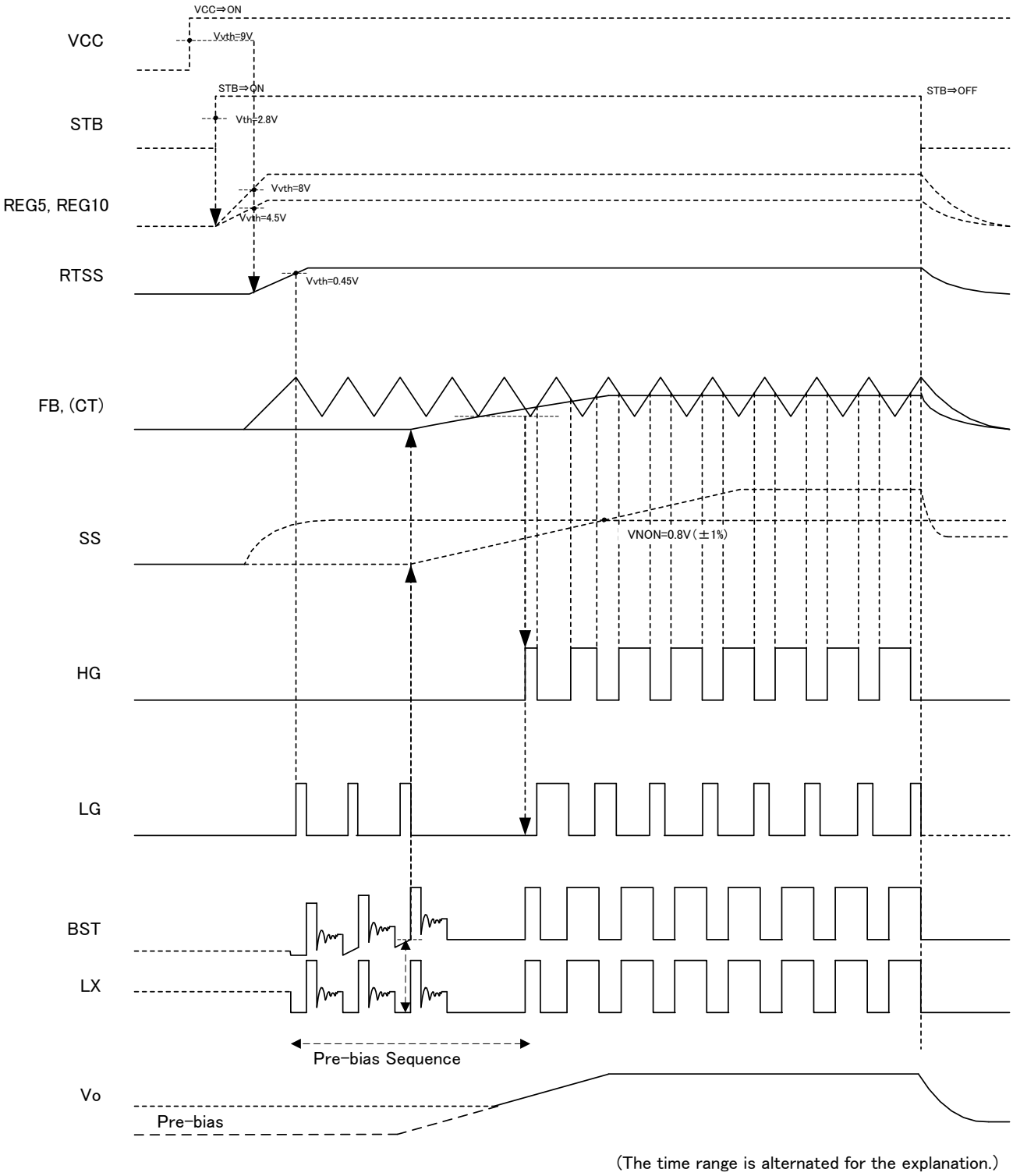
◆About load current

There is not limitation in Vout≧10V between load current and output programmed voltage.

But it is not compliant that Vout is under 10V because of the Pre-bias sequence.

Please refer to (12)PRE-BIAS on page 16.

●TIMING CHART (START-UP)



(The time range is alternated for the explanation.)

Fig.35 TIMING CHART(START-UP)

●Selection of Components Externally Connected

(1)INDUCTOR

It is recommended that the inductor which satisfying the absolute maximum current and having low dc resistance and shielded type.
The Inductance is affected to the ripple current and cause Vo ripple voltage.
Increasing the inductance or the switching frequency make the ripple current small.

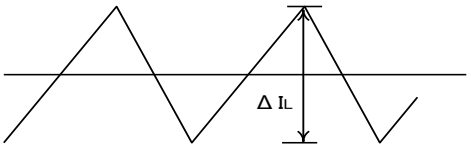


Fig.36 Inductor Current

Ipeak = Iout ＋ 1/2×⊿IL [A] (1)

⊿IL= (Vin-Vout) / L ×(Vout / Vin) × (1 / fosc) [A] (2)

(⊿IL：Inductor ripple current、fosc : Switching frequency)

Generally, ⊿IL is chosen so that the converter enters discontinuous mode at 20-40% of nominal load.

If the inductor current is over the maximum current, the inductor may cause saturation and the efficiency become worse and sometime the DC/DC may cause an oscillation. It is very important to select the large absolute current inductor with enough dilating.

(2)COUT

It is recommended to choice the small ESR capacitor for decreasing Vout ripple voltage.
Also it is important to use high absolute voltage capacitor with care for DC bias characteristic.
The Vout ripple voltage is calculated by the following equation.

Vripple = ⊿IL×1 / (2π x f x Cout) + ⊿IL×Resr (3)

If the capacitance of Cout is too large, it is not able to start up. Please refer the following equation.

Cout ≦ tss × (Iocp – Iout) / Vout (4)

（tss：soft start time, Iocp：OCP detect current）

(3)SETTING OF VOUT

The reference voltage of the ERROR AMP is set to 0.8V.
The Vout voltage is calculated by the following equation

VOUT = (R1+R2) / R2 ×0.8[V] (5)

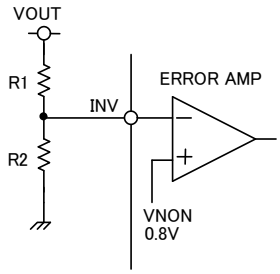


Fig.37 Vout setting

(4)FET

It is needed to select high dilated FET because of the short current or the high switching spike noise
Please choise the low Ciss or low Qg FET considering for the low noise and high efficiency application.
Also It should be care for gate bias voltage, the BD9610AMUV drive the FET by 10V driver.

(5)CBST

A capacitor connected from BST to LX is the power supply for high side FET driver. It should be connected the ceramic capacitor 0.47uF in the general application.

(6)CIN

It should be careful for the absolute maximum voltage, ripple current and low ESR devise.
Please refer the Irms equation for calculating ripple current.

Irms = Iout × √ (Vout・(Vin - Vout) / Vin) (6)

(7)About adjusting frequency characteristic of DC/DC convertor

This IC is PWM controller with voltage mode.

1st lead compensation(fz1,fz2) is adjusted using C,R around INV,FB as against 2nd lag(fp2) consisted of L,COUT for the whole of DC/DC system stability .

As target frequency of the whole system

- Unity gain frequency (Gain =0dB):1/10~1/30 times of switching frequency(FOSC)
- Phase margin $\theta \geqq 30$deg

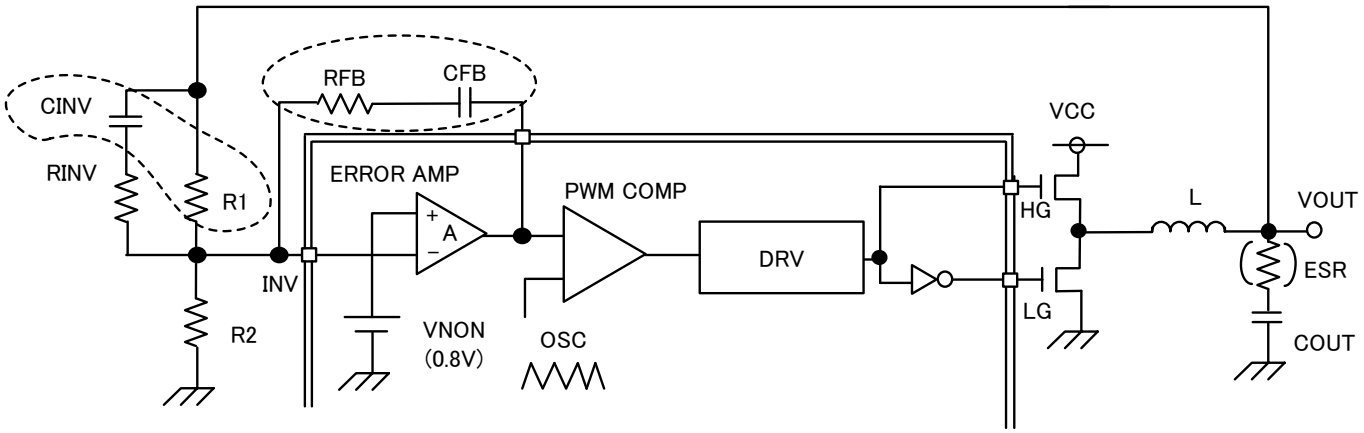


Fig.38 The phase compensation whole DC/DC system

There are two poles (phase lag) regarding DC/DC behavior in case of above figure system.

①1st pole around ERR_AMP (fp1)

$fp1 = 1 / [2 \cdot \pi \cdot (R1//R2) \cdot A \cdot CFB]$ ・・・1st lag(90deg)

②Pole of LC filter(fp2)

$fp2 = 1 / [2 \cdot \pi \cdot \sqrt{(L \cdot C)}]$ ・・・2nd lag (180deg)

Fix two phase lead compensation following zero points against the 2nd lag pole ②of LC filter so that these phase may not become 180° lag.

Please set up CR constant that each frequency fz1,fz2(,fz3) became about fp2.

③Zero of output capacitor ESR (fz1)

$fz1 = 1 / (2 \cdot \pi \cdot COUT \cdot ESR)$ ・・・1st lead(90deg)

④Zero around ERR_AMP(fz2)

$fz2 = 1 / (2 \cdot \pi \cdot CFB \cdot RFB)$ ・・・1st lead (90deg)

⑤※Zero around ERR_AMP(fz3)

$fz3 = 1 / (2 \cdot \pi \cdot CINV \cdot R1)$ ・・・1st lead (90deg)

※There is not need to set fz3 for usable fz1 with high ESR capacitor on output for example the electrolytic.

In addition, there is need to set fz3 for being fz1 at high frequency range with low ESR capacitor for example the ceramic .

It is possible to adjust frequency characteristic using RINV connected value of same R1 and R2 or 1/10 times(add pole and shifted zero point)

Please confirm actual production fully ,because ESR characteristic using electrolytic capacitor, DC bias characteristic of ceramic changes using ceramic, temperature ,or output voltage are changed.

（Recommendation　confirming bode diagram using FRA）

●Cautions on PC Board layout

(1) It is very important to minimize the loop① and loop② for reducing switching noise caused to parasitic inductance of the pattern. Also it should be care to the gate wiring.

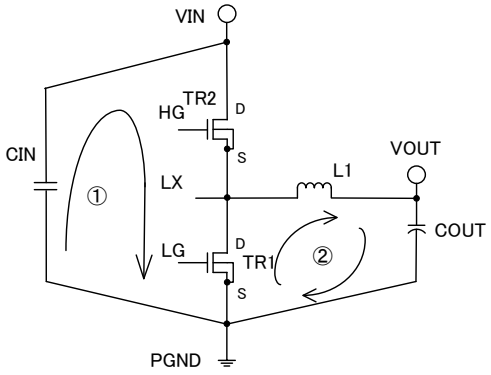


Fig.39 Current loop paths on PCB

(2) The large pattern of the switching node like LX, HG and LG which change the voltage widely may cause low efficiency and dispatch some large noises. Please minimize the switching node pattern with an enough current tolerance.

(3) The FETs are almost the hottest device in DC/DC application. Please take care for of the heat, for example use plural layer board and connect the each drain patterns with a many thermal via. The pad of the bottom of the IC should be connected to GND pattern.

(4) The PGND plane should be shorted at the under the BD9610AMUV to the GND plane. All GND plane should be low impedance with using the GND plane of the middle layer. It is important to be low impedance for the stable operation.

(5) The analog sensitive nodes are affected by the switching modes. Please keep away the periphery of the analog control section of REG5, SS, INV, FB, RCL, RTSS and RT from the periphery of the switching power section of BST, HG, LX, REG10 and LG or the periphery of the switching clock section of SYNC and CLKOUT.

(6) For stable operation, the capacitors of VCC, REG5, RTSS and the resistors of RT and RTSS should be connected to the stable GND plane (which connected with GND pin) without common impedance with a large current node.

(7) VCC and GND nodes should be wide for reducing a line impedance to keep under a drop and a noise effect.

●**Power Dissipation**

It is shown below reducing characteristics of power dissipation to mount 70mm × 70mm × 1.6mm^t, 4 layer PCB.
Junction temperature must be designed not to exceed 150℃

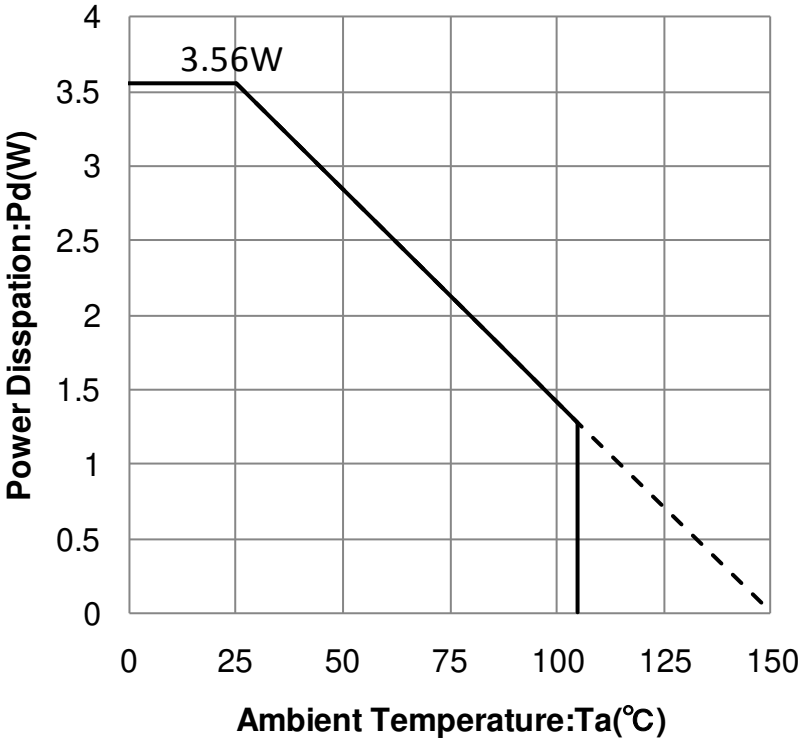
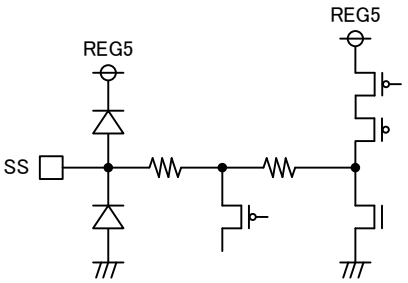
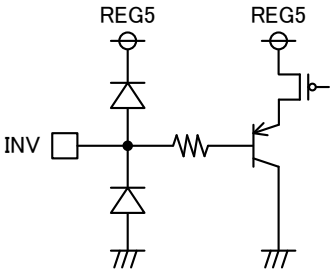
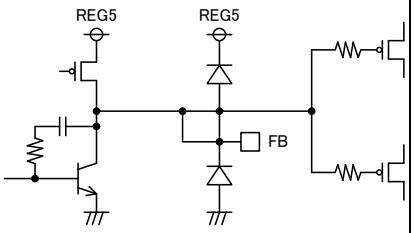
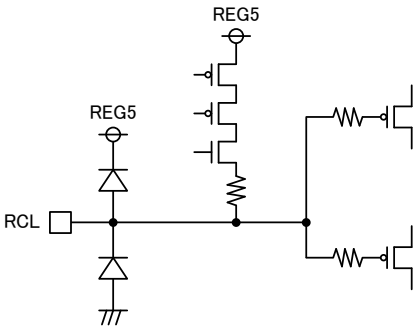
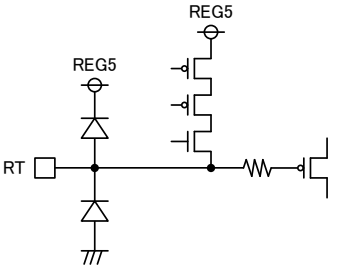
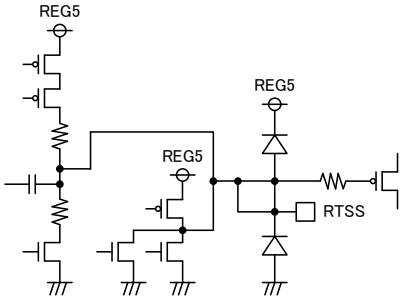
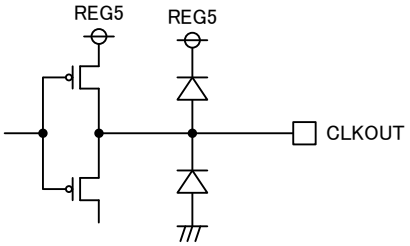
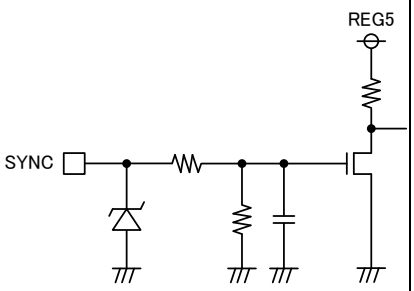
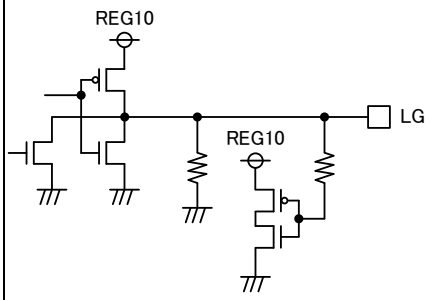
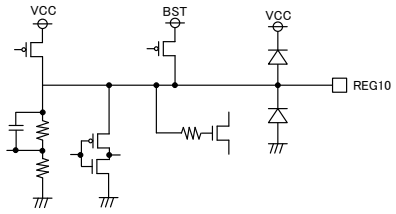
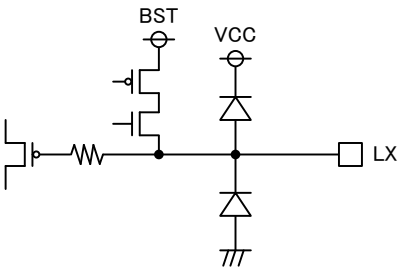
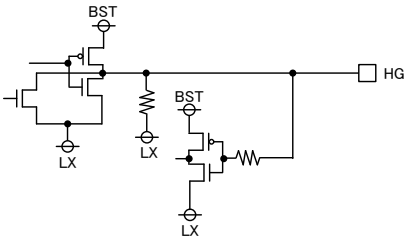
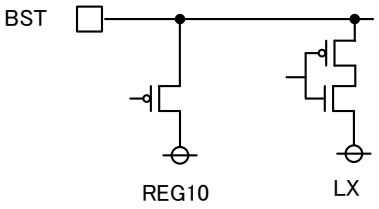
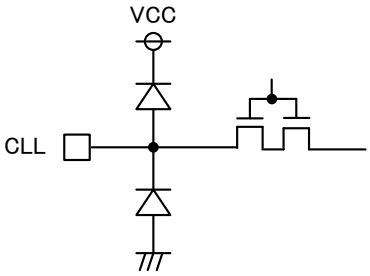
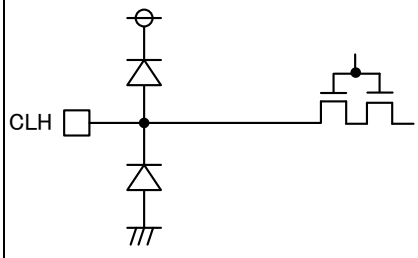
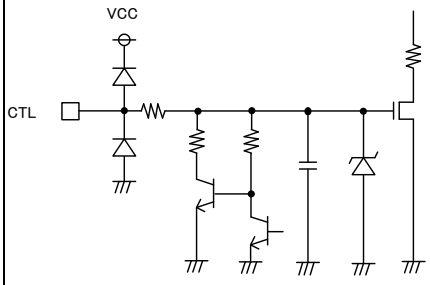
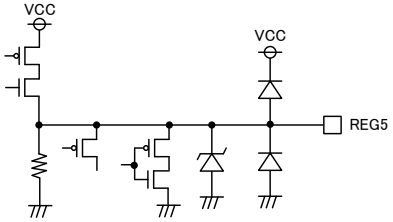


Fig.40 Power Dissipation

●**I/O equivalence circuit**

Pin. No	Pin Name	Equivalence Circuit	Pin. No	Pin Name	Equivalence Circuit
1	GND		2	SS	
3	INV		4	FB	
5	RCL		6	RT	
7	RTSS		8	CLKOUT	
9	PGND		10	SYNC	

Pin. No	Pin Name	Equivalence Circuit	Pin. No	Pin Name	Equivalence Circuit
11	LG		12	REG10	
13	LX		14	HG	
15	BST		16	CLL	
17	CLH		18	VCC	
19	CTL		20	REG5	

●Cautions for Use

(1)About Absolute Maximum Rating

When the absolute maximum ratings of application voltage, operating temperature range, etc. was exceeded, there is possibility of deterioration and destruction. Also, the short Mode or open mode, etc. destruction condition cannot be assumed. When the special mode where absolute maximum rating is exceeded is assumed, please give consideration to the physical safety countermeasure for the fuse, etc.

(2)About GND Electric Potential

In every state, please make the electric potential of GND Pin into the minimum electrical potential. Also, include the actual excessive effect, and please do it such that the pins, excluding the GND Pin does not become the voltage below GND.

(3)About Heat Design

Consider the Power Dissipation (Pd) in actual state of use, and please make Heat Design with sufficient margin.

(4)About short circuit between pins and erroneous mounting

When installing to set board, please be mindful of the direction of the IC, phase difference, etc. If it is not installed correctly, there is a chance that the IC will be destroyed. Also, if a foreign object enters the middle of output, the middle of output and power supply GND, etc., even for the case where it is shorted, there is a change of destruction.

(5)About the operation inside a strong electro-magnetic field

When using inside a strong electro-magnetic field, there is a possibility of error, so please be careful.

(6)Temperature Protect Circuit (TSD Circuit)

Temperature Protect Circuit(TSD Circuit) is built-in in this IC. As for the Temperature Protect Circuit (TSD Circuit), because it a circuit that aims to block the IC from insistent careless runs, it is not aimed for protection and guarantee of IC. Therefore, please do not assume the continuing use after operation of this circuit and the Temperature Protect Circuit operation.

(7)About checking with Set boards

When doing examination with the set board, during connection of capacitor to the pin that has low impedance, there is a possibility of stress in the IC, so for every 1 process, please make sure to do electric discharge. As a countermeasure for static electricity, in the process of assembly, do grounding, and when transporting or storing please be careful. Also, when doing connection to the jig in the examination process, please make sure to turn off the power supply, then connect. After that, turn off the power supply then take it off.

(8)About common impedance

For the power supply and the wire of GND, lower the common impedance, then, as much as possible, make the ripple smaller (as much as possible make the wire thick and short、and lower the ripple from L,C), etc. then and please consider it sufficiently.

(9)About bypass diode

In the application, when the mode where the VCC and each pin electrical potential becomes reversed exists, there is a possibility that the internal circuit will become damaged. For example, during cases wherein the condition when charge was given in the external capacitor, and the VCC was shorted to GND, it is recommended to insert the bypass diode to the diode of the back current prevention in the VCC series or the middle of each Pin-VCC.

(10)About IC Pin Input

This IC is a Monolithic IC、and between each element, it has P $^+$ isolation for element separation and P board. With the N layer of each element and this , the P - N junction is formed、and the parasitic element of each type is composed.

For example、like the diagram below、when resistor and transistor is connected to Pin,

○When GND > (Pin A) in Resistor、 when GND > (Pin A)、when GND > (Pin B) in Transistor (NPN), the P - N junction will operate as a parasitic diode.

○Also, during GND > (Pin B) in the Transistor (NPN), through the N layer of the other elements connected to the above-mentioned parasitic diode , the parasitic NPN Transistor will operation.

On the composition of IC, depending on the electrical potential, the parasitic element will become necessary. Through the operation of the parasitic element interference of circuit operation will arouse, and error, therefore destruction can be caused. Therefore please be careful about the applying of voltage lower than the GND (P board) in I/O Pin, and the way of using when parasitic element operating.

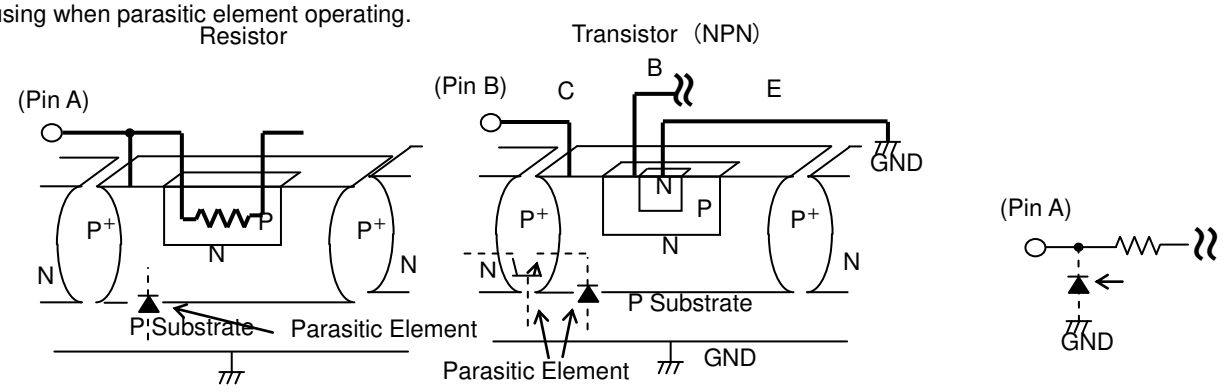


Fig.41 Example of simple structure of Bipolar IC