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High Performance Switching Regulator

# 60V Synchronous Step-down Switching Regulator (Controller Type)

## BD9611MUV

### ● General Description

The BD9611MUV is a high-resistance, wide voltage input (10V to 56V), synchronous step-down switching regulator. BD9611MUV offers design flexibility through user-programmable functions such as soft-start, operating frequency, high-side current limit, and loop compensation. BD9611MUV uses voltage pulse width modulation, and drives 2 external N-channel FETs.

The Under-Voltage Locked Output (EXUVLO) protection connected to its CTL terminal has high accuracy reference voltage. Its threshold voltage can be adjusted by the resistance ratio between VCC and GND as seen by pin CTL.

BD9611MUV is safe for pre-biased outputs. It does not turn on the synchronous rectifier until the internal high-side FET has already started switching

### ● Features

- High Resistance and Wide Range Voltage Input : VCC=10V to 56V
- Regulated Voltage Output to Drive External FET gate: REG10=10V
- Internal Reference Voltage Accuracy: 0.8V±1.0%
- Safe for Pre-biased Outputs
- Adjustable Operating Frequency and Soft-start
- Master/Slave Synchronization
- Over Current Protection (OCP)
- Under Voltage Locked Output (UVLO, EXUVLO)
- Thermal Shut-down (TSD)

### ● Key Specifications

| | |
|---|---|
| Input Supply Voltage | 10 to 56 [V] |
| Output Voltage | 1.0 to (Vin×0.8) [V] |
| Reference Voltage Accuracy | ±1.0 [%] |
| Gate Drive Voltage (REG10) | 9 to 11 [V] |
| Operating frequency | 50 to 500 [kHz] |

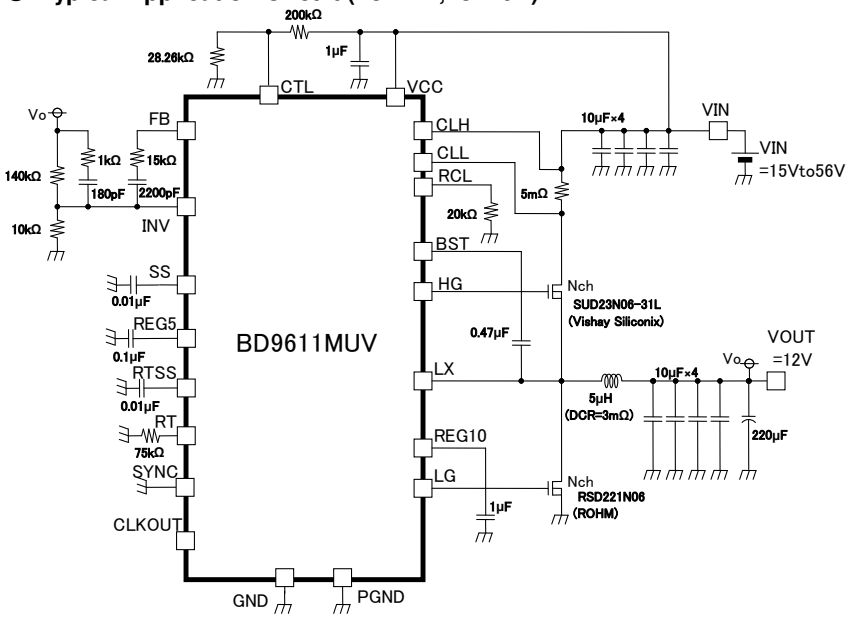
### ● Package

VQFN020V4040 4.00 ㎜×4.00 ㎜×1.00 ㎜

### ● Applications

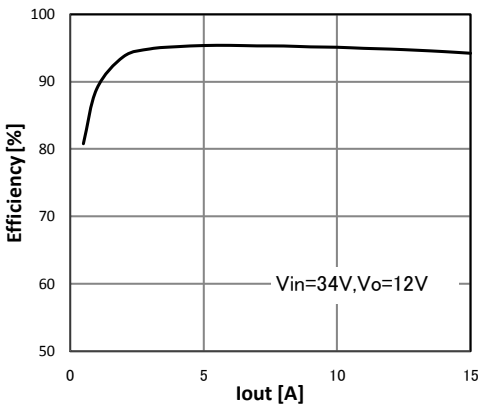
- Amusement machines
- Factory Automation Equipment
- Office Automation Equipment
- LED lighting
- General equipment that require 24V or 48V supply

### ● Typical Application Circuit (Vo=12V, Io=10A)



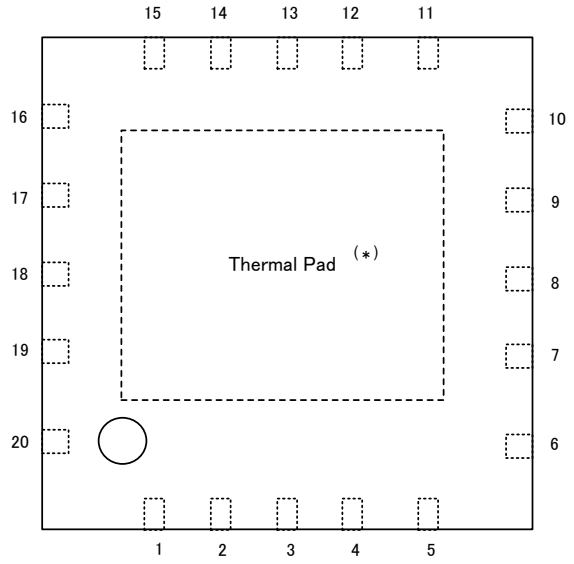

### ● Efficiency Curve

Efficiency: $\eta$ =95%
($V_{IN}$=34V, $I_{OUT}$=10A, $f_{OSC}$=250kHz)




○ **STRUCURE:** Silicon Monolithic Integrated Circuit ○ Not designed to operate under radioactive environments

## ● Pin Configuration (Top View)

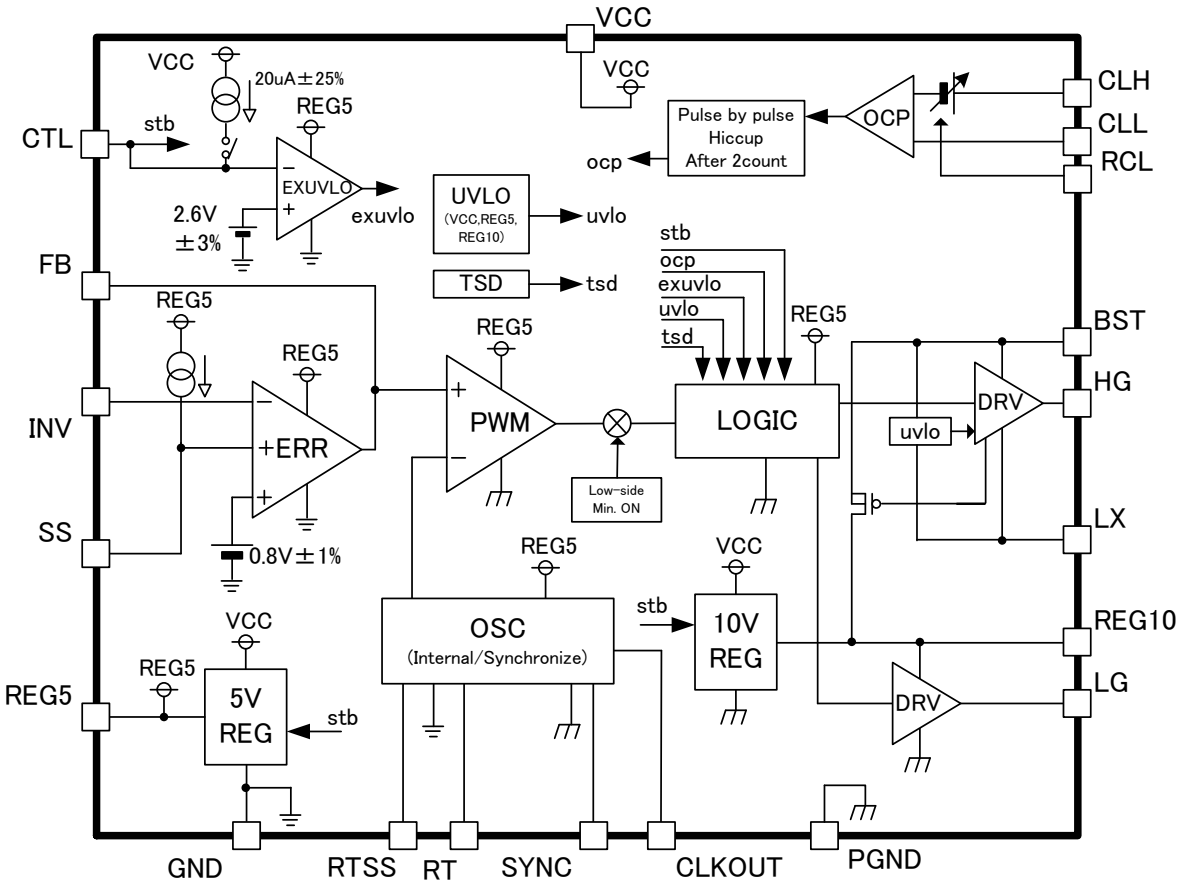



( * ) Connecting the thermal pad to GND is recommended to improve thermal dispersion characteristic.

## ● Pin Description

| Pin no. | Pin Name | Description |
|---|---|---|
| 1 | GND | Ground |
| 2 | SS | Programmable Soft-start |
| 3 | INV | Inverting input to the error amplifier |
| 4 | FB | Output of the error amplifier |
| 5 | RCL | Programmable current limit setting |
| 6 | RT | Programmable frequency setting |
| 7 | RTSS | Reference voltage pin for RT |
| 8 | CLKOUT | Internal clock pulse output |
| 9 | PGND | Ground |
| 10 | SYNC | Synchronization input for the device |
| 11 | LG | Gate driver for external Low-side, N-channel FET |
| 12 | REG10 | Output of 10V internal regulator |
| 13 | LX | Connect to switching node of the converter |
| 14 | HG | Gate driver for external High-side, N-channel FET |
| 15 | BST | Gate drive voltage input for the High-side N-channel FET |
| 16 | CLL | Inverting input to current detector |
| 17 | CLH | Input to current detector |
| 18 | VCC | Power supply |
| 19 | CTL | Shutdown pin |
| 20 | REG5 | Output of 5V internal regulator |

## ● Block Diagram



## ● Functional Description of Blocks

1. 5VREG

Supplies regulated 5V to internal circuits (5V ± 2%).
It is available as an external supply for applications requiring a maximum current of 2mA or less.

2. ERR (Error Amp)

Error amplifier output depends on detected VOUT output and is used as PWM control signal.
Internal reference voltage is 0.8V (Accuracy: ±1%).
Connect capacitor and resistor between inverting pin (INV) and output pin (FB) as phase compensation elements.

3. Soft Start

A circuit that prevents in-rush current during startup through soft start operation of DC-DC comparator output voltage. The external capacitor of pin SS is charged with an internal source current (1uA). This produces a voltage slope input to the error amplifier and performs as the start-up reference voltage.

4. OSC

This is an oscillator that serves as reference of the PWM modulation. The frequency of the internally generated triangle wave is controlled by an external resistor RRT connected to RT pin, and can vary within 50kHz to 500kHz. RT pin outputs the RTSS voltage buffer. CLKOUT outputs the oscillator-generated square wave.
OSC can be synchronized to an external clock through the SYNC pin.

5. PWMCOMP

This is a comparator for PWM modulation which compares the output of the error amplifier and ramp wave from OSC to decide the switching duty. Switching duty is limited by HG min OFF time (350ns) because of the charging of BST-LX capacitor.

6. DRV

It drives the external FETs. High side DRV in particular has built in UVLO.

7. 10VREG

It outputs a regulated 10V that is used as supply voltage for the low-side driver. It is also used to charge the capacitor between BST and LX through an internal switch.

8. UVLO

This is a low voltage error prevention circuit. It prevents internal circuit error during changes in the power supply voltage by monitoring VCC, REG5 and REG10. Its operation turns off both external FETs and resets the soft-start function whenever a threshold is met for any of the monitored voltages.

9. EXUVLO

This is a low voltage error prevention circuit with adjustable VCC detect and release threshold voltages. The threshold voltages can be adjusted through external resistances between VCC and GND.
When the CTL input voltage is greater than the EXUVLO threshold voltage of 2.6V (±3%), a 20uA (±25%) constant current flows to the CTL terminal. Once the CTL input voltage becomes lower than this threshold, both the high-side and low-side FETs are turned off and the SS terminal capacitor is discharged.

10. TSD

This is a circuit which protects the IC from excessive heat by executing thermal shut down.
When it detects an abnormal temperature exceeding the Maximum Junction Temperature ($T_J$=150℃), it turns off both external FETs. TSD employs hysteresis and the IC automatically resumes normal operation once the temperature is less than the release threshold.

11. OCP

This is an Over Current Protection circuit that uses a two-tier approach.
The first tier is a pulse-by-pulse protection scheme. Current limit is implemented on the high-side FET by sensing the CLH-CLL voltage when the gate is driven high. The CLH-CLL voltage is compared to the threshold voltage configured by the RCL resistor. If the CLH-CLL voltage exceeds the threshold, the switching pulse is immediately terminated. The FET remains off until the next switching cycle is initiated.
The second tier consists of a fault counter. The fault counter is incremented whenever an over-current pulse is detected. When the counter reaches two within three successive pulses, both FETs, FB and SS are all turned off for a specified time. Afterwards, both FETs, FB and SS are released and automatically restarted with soft-start.

12. CTL

The voltage applied to pin CTL (VCTL) can control the ON / OFF state of the IC.
When VCTL > 2.4V is applied, internal regulators turn on. DRV turns on next when VCTL > 2.8V is applied.
A current value of approximately (VCTL - 5.6V) / 100kΩ sink to CTL whenever VCTL > 5.6V because of a 5.6V clamping circuit connected after a 100kΩ internal resistance and the CTL terminal.
If the CTL terminal becomes open after reaching the release voltage of EXUVLO, the IC is unable to turn off because of the internal constant current source at CTL.
The IC turns off when VCTL < 0.3V is applied. In this condition, the stand-by current is approximately 0uA.

● **Absolute Maximum Ratings**

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | VCC | 60 | V |
| CTL pin | VCTL | VCC | V |
| BST pin | VBST | 70 | V |
| LX pin | VLX | VCC | V |
| Between BST pin – LX pin | VBSTLX | 15 | V |
| HG pin | VHG | VLX to VBST | V |
| LG pin | VLG | 0 to VREG10 | V |
| REG10 pin | VREG10 | 15 | V |
| REG5 pin | VREG5 | 7 | V |
| SYNC pin | VSYNC | 7 | V |
| INV pin | VINV | VREG5 | V |
| CLH pin | VCLH | VLX | V |
| CLL pin | VCLL | VLX | V |
| Power Dissipation | $P_D$ | 3.56 *1 | W |
| Operating Temperature Range | $T_{OPR}$ | -40 to +105 | ℃ |
| Storage Temperature Range | $T_{STG}$ | -55 to +150 | ℃ |
| Junction Temperature | $T_{JMAX}$ | 150 | ℃ |

*1 When mounting on a 70×70×1.6 mm 4-layer board (Copper area: 70mm×70mm).
Pd is reduced by 28.5mW for every 1℃ increase in temperature above 25℃.

● **Operating Ratings**

| Item | Symbol | Range | Unit |
|---|---|---|---|
| Power supply voltage | VCC | 10 to 56 | V |
| Configurable output voltage | VOUT | 1.0 to (Vin × 0.8V) *2 | V |
| CTL input voltage | CTL | 0 to VCC *3 | V |
| Frequency | FOSC | 50 to 500 | kHz |
| RT resistor | RRT | 33 to 470 | kΩ |
| RTSS capacitor | CRTSS | 0.01 to 1.0 | uF |
| Synchronization frequency | SYNCFRQ | FOSC ± 10% | kHz |
| SYNC input duty | SYNCDTY | 40 to 60 | % |
| OCP program resistor | RRCL | 3.3 to 20 | kΩ |

*2 Please refer to p.25 (13) regarding programmed output voltage (for output voltage dependent on input voltage, frequency, load current etc.)

*3 CTL remains at “H” state due to hysteresis constant current, whenever CTL terminal is opened after EXUVLO release voltage had been detected. Please refer to p.26 (14).

● **Electrical Characteristics**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

| PARAMETER | SYMBOL | LIMIT | | | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| 【OSCILLATOR】 | | | | | | |
| Frequency | FOSC | 93 | 100 | 107 | kHz | RT=200kΩ |
| RTSS maximum current (sink/source) | IRTSS | 2.5 | 5 | 10 | uA | VRTSS=0V/1.0V |
| RTSS pre-charge threshold | VRTSSTH | 0.45 | 0.5 | 0.55 | V | |
| RTSS pre-charge current | IRTSSP | 50 | 100 | 200 | uA | VRTSS=0.3V |
| 【SOFT START】 | | | | | | |
| SS source current | ISSSO | 0.7 | 1 | 1.3 | uA | SS=1.0V |
| 【UVLO】 | | | | | | |
| UVLO threshold (VCC) | VUTHVCC | 8.5 | 9.0 | 9.5 | V | VCC rise-up |
| UVLO threshold (REG10) | VUTHR10 | 7.9 | 8.7 | 9.5 | V | REG10 rise-up |
| UVLO threshold (REG5) | VUTHR5 | 4.2 | 4.5 | 4.8 | V | REG5 rise-up |
| UVLO hysteresis (VCC) | VUHSVCC | - | 0.5 | 1.0 | V | VCC pin |
| UVLO hysteresis (REG10) | VUHSR10 | - | 0.5 | 1.0 | V | REG10 pin |
| UVLO hysteresis (REG5) | VUHSR5 | - | 0.2 | 0.4 | V | REG5 pin |
| UVLO threshold (CTL) | VEXUTH | 2.522 | 2.6 | 2.678 | V | CTL rise-up |
| UVLO hysteresis current | IUVHYS | -25 | -20 | -15 | uA | CTL=5V |
| 【ERROR AMPLIFIER】 | | | | | | |
| Reference voltage | VNON | 0.792 | 0.8 | 0.808 | V | INV=FB |
| INV input bias current | IBINV | - | 0.01 | 1.0 | uA | INV=0.8V |
| FB max voltage | VFBH | REG5-0.5 | - | REG5 | V | |
| FB min voltage | VFBL | - | 0 | 0.5 | V | |
| FB sink current | IFBSI | 0.5 | 2 | - | mA | FB=1.25V, INV=1.5V |
| FB source current | IFBSO | 60 | 120 | - | uA | FB=1.25V, INV=0V |
| 【PWM COMPARATOR】 | | | | | | |
| Input threshold voltage | VT0 | 1.4 | 1.5 | 1.6 | V | 0% Duty, FB pin vol. |
| HG min OFF pulse width | $HG_{MIN}$ | 150 | 350 | 450 | ns | FB=3V |
| 【OUTPUT DRIVER】 | | | | | | |
| Output driver PchFET Ron | RONH | - | 6 | 10 | Ω | Iout=0.1A |
| Output driver NchFET Ron | RONL | - | 1 | 3 | Ω | Iout=0.1A |

● **Electrical Characteristics**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

| PARAMETER | SYMBOL | LIMIT | | | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| 【CURRENT LIMIT】 | | | | | | |
| OCP threshold voltage | VOCPTH | 160 | 200 | 240 | mV | Between CLH and CLL (RCL=7.5kΩ) |
| OCP propagation delay to output | TOCP | - | 200 | 300 | ns | |
| OCP counts to hiccup | NOCP | - | 2 | - | counts | In series or in every other cycle |
| OCP shut-down hold cycles | THICCUP | - | 32768 | - | cycles | T=1/FOSC, Hold time=T×THICCUP |
| 【REGULATOR】 | | | | | | |
| REG10 output voltage | VREG10 | 9 | 10 | 11 | V | |
| REG5 output voltage | VREG5 | 4.9 | 5.0 | 5.1 | V | |
| REG5 current ability | IREG5 | 10 | 30 | - | mA | V=VREG5×0.95 |
| 【SYNCHRONIZE OSCILLATOR】 | | | | | | |
| SYNC input current | ISYNC | - | 8 | 16 | uA | SYNC=5V |
| SYNC input voltage H | VSYNCH | 2.8 | - | 5.0 | V | |
| SYNC input voltage L | VSYNCL | GND | - | 0.3 | V | |
| CLKOUT output range | VCLKOUT | REG5-0.5 | REG5 | REG5+0.5 | V | |
| CLKOUT sink current | ICLKSI | 1.5 | 3 | - | mA | CLKOUT=0.5V |
| CLKOUT source current | ICLKSO | 1.5 | 3 | - | mA | CLKOUT=4.5V |
| 【WHOLE DEVICE】 | | | | | | |
| CTL output current | ICTL | 15 | 20 | 25 | uA | CTL=5V |
| CTL input voltage L | VCTLL | GND | - | 0.3 | V | |
| CTL input voltage1 H | VCTL1H | 2.2 | - | 2.4 | V | REG5, REG10 start up |
| CTL input voltage2 H | VCTL2H | 2.8 | - | VCC | V | DRV start up |
| Stand-by current | ISC | - | 0 | 5.0 | uA | CTL=0V |
| Quiescent current | ICC | 1.0 | 2.0 | 4.0 | mA | INV=5V |

● **Typical Performance Curves 1**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

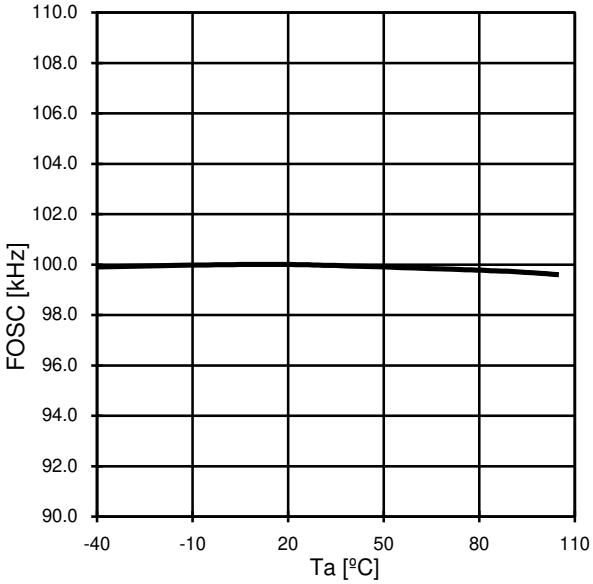



Fig.1 FOSC-Ta

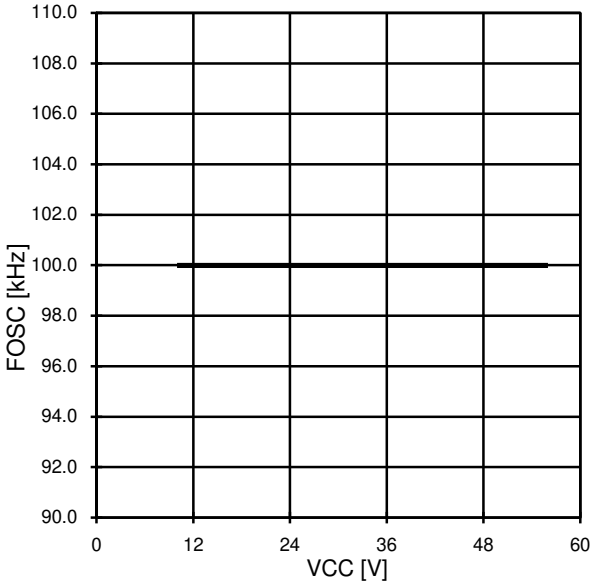



Fig.2 FOSC-VCC

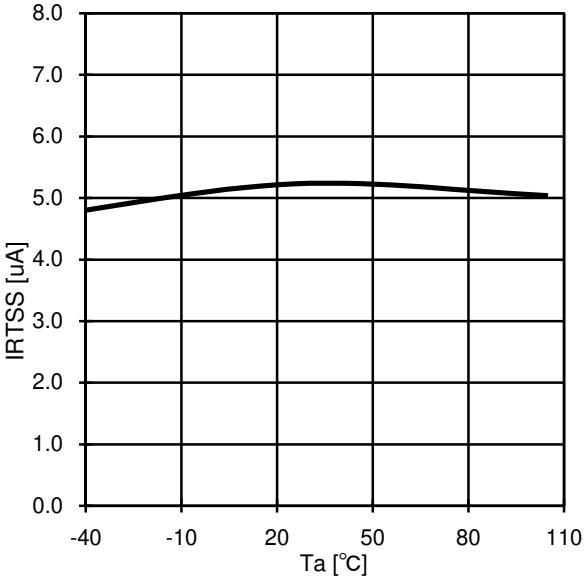



Fig.3 IRTSS-Ta (VRTSS=0V)

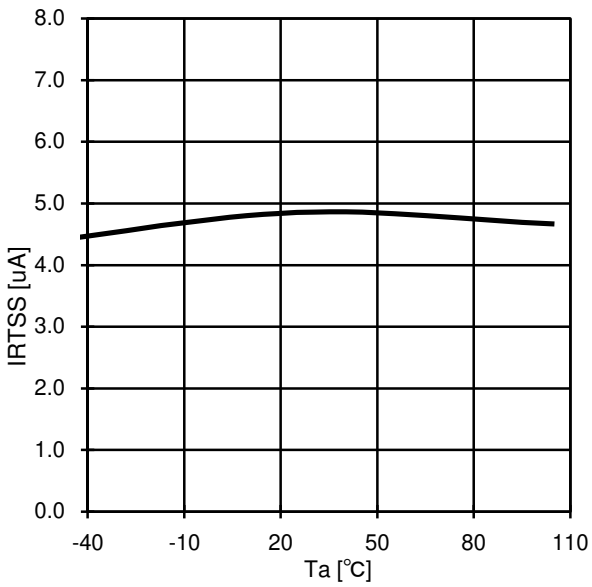



Fig.4 IRTSS-Ta (VRTSS=1V)

● **Typical Performance Curves 2**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

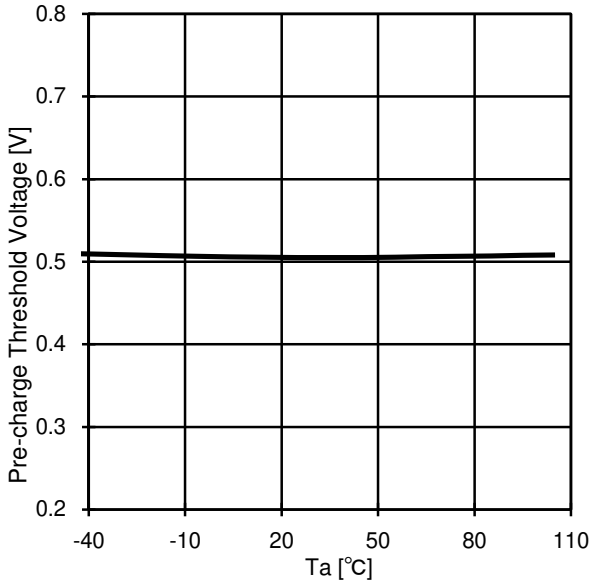



Fig.5 RTSS Pre-charge Threshold-Ta

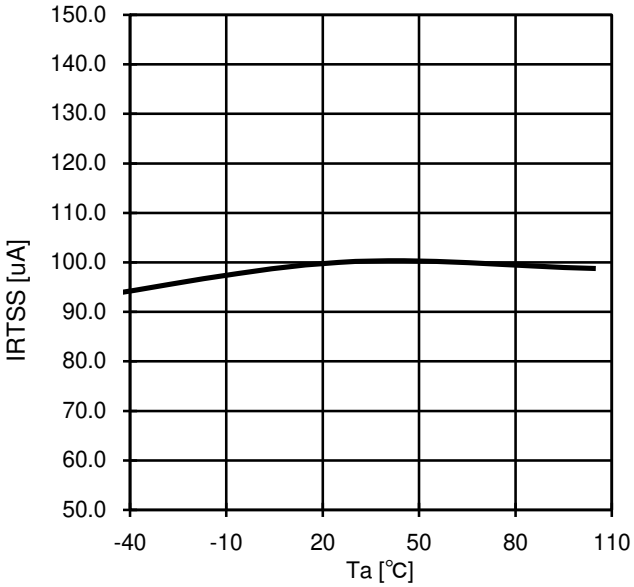



Fig.6 RTSS Pre-charge Current-Ta

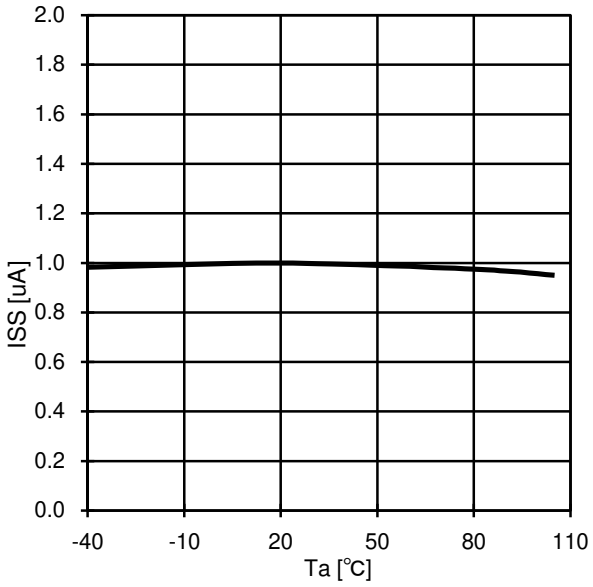



Fig.7 SS Source Current-Ta (VSS=1V)

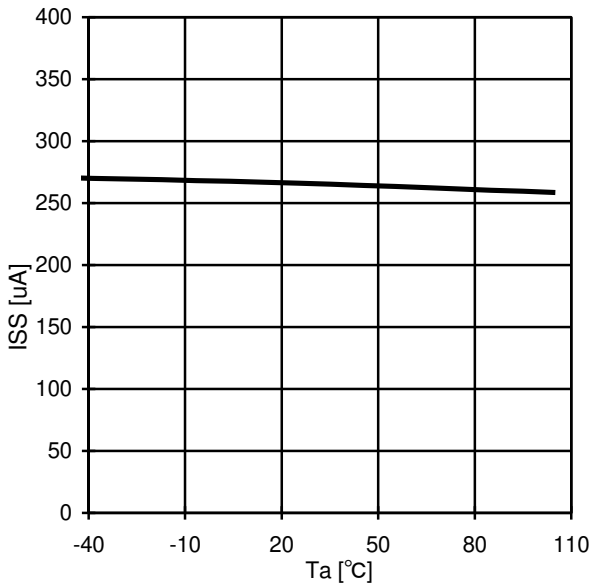



Fig.8 SS Sink Current-Ta (VSS=1V, Protection)

● **Typical Performance Curves 3**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

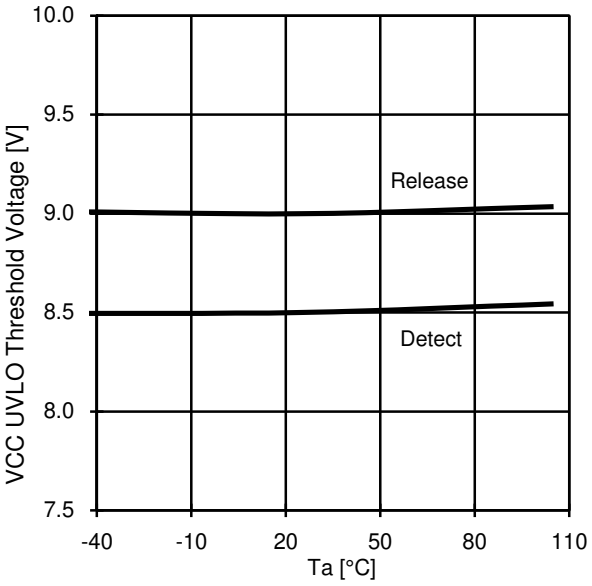



Fig.9 VCC UVLO-Ta

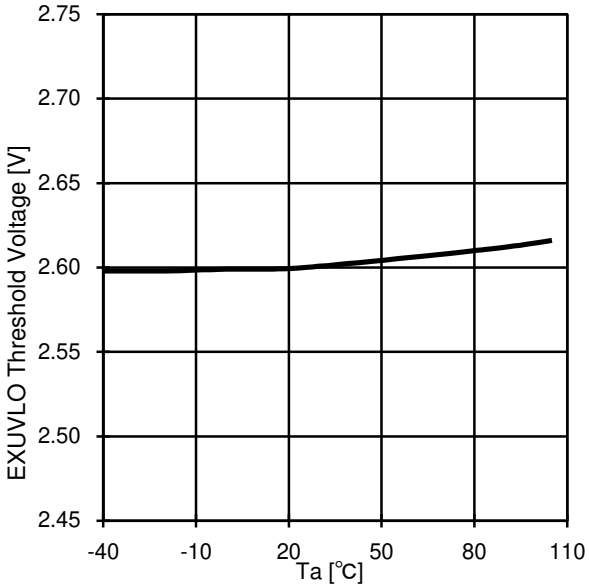



Fig.10 EXUVLO (CTL)-Ta

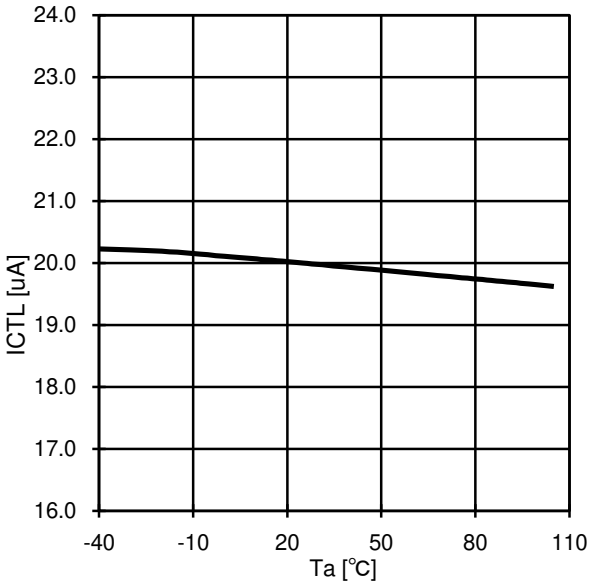



Fig.11 UVLO Hysteresis Current-Ta

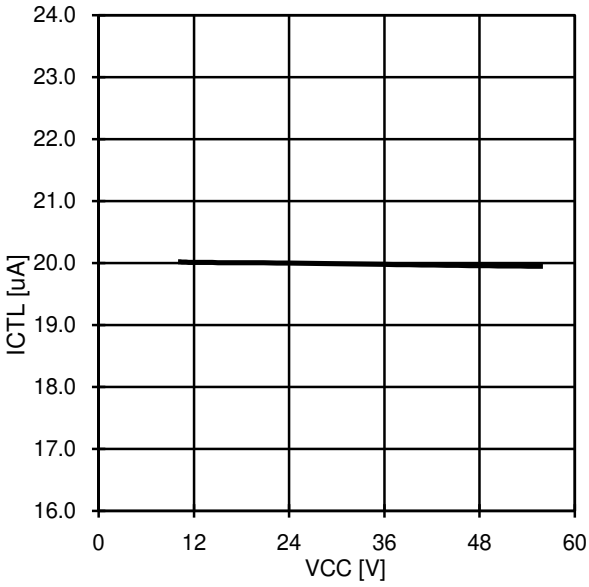



Fig.12 UVLO Hysteresis Current-VCC

● **Typical Performance Curves 4**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

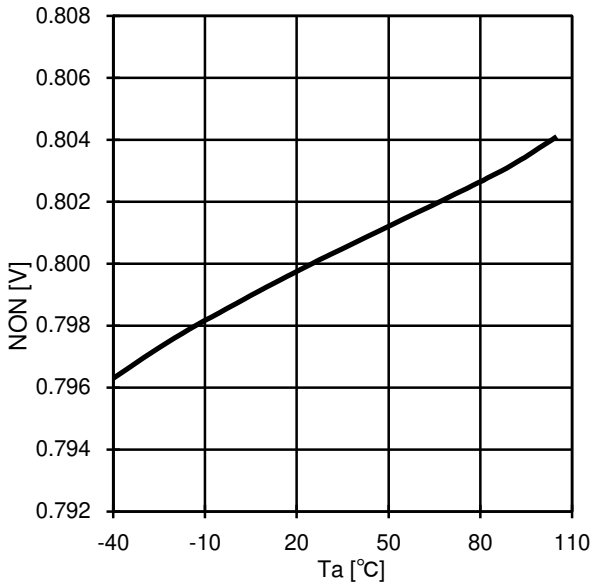



Fig.13 Reference Voltage-Ta

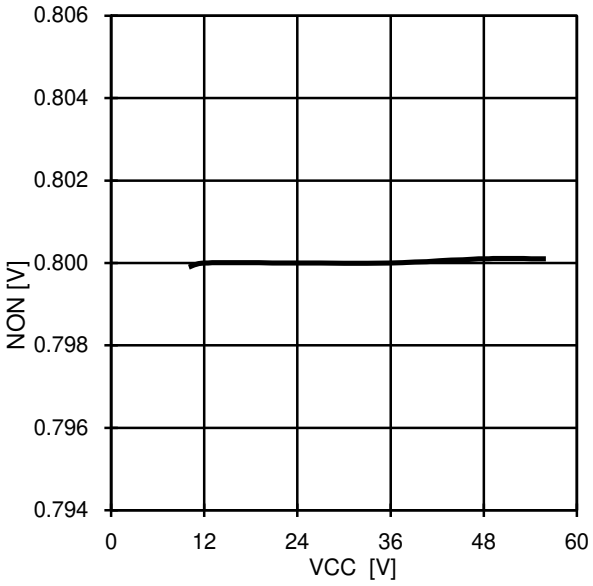



Fig.14 Reference Voltage-VCC

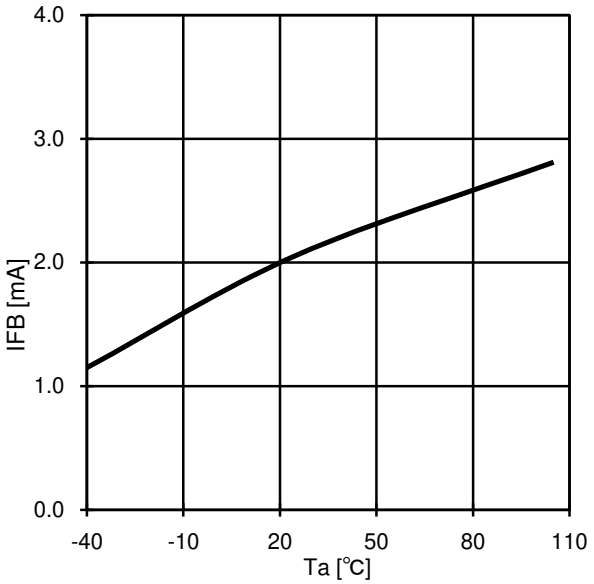



Fig.15 FB Sink current-Ta

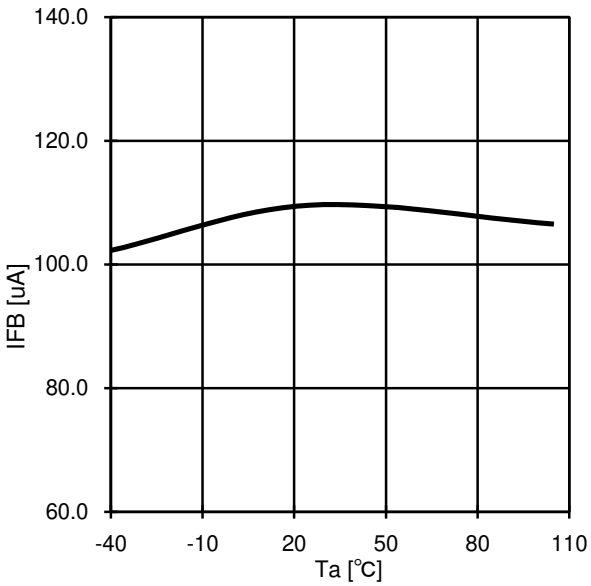



Fig.16 FB Source current-Ta

● **Typical Performance Curves 5**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

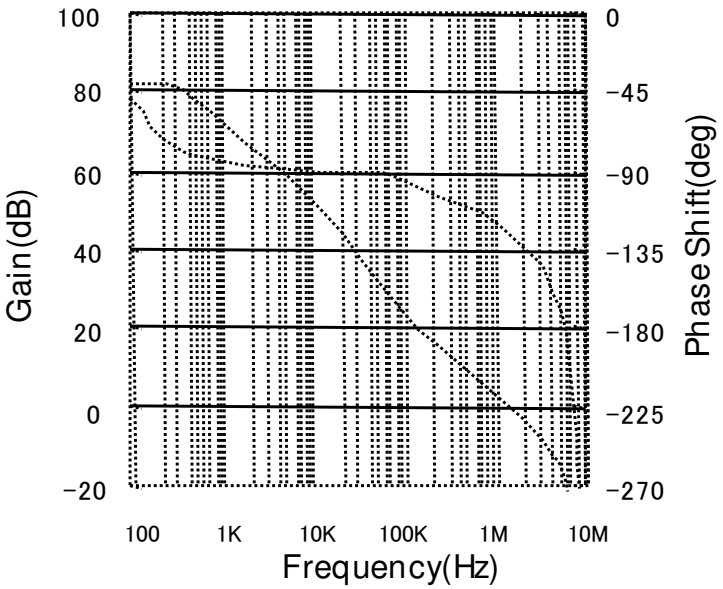



Fig.17 Error Amp Response-Frequency

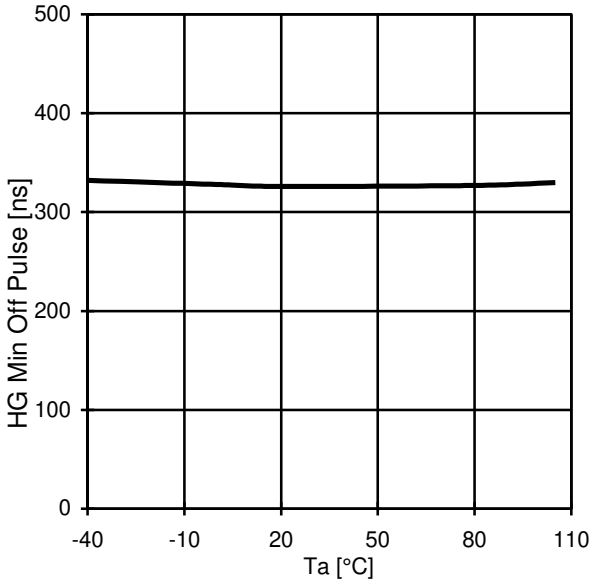



Fig.18 HG Min Off Pulse-Ta

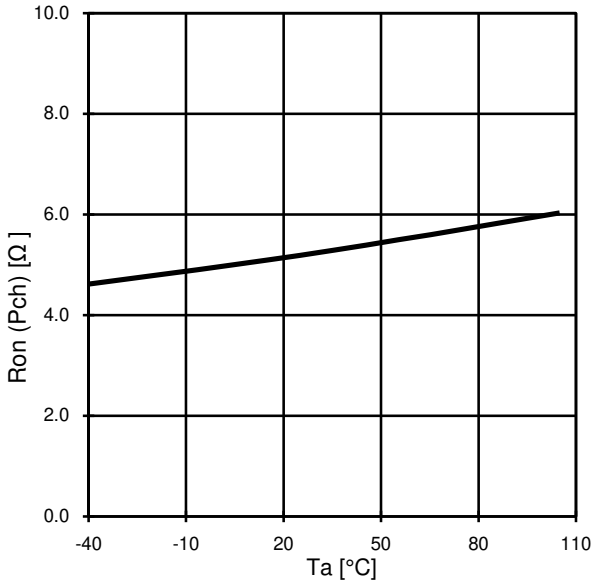



Fig.19 FET Ron –Ta (Pch)

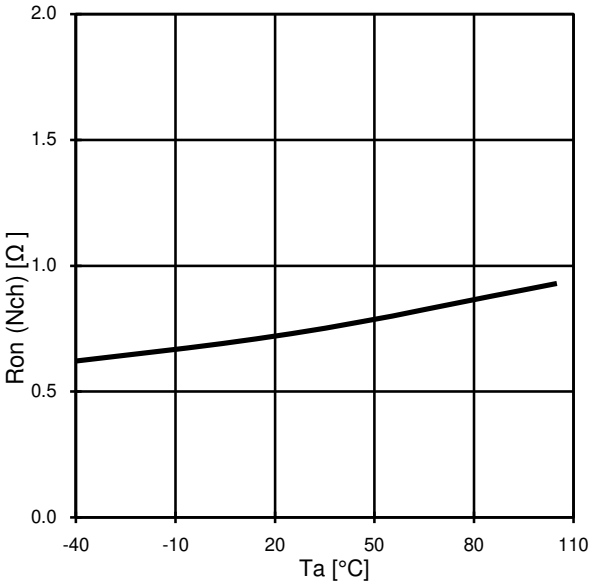



Fig.20 FET Ron –Ta (Nch)

● **Typical Performance Curves 6**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

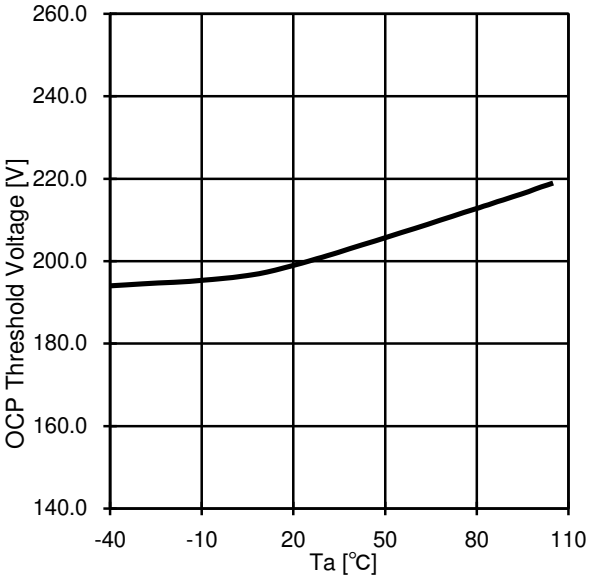



Fig.21 OCP Threshold Voltage-Ta

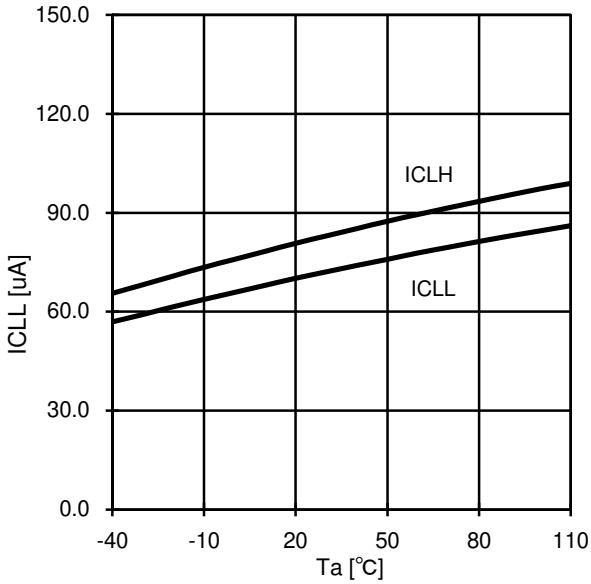



Fig.22 ICLH, ICLL-Ta

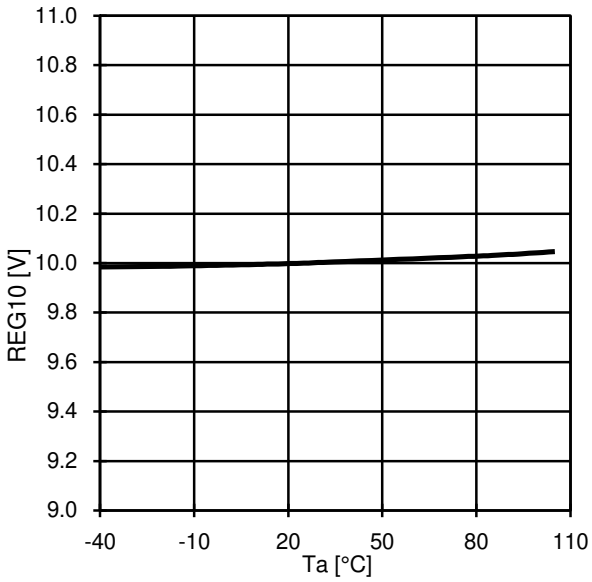



Fig.23 REG10-Ta

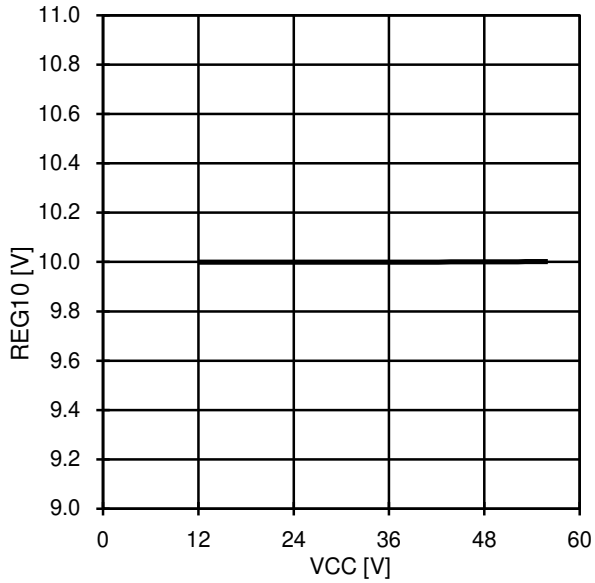



Fig.24 REG10 Line Regulation

● **Typical Performance Curves 7**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

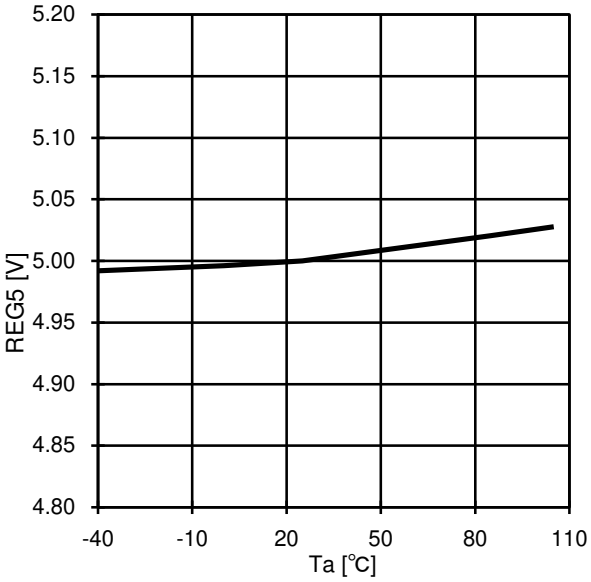



Fig.25 REG5-Ta

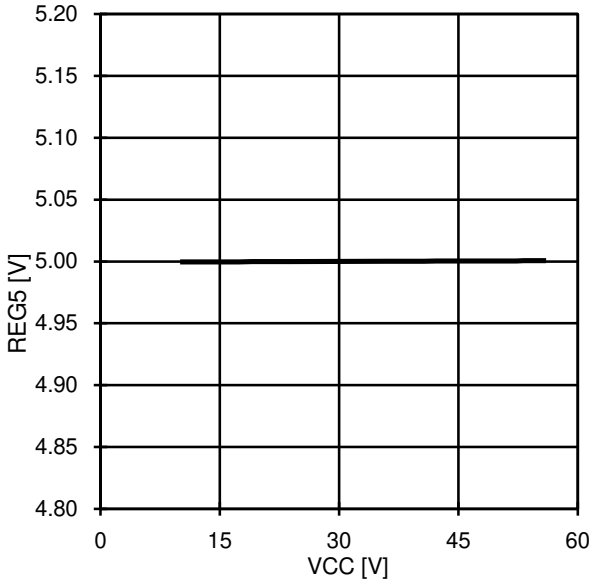



Fig.26 REG5-VCC

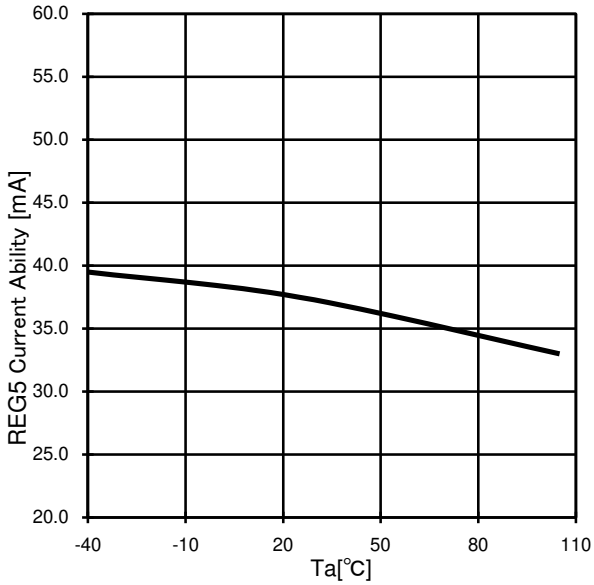



Fig.27 REG5 Current Ability -Ta

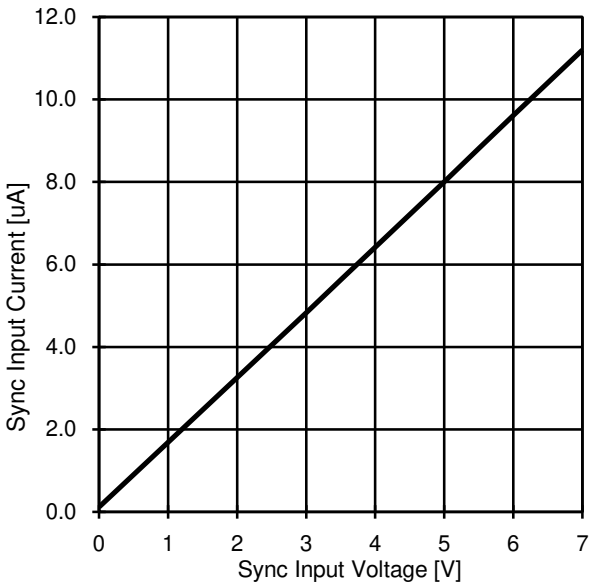



Fig.28 ISYNC-VSYNC

● **Typical Performance Curves 8**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

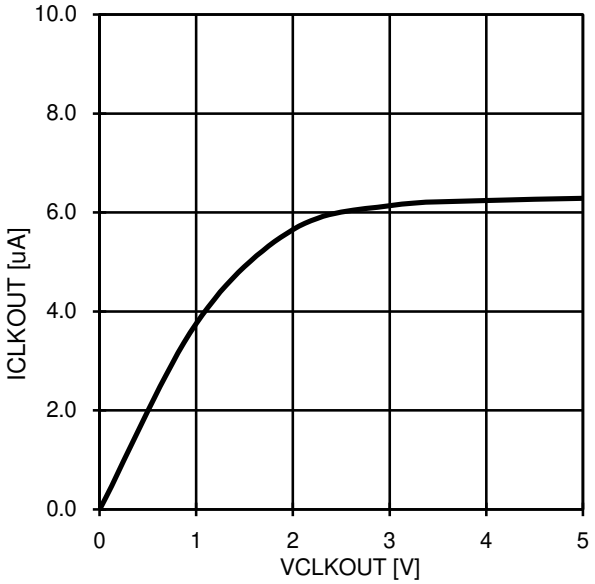



Fig.29 CLKOUT Sink Current - VCLKOUT

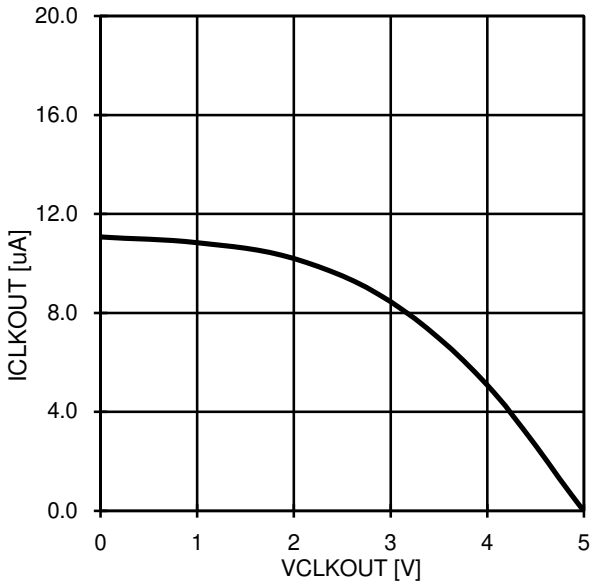



Fig.30 CLKOUT Source Current - VCLKOUT

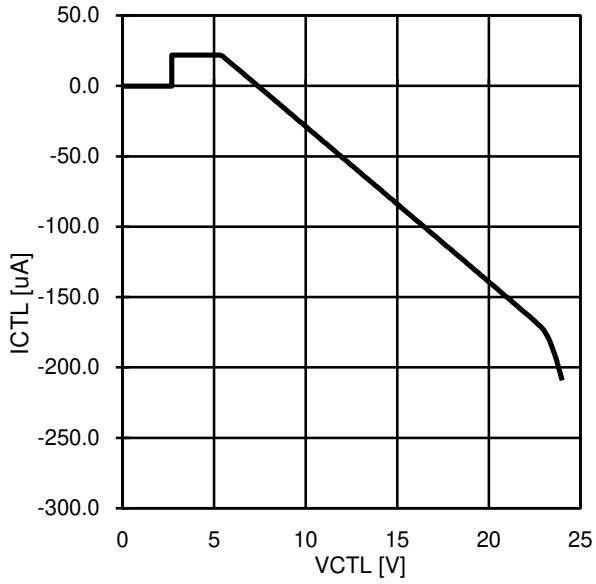



Fig.31 ICTL-VCTL

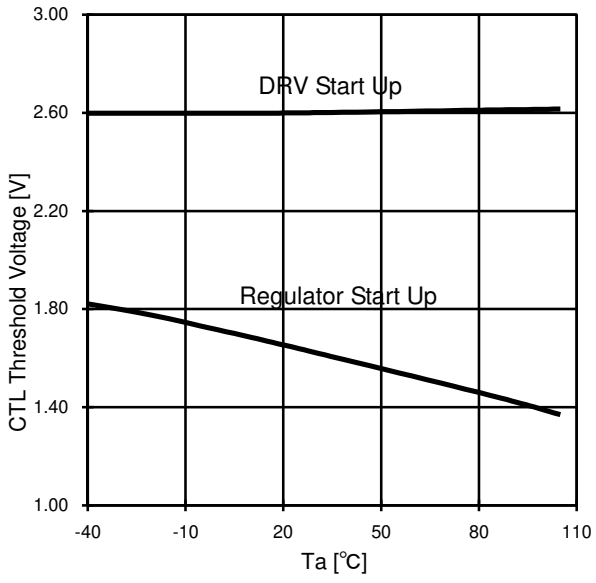



Fig.32 CTL Threshold Voltage -Ta

● **Typical Performance Curves 9**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

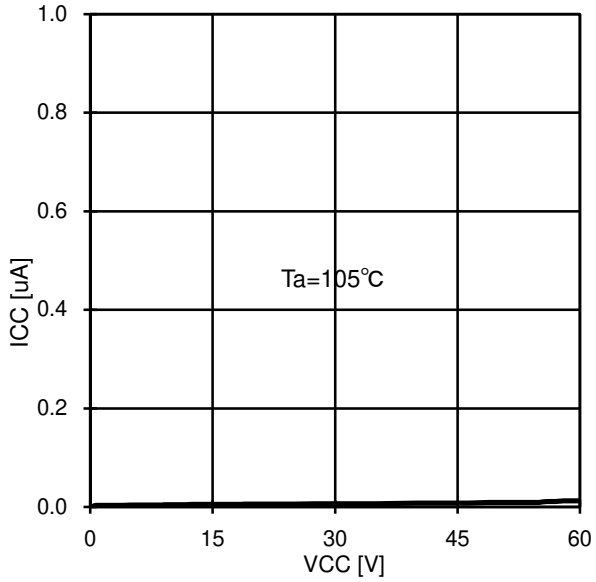



Fig.33 Stand-by Current -VCC

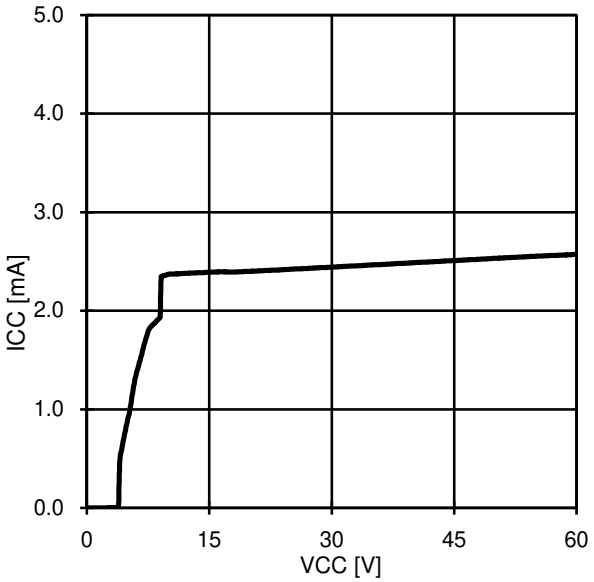



Fig.34 Quiescent Current -VCC

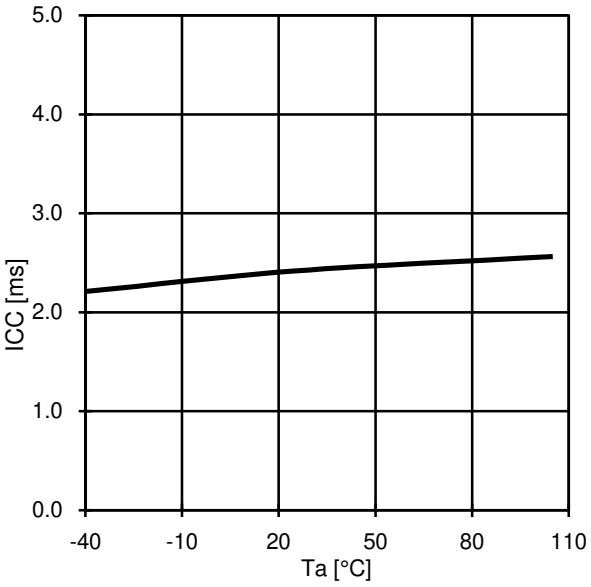
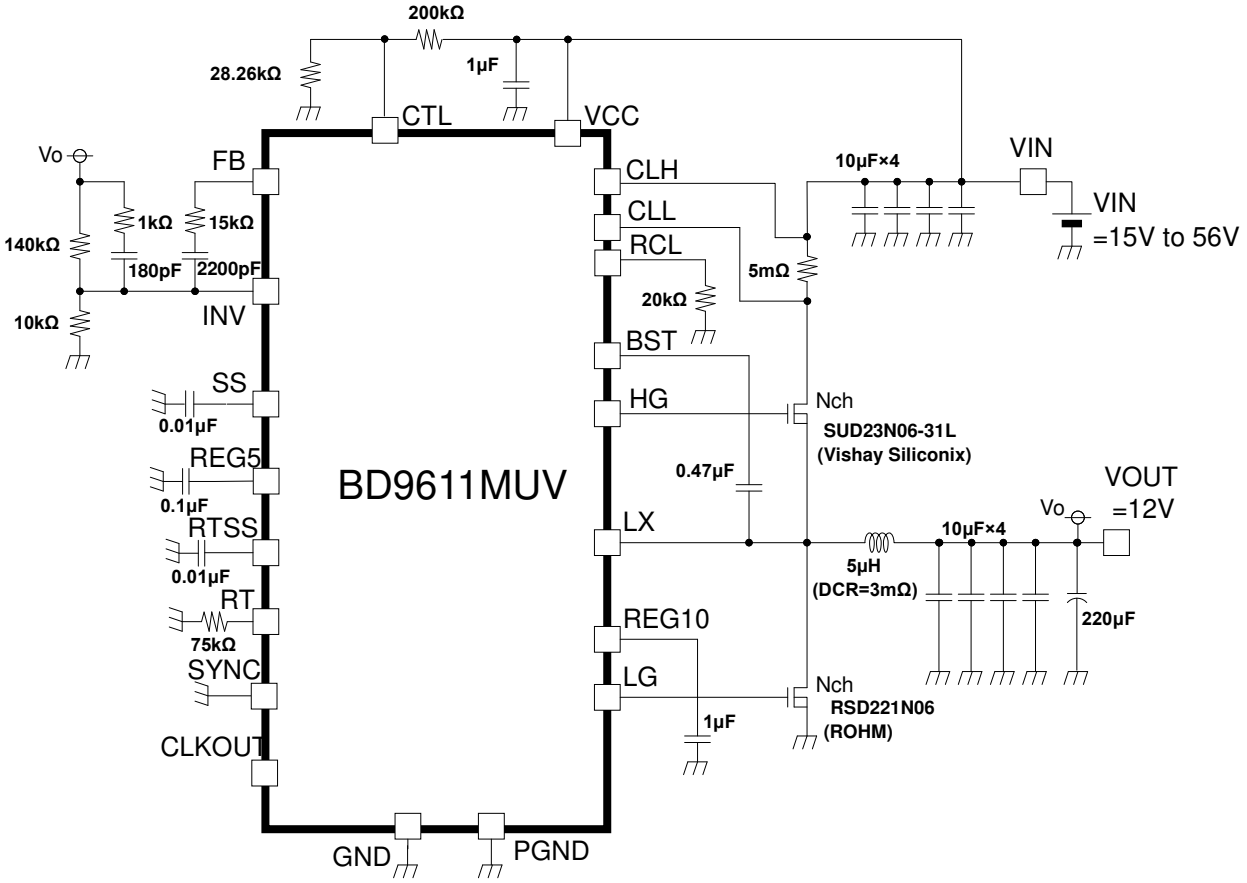



Fig.35 Quiescent Current -Ta

● **Reference Application (Vo=12V/ Io=10A)**




● **Reference Application data**
(VCC=34V, Vo=12V, Ta=25℃)

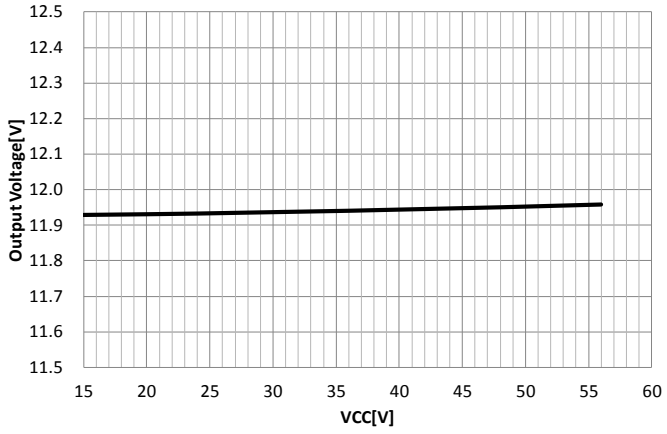



Fig.36 Line Regulation
(Io=10A)

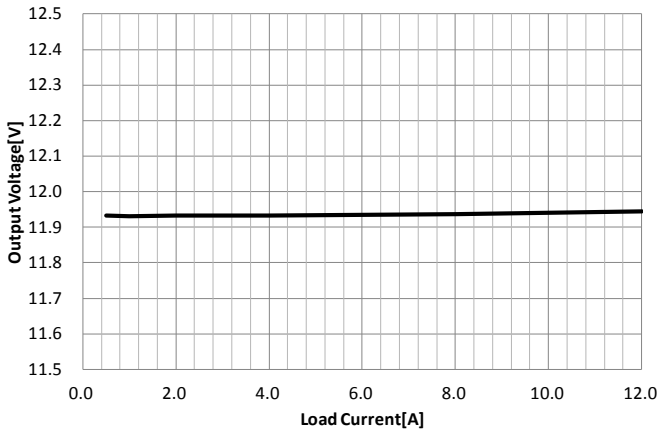



Fig.37 Load Regulation
(VCC=34V)

● **Reference Application data**
(VCC=34V, Vo=12V, Ta=25℃)

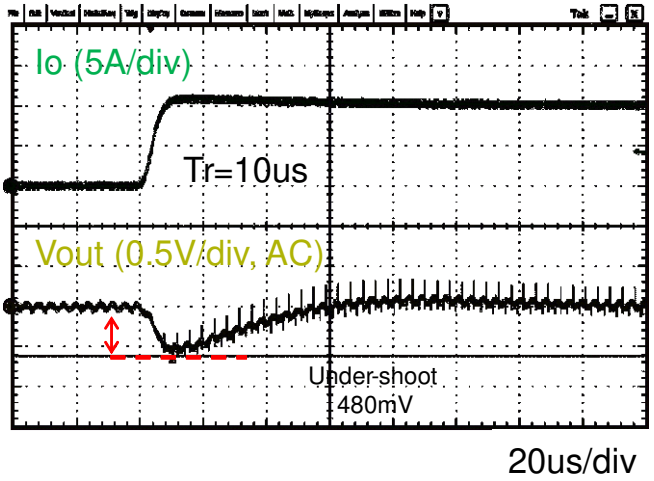



Fig.38 Load Response (Io=0A→10A)

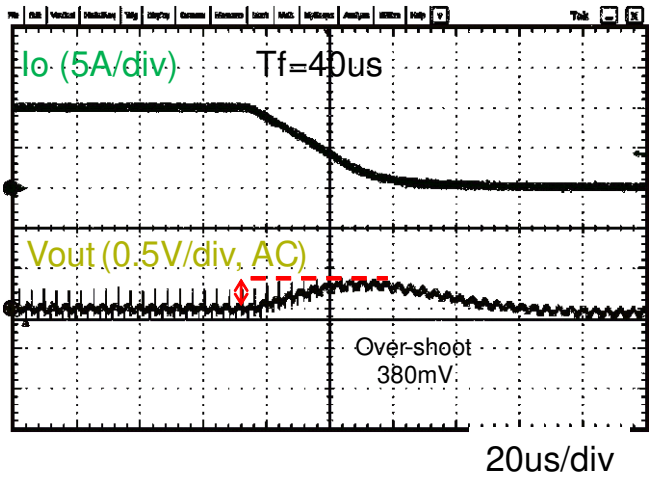



Fig.39 Load Response (Io=10A→0A)

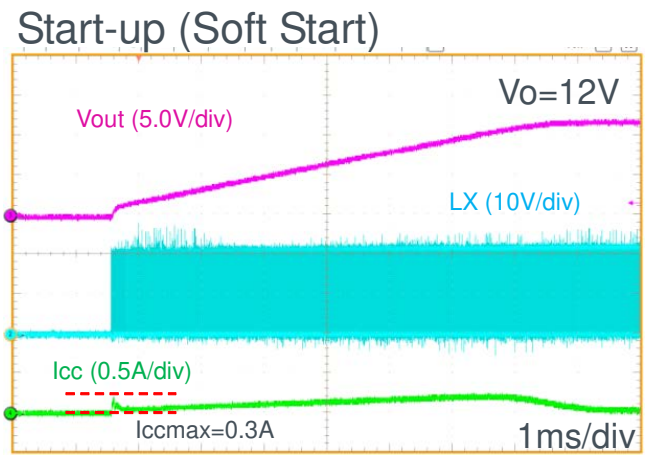



Fig.40 Start-up Waves (Soft Start)

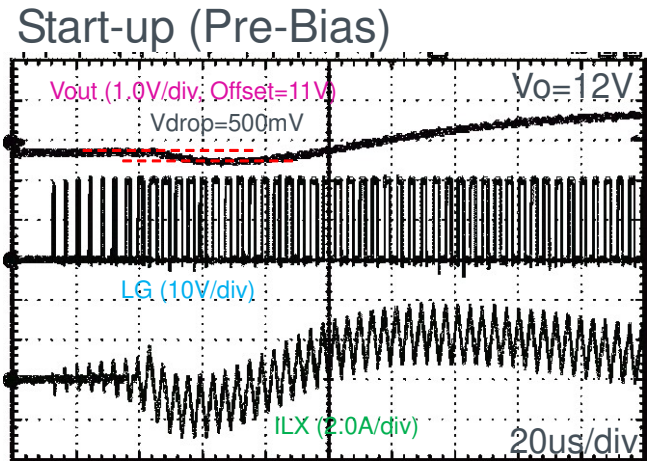



Fig.41 Start-up Waves (Pre-Bias)

● Function Description

(1) REG5 REGULATOR

REG5 is used as an internal power supply and reference voltage. Its maximum load should be less than 2mA.
Please connect a ceramic capacitor (CREG5=0.1uF) between REG5 and GND.

(2) REG10 REGULATOR

This is a regulator for the low-side DRV. It also charges the external BST-LX capacitor through an internal FET switch.
Please connect a ceramic capacitor (CREG10=1.0uF) between REG10 and GND.
When REG10 pin is shorted to GND, its short circuit detection function limits the load current to 20mA.

(3) SOFT START

To prevent in-rush current or overshoot, a reference voltage is ramped at startup.
The reference voltage comes from the voltage generated across capacitor CSS connected to the SS pin.
A ramp voltage is generated at this pin as CSS is charged by an internal constant current source (ISS=1uA).
Soft-start time (tss) is defined as the time it takes for the SS voltage to reach 0.8V:

$$tss = (CSS \times VNON) / ISS$$

(Ex.) CSS=0.01uF → tss = (0.01uF × 0.8V) / 1uA = 8 [ms]

Before soft start begins, the start-up time for RTSS takes first as described next.

(4) OSCILLATOR (RT, RTSS, CLKOUT)

The switching frequency of the oscillator is set by an external resistor RRT that is connected to pin RT and ground.
The clock frequency FOSC is related to RRT as shown in Figure 42 and is defined by the equation below.
Note that the amplitude of the generated triangle wave of the oscillator is 1.5V to 2V.

$$FOSC = 15900 \times RRT^{-0.955} \text{ [kHz]}$$ （RRT: RT resistor [kΩ] ）

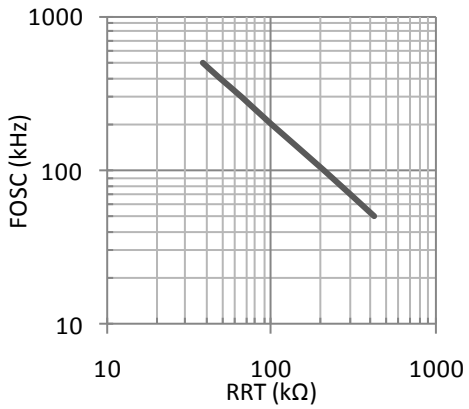



Fig.42 Switching Frequency vs RRT Resistance

In case external synchronization is not used, the RTSS terminal outputs the internal reference voltage (0.5V) through its internal voltage buffer. Terminal RT outputs the buffer of the RTSS voltage.
A 0.01uF ceramic capacitor (CRTSS) should be connected from terminal RTSS to ground.

When the UVLO is about to be released, the RTSS pin is quickly charged up to VRTSS=0.45V by an internal current source (IRTSS=100uA) due to pre-charge function. CRTSS is later discharged during UVLO.
If the voltage of pin RTSS reaches 0.45V, the UVLO is released and soft start function is started.
The CRTSS charging time (TRTSS) is the time it takes before CSS is charged at start-up of DC/DC operation.
TRTSS is given by:

(ex.) CRTSS=0.01uF
TRTSS= (0.01uF × 0.50V) / 100uA = 50 [us]

The CLKOUT pin outputs a square wave synchronized to the internal oscillator.
CLKOUT is intended to serve as clock for synchronizing master-slave configurations.

(5) EXTERNAL SYNCHRONIZATION (SYNC)

This IC can be synchronized to an external clock through the SYNC pin for noise management. It can either be used as a Master IC which outputs a clock signal through the CLKOUT terminal, or as a Slave IC which accepts an input clock signal through the SYNC terminal. The SYNC pin is connected to GND when the IC is not configured as Slave.

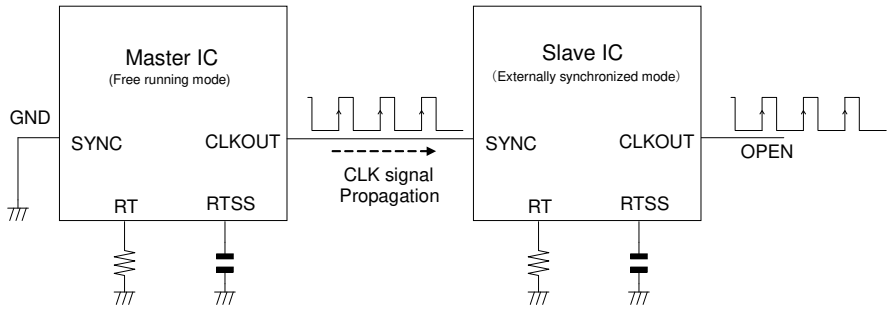



Fig.43 Example of an External Synchronization Circuit

Synchronization happens after three consecutive rising edges at the SYNC terminal. The clock frequency at the SYNC pin replaces the master clock generated by the internal oscillator circuit.
Pulling the SYNC pin low configures the BD9611MUV to freely run at the frequency programmed by RRT.

◆ Input Wave Conditions into the SYNC Pin

The synchronization frequency should be in the range of -10% to +10% in relation to the programmed free-run frequency, that is within the range of 50 to 500kHz. The input pulse width should be more than 500ns and its high level should be within 2.8V to 5.0V. There is no special sequence against VCC or CTL. Please refer to the discussion of RRT vs Frequency from the previous page in deciding the RT resistor value to be used when using fixed-frequency input signal into SYNC.

It is recommended to decide whether the BD9611MUV synchronizing function is used or not before start-up.
If synchronization is done after start-up, please consider the fluctuation of Vout caused by the momentary instability of oscillation. When the SYNC pin becomes open, the oscillator state is changed from synchronized mode to free-run mode after eight consecutive pulses had not been detected. The BD9611MUV operating frequency will gradually change to the free-run frequency programmed by RRT. The speed of transition depends on how fast the RTSS voltage stabilize to 0.5V by charging or discharging CRTSS with IRTSS (=5uA max). The frequency changes as RTSS shifts.
The RT voltage is fixed to almost 0.5V during free-run mode. In synchronized mode, the RT voltage adjusts freely between 0.25V and 1.0V for the oscillator to be able to output the synchronized frequency. The movement of the RT voltage is smoothed out by CRTSS. When the capacitance of the CRTSS is too small, the frequency fluctuates. However, if the capacitance is too large, it takes longer to synchronize the frequency. CRTSS should be adjusted accordingly to the intended circuit behavior.

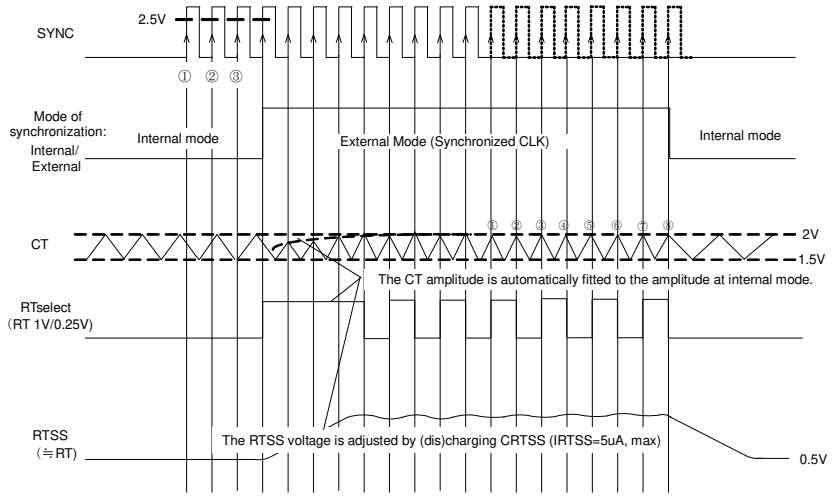



Fig.44 Timing Chart of External Synchronization

(6) PWM / BOOST (PRE-CHARGE MODE)

Charging capacitor CBST (BST-LX) is needed to drive the high-side N-channel FET.
CBST is charged to the voltage of REG10 through the internal FET switch between REG10 and BST, whenever the low side external FET is turned on.
The maximum on duty does not reach 100% because of the LG minimum ON pulse. It is possible to charge CBST even if the voltage of the FB pin is over 2.0V (high voltage of the internal ramp wave) and for terminal HG to always output HIGH. In case the voltage values of Vin and Vout are becoming close, the voltage of Vout can never become equal to the voltage of the Vin.

※ MAX DUTY

BD9611MUV turns off for almost 350nsec at every turn. This is the High-side Min Off Pulse (HGmin).
The 350ns duration of HGMIN consists of the LG Min pulse (about 100ns) and the anti-cross conduction time between HG and LG (100ns each).
The Max ON Duty is calculated in the following equation:

$D(on) = (T - Toff) / T$ Where: T: Switching Cycle (=1/FOSC), Toff: OFF time (≒350ns Typ)

※ PRE-CHARGE MODE

The BD9611MUV operates at pre-charge mode during the time when CBST is charged at start-up. By dropping the voltage of CBST and releasing the protect functions (UVLO, TSD, OCP hiccup-mode), CBST is charged in advance. In this mode, capacitor CBST is charged by the LG ON pulse which is limited to almost 300ns at every cycle.
Pre-charge mode changes to normal switching mode after the release threshold of BSTUVLO had been detected.

(7) STAND-BY

It is possible to make the quiescent current value go as low as 0uA by turning off the IC using the CTL pin.
All IC functions such as REG5 and REG10 are terminated in this mode.

(8) UVLO

The UVLO circuits shut down HG, LG, SS and FB, when the voltage of any of the three supplies VCC, REG10 or REG5 are under their respective UVLO threshold (VCC<9V, REG10<8V, REG5<4.5V). Voltage hysteresis is also present for the supplies VCC, REG10 and REG5 (VCC: 0.5V, REG10: 0.5V, REG5: 0.2V). Whenever the UVLO is released, soft-start begins after the voltage of RTSS is over 0.5V. In case quick start-up is needed, please adjust the capacitance of CRTSS accordingly.
BST_UVLO protection exists between BST and LX. When the BST_UVLO threshold is detected, HG, SS and FB are all shut down, then BD9611MUV shifts to pre-charge mode where CBST is charged every LG pulse (t≅300ns).

(9) TSD

TSD is the protection of the IC against abnormal temperature, which starts at temperature greater than $T_{JMAX}$ (150°C). The TSD gets triggered at almost 175°C, so it doesn't work in the normal operating temperature range. TSD is automatically released after being cooled back to 150°C or lower. Under TSD protection, HG, LG, SS and FB are all shut down similar to UVLO.

(10) LG short protection

When the LG pin short to GND, an exceptional large current flow occurs in BD9611MUV.
(Reason: The DC/DC is able to output under diode-rectifier mode by the body diode of the low side Nch-FET.)
For this case, BD9611MUV checks after the PWM low output in every cycle before turning on LG. If LG doesn't turn on, the DC/DC will be shut down.

(11) PROGRAMING OCP

This IC monitors the voltage between CLH and CLL when turning on the High-side driver (HG=ON).
When this voltage exceeds the threshold as configured by RRCL, the output is turned off immediately.
The switching current is monitored using the current sense resistor Rs, which is usually connected to the drain of the high-side FET.

The value of the OCP current is determined by the following:

$$IOCP = VOCPTH / Rs \quad (8)$$

IOCP：OCP trigger current
VOCPTH：OCP threshold voltage between CLH and CLL configured using RCL
Rs：Current sense resistor

The OCP threshold is set by the resistor RRCL connected from terminal RCL to ground.
Please refer to the graph below:
Using RRCL>12.5kΩ, take into consideration the increase of OCP variability.

$$VOCPTH = (0.8 / RRCL) \times 1850 \ [mV]$$ RRCL: Resistor connected to the RCL pin [kΩ]

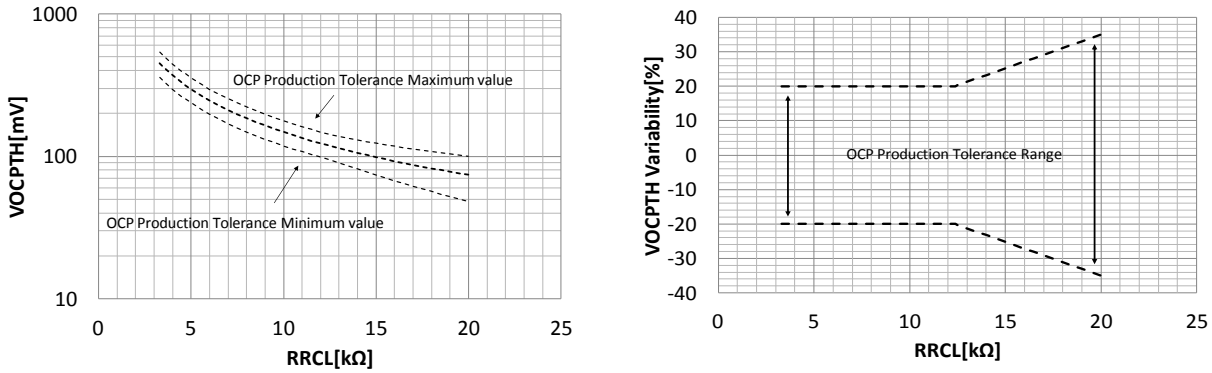



Fig.45 OCP Threshold vs RRCL

Resistor Rs senses the OCP voltage and is connected between VCC and the drain of the High-side Nch-FET.
It is recommended that sensing be improved by using an RC filter between CLH and CLL as shown Figure 46.
This filter should be available for response stability in controlling detected variation. Ensure that CLH and CLL are not connected to traces subjected to common impedance, such as when connecting it to the large-current trace far from either side of Rs. The RC filter is connected between CLH, CLL and at either ends of Rs. It is comprised of Cocp and Rocp as shown below. The impedance of Cocp should be the lowest possible under noise frequency (adjust noise frequency and self-resonant frequency if needed) and should maintain a fixed filter constant with Rocp.

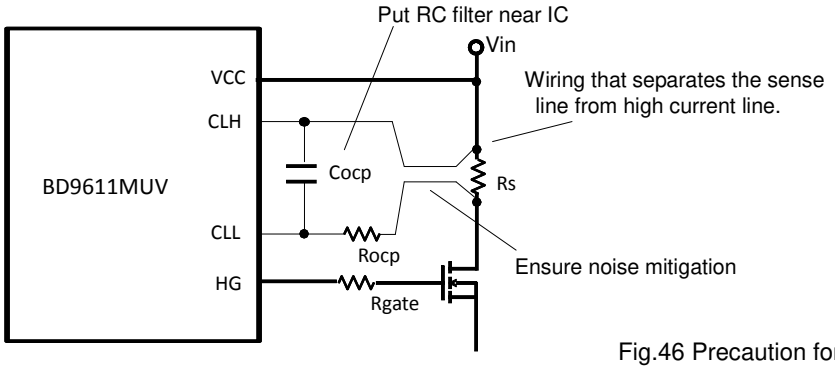



Fig.46 Precaution for CLH, CLL filter

Please take into consideration the ON resistance of the external FET and the wiring pattern when setting up OCP.
Due to variable FET ON resistance and large switching noise, false over-current detection might happen.

Please connect CLH to the VCC line and CLL to the line which connects to LX when the FET is on.

Connect RCL to REG5 and CLH/CLL to VCC without using the shortest lines with high common impedance.

＜Pulse by Pulse Protection＞
The over-current detection of OCP initially does not work for almost 60ns due to the blanking time against LX ringing noise. It also has an action delay time of almost 140ns after over-current is detected.
When the switching frequency and the ratio of Vin and Vout are both high, this IC might not detect over-current. Please take into consideration the minimum pulse width and refer to the graph of item no (13) “About Output programmed voltage range”.

＜Hiccup Protection＞
When over-current is detected twice in either two or three consecutive pulses, the outputs FB and SS are turned off within the specified OCP shut-down hold cycles (equivalent to 32768 clock cycles).
(ex.) FOSC = 300kHz

$$\text{OCP shut-down hold cycles (THICCUP)} = T = (1 / FOSC) \times 32768$$
$$= (1 / 300k) \times 32768 = 108\ [ms]$$

At the end of the OCP shut-down hold cycles, the soft start procedure begins automatically.

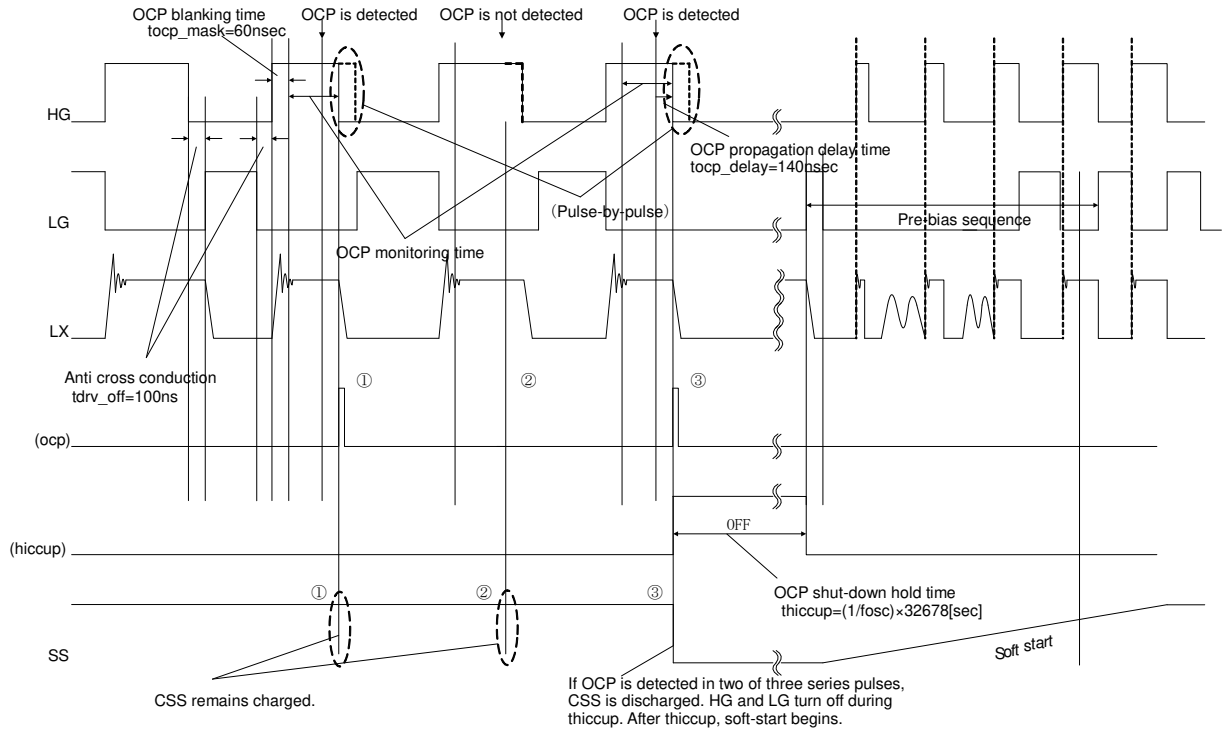



Fig.47 OCP Timing Chart (※To explain the sequences, the time axis of this graph is not scaled to actual)

(12) PRE-BIAS

This IC is designed not to sink large current from Vout, even if Vout had been biased at high voltage upon startup. However, there is a potential of an increase in output voltage through Body-Di of BST, during the charge cycle of switching. This happens when the programmed output voltage is under 10V.
To prevent this, connect a load resistor between Vo and PGND to serve as discharge path when using Vo<10V. Please use the table in Figure 49 as reference in choosing the discharge resistance value.
This issue does not exist when Vo≧10V.

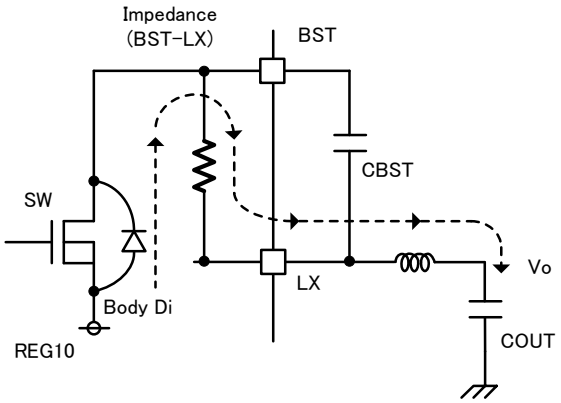
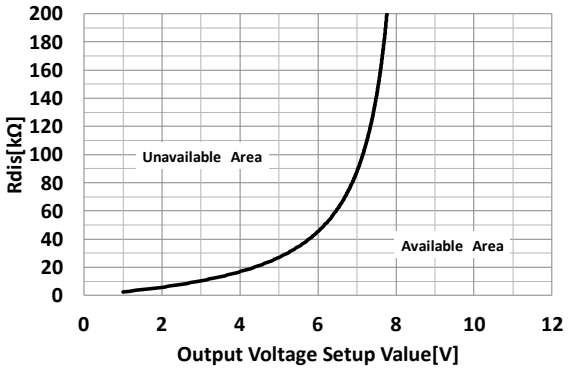



Fig.48 Current Passes Through PRE-BIAS at Low Output Voltage Setting




| Vo[V] | Rdis[kΩ] |
|---|---|
| 1.0 | 2.5 |
| 2.0 | 6.5 |
| 3.0 | 10.5 |
| 3.3 | 12.0 |
| 4.0 | 17.0 |
| 5.0 | 27.0 |
| 6.0 | 45.5 |
| 7.0 | 88.5 |
| 8.0 | 302.0 |

Fig.49 Output Voltage Setting vs Load Resistance

(13) Programmed Output Voltage Range

This IC's programmable output voltage is limited to the available area shown on Figure 50. In application, the programmable output voltage is restricted from the unavailable area on the graphs due to input-voltage, frequency, high-side minimum off pulse and load current.

◆ Relation Between Frequency and Input-Output Voltage Ratio

This IC has a limitation in programmed output voltage as shown on the following graphs due to the minimum pulse available for feedback control and programmed OCP detect voltage.

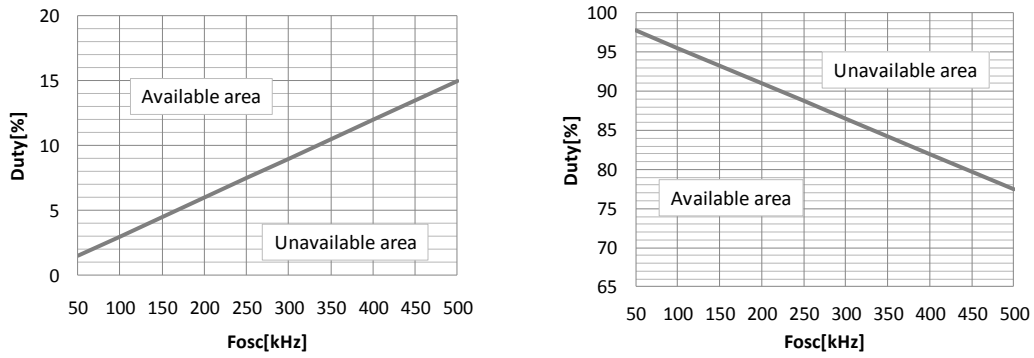



Fig.50 Frequency vs Input-Output Voltage Ratio (Duty)

◆ High-side (HG) Minimum Off Pulse

This IC has a limitation in programmed output voltage due to the Hi-side Minimum Off Pulse for charging BST capacitor (CBST) which adopts the Bootstrap system.

Consider toff=450ns as the OFF duty pulse.

In cases where the configured output voltage is near the input value, the output voltage gets affected by this off pulse.

Take into consideration the reduced output voltage limit when the programmed output voltage is near input value.

For example:

Programmed output voltage: Vo = 12V, Frequency: f = 250kHz (T = 1/f = 4us)

OFF_Duty = 1 – (Vo / Vin), Minimum OFF pulse: toff_min = T × OFF_Duty

toff_min = T × (1 - Vo /Vin) = 4us × (1 – 12V / Vin) ≧ 450ns → Vin ≧14.95V

It is necessary that the condition Vin ≧ 14.95V is satisfied to ensure that the programmed output Vo = 12V is reached.

Additionally, take into consideration the Ron voltage drop of the high-side FET, the DCR of coil and the PCB pattern impedance.

◆ Load current

There are no limitations on the load current when the programmed output voltage holds the condition Vo ≧ 10V.

However, certain limitations are imposed when Vout is under 10V because of the Pre-bias sequence.

Please refer to No. (12) PRE-BIAS on page 24.