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ROHM Switching Regulator Solutions

Synchronous Buck Converter Controller

BD9611MUV-EVK-001

Description

Using a synchronous rectified step-down DC/DC converter IC BD9611MUV BD 9611MUV-EVK-001 evaluation board 15.0 V ~ output a 24 V input voltage 12.0 V. Provides 10.0A output current. Output current is possible with current settings by selecting high rated current FET and coil. You can adjust the loop characteristics by phase compensation components, can set the output voltage to change the IC external parts.

Evaluation Board Operating Limits and Absolute Maximum Ratings (This is not typical and the characteristics)

Unless otherwise specified : $V_{IN} = 24V$, $V_{OUT} = 12.0V$, $I_{out}=6A$

| Parameter | Min | Typ | Max | Units | Conditions |
|------------------------|-----|---------|---------------------|---------|---|
| Supply Voltage | 15 | | 36 | V | |
| Output Voltage | | 12.0 | | V | RU1=120k Ω , RU2=20k Ω , RD1=10k Ω |
| Output Voltage range | 1 | | $V_{IN} \times 0.8$ | V | |
| Output Current | 0 | | 10 | A | |
| Closed Loop Band Width | | 30.19 | | kHz | |
| Phase margin | | 130. 27 | | degrees | $I_{out}=8A$ |
| Soft Start Time | | 8 | | ms | |
| Operating frequency | | 250 | | kHz | |
| Maximum Efficiency | | 95.1 | | % | $I_O = 4A$ |

Evaluation Board Operation Procedures

1. Connect power supply's GND terminal to GND on the evaluation board.
2. Connect power supply's VCC terminal to Vcc test point on the evaluation board. This will provide VCC to the IC U1. Please note that the VCC should be in range of 10V to 56V.
3. The output voltage can be measured at the test point V_{OUT}. Now turn on the load. The load can be increased up to 10A MAX.

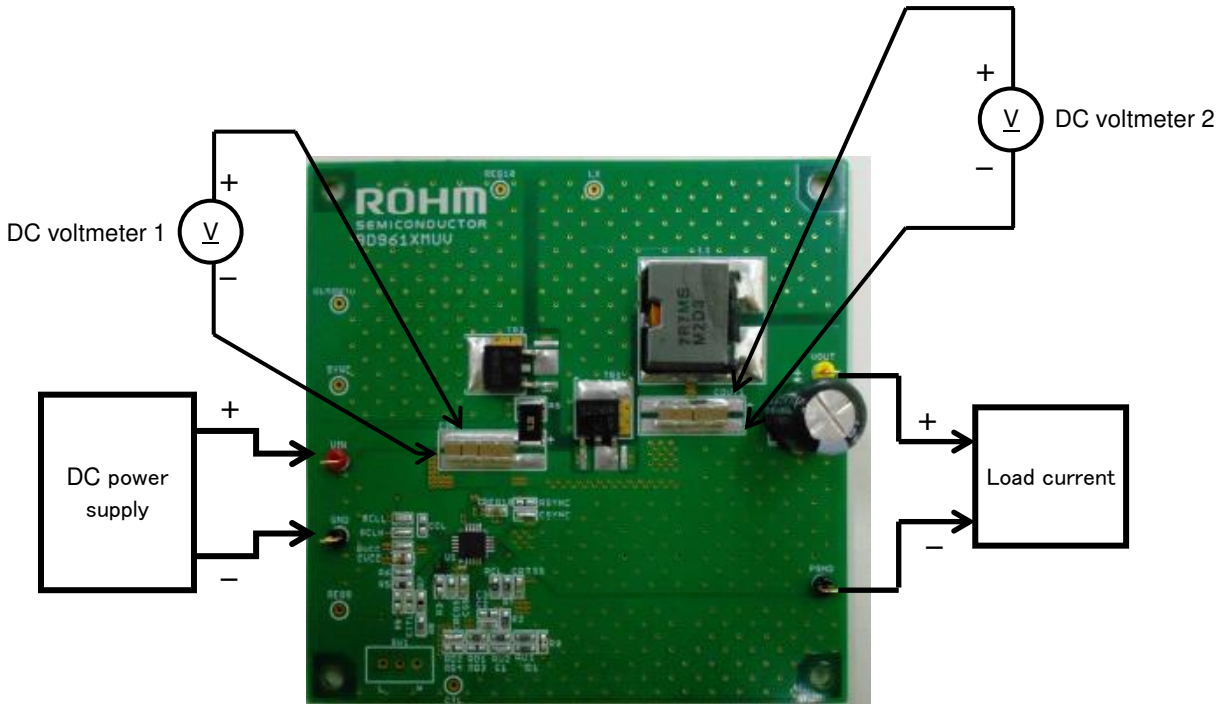


Figure 1. Evaluation board setup

Enable

You can switch between normal operation and standby mode to minimize power consumption by controlling the CTL of the IC (19 pin). Open to short and SW1 R9, as VIN pin resistance partial pressure using R5, R6, R7, R8, switch SW1 on the off side and in standby mode. Short between the middle and ON-side.

You can also by CTL pin and GND terminals of voltage to control and eliminate the R9 standby mode or normal behavior. CTL Terminal voltage is 2.6 V or less in standby mode: 2.6 V or more usually works. If CTL terminals directly controlling voltage hysteresis voltage at low current internal and external resistance is set so the hysteresis voltage voltage supplying CTL terminal by the impedance of the power supply and internal constant current.

Application circuit (V_{out}=12.0)

V_{IN} = 15.0V~30V, V_{OUT} = 12.0V

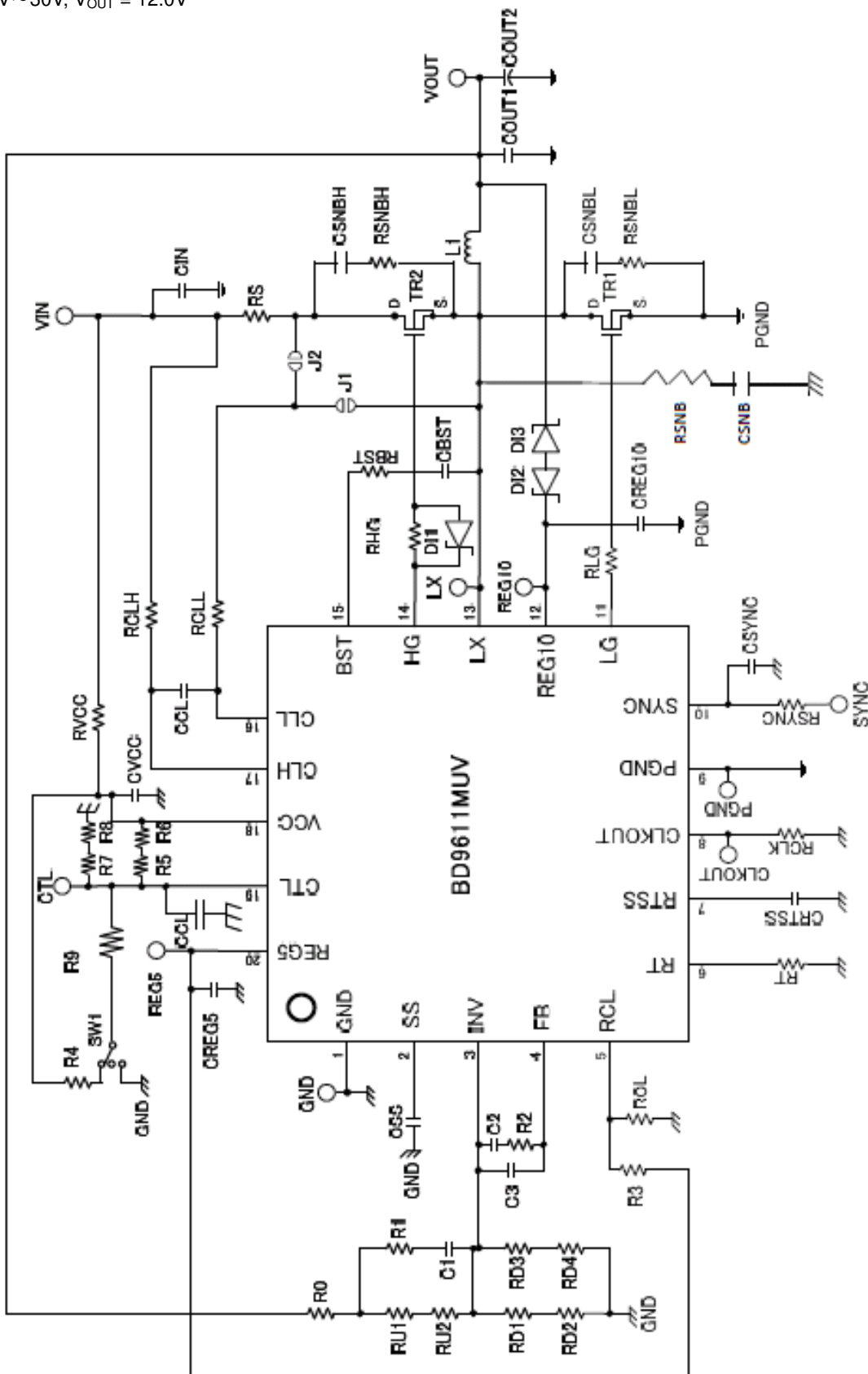


Figure 2. BD9611MUV-EVK-001 Application circuit

Evaluation Board BOM (Vout =12.0V)

| Item | Qty | Reference designator | Description | Manufacture | Parts number |
|------|-----|--|----------------------------------|-------------|--------------------|
| 1 | 1 | U1 | BD9611MUV | ROHM | BD9611MUV |
| 2 | 1 | R1 | RES 1K OHM 1/10W 1% 0603 SMD | ROHM | MCR03EZPFX1001 |
| 3 | 1 | R2 | RES 15K OHM 1/10W 1% 0603 SMD | ROHM | MCR03EZPFX1502 |
| 4 | 1 | R5 | RES 27K OHM 1/10W 1% 0603 SMD | ROHM | MCR03EZPFX2702 |
| 5 | 1 | R7 | RES 5.1K OHM 1/10W 1% 0603 SMD | ROHM | MCR03EZPFX5101 |
| 6 | 1 | R8 | RES 430 OHM 1/10W 1% 0603 SMD | ROHM | MCR03EZPFX4300 |
| 7 | 1 | RU1 | RES 120K OHM 1/10W 1% 0603 SMD | ROHM | MCR03EZPFX1203 |
| 8 | 2 | RU2, RCL | RES 20K OHM 1/10W 1% 0603 SMD | ROHM | MCR03EZPFX2002 |
| 9 | 1 | RD1 | RES 10K OHM 1/10W 1% 0603 SMD | ROHM | MCR03EZPFX1002 |
| 10 | 1 | RT | RES 75K OHM 1/10W 1% 0603 SMD | ROHM | MCR03EZPD7502 |
| 11 | 1 | RHG | RES 10 OHM 1/10W 1% 0603 SMD | ROHM | MCR03EZPFX10R0 |
| 12 | 2 | DI1, DI2 | RB161VA-20 | ROHM | RB161VA-20 |
| 13 | 1 | RS | RES 5m OHM 2W 1% 6432 SMD | ROHM | PMR100HZPFU5L00 |
| 14 | 1 | C1 | CAP CER 180PF 50V 5% NPO 0603 | MURATA | GRM1885C1H181JA01D |
| 15 | 1 | C2 | CAP CER 2200PF 50V 10% X7R 0603 | MURATA | GRM188R71H333KA01D |
| 16 | 2 | CSS, CRTSS | CAP CER 10000PF 16V 10% X7R 0603 | MURATA | GRM188R71C103KA01D |
| 17 | 1 | CREG10 | CAP CER 1UF 16V 10% X7R 0603 | MURATA | GRM188R71C105KA01D |
| 18 | 1 | CBST | CAP CER 0.47UF 25V 10% X7R 0603 | MURATA | GRM188R71E474KA12D |
| 19 | 4 | CIN | CAP CER 10UF 50V 10% X7R 3225 | MURATA | GRM32ER71H106KA12L |
| 20 | 1 | COUT1 | CAP ALUM 220UF 50V 20% RADIAL | nichicon | UVR1H221MPD1TD |
| 21 | 4 | COUT2 | CAP CER 10UF 50V 10% X7R 3225 | MURATA | GRM32ER71H106KA12L |
| 22 | 1 | CVCC | CAP CER 1UF 50V 10% X7R 2125 | MURATA | GRM21BB31H105KA12L |
| 23 | 1 | CREG5 | CAP CER 0.1UF 25V 10% X5R 0402 | MURATA | GRM155R61E104KA87D |
| 24 | 2 | Tr1, Tr2 | Nch-FET 60V 22A 20W 26mOHM | ROHM | RSD221N06TL |
| 25 | 1 | L1 | INDUCTOR POWER 7.7UH 10A SMD | Sumida | CDEP147NP-7R7MC-95 |
| 26 | 11 | R0, R6, RD2, RLG, RBST, RCLH, RCLL, RVCC, CSYNC, J2, DI3 | short | - | - |
| 27 | 10 | R3, R4, R9, RD3, RD4, C3 RCLK, RSYNC, CCL, J1 | open | - | - |

About the LX pin overshoot voltage measures snubber circuit

To LX pin voltage overshoot voltage by the parasitic inductance of the parasitic capacitance of the high-side and low-side FET and board layout pattern occurs. You need to use power supply voltage range and load range, and output short circuit during the LX pin voltage does not exceed the recommended operating range.

Snubber circuits described in Figure 2 overshoot LX pin voltage is greater if the LX pin and PGND between RSNB resistor and capacitor CSNB connected in series and set the to overshoot.

※CSNB is RSNB evaluation board pattern. We recommend placing the pattern during the overshoot occurs in the set assessment measures allow.

< matters to be attended to >

This article is not what 1 example of application BD9611MUV circuits and the operation.

Curve data

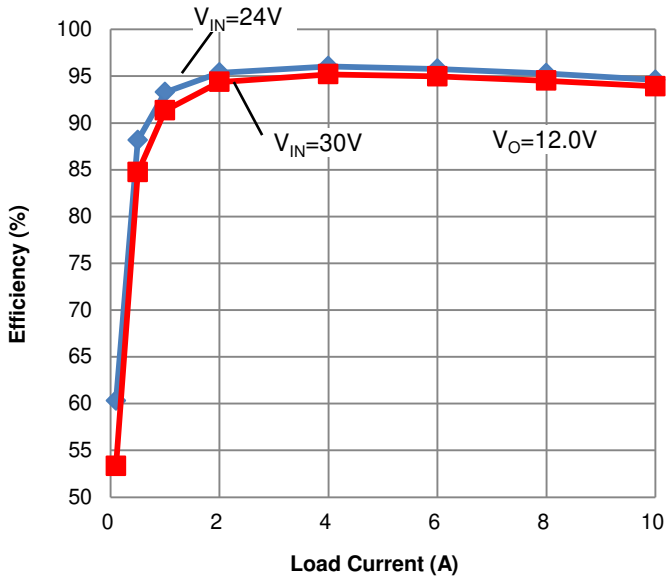


Figure 9. Efficiency-Load Current

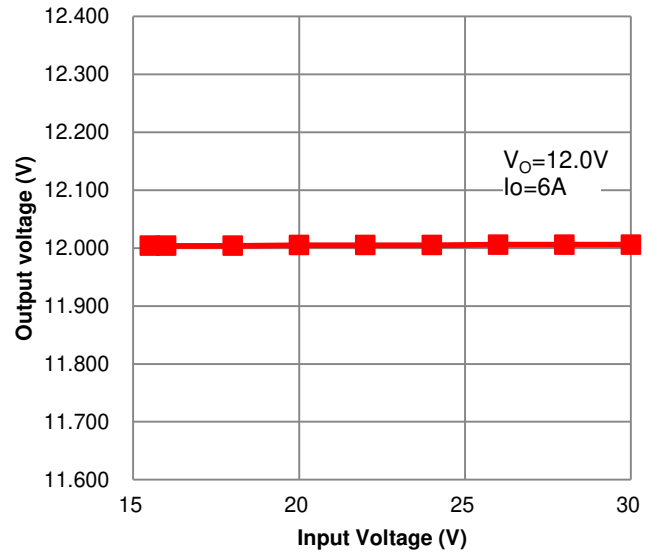


Figure 10. Line regulation

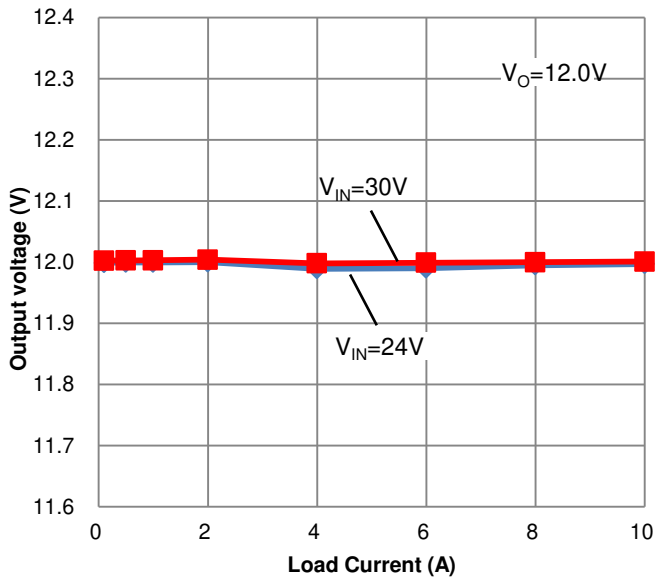


Figure 11. Load regulation

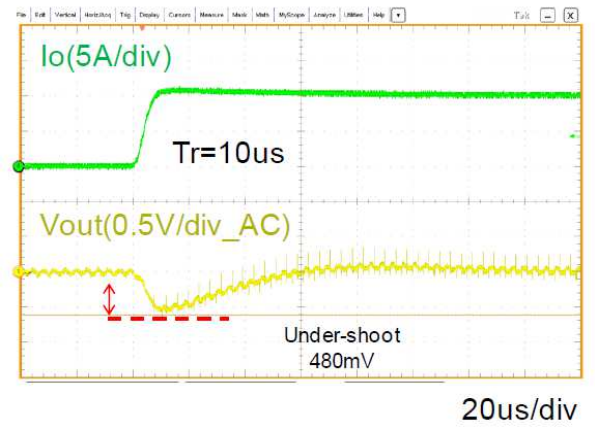


Figure 12. Load Response Characteristics
0A→10A

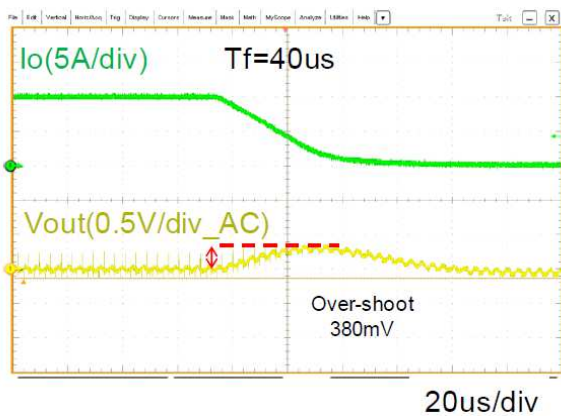


Figure 13. Load Response Characteristics
10A→0A

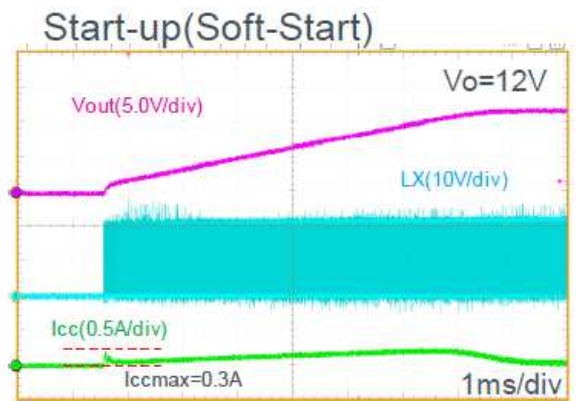


Figure 14. Start-up waves (Soft start)

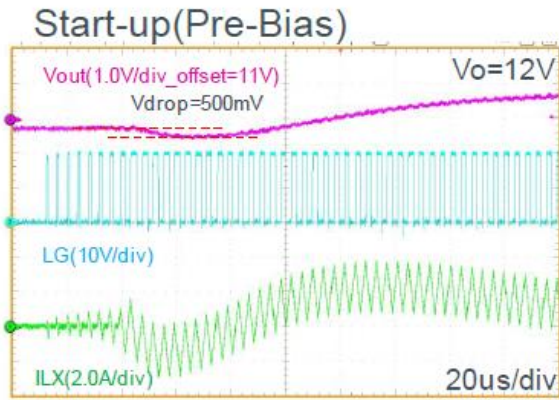


Figure 15. Start-up waves (Pre-bias)

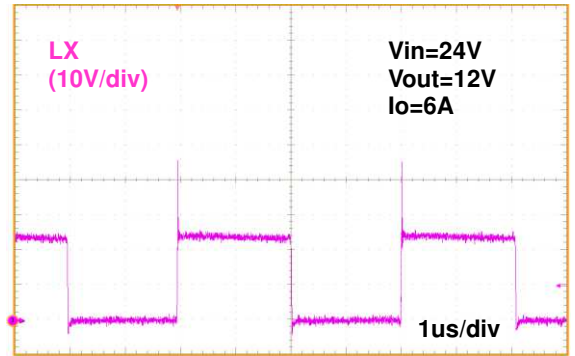


Figure 16. LX terminal waves

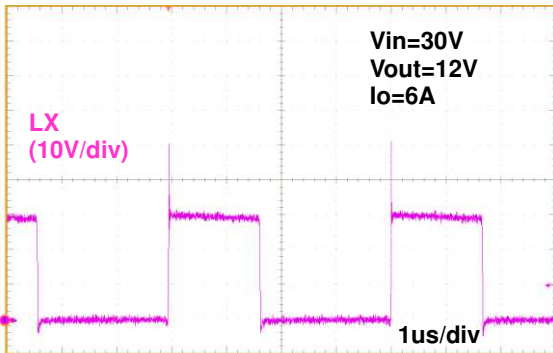


Figure 17. LX terminal waves

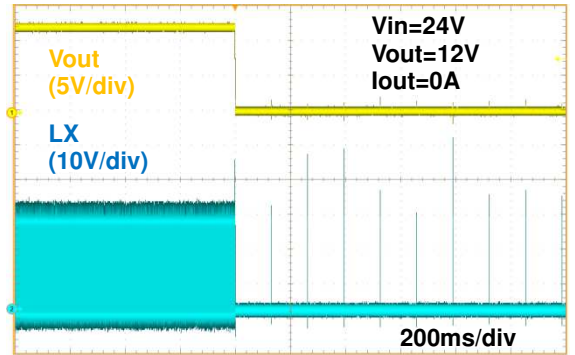


Figure 18. Output short waves

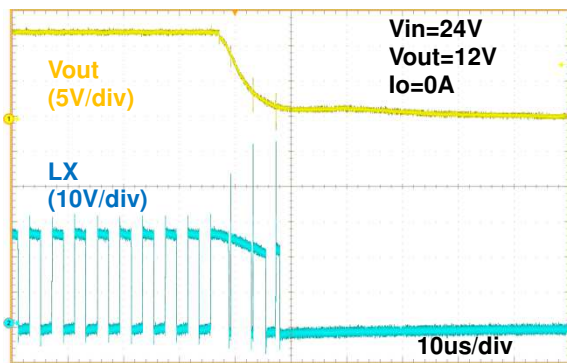


Figure 19. Output shorted waves(Extend)

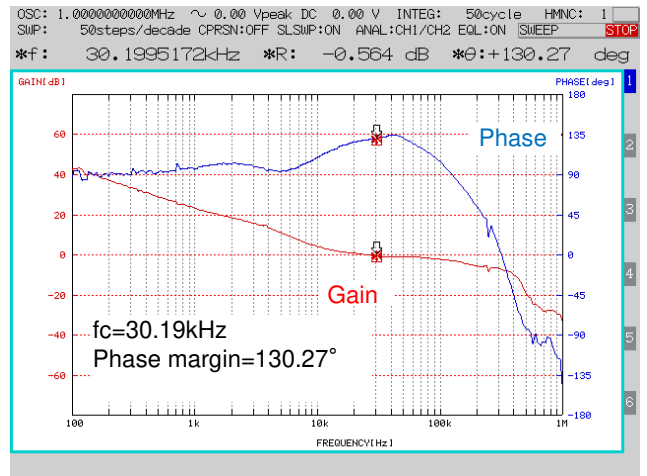


Figure 20. Frequency Response $V_{IN} = 24V$, $V_O = 12.0V$, $I_O = 8A$

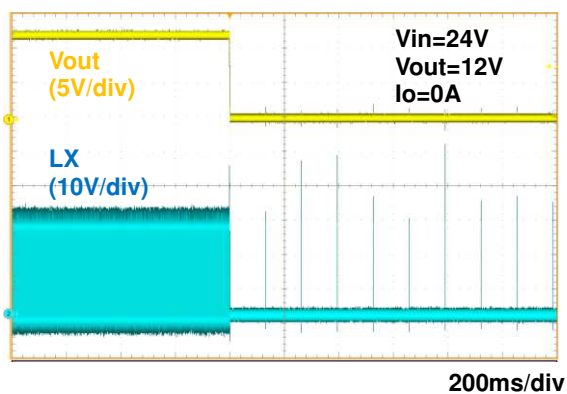


Figure 21. OCP Detect waves

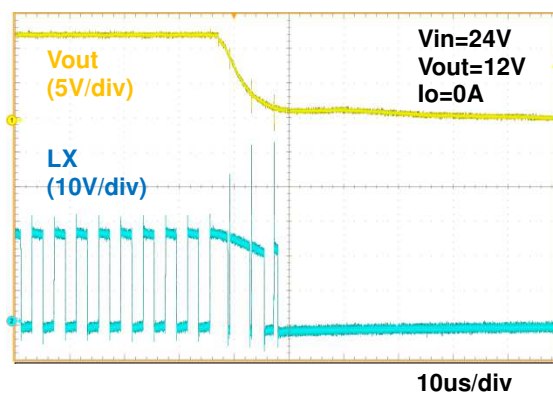


Figure 22. OCP Detect waves (Extend)

Layout pattern

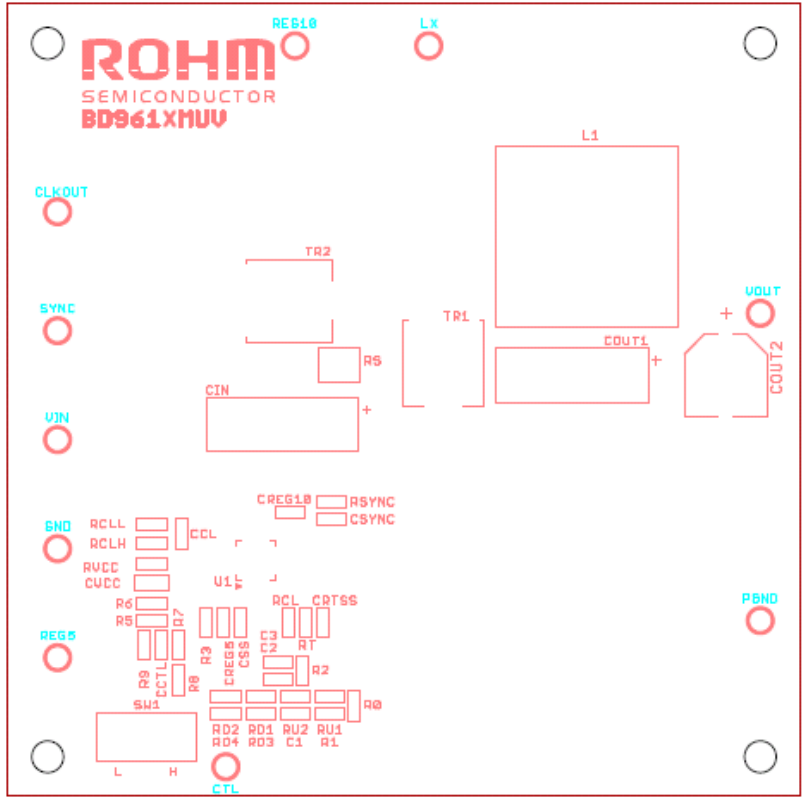


Figure 3. Top Silkscreen (Top view)

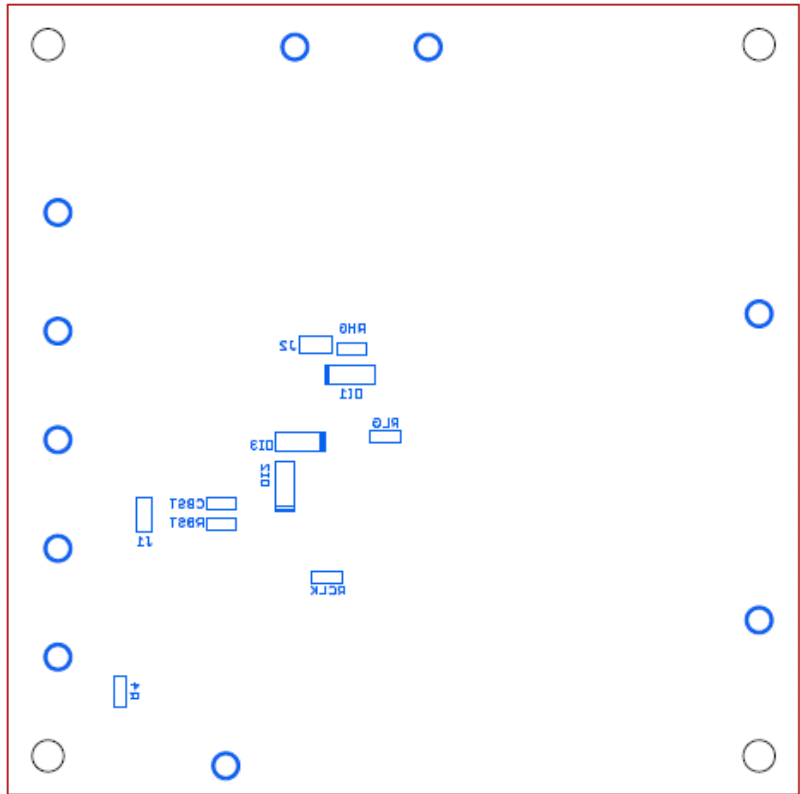


Figure 4. Bottom Silkscreen (Bottom view)

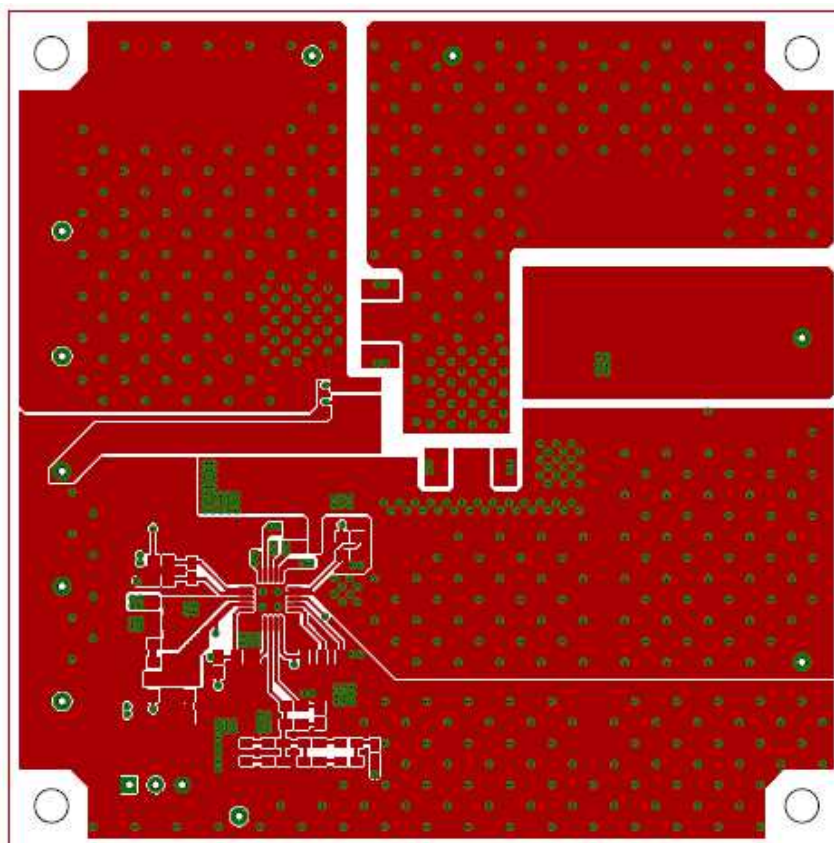


Figure 5. Top Layer (Top view)

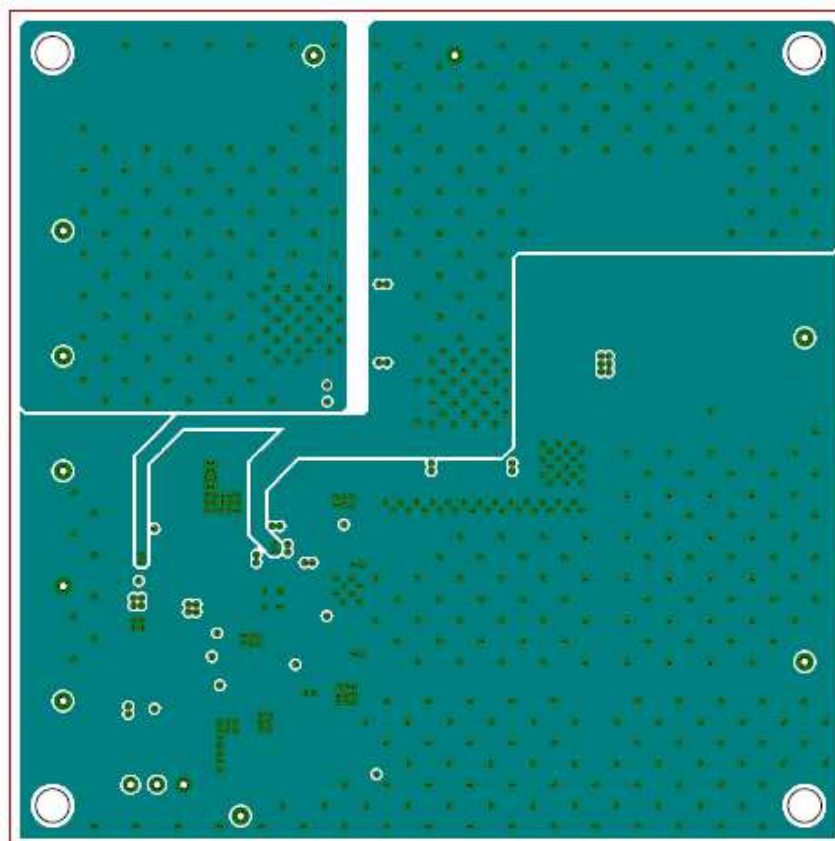


Figure 6. L2 Layer (Middle view)

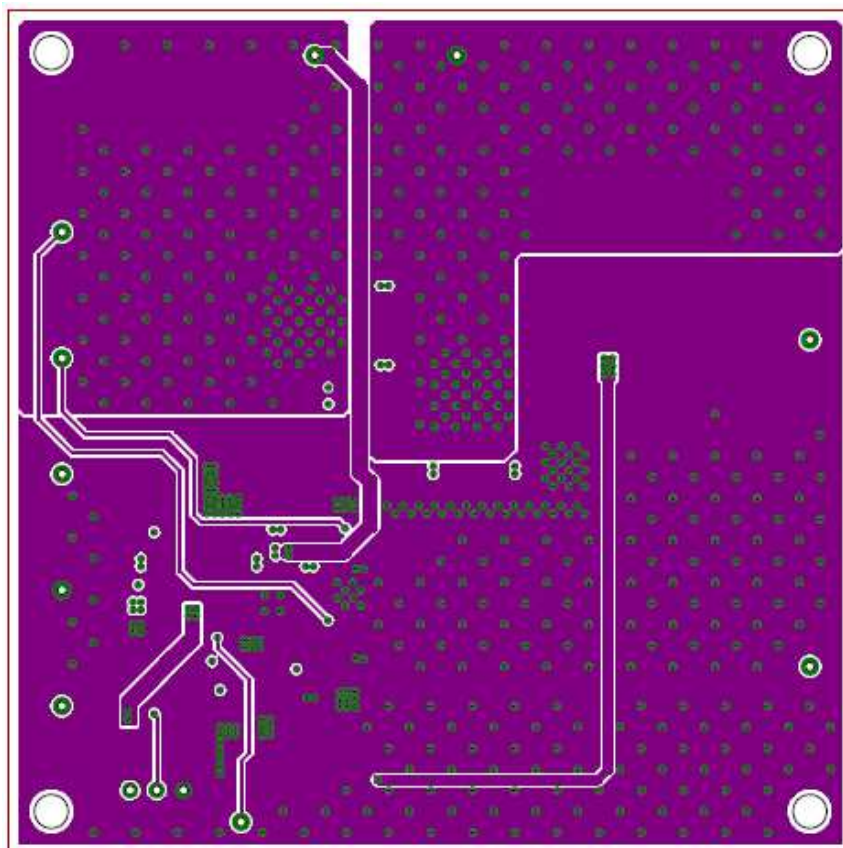


Figure 7. L3 Layer (Middle view)

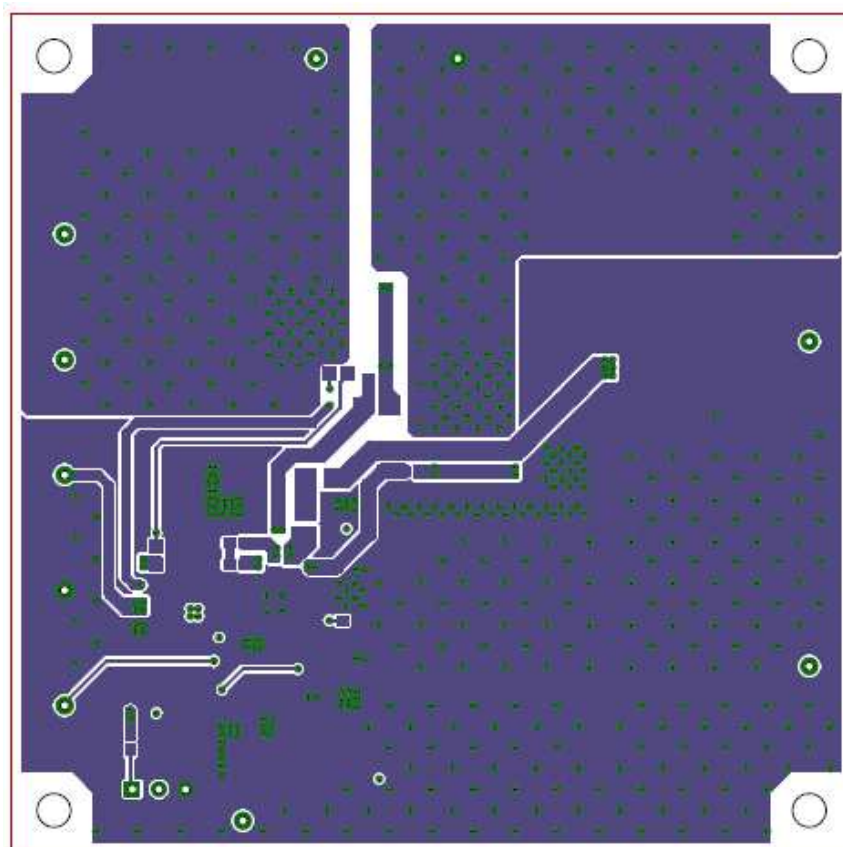


Figure 8. Bottom Layer (Bottom view)

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