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3.5V to 60V Input

1ch Boost DC/DC Controller

BD9615MUV-LB

General Description

This is the product guarantees long time support in Industrial market.

BD9615MUV-LB is a low side MOSFET controller with high withstand voltage (60V). It is suitable for circuits requiring low side FET such as boost and flyback, and it can be used in various applications.
An external resistor can adjust the switching frequency from 100kHz to 2500kHz. It reduces the total mounting area because It can operate at extremely high switching frequency. In addition, it has an external clock synchronization function to perform noise management.
BD9615MUV-LB has Thermal Shutdown (TSD), Over Voltage Protection (OVP), and Over Current Protection (OCP) to prevent damage caused by various abnormal modes.

Features

- Long Time Support Product for Industrial Applications
- Wide Input Voltage Range: 3.5V to 60V
- Frequency Setting Function: 100kHz to 2500kHz
- External Clock Synchronization Function
- Soft Start Time Control Function
- ON/OFF Control by the EN Pin (Standby Current 0μA)
- Over Voltage Protection Function by an Independent Pin
- Normal/Abnormal Signal Output by the PGDB Pin
- UVLO Control Function by External Resistors
- MAX DUTY Change Function: (50%/90%)
- High Power Small Package (VQFN16KV3030)

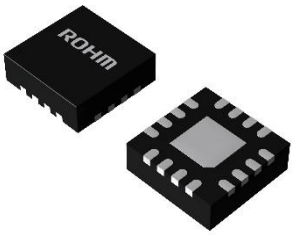
Applications

- Industrial Instruments

Key Specifications

- Input Voltage Range: 3.5V to 60V
- Reference Voltage Precision: (Ta=25°C) 0.8V±1.5%
  (Ta=-40°C to +105°C) ±2.0%
- Frequency Range: 100kHz to 2500kHz
- Operating Temperature Range: -40°C to +105°C

Package	W (Typ) x D (Typ) x H (Max)
VQFN16KV3030	3.00mm x 3.00mm x 1.00mm



VQFN16KV3030
3.00mm x 3.00mm x 1.00mm

Typical Application Circuit

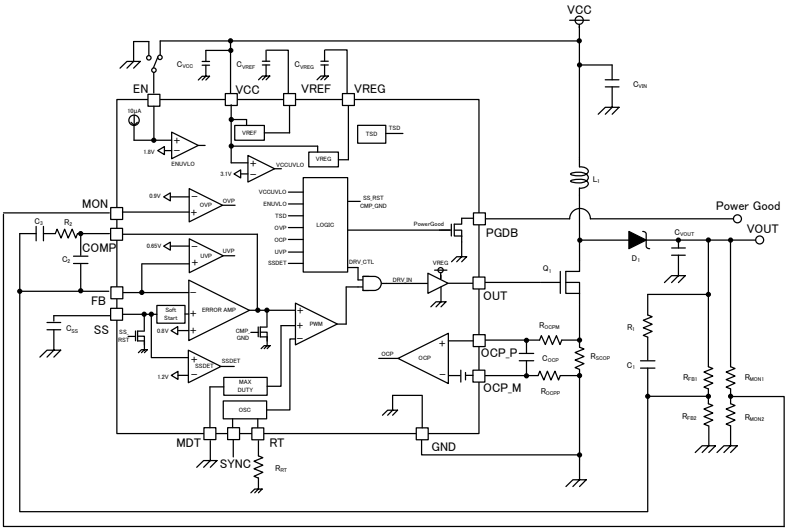


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

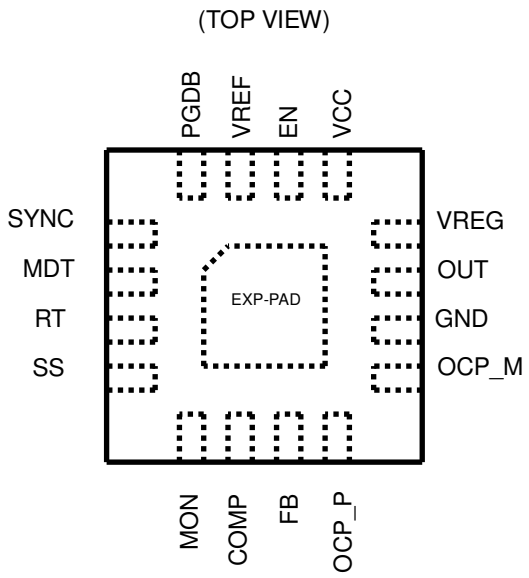
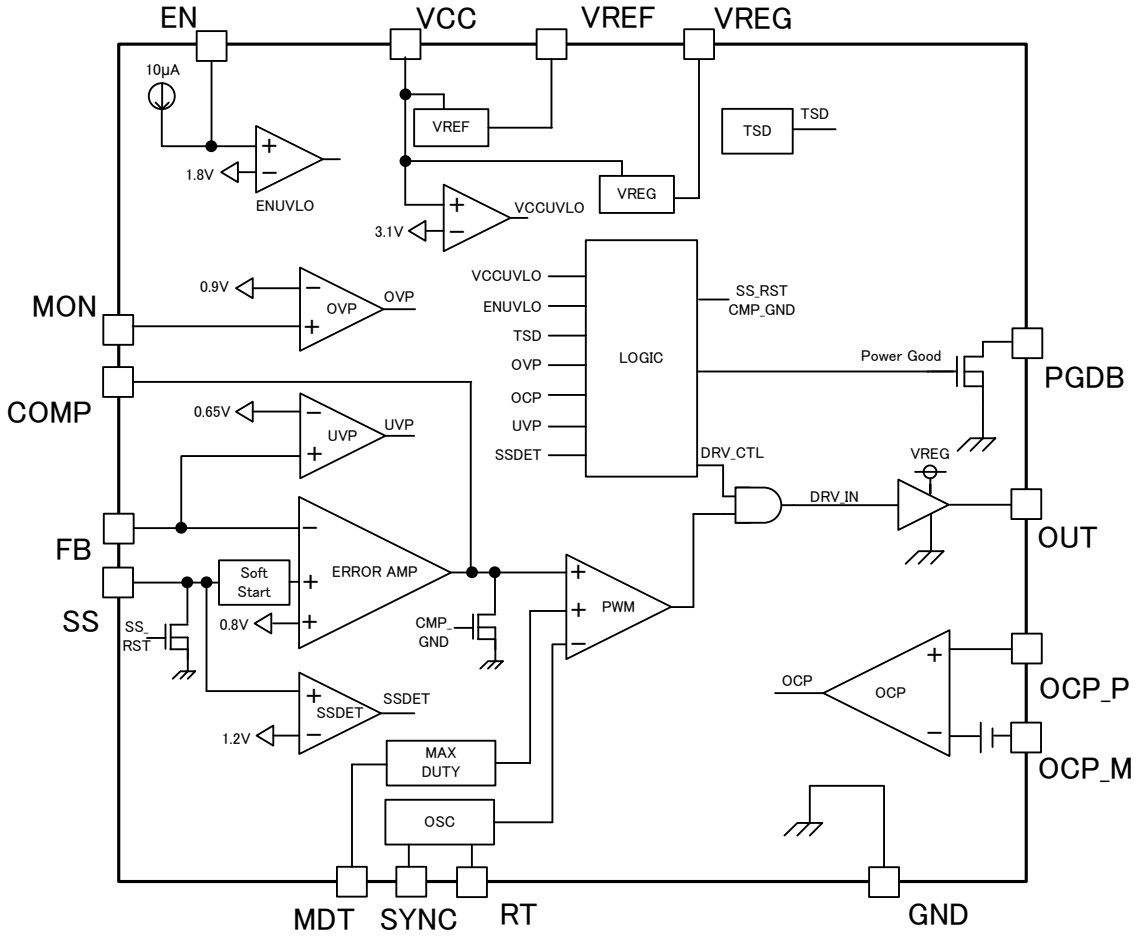


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	SYNC	External clock input pin
2	MDT	MAX DUTY setting input pin
3	RT	Resistor pin for setting frequency
4	SS	Pin for setting soft start time
5	MON	Output voltage monitor input Pin
6	COMP	ERROR AMP output pin
7	FB	ERROR AMP input pin
8	OCP_P	Over current detect pin plus input pin
9	OCP_M	Over current detect pin minus input pin. Connect to GND
10	GND	GND pin
11	OUT	Output pin for external FET driver
12	VREG	Power voltage output pin for driver
13	VCC	Power input pin
14	EN	ON/OFF control pin
15	VREF	Internal power voltage output pin
16	PGDB	Power Good output pin
-	EXP-PAD	Thermal pad for heat dissipation. Connect to GND for increased heat dissipation.

Block Diagram



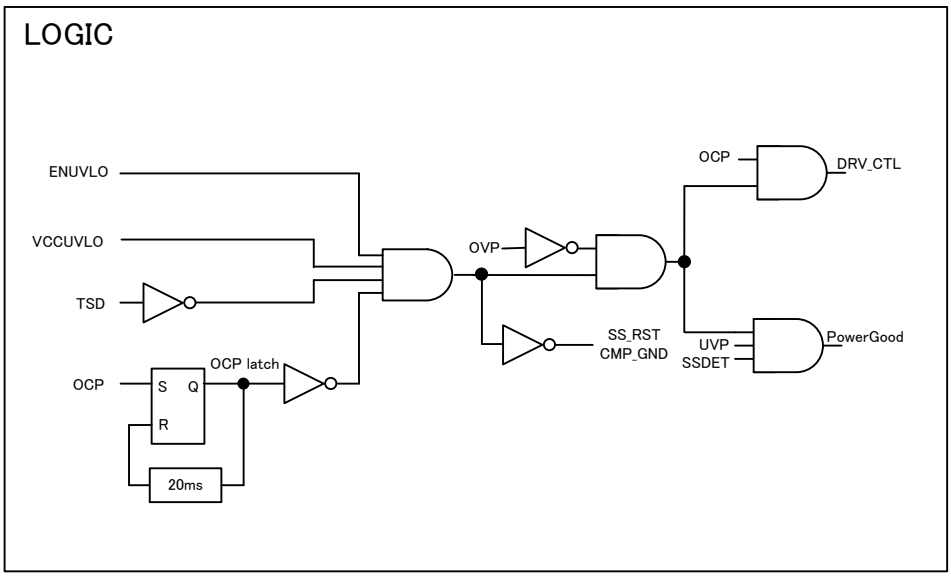


Figure 3. Block Diagram

Description of Blocks

1. ERROR AMP
   The ERROR AMP block is an error amplifier that detects the output signal and outputs the PWM control signal.
   The internal reference voltage is set to 0.8V (Typ).
   Connect a phase compensation element at the COMP pin.

2. OSC
   OSC block is an oscillation circuit with frequency setting function and external synchronization function.
   The oscillation frequency can be set by the RT pin.
   It can do external clock synchronous operation by inputting an external clock at the SYNC pin that is within ±20% of the set frequency.
   When not using the external synchronization function, connect the SYNC pin to GND.

3. MAX DUTY
   It is a MAX DUTY switching function. It can switch MAX DUTY 50% and 90% by setting H/L voltage. (H: 50%, L: 90%)

4. PWM
   PWM is a voltage – pulse width converter for controlling output voltage depending on the input voltage.
   It compares the internal sawtooth waveform with the ERROR AMP output voltage, controls the pulse and outputs it to the driver.

5. VREF
   The VREF block is an internal circuit power supply regulator. This voltage is 3.0V (Typ).

6. VREG
   VREG block is regulator for FET drive voltage. This voltage is 5.0V (Typ).
   Voltage can be applied from an output voltage to the VREG pin.

7. VCCUVLO
   The VCCUVLO block prevents internal circuit error during decrease of power supply voltage.
   It monitors the VCC pin voltage. When the VCC voltage becomes 3.1V (Typ) or less, it turns off output FET and DC/DC converter output, and resets Soft Start circuit.

8. ENUVLO
   It can set low input voltage protection setting by configuring the EN pin with a resistor divider from VCC.
   If the voltage from this pin is 0.3V or less, IC operation is off. If it is between 1.4V and 1.7V, internal REG circuit turns on. If it is 1.8V (Typ) or more, the IC operates and a hysteresis generation current of 10μA (Typ) is sourced from the internal circuit. To turn off the IC, source current should be removed.

9. TSD
   The TSD block is for thermal protection. When it detects the temperature exceeding Maximum Junction Temperature (Tj=150°C), it turns off the output FET, and resets Soft Start circuit. When the temperature is decreased, the IC automatically returns to normal operation with hysteresis.

10. OCP
    This IC has over current protection to protect the FET from over current.
    If over current flows in FET, OCP function turns off the output and protects FET.

11. OVP
    The OVP block is an over voltage output detect function. If the MON pin voltage is 0.9V (Typ) or more, IC operation is OFF. OVP detect threshold has a hysteresis of 50mV (Typ).

12. UVP
    The UVP block is an under voltage output detect function. If the FB pin voltage is 0.65V (Typ) or less, the comparator output is low. The output signal is added with other protection feature detection signals, and is output from the PGDB pin.

13. Soft Start
    The Soft Start circuit raises slowly the output voltage of the DC/DC converter to prevent in-rush current during start-up.
    Soft Start time can be adjusted by an external capacitor C_{SS}.

14. SSDET
    This is a Soft Start finish detect block. If the SS pin voltage is SS_{DETTH} (1.2V (Typ)) or more, SSDET output is high.
    Output signal is added with other protection feature detection signals, and is output from the PGDB pin.

15. Power Good
    This block generates an output signal that is the output voltage state of Normal or Error.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage VCC to GND EN to GND PGDB to GND	VCC V_{EN} V_{PGDB}	62	V
Supply Voltage VREG to GND OUT to GND	V_{REG}	12	V
Supply Voltage VREF, SS, FB, COMP, MDT, RT, SYNC, OCP_P, OCP_M, MON to GND	V_{REF}, V_{SS}, V_{FB}, V_{COMP}, V_{MDT}, V_{RT}, V_{SYNC}, V_{OCP_P}, V_{OCP_M}, V_{MON}	7	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. Increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN16KV3030				
Junction to Ambient	θ_{JA}	189.0	57.5	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	23	10	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VCC	3.5	12	60	V
Switching Frequency	f_{OSC}	100	500	2500	kHz
Switching Frequency Setting Resistor	R_{RT}	19	100	500	kΩ
External Synchronize Frequency	f_{EXT}	100	-	2500	kHz
External Synchronize Frequency for RT Setting Frequency	-	-20	-	+20	%
Operating Temperature	Topr	-40	+25	+105	°C

Electrical Characteristics (Unless otherwise specified Ta=25°C, VCC=12V, V_{EN}=3V, R_{RT}=100kΩ)

Parameter		Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
Circuit Current							
Standby Current		I_{ST}	-	0	10	μA	V_{EN}=0V
Operating Current		I_{CC}	-	2.0	4.0	mA	V_{FB}=1.2V
VCCUVLO							
UVLO Detect Threshold Voltage		V_{UV}	2.9	3.1	3.3	V	VCC sweep down
UVLO Hysteresis		V_{UVHYS}	-	100	200	mV	
VREF							
Output Voltage		V_{REF}	-	3.0	-	V	
VREG							
Output Voltage		V_{REG}	4.8	5.0	5.2	V	
OVLO Threshold Voltage		V_{REGOV}	5.2	5.4	5.6	V	V_{REG} sweep up
OVLO Hysteresis		$V_{REGOVHYS}$	-	100	200	mV	
Oscillator							
Oscillating Frequency		f_{OSC}	450	500	550	kHz	R_{RT}=100kΩ
MAX DUTY Cycle	MAX DUTY1	D_{MAX1}	82	90	98	%	V_{MDT}=L, V_{SYNC}=0V
	MAX DUTY2	D_{MAX2}	42	50	58	%	V_{MDT}=H, V_{SYNC}=0V
MDT Pin Input High Level		V_{IH_MD}	0.8 x V_{REF}	-	V_{REF} + 0.2	V	
MDT Pin Input Low Level		V_{IL_MD}	-0.3	-	0.2 x V_{REF}	V	
MDT Pin Input Current		I_{IH_MD}	-	3	8	μA	V_{MDT}=3.0V
ERROR AMP							
FB Threshold Voltage		V_{FB}	0.788	0.800	0.812	V	Ta=25°C
			0.784	0.800	0.816	V	Ta=-40°C to +105°C
FB Pin Input Current 1		I_{FB1}	-1	0	+1	μA	V_{FB}=0V
FB Pin Input Current 2		I_{FB2}	-1	0	+1	μA	V_{FB}=3.0V
Maximum Output Voltage		V_{CMPH}	2.7	V_{REF}	-	V	
Minimum Output Voltage		V_{CMPL}	-	0	0.3	V	
Output Sink Current		I_{CMPSI}	0.5	1.5	-	mA	V_{COMP}=1.25V, V_{FB}=1.5V
Output Source Current		I_{CMPSO}	100	180	-	μA	V_{COMP}=1.25V, V_{FB}=0V
Soft Start							
SS Pin Source Current		I_{SSSO}	1.4	2	2.6	μA	V_{SS}=0.5V
SS Pin Sink Current		I_{SSSI}	5	12	-	mA	V_{SS}=0.5V
Power Good Signal Output							
PGDB Pin Output Low Level Voltage		V_{PGBOL}	-	-	0.4	V	I_{PGDB}=1mA
PGDB Pin Leak Current		I_{PGBLK}	-	0	10	μA	V_{PGDB}=60V
Monitor Output Voltage							
UVP Detect Threshold Voltage		V_{PGTH}	0.60	0.65	0.70	V	V_{FB} sweep down
UVP Detect Hysteresis		V_{PGHYS}	-	50	75	mV	
OVP Detect Threshold Voltage		V_{OVPTH}	0.85	0.90	0.95	V	V_{MON} sweep up
OVP Detect Hysteresis		V_{OVPHYS}	-	50	75	mV	
MON Pin Input Current 1		I_{MON1}	-1	0	+1	μA	V_{MON}=0.0V
MON Pin Input Current 2		I_{MON2}	-1	0	+1	μA	V_{MON}=3.0V
Output							
Output High Side ON Resistance		R_{ONH}	-	3	-	Ω	V_{REG}=5.0V
Output Low Side ON Resistance		R_{ONL}	-	1.7	-	Ω	V_{REG}=5.0V

Electrical Characteristics (Unless otherwise specified Ta=25°C, VCC=12V, V_{EN}=3V, R_{RT}=100kΩ) - continued

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
OCP						
Over Current Detect Threshold	V_{OCPTH}	80	100	120	mV	
OCP_P Pin Input Bias Current	I_{OCP_P}	-	20	100	µA	V_{OCP_P}=0.1V
OCP_M Pin Input Bias Current	I_{OCP_M}	-	50	100	µA	V_{OCP_M}=GND
Over Current Detect Latch Stop Time	t_{OCP}	10	20	30	ms	
CTL						
EN Pin Internal REG ON-Threshold	V_{ENON}	0.3	-	1.4	V	
EN Pin UVLO Threshold	V_{ENUV}	1.7	1.8	1.9	V	IC Output ON condition
EN Pin Source Current	I_{EN}	9.0	10.0	11.0	µA	V_{EN}=3V
SYNC						
SYNC Pin Threshold Voltage High	V_{SYNCH}	2.0	-	5.5	V	
SYNC Pin Threshold Voltage Low	V_{SYNCL}	-0.3	-	+0.8	V	
SYNC Pin Input Current	I_{SYNC}	6	12	24	µA	V_{SYNC}=3V

Detailed Description

- **Frequency Setting Function**
  It can determine frequency input to PWM by using the RT pin.
  It establishes constant current in the IC by connecting a timing resistor, R_{RT}.
  Oscillation frequency can be set from 100kHz to 2500kHz and calculated as follows.

$$f_{osc} = \frac{1}{20\times10^{-9}+R_{RT}/(50\times10^{9})} \text{ [Hz]}$$

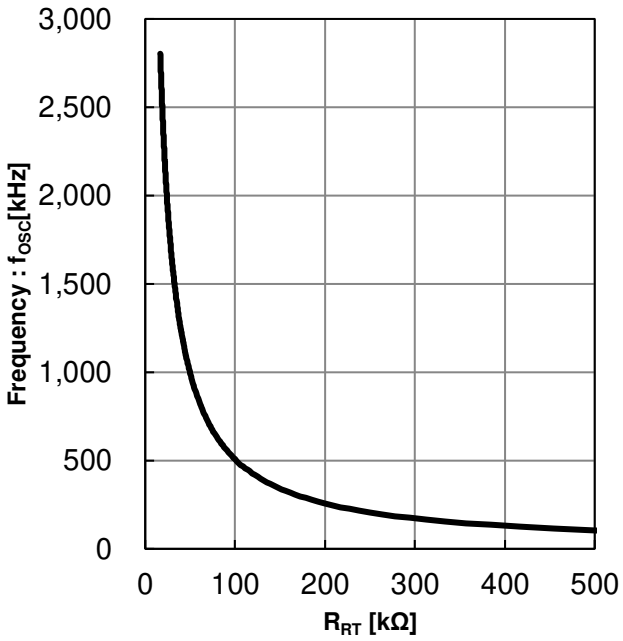


Figure 4. Frequency vs R_{RT}

- **External CLK for SYNC Function**
  This IC can operate synchronization function by inputting an external CLK signal to the SYNC pin.
  Input CLK signal is limited within ±20% of the frequency set by the RT pin. LOW level is 0.8V or less, and HIGH level is 2.0V or more. Required width of H section and L section is 100ns or more.
  After the 3rd input pulse at the SYNC pin, falling edge of internal sawtooth wave synchronizes with the falling edge of the SYNC pin. If external CLK stops, the device transitions to self-running mode after 1.5 times of oscillation period.

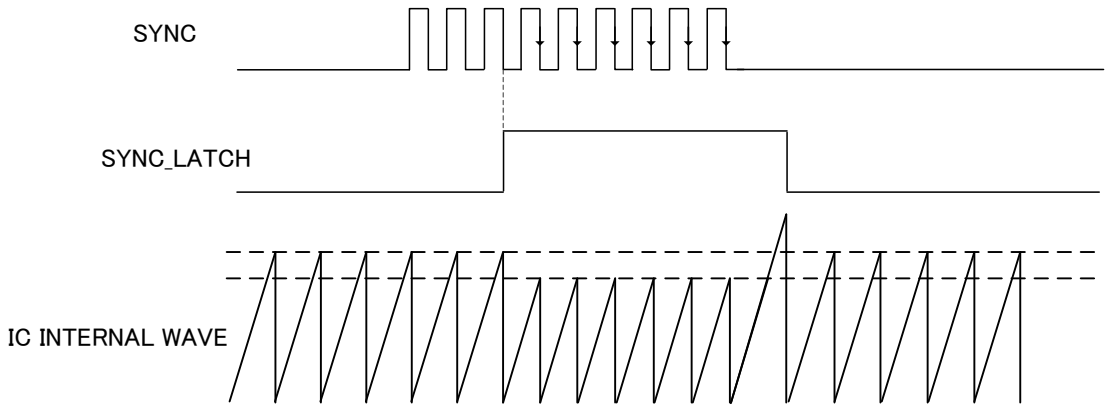


Figure 5. Frequency Synchronization Function Timing Chart

Detailed Description - continued

- **In the Case of Not Using the Synchronization Function**
  Although the SYNC pin is internally pulled down by a resistor, it is recommended to connect the SYNC pin to GND if the synchronization function is not in use.

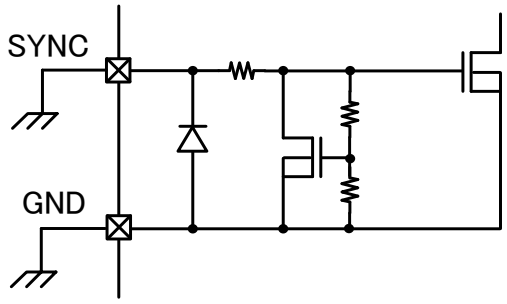


Figure 6. Circuit Diagram of SYNC Pin Not in Use

- **MDT Pin Function**
  It can change MAX DUTY by processing the MDT pin
  If the MDT pin is connected to the GND pin, MAX DUTY is prescribed in D_{MAX1} and is limited to 90% (Typ).
  If the MDT pin is connected to the VREF pin, MAX DUTY is prescribed in D_{MAX2} and is limited to 50% (Typ).
  To prevent malfunction caused by noise, connect the MDT pin to the GND pin or the VREF pin.
  When External Synchronize Frequency is input from SYNC (f_{EXT}), MAX DUTY is determined by the frequency (f_{OSC}) set by the RT pin and MAX DUTY set by the MDT pin and is prescribed in D_{MAX_SYNC} by following formula.

$$D_{MAX\_SYNC} = \left(1 - \frac{\frac{1}{f_{OSC}} \times (1 - D_{MAX})}{\frac{1}{f_{EXT}}}\right) \times 100\ [\%]$$

  Where:
  MDT=GND: $D_{MAX} = D_{MAX1}$: 90% (Typ)
  MDT=VREF: $D_{MAX} = D_{MAX2}$: 50% (Typ)

- **UVLO Control Function by External Resistors**
  The EN pin has built-in precise reset function. The EN pin connected with a resistor divider from VCC, as shown in Figure 7, can set low voltage malfunction prevention more than internal UVLO.
  When it is used, establish R_{EN1} and R_{EN2}, as shown in Figure 7, for any VCC start-up voltage V_{START} [V] and VCC shutdown voltage V_{STOP} [V].

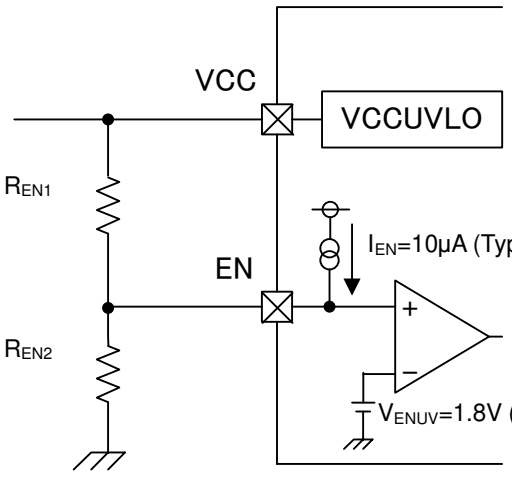


Figure 7. Circuit Diagram of UVLO External Setting Method

$$R_{EN1} = \frac{V_{START} - V_{STOP}}{I_{EN}}\ [\Omega]$$

$$R_{EN2} = \frac{V_{ENUV} \times R_{EN1}}{V_{START} - V_{ENUV}}\ [\Omega]$$

Detailed Description - continued

- **Soft Start Time**

Soft Start Time t_{SS} is determined by Soft Start Time Setting Capacitor C_{SS}, SS Source Current I_{SSSO}, and the FB pin Threshold Voltage V_{FB}. Set C_{SS} capacitance that can be fully discharged during the "Hiccup" time when OCP is detected.

$$t_{ss} = C_{SS} \times \frac{V_{FB}}{I_{SSSO}} \text{ [s]}$$

In addition, when COMP terminal capacitor C_3 is big and C_{SS} is small, rise voltage ΔV_{SS} of the SS pin voltage becomes big at time t_{COMP} before COMP pin voltage arriving at lower voltage of the internal saw-tooth wave (1.0V) from EN ON, and rush current occurs at the time of switching start. t_{COMP}, ΔV_{SS} is calculated in the following formula.
Set C_{SS} and C_{OUT} in consideration of rush current to be proportional to ΔV_{SS} and C_{OUT}.

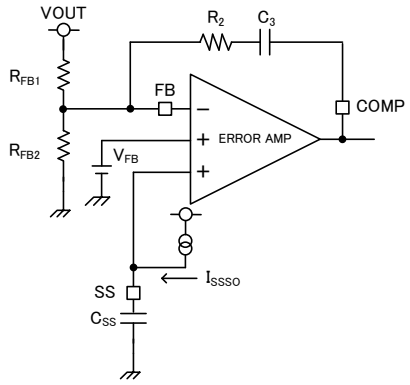


Figure 8. Error amplifier circuit diagram

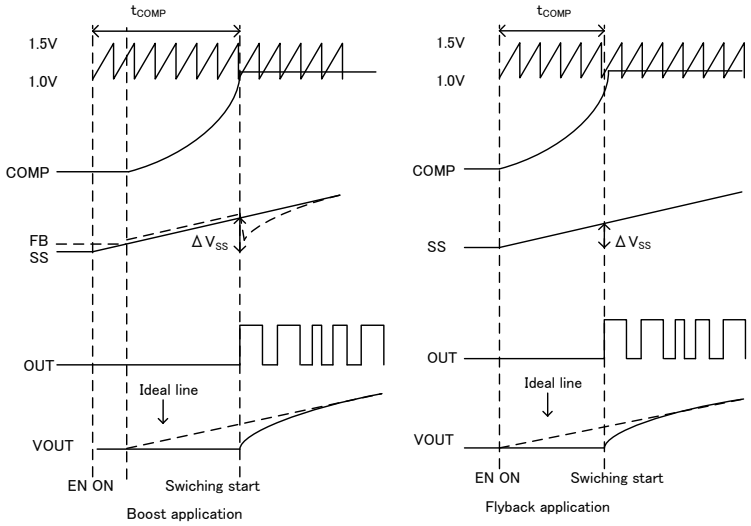


Figure 9. Output voltage starting diagram

Boost application

$$t_{COMP} = C_3 \left(\sqrt{(R_{FB2} + R_2)^2 + \frac{2 \times C_{SS} \times R_{FB2}}{C_3 \times I_{SS}} \left(\frac{R_2 \times VCC}{R_{FB1} + R_{FB2}} + 1 \right)} - (R_{FB2} + R_2) \right) + \frac{C_{SS} \times VCC \times R_{FB2}}{I_{SS} \times (R_{FB1} + R_{FB2})} \text{ [s]}$$

Flyback application

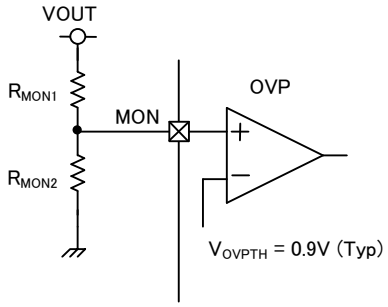
$$t_{COMP} = C_3 \left(\sqrt{(R_{FB1} // R_{FB1} + R_2)^2 + \frac{2 \times C_{SS} \times R_{FB1} // R_{FB1}}{C_3 \times I_{SS}}} - (R_{FB1} // R_{FB1} + R_2) \right) \text{ [s]}$$

$$\Delta V_{SS} = \frac{I_{SS}}{C_{SS}} \times t_{COMP} \text{ [V]}$$

Detailed Description - continued

- **OVP Function**

The MON pin has built-in OVP function. When the MON pin voltage becomes V_{OVPTH} or more, switching of the OUT pin is stop and switching is reopened if the MON pin voltage becomes V_{OVPTH}-V_{OVPHYS} or less. The OVP detect voltage (V_{OVP}) can be set by connecting the MON pin with a resistor divider from V_{OUT}, as shown in Figure 10.



$$V_{OVP} = \frac{R_{MON1}+R_{MON2}}{R_{MON2}} \times V_{OVPTH} \text{ [V]}$$

Figure 10. Circuit Diagram of OVP Function Setting Method

- **OCP Function**

If over current flows in FET, OCP function turns off the output and protects FET.
The voltage between the OCP_P pin and the OCP_M pin is monitored by OCP sense resistance. If the voltage exceeds the overcurrent detection voltage (100mV (Typ)), the OUT pin is set to Low during the period (pulse by pulse control). When OCP is detected twice consecutively, the IC is turned off 20ms (Typ) (“hiccup” operation), and the IC is turned on if the voltage between the OCP_P pin and the OCP_M pin is lower than the over current detect voltage.

$$R_{SOCP} = \frac{V_{OCPTH}}{I_{OCP}} \text{ [Ω]}$$

Where:
V_{OCPTH} Over Current Detect Threshold (100mV (Typ))
I_{OCP} OCP detect current

If OCP detect circuit is unused, short the OCP_P pin and the OCP_M pin to the GND pin near the IC.

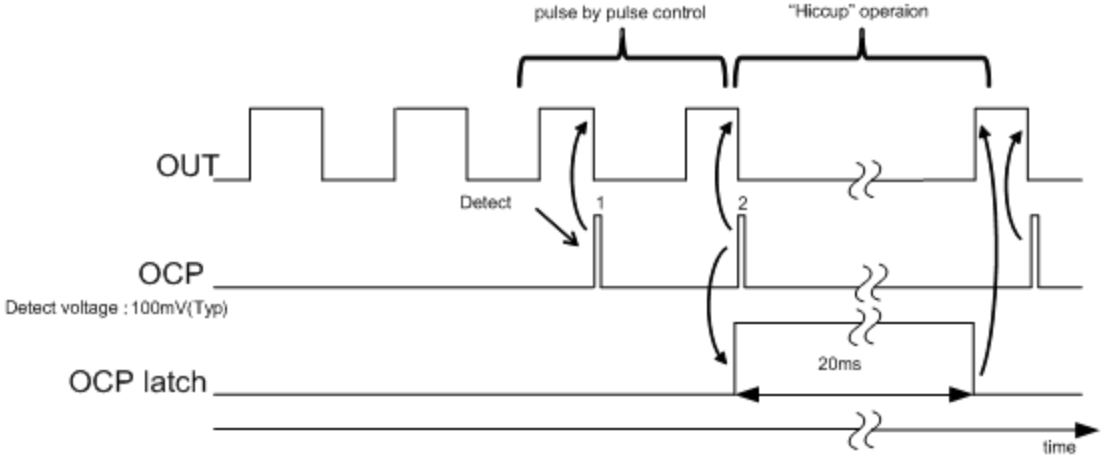


Figure 11. Timing Chart at OCP Operation

Detailed Description – continued

[Noise Design for the OCP_P pin and the OCP_M pin]
The OCP input OCP_P OCP_M is a very sensitive circuit.
Therefore, there is a possibility of erroneous detection due to generated noise on the board.

As a measure to prevent erroneous detection at the OCP_P and the OCP_M pin, insert coupling capacitor and resistance near and between the OCP_P and the OCP_M pin.

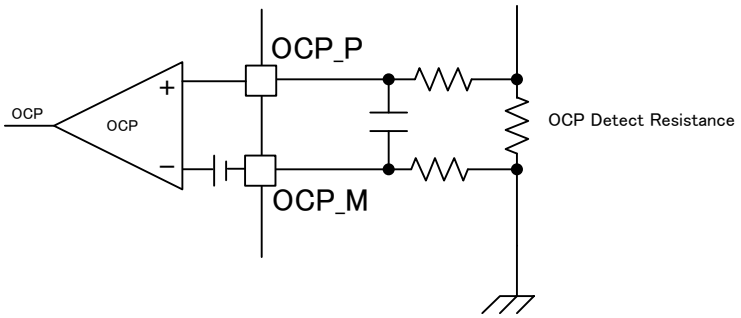


Figure 12. Circuit Diagram of Noise Measurement

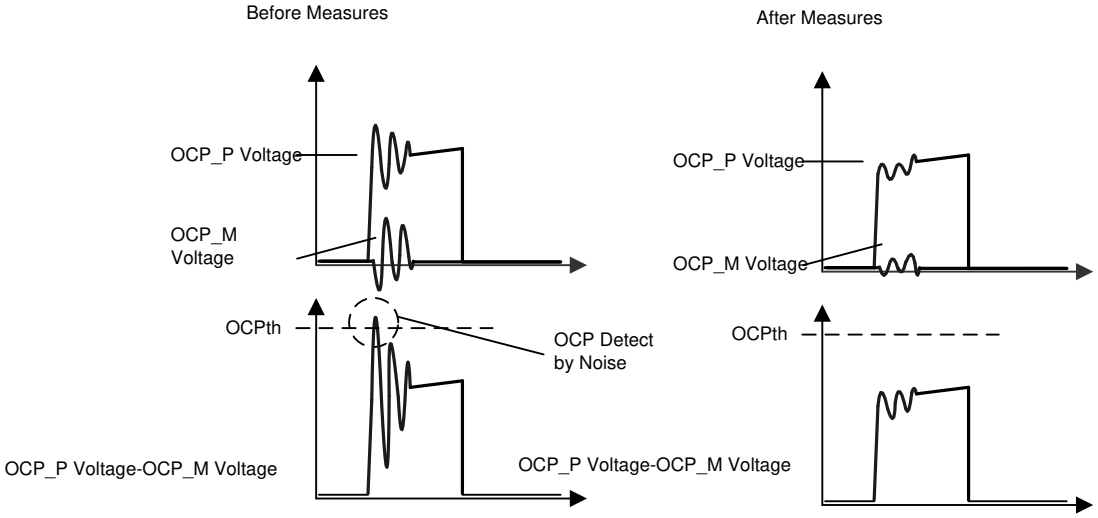


Figure 13. Effect of Noise Measurement

Consider in advance noise reduction on the board because there is limit to noise attenuation by the above measures.
As precaution on pattern, make current path as short as possible, and shorten the wiring to the OCP_P and OCP_M pin as much as possible.
For peripheral components, select FET with small gate amount of charge Qg and select Di with small equivalent capacitance and short reverse recovery time t_{RR} for noise reduction.
Aside from adding a bypass capacitor, adding an R_{GATE} makes the waveform duller (concern about the efficiency deterioration as contradictory matter).

Detailed Description – continued

- **VREG Pin Function**
  The VREG pin is output pin of internal regulator and it supplies 5.0V (Typ).
  It drives Nch MOSFET via the OUT pin of driver output.

  [Output Voltage Regenerative Function]
  For the power consumption improvement of the VREG, it can regenerate to the VREG pin via diode when voltage is upper than V_{REGOV}. Voltage range that can regeneration is V_{REGOV} (5.4V (Typ)) to 10V.

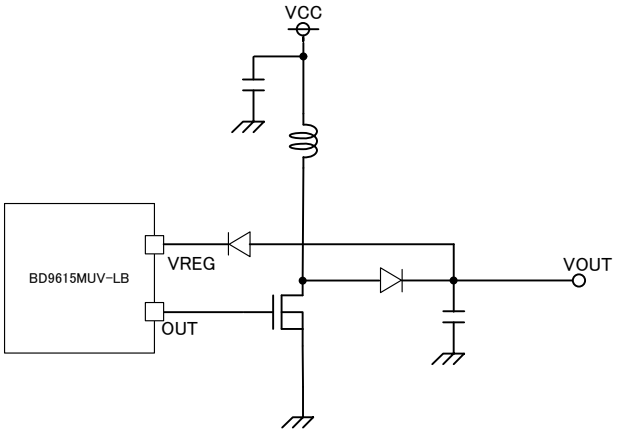


Figure 14. Example of Regeneration Application

[VCC Reduced Voltage]
Due to decrease of VCC supply voltage, drive voltage output from the VREG pin also decrease and driver R_{ON} of the OUT pin is increased.
Optimal drive voltage of FET is changed by oscillation frequency and the gate capacitance.
Selects FET and oscillation frequency that consider characteristic data when use at VCC is less than or equal to 5V.

- **Power Good Output Function**
  The PGDB pin is the open drain output of the internal Nch FET. Using external resistance, pull up the PGDB pin to external power supply by external resister, to use Power Good Output function.
  When an internal detection function is the non-detection, and output voltage is within the range from UVP (the FB pin) to OVP (the MON pin), the PGDB pin is Low. When other operation mode or shutdown (EN=L), Nch MOSFET turns off and the PGDB pin turns HIGH (pull-up voltage).
  In addition, a connection between power supply (VCC) and output (V_{OUT}) can be cut by connecting the PGDB pin like Figure 15. Pull-up voltage of the PGDB pin has to be below its absolute maximum rating of 62V.

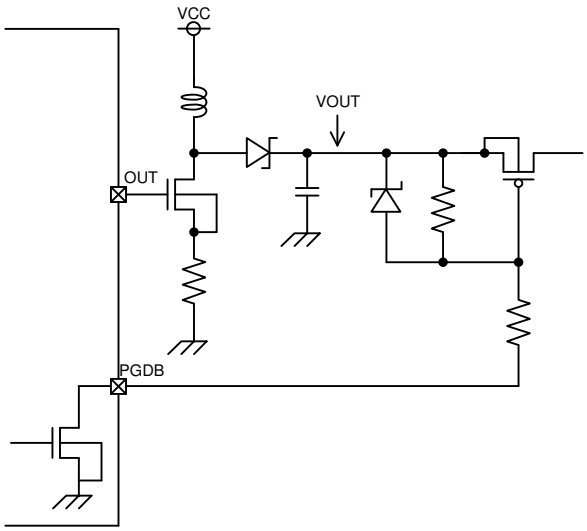


Figure 15. Circuit Diagram of Power Line Cutting Method

Performance Curves (Reference Data)
(Unless Otherwise Specified, Ta=25°C, VCC=12V)

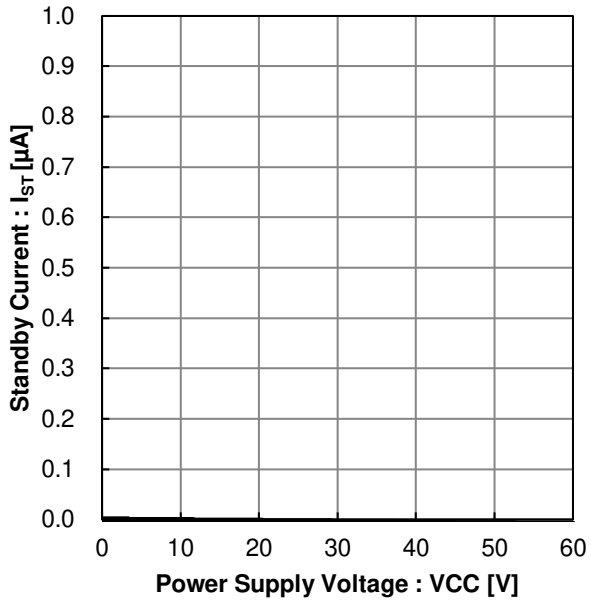


Figure 16. Standby Current vs Power Supply Voltage

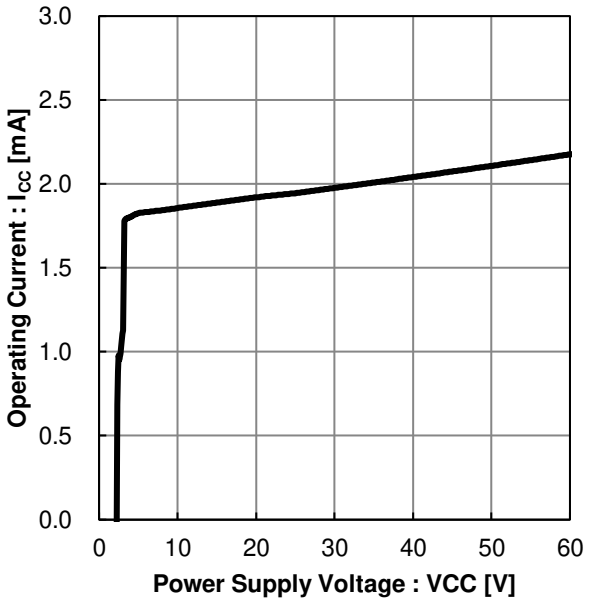


Figure 17. Operating Current vs Power Supply Voltage (V_{FB}=1.2V)

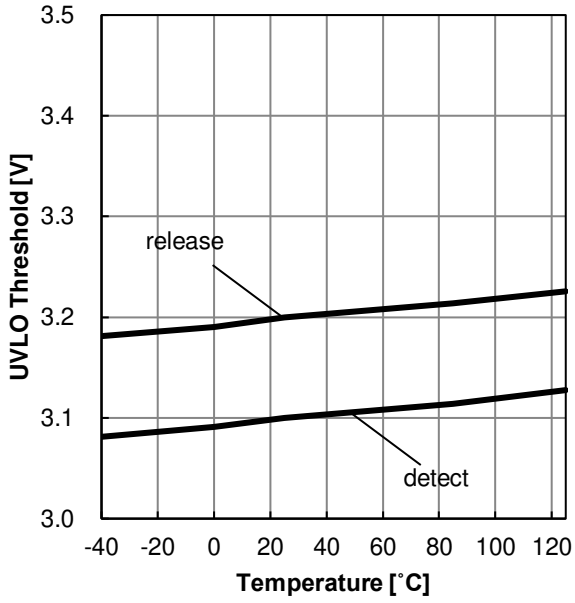


Figure 18. UVLO Threshold vs Temperature

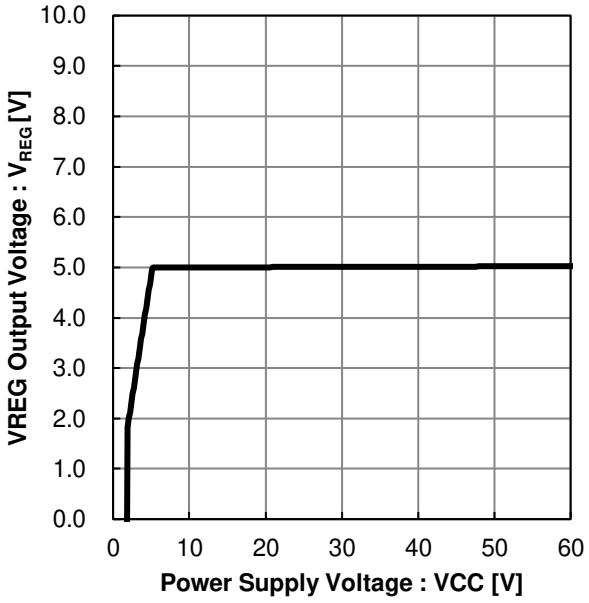


Figure 19. VREG Output Voltage vs Power Supply Voltage

Performance Curves (Reference Data) - continued

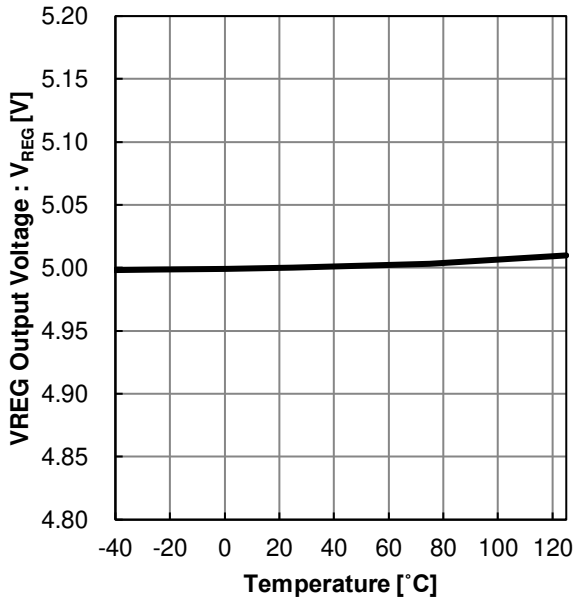


Figure 20. VREG Output Voltage vs Temperature

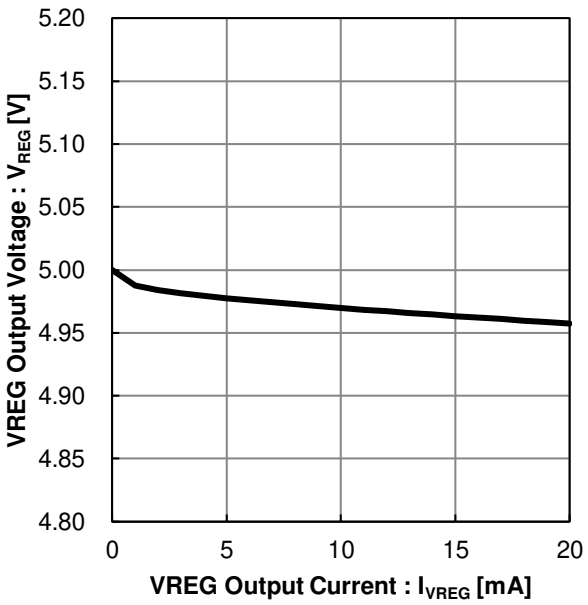


Figure 21. VREG Output Voltage vs VREG Output Current

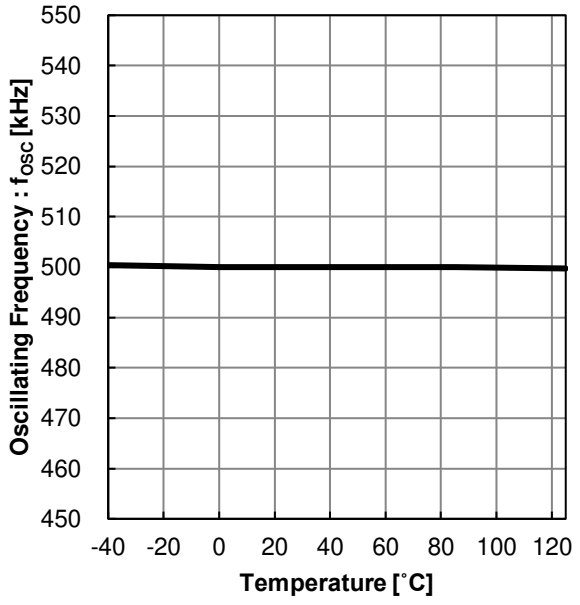


Figure 22. Oscillating Frequency vs Temperature

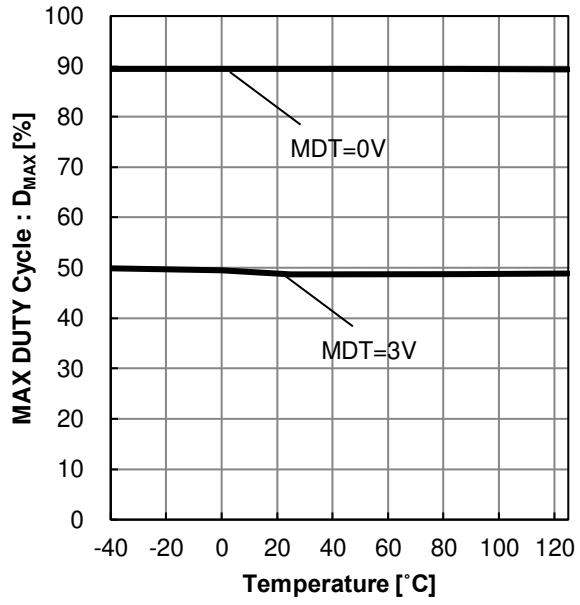


Figure 23. MAX DUTY Cycle vs Temperature

Performance Curves (Reference Data) - continued

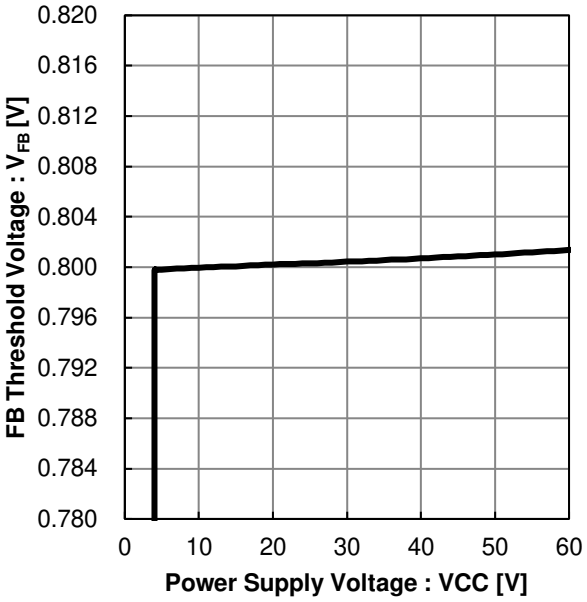


Figure 24. FB Threshold Voltage vs Power Supply Voltage

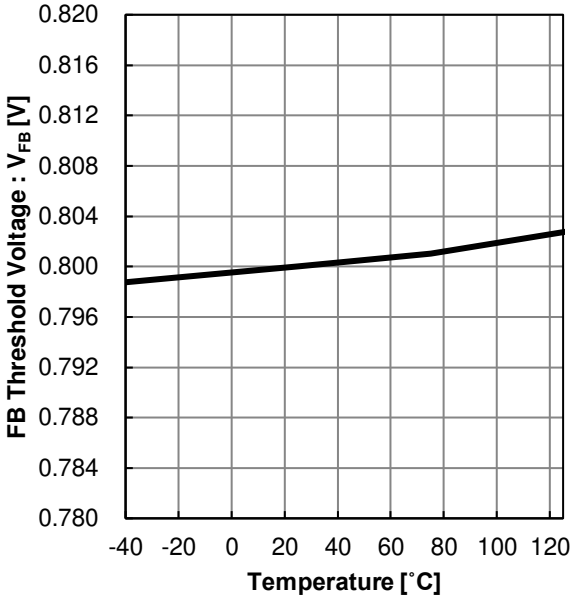


Figure 25. FB Threshold Voltage vs Temperature

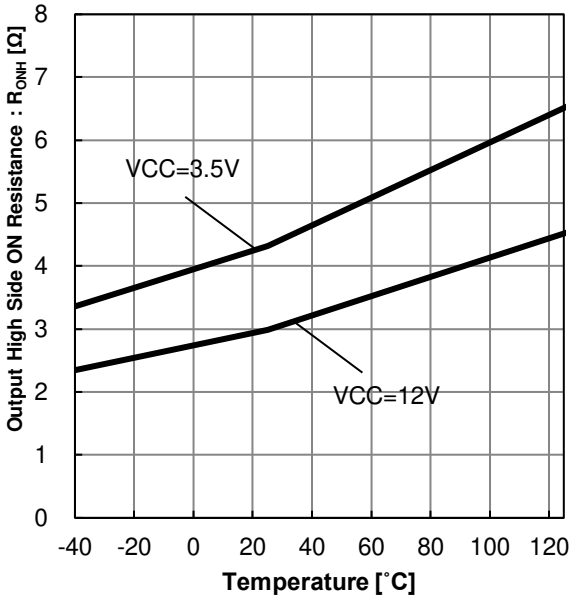


Figure 26. Output High Side ON Resistance vs Temperature

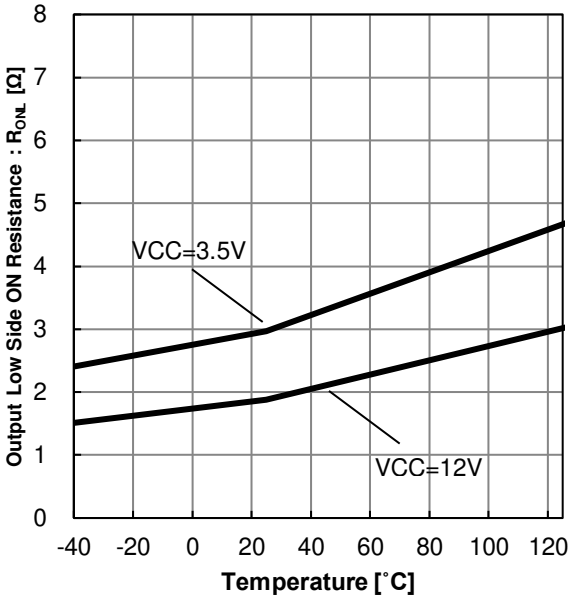


Figure 27. Output Low Side ON Resistance vs Temperature

Performance Curves (Reference Data) - continued

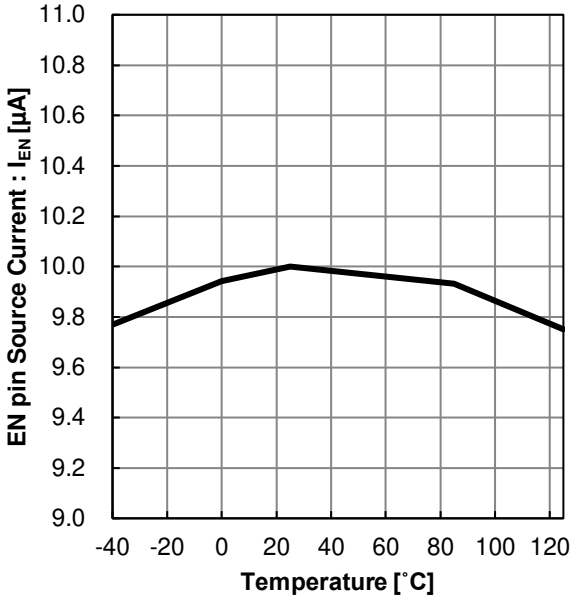


Figure 28. EN pin Source Current vs Temperature

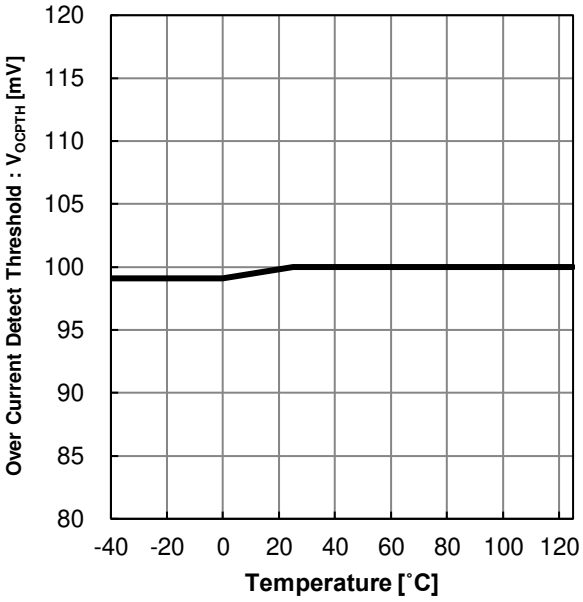
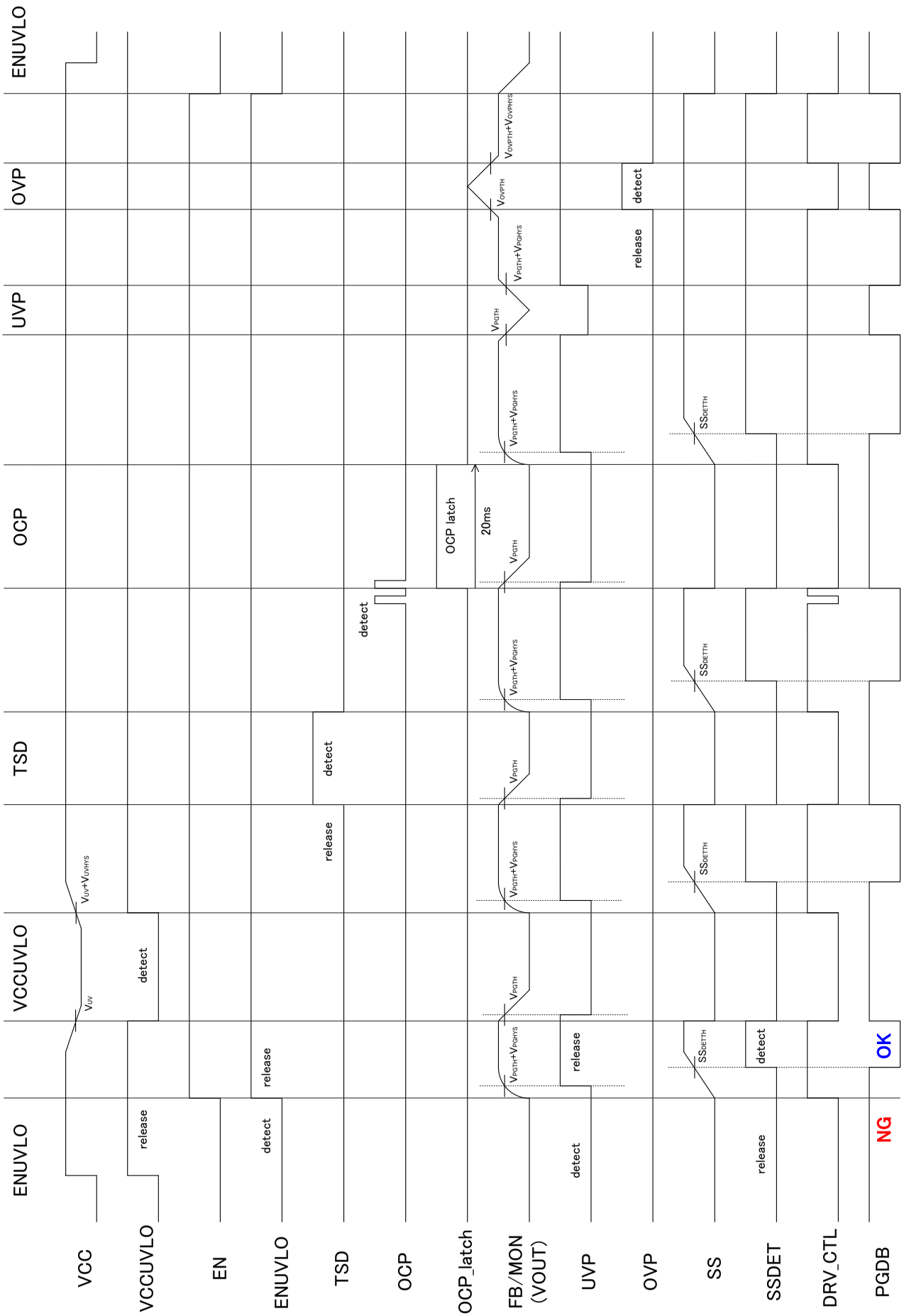


Figure 29. Over Current Detect Threshold vs Temperature

Timing Chart



Reference Characteristics of Typical Application Circuit

VIN=3.5V, VOUT=5.1V,
f_{OSC}=500kHz, Output Current=1A

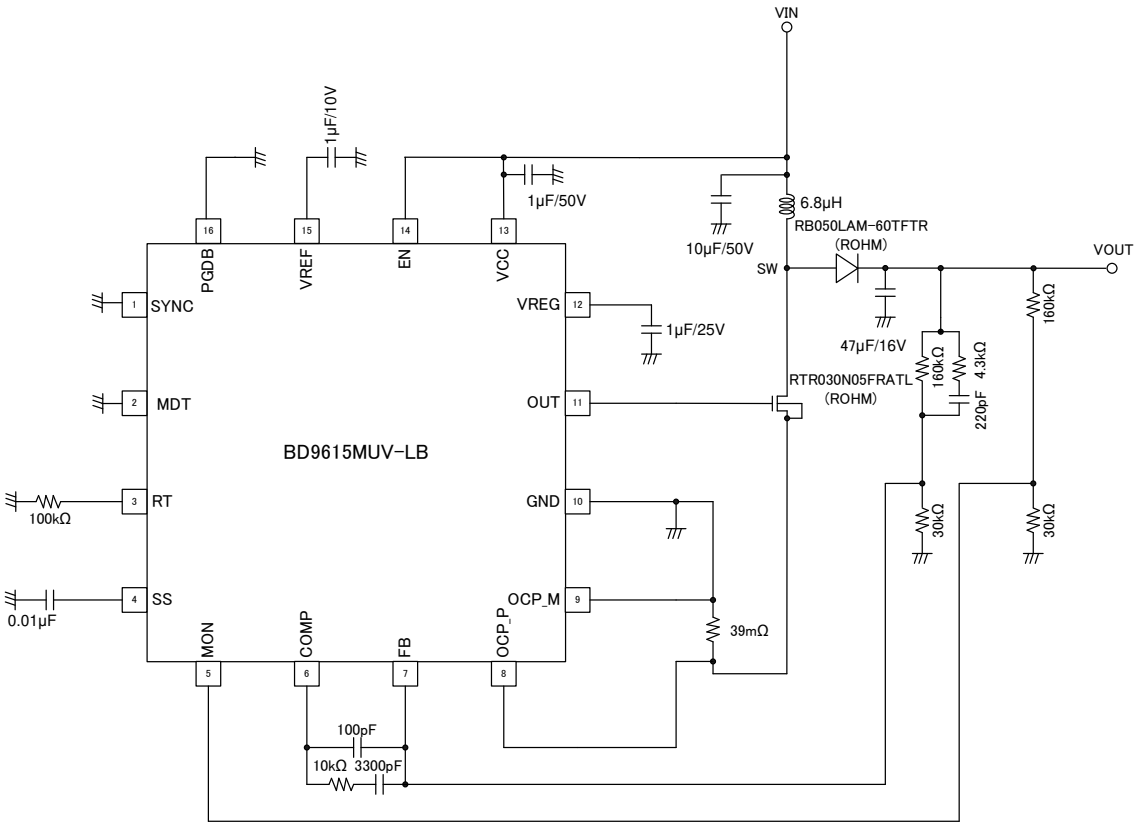


Figure 30. Typical Application Circuit

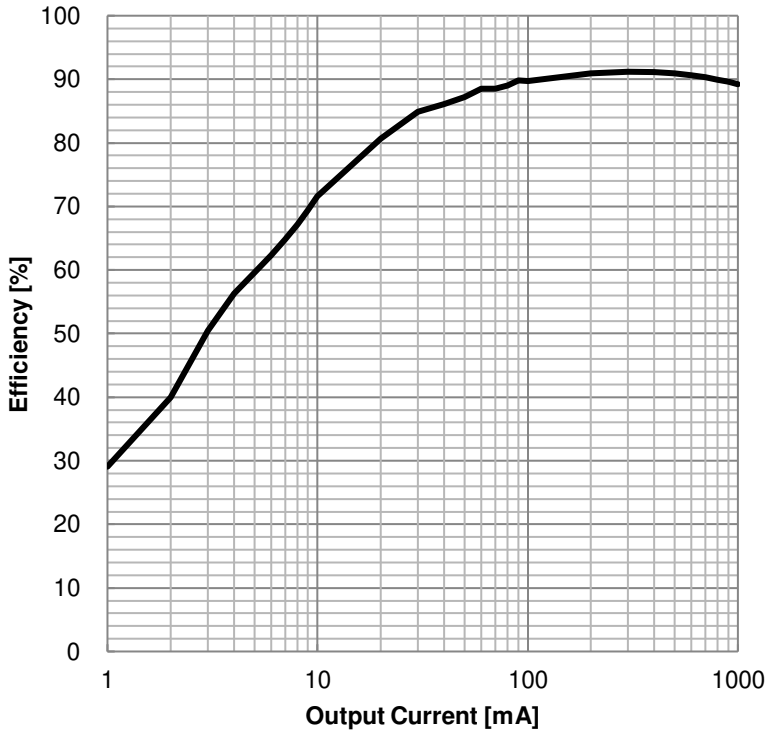


Figure 31. Efficiency vs Output Current

Reference Characteristics of Typical Application Circuits - continued

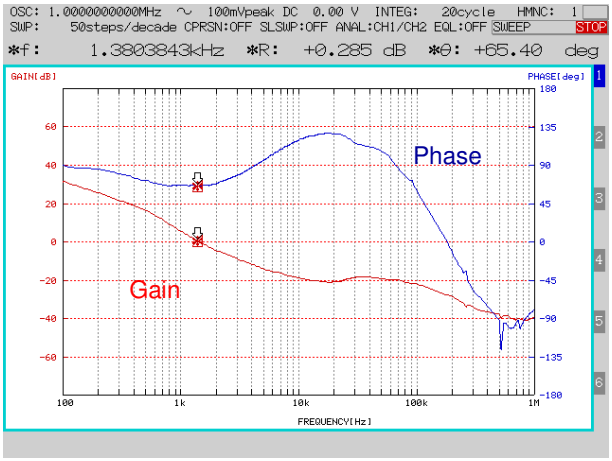


Figure 32. Frequency Characteristics Output Current=0.1A

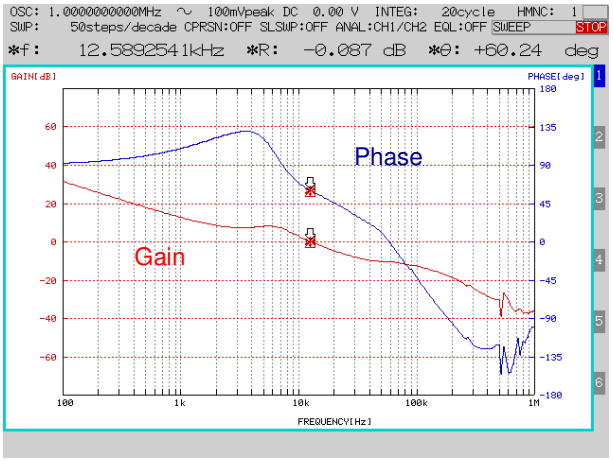


Figure 33. Frequency Characteristics Output Current=1.0A

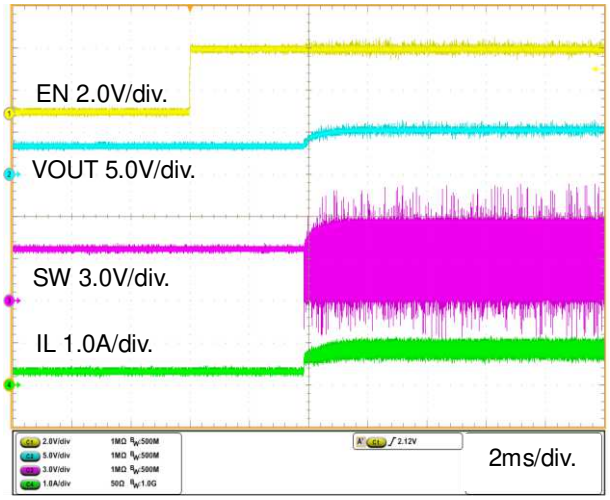


Figure 34. Startup Waveform

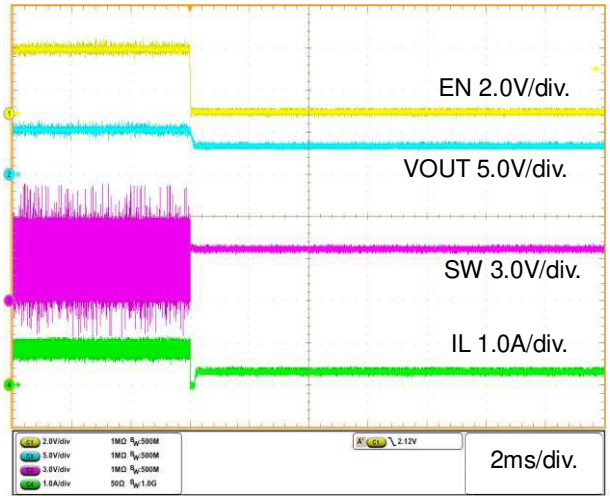


Figure 35. Shutdown Waveform

Application Part Setting Method

(1) Inductor
It is recommended to use shielded type inductor that satisfies the current rating (I_{PEAK}) and has low DCR (direct current resistance). Inductor value affects inductor ripple current and causes the output ripple. This ripple current can become small when inductor is large and switching frequency is high.

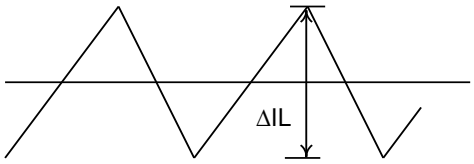


Figure 36. Inductor Current

$$I_{PEAK} = I_{OUT}\frac{VOUT}{\eta \times VIN} + \Delta I_L/2 \ \text{[A]} \qquad (1)$$

$$\Delta I_L = \frac{VIN(VOUT-VIN)}{VOUT \times f_{OSC} \times L} \ \text{[A]} \qquad (2)$$

where:
η is the efficiency
ΔIL is the output ripple current
f_{OSC} is the switching frequency

Normally, ΔIL is set 30% or less of Max Output Current (I_{OUTMAX}).

When a current flowing into the inductor exceeds the inductor current rating, it causes a magnetic saturation which causes a decrease in efficiency and oscillation at the output. Choose an inductor with a sufficient margin so that peak current does not exceed current rating of the inductor.

(2) About Switching Components FET and Di
Set switching components with sufficient margin of current tolerance obtained by the formula (1).
For noise and efficiency improvement, select FET with small input capacitance (C_{ISS}, Qg) and ON resistance.
Select Di with small equivalent capacitance, short reverse recovery time t_{RR}, and small forward voltage V_F.

(3) Output Capacitor
Choose output capacitor with the lower Equivalent Series Resistance (ESR).
Output Ripple Voltage V_{PP} is determined in the formula (3).

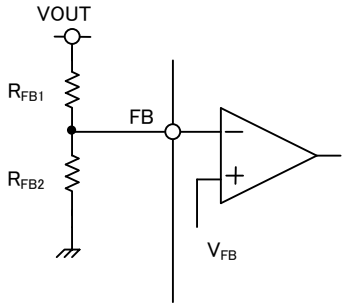
$$V_{PP} = IOUT \times \frac{VOUT-VIN}{F_{OSC} \times C_{OUT} \times VOUT} + I_{PEAK} \times ESR \ \text{[V]} \qquad (3)$$

Set within the range of allowable ripple voltage.

The VREF pin, the VREG pin connection capacitor
Between the VREF pin, the VREG pin and the GND pin is need to connect 1μF ceramic capacitor.
It is needed to select capacitor from 0.5μF to 1.5μF that considers DC bias effect and temperature characteristics.
In case capacitor short Grand fault is supposed, there is a possibility of destruction by generation of heat.
Therefore, it is needed to measure set the capacitor in two series.

(4) Input Capacitor
Input capacitor needs to use electrolytic capacitor and ceramic capacitor.
Output switching current is supplied by Input Capacitor (C_{IN}), so set ceramic bypass capacitor near FET and Di.
When using electrolytic capacitor, consider the allowable ripple current.

(5) Output Voltage Setting
Output Voltage is determined in the formula (4)



$$VOUT = \frac{R_{FB1}+R_{FB2}}{R_{FB2}} \times V_{FB} \ \text{[V]} \qquad (4)$$

Figure 37. Circuit Diagram of Voltage Feedback Resistor Setting Method

Application Part Setting Method - continued

(6) Selection of External Phase Compensation
Stable condition of application
Negative feedback is applied is as follows.
When Gain is 1(0dB), phase delay is 135 degrees or less (phase margin is 45 degrees or more).
DC/DC converter application is sampled by switching frequency, so as a whole f_{BW} (frequency at which gain is 0dB) is set 1/10 or less of the switching frequency.
Also set f_{BW} in less than 1/5 of boost converter peculiar right half plane zero (f_{RHPZ}) so that right half plane zero frequency does not influence a control loop.

In conclusion, Application target specifications are as follows.
(A) Gain is 1 (0dB), phase delay is 135 degrees or less (phase margin is 45 degrees or more).

(B) f_{BW} is 1/10 or less of switching frequency

(C) f_{BW} is 1/5 or less of f_{RHPZ}

It set C_1, C_3, R_1, and R_2 of Figure 38 that meet the above.

f_{BW} that determines DC/DC converter responsiveness is able to calculate by evaluate 1st pole frequency and DC gain.

1st pole frequency $fp1 = \frac{1}{\left(2\pi \times A \times \frac{R_{FB1} \times R_{FB2}}{R_{FB1}+R_{FB2}} \times C_3\right)}$ [Hz]

DC Gain $DCgain = \frac{A}{B} \times V_{FB} \times \frac{VOUT}{VIN}$

Where
A: ERROR Amp Gain=10^4 (=80dB)
B: Oscillator amplitude=0.5V

$f_{BW} = DCgain \times fp1$ [Hz]

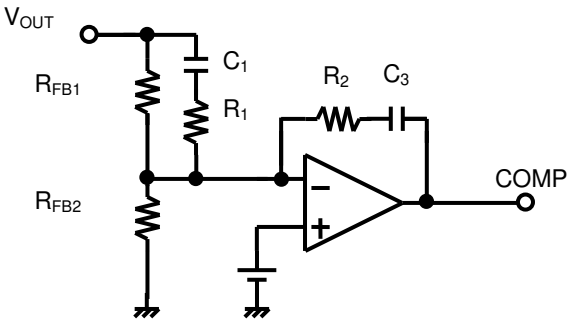


Figure 38. Example of Phase Compensation Setting

$f_{RHPZ} = \frac{1}{2\times\pi\times L\times IOUT} \times \frac{VIN^2}{VOUT}$ [Hz]

Insert second order phase lead in order to cancel the second order phase delay by LC. Insert phase lead near LC resonance frequency.

Phase Lead $fz1 = \frac{1}{2\pi \times R_{FB1} \times C_1}$ [Hz]

Phase Lead $fz2 = \frac{1}{2\times\pi\times R_2\times C_3}$ [Hz]

LC Resonance Frequency $= \frac{1-D}{2\times\pi\sqrt{L\times C_{OUT}}}$ [Hz]

Where
C_{OUT}: Output Capacitor
D: ON Duty=(VOUT-VIN)/VOUT

If f_{BW} goes excessive high frequency by second order phase lead, it may be stabilized by inserting first order phase delay to frequency above LC resonance frequency to further compensate it.

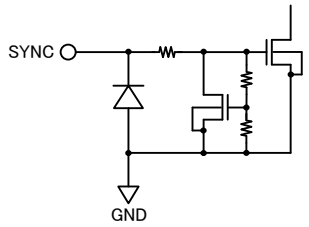
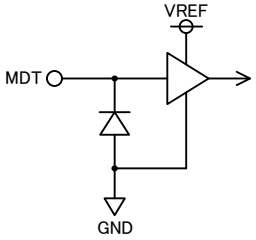
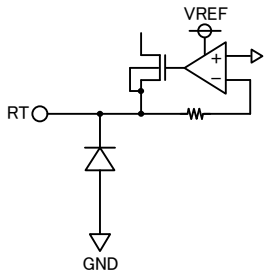
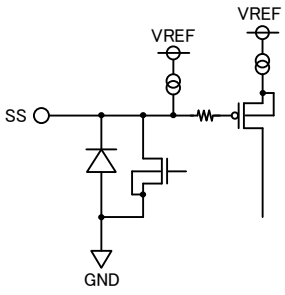
Phase Delay $fp2 = \frac{1}{2\times\pi\times R_1\times C_1}$ [Hz]

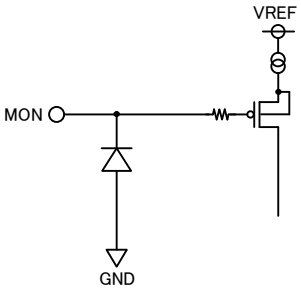
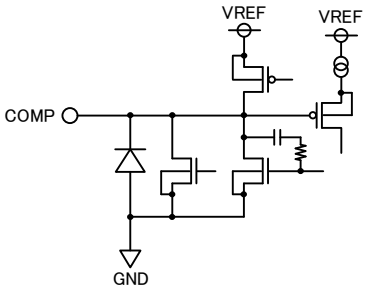
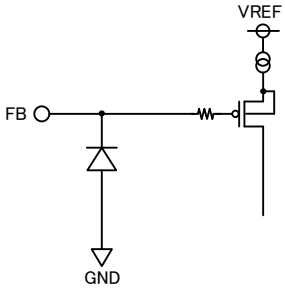
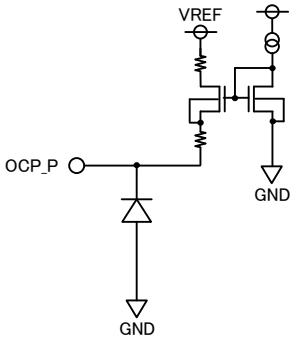
PCB Layout

Consider the following general points to bring out the IC performance.

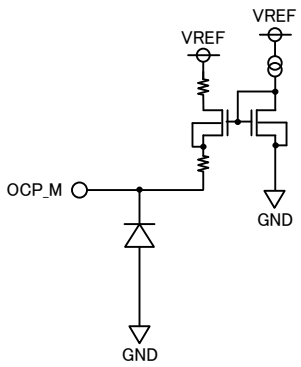
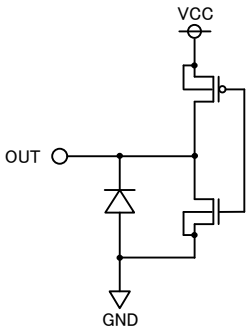
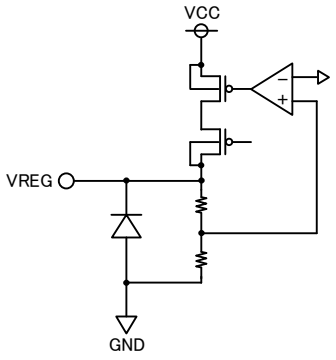
1. Each input of the OCP_P pin and the OCP_M pin are very sensitive. Consider the above-mentioned contents.
2. For noise caused by parasitic capacitance coupling, consider routing by keep distance to providing a buffer zone. Especially wiring those are sensitive to noise such as the OCP_P pin, the OCP_M pin and the COMP pin.
3. Near the OCP_P pin, the OCP_M pin and phase compensation circuit need to set pre-pattern about capacitor as insurance.
4. Place the bypass capacitor near the input of the IC, FET, and Di and wire it as short as possible.
5. Be careful not to have common impedance to high current system with analog system VCC (GND).

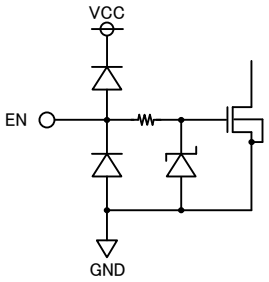
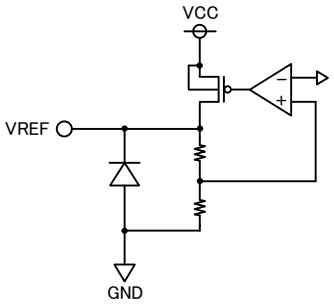
I/O Equivalence Circuit

Pin No.	Pin Name	Pin Equivalence Circuit
1	SYNC	
2	MDT	
3	RT	
4	SS	

Pin No.	Pin Name	Pin Equivalence Circuit
5	MON	
6	COMP	
7	FB	
8	OCP_P	

I/O Equivalence Circuit - continued

Pin No.	Pin Name	Pin Equivalence Circuit
9	OCP_M	
11	OUT	
12	VREG	

Pin No.	Pin Name	Pin Equivalence Circuit
14	EN	
15	VREF	
16	PGDB