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STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	8 Channel Switching Regulator Controller and 1 Series Regulator for DVC
PRODUCT SERIES	BD9833KV
PRODUCT SERIES FEATURES	BD9833KV8 DC/DC controller,1 Series Regulator

Series Regulator: Variable output voltage

stable with Ceramic Output Capacitor

Package: VQFP48C(0.5mm pitch)

OAbsolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Units
Power Supply Voltage1	VCC, VIN2345, VIN6789	12	V
Power Supply Voltage2	VIN1	12	V
Power Dissipation	Pd	600(*1) 950(*2)	mW mW
Operating Temperature	Topr	-25~+85	°C
Storage Temperature	Tstg	-55~+125	°C

(*1) Without external heat sink, the power dissipation degrades by $6.0 \text{mW/}^{\circ}\text{C}$ above 25°C .

(*2) Power dissipation degrades by 9.5mW/°C above 25°C, when mounted on a PCB (70.0mm × 70.0mm × 1.6mm).

ORecommended operating conditions (Ta=-25~+75°C)

Parameter	Symbol	Spec.	Units
Power Supply Voltage	VCC,VIN2345,VIN6789 VIN1	4.0~10 2.8~10	V
Oscillator Frequency	fosc	100kHz~1.2MHz	

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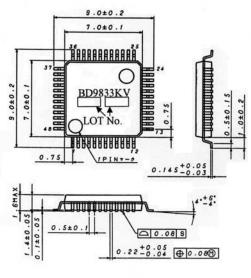


OElectrical characteristics (Ta=25°C, VCC=7V, VIN1=7V STB=3V, unless otherwise specified)

Parameter	Symbol	Min	Spec.	Maria	Units	Conditions.
DC/DC controller		Min.	Тур.	Max		
Controller						
Reference Voltage	Vref	2.475	2.500	2.525	V	1
Line Regulation	DVLi	-	-	10	mV	Vcc=4.0V~10V
Load Regulation	DVLo	-	-	10	mV	Iref=-0.1mA~ -1.0mA
Short-Circuit Output Current	los	-40	-12	-5	mA	Vref=0V
[Load Regulation]		1	I			h
Short-Circuit Output Current1(VCC)	Vstd1	3.55	3.65	3.75	V	VCC monitor Sweep down
Hysteresis width (VCC)	∆Vst1	0.6	0.11	0.16	V	
Threshold Voltage 2(VREF)	Vstd2	2.2	2.3	2.4	V	VREF monitor
Soft start] Soft standby voltage	Vecal	-	10	100	m\/	
Input Source Current	Vsso1 ISOFT1	-2.0	10 -1.0	100 -0.5	mV μA	
[Protection Circuit]	100111	-2.0	-1.0	-0.5	μ	
NV Threshold Voltage	Vscpth	0.65	0.75	0.85	v	CH2,3,4,5,6,7, INV Voltage"L" detect
SCP Output Current	lscp	-3.0	-2.0	-1.5	μA	VSCP=0.75V
SCP Threshold Voltage	Vtsc	1.4	1.5	1.6	V	
SCP Standby Voltage	Vssc	-	10	100	mV	
Triangular wave oscillator]						
Oscillator Frequency	fosc	580	680	780	kHz	RT=11kohm,CT=180pF
Frequency Stability (Vcc)	Df	-	0.3	2	%	VCC=4.0~10V
RT Output Voltage	VRT	0.95	1.00	1.05	V	
DC/DC controller		0.000		1 6 6 6	11	
Reference Voltage	Vthea	0.980	1.00	1.020	V	CH2,3,4,5,6,7 CH8,9
Reference Voltage	VOFST	-	-	10	mV	CH2,3,4,5,6,7 INV pin
ine Regulation	Ibias1 Ibias2	-150 -170	0 -40	150	nA nA	CH8,9 INV pin
Short-Circuit Output Current	Ibias2	-170	-40	-	nA	CH8,9 NON pin
	AV	50	-40 65	80	dB	DC Design
Load Regulation			1		-	Guarantee AV=0dB
Short-Circuit Output Current1(VCC)	BW	0.5	1	2	MHz	Design Guarantee
Hysteresis width (VCC)	Vfbh	Vref -0.1	-	-	V	
Threshold Voltage 2(VREF)	Vfbl	-	-	0.1	V	
[Soft start]	Isink1	1.3	2.6	3.9	mA	
Soft standby voltage	lsink2	3.4	6.7	10	mA	
Protection Circuit	Isource1	-240	-150	-90	μΑ	
INV Threshold Voltage	Isource2 VCM	-280 0	-190	-130 VCC-2	μA V	
[PWM Comparator]	VOIVI	0	-	V00-2	v	
nput Threshold Voltage	Vt0	1.730	1.820	1.910	٧	DUTY0%
2,3,4,5,6,7,8,9	Vt100	2.090	2. 180	2. 270	٧	DUTY100%
[FET Driver]	RonH11	7	14	21	Ω	VG2, 3, 4, 5, 6, 7, 8, 9 VG="H"
ON Resistance	RonL01	6	14	18	Ω	VG2, 3, 4, 5, 6, 7, 8, 9 VG="L"
	Isink1	70	170	250	mA	VG2, 3, 4, 5, 6, 7, 8, 9 VG="L"
Current Ability	l source1	-240	-160	-80	mA	VG2, 3, 4, 5, 6, 7, 8, 9 VG="H"
[Control]						•
STB Threshold Voltage	Vstb	1.0	1.5	2.0	V	
STB Input Current STB5,6 Threshold Voltage	lstb Vstb5.6	-	- 1.5	30	μA V	STB=3V
STB5,6 Input Current	Istb5,6	1.0	1.5	2.0	μA	STB5, 6=3V
[Circuit Current]	13150, 0			00	μΛ	0100, 0-01
Standby Current	lccs	-	0	5	μA	STB=0V
Circuit Current on Driving	lcc	1	5	10	mA	
Series Regulator]						P1-200KO P2-100KODafaz +
Output Voltage	Vo1	2. 94	3.00	3.06	۷	R1=200K Ω , R2=100K Ω Refer to be figure
Reference Voltage	VFB1	0. 98	1.00	1.02	V	
Output Current Ability	lo1	300	-	-	mA	VIN1=VOUT1x0.97,
	DV1	70	120	250	mV	IOUT1=20mA VIN1=4V to10V
The Difference between Input voltage and output voltage						
The Difference between Input voltage and output voltage	DVLi11	-	4	10	mV	10UT1=100mA
The Difference between Input voltage and output voltage .ine Regulation11		-	4	10	mV mV	VIN1=3.5V to10V IOUT1=10mA
The Difference between Input voltage and output voltage .ine Regulation11 .ine Regulation12 .oad Regulation1	DVLi11 DVLi12 DVLo1		4	10 30	mV mV	VIN1=3.5V to10V IOUT1=10mA IOUT1=1mA to 100mA
The Difference between Input voltage and output voltage .ine Regulation11 .ine Regulation12 .oad Regulation1 .oad Regulation2	DVLi11 DVLi12 DVLo1 DVLo2	- - -	4 10 30	10 30 90	mV mV mV	VIN1=3.5V to10V IOUT1=10mA IOUT1=1mA to 100mA IOUT1=1mA to 300mA
The Difference between Input voltage and	DVLi11 DVLi12 DVLo1		4	10 30	mV mV	VIN1=3.5V to10V IOUT1=10mA IOUT1=1mA to 100mA

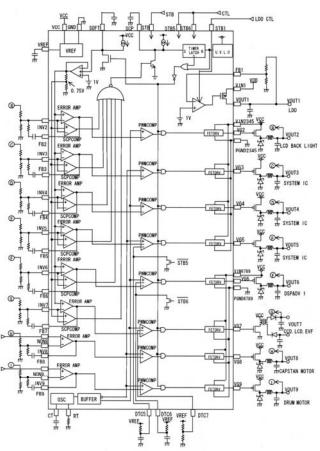


OPackage Dimensions



VQFP48C (Unit:mm)

OBlock Diagram



OPin Description 番号 端子名 機能 Error Amp inverted input (CH5) 1 INV5 Error Amp output (CH5) 2 FB5 Error Amp inverted input (CH6) 3 INV6 Error Amp output (CH6) 4 FB6 5 Error Amp inverted input(CH7) INV7 Error Amp output (CH7) 6 FB7 Error Amp non-inverted input (CH8) 7 NON8 Error Amp inverted input (CH8) 8 INV8 Error Amp output (CH8) 9 FB8 Error Amp non-inverted input (CH9) 10 NON9 Error Amp inverted input (CH9) 11 INV9 Error Amp output (CH9) 12 FB9 FET Driver Output (CH9) 13 VG9 FET Driver Output (CH8) 14 VG8 Power supply for the output circuit (CH6,7,8,9) 15 VIN6789 Power Ground for the output circuit (CH6,7,8,9) 16 PGND6789 FET Driver Output (CH7) 17 VG7 18 VG6 FET Driver Output (CH6) FET Driver Output (CH5) 19 VG5 FET Driver Output (CH4) VG4 20 Power supply for the output circuit (CH2,3,4,5) 21 VIN2345 PGND2345 Power Ground for the output circuit (CH2,3,4,5) 22 23 FET Driver Output (CH3) VG3 FET Driver Output (CH2) 24 VG2 Error Amp output (CH2) 25 FB2 26 INV2 Error Amp inverted input (CH2) Error Amp output (CH3) 27 FB3 INV3 Error Amp inverted input (CH3) 28 SW for CH2~9, Hi: Operating 29 STB Ground 30 GND Error Amp output (CH4) 31 FB4 Error Amp inverted input (CH4) 32 INV4 33 STB5 SW for CH5, Hi: Operating SW for CH6, Hi: Operating 34 STB6 SW for CH1, Hi: Operating 35 STB1 Series Regulator Output 36 VOUT1 Power supply for Series Regulator 37 VIN1 Amp inverted input 38 FB1 Non-Connected pin N. C. 39 A capacitor is placed to set up the delay time of the SCP 40 SCP

Soft start/This pin connects to a capacitor to

A capacitor is to set up the triangular-wave frequency

A resistor is to set up the triangular-wave frequency

Dead time control pin for CH7.And this pin connects to a

set up the start-up time

Power supply for DC/DC

Reference Voltage Output pin

Dead time control pin for CH5

Dead time control pin for CH6

capacitor to set up the start-up time.

41

42

43

44

45

46

47

48

SOFT

VREF

VCC

СТ

RT

DTC5

DTC6

DTC7



OOperation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC

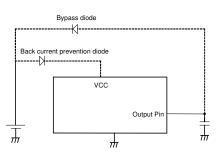
- 5) Operation in a strong electromagnetic field
- Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction. 6) Thermal shutdown circuit (TSD circuit)

This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

7) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during a ssembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. 8) Common impedance

- Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance). 9) Applications with modes that reverse VCC and pin potentials may cause damage to internal IC circuits.
- For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.



10) Timing resistor

Timing resistor connected between RT and GND, has to be placed near RT terminal (45pin). With the connection must be as short as possible.

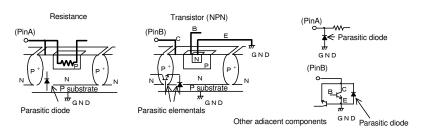
11) IC pin input

This monolithic IC contains P+ isolation and PCB layers between adjacent elements in order to keep them isolated.

P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when a resistor and transistor are connected to pins as shown in follow chart,

O the P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN). O Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input and output pins.



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