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ROHM Switching Regulator Solutions

# Evaluation Board: Step-down Switching Regulator With Built-in Power MOSFET

**BD9673EFJ / BD9876EFJ (5V | 1.5A / 2.75A Output)**

No.0000000013

## ●Introduction

This application note will provide the steps necessary to operate and evaluate ROHM's step-down switching regulator using the BD9673EFJ/BD9876EFJ evaluation boards. Component selection, board layout recommendations, operation procedures and application data is provided.

## ●Description

This evaluation board has been developed for ROHM's step-down switching regulator customers evaluating BD9673EFJ and/or BD9876EFJ. While accepting a wide power supply of 7-42V, a step down output of 1.2V/1.8V/3.3V/5V or any other user defined voltage can be produced. The ICs have an internal 200mohm Nch MOSFET (3.5A max) and a synchronization frequency range of 200 kHz to 500 kHz. A Soft Start circuit prevents in-rush current during startup along with UVLO (low voltage error prevention circuit) and TSD (thermal shutdown detection) protection circuits. An EN pin allows for simple ON/OFF control of the IC to reduce standby current consumption.

## ●Applications

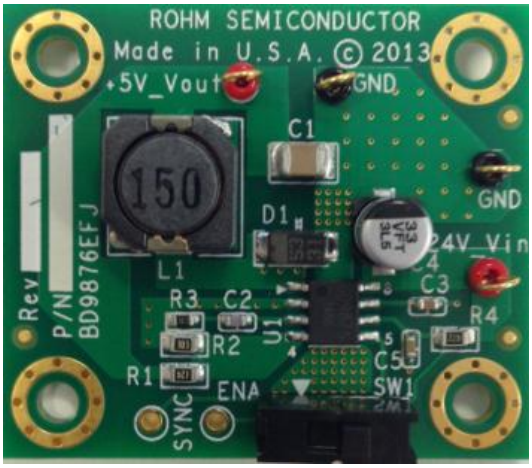
For general devices that have 12V/24V lines

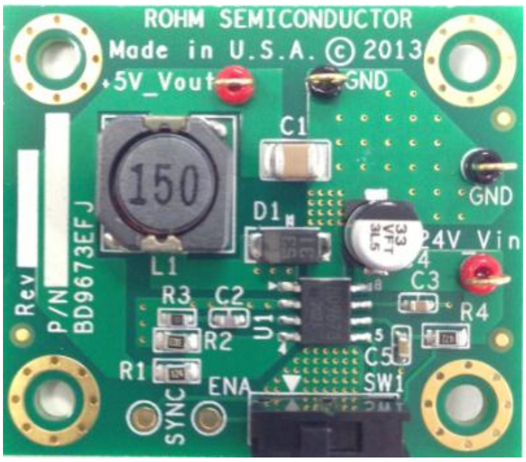
## ●Evaluation Board Operating Limits and Absolute Maximum Ratings

| Parameter | | Symbol | Limit | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | |
| **Supply Voltage** | | | | | | | |
| | BD9673EFJ | VCC | 7 | - | 24 | V | 24V for Eval board operation |
| | BD9876EFJ | VCC | 7 | - | 24 | V | 24V for Eval board operation |
| **Output Voltage / Current** | | | | | | | |
| | BD9673EFJ | VOUT | 1* | - | VCCx0.7 | V | *Restricted by minimum on pulse typ. 200ns |
| | BD9876EFJ | VOUT | 1* | - | VCCx0.7 | V | *Restricted by minimum on pulse typ. 200ns |
| | BD9673EFJ | IOUT | - | - | 1.5 | A | |
| | BD9876EFJ | IOUT | - | - | 2.75 | A | |

## ●Evaluation Board

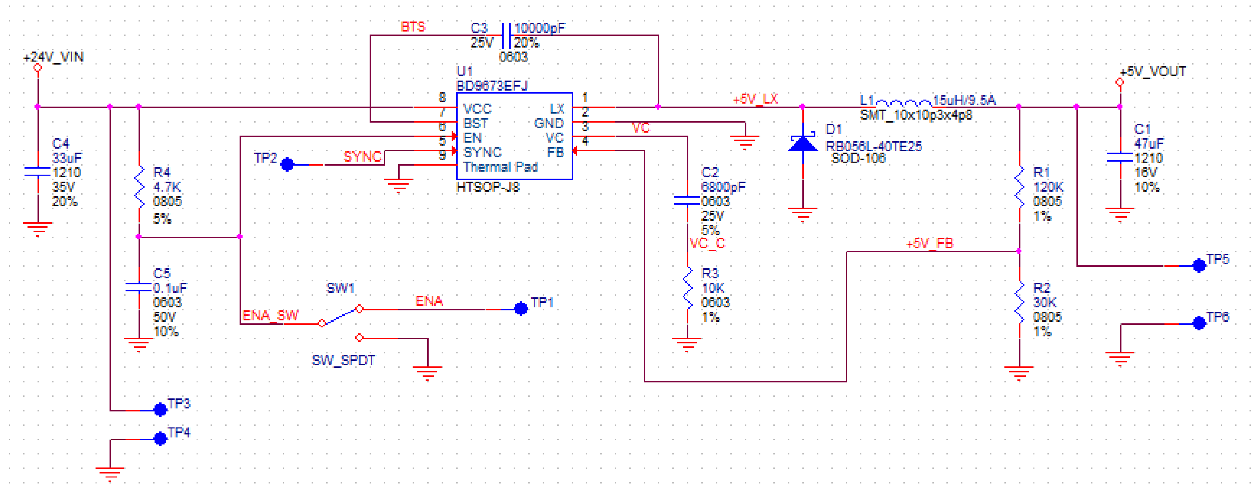
Below is the evaluation board with the BD9673EFJ. BD9876EFJ eval board uses the same components and board layout



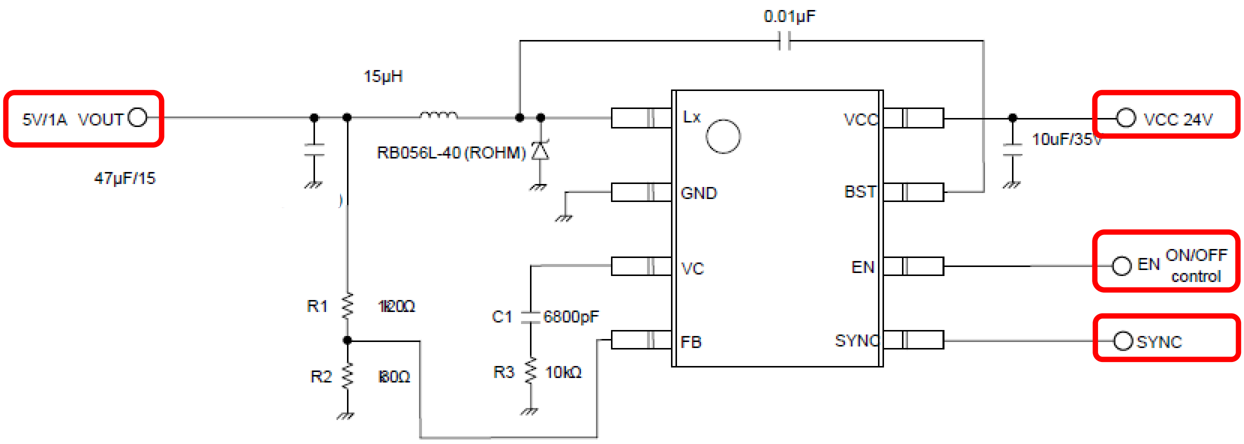
## ●Evaluation Board Schematic

Below is the evaluation board schematic for BD9673EFJ. BD9876EFJ eval board uses the same schematic




## ●Evaluation Board I/O

Below is the reference application circuit that shows the inputs (Vcc, EN and Sync) and the output (Vout)



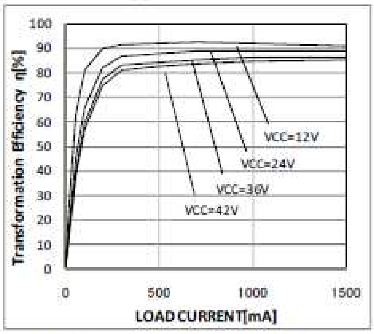

## ●Evaluation Board Operation Procedures

Below is the procedure to operate the evaluation board

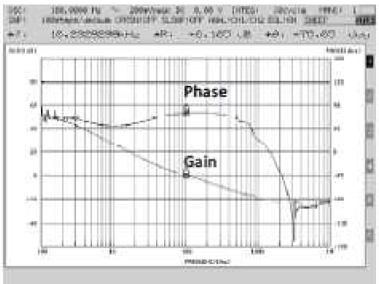
1. Connect GND to a GND pin on the evaluation board
2. Connect Vcc to the +24V_Vin pin. This will provide Vcc to the Vcc pin of the IC
    i. Note: EN pin is pulled high as default
3. Now output power can be measured from the +5V_Vout pin on the evaluation board with a load attached. The load can be increased up to 2.75A MAX.

**●Reference Graphs Application Data for BD9673EFJ**

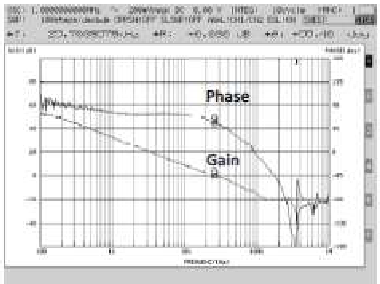
Below graphs show efficiency, frequency response and load characteristics of the BD9673EFJ eval board.



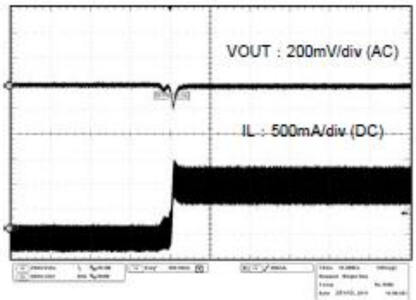

Electric Power Conversion Rate



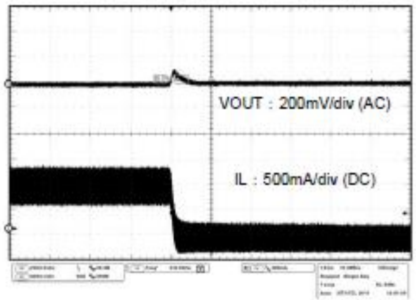

Frequency Response Characteristics(Io=0.5A)



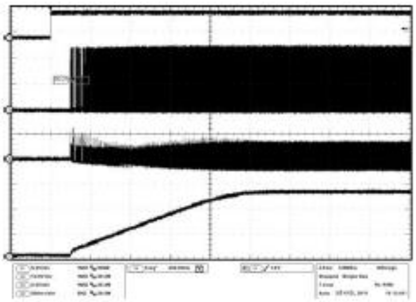

Frequency Response Characteristics (Io=1.0A)




Load Response Characteristics (Io=0A→1.5A)

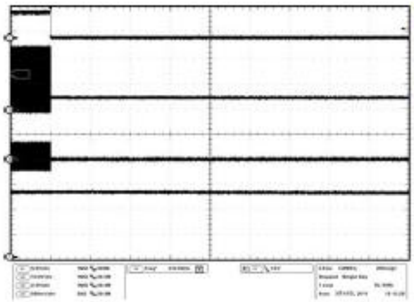



Load Response Characteristics (Io=1.5A→0A)



EN : 5V/div (DC)
LX : 10V/div (DC
IL : 0.5A/div (DC)
VOUT : 2V./div (DC)

startup Waveform

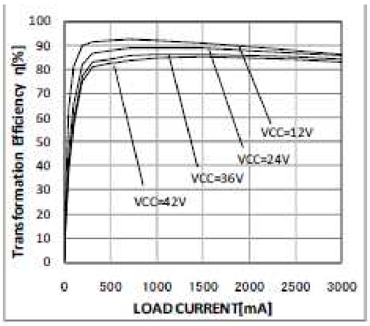


EN : 5V/div (DC)
LX : 10V/div (DC
IL : 0.5A/div (DC)
VOUT : 2V./div (DC)

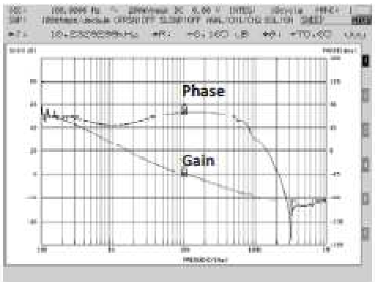
Stop Waveform

**●Reference Graphs Application Data for BD9876EFJ**

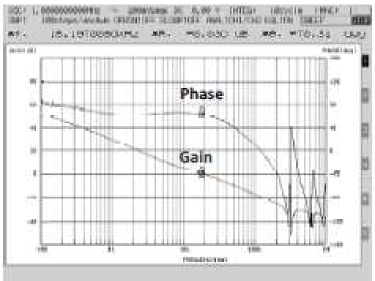
Below graphs show efficiency, frequency response and load characteristics of the BD9876EFJ eval board.



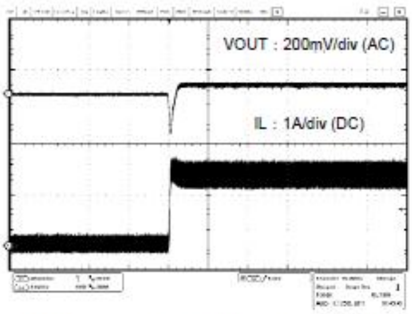

Electric Power Conversion Rate



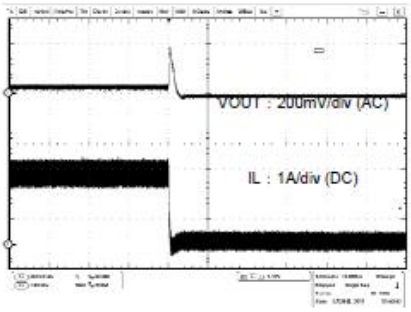

Frequency Response Characteristics (Io=0.5A)



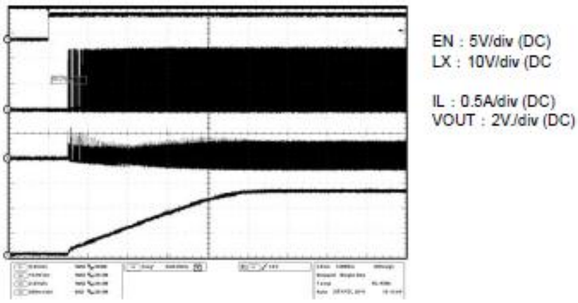

Frequency Response Characteristics (Io=3.0A)



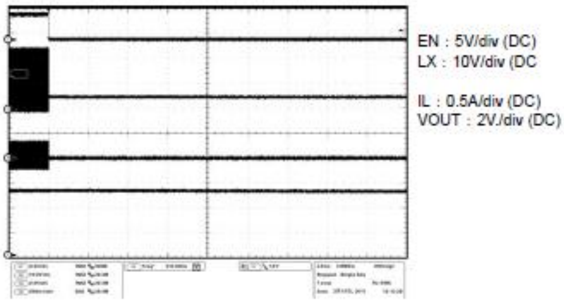

Load Response Characteristics (Io=0A→3.0A)




Load Response Characteristics (Io=3.0A→0A)




startup Waveform

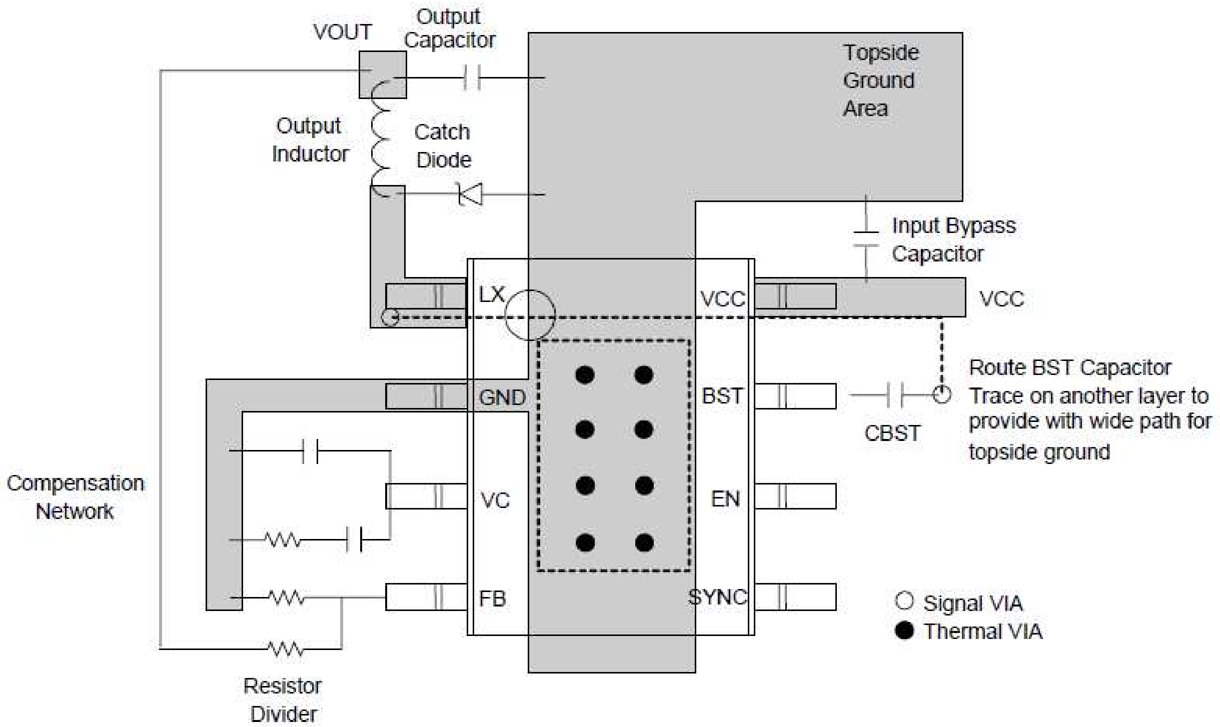



Stop Waveform

## ●Evaluation Board Layout Guidelines

Below are the guidelines that have been followed and recommended for BD9673 and BD9876 designs

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VCC pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VCC pin, and the anode of the catch diode. See Fig.28 for a PCB layout example. The GND pin should be tied directly to the thermal pad under the IC and the thermal pad.
The thermal pad should be connected to any internal PCB ground planes using multiple VIAs directly under the IC. The LX pin should be routed to the cathode of the catch diode and to the output inductor. Since the LX connection is the switching node, the catch diode and output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts; however this layout has been shown to produce good results and is meant as a guideline.




Note:

For applications operating at or near maximum voltage conditions (45V max.), additional precautions regarding heat dissipation need to be considered during board layout. The provided evaluation board is a 2-layer board meant for evaluation purposes only. At maximum conditions, the IC's internal thermal shutdown detection circuit will be potentially initiated and the output disabled until the junction temperature falls. For final designs operating near these conditions, we recommend using one of the below PCB options for better heat dissipation of the IC.

1) Use of a 4-layer PCB with internal GND planes connected to the IC GND pins
2) Use of a 2-layer PCB with a heat sink attached to the IC package
3) Use of a 2-layer PCB with a copper plane (>1oz) attached to the IC

## ●Application Components Selection Method

(1) Inductor

Something of the shield Type that Fulfills the Current Rating (Current value Ipecac below), with low DCR (Direct Current Resistance element) is recommended.
Value of Inductor influences Inductor Ripple Current and becomes the cause of Output Ripple.
In the same way as the formula below, this Ripple Current can be made small for as big as the L value of Coil or as high as the Switching Frequency.

$$I_{peak} = I_{out} + \Delta IL/2 \ [A] \qquad (1)$$

$$\Delta IL = \frac{V_{in}-V_{out}}{L} \times \frac{V_{out}}{V_{in}} \times \frac{1}{f} \ [A] \qquad (2)$$

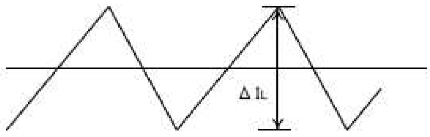


Fig.29 Inductor Current

(η: Efficiency, ΔIL: Output Ripple Current, f: Switching Frequency )

For design value of Inductor Ripple Current, please carry out design tentatively with about 20%～50% of Maximum Input Current.

※When current that exceeds Coil rating flows to the coil, the Coil causes a Magnetic Saturation, and there are cases wherein a decline in efficiency, oscillation of output happens. Please have sufficient margin and select so that Peak Current does not exceed Rating Current of Coil.

(2) Output Capacitor

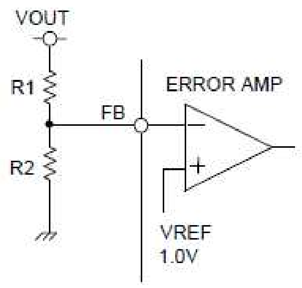
In order for Capacitor to be used in Output to reduce Output Ripple, Low Ceramic Capacitor of ESR is recommended.
Also, for Capacitor Rating, on top of putting into consideration DC Bias Characteristics, please use something whose Maximum Rating has sufficient margin with respect to the Output Voltage.
Output Ripple Voltage is looked for using the following formula.

$$V_{pp} = \Delta IL \times \frac{1}{2\pi \times f \times C_o} + \Delta IL \times R_{ESR} \quad [V] \quad \cdot\cdot\cdot \ (3)$$

Please design in a way that it is held within Capacity Ripple Voltage.

(3) Output Voltage Setting

ERROR AMP internal Standard Voltage is 1.0V. Output Voltage is determined as seen in (4) formula.




$$V_o = \frac{(R1+R2)}{R2} \times 1.0 \ [V] \quad \cdot\cdot\cdot \ (4)$$

Fig.30 Voltage Return Resistance Setting Method

(4) Boost Capacitor

Please connect CBST = 0.01μF (Laminate Ceramic Capacitor) between BST Pin-Lx Pins as Output capacitors of Gate Drive Voltage Generator REG(5V).

(5) About Adjustment of DC/DC Comparator Frequency Characteristics
Role of Phase compensation element CC1, CC2, RC (See P.7. Example of Reference Application Circuit)

Stability and Responsiveness of Loop are controlled through VC Pin which is the output of Error Amp.
The combination of zero and pole that determines Stability and Responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the VC Pin.

DC Gain of Voltage Return Loop can be calculated for using the following formula.

$$Adc = RI \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{VOUT}$$

Here, VFB is Feedback Voltage (1.0V).$A_{EA}$ is Voltage Gain of Error amplifier (typ: 77dB),
Gcs is the Trans-conductance of Current Detect (typ: 10A/V), and RI is the Output Load Resistance value.

There are 2 important poles in the Control Loop of this DC/DC.
The first occurs with/ through the output resistance of Phase compensation Capacitor (C1) and Error amplifier.
The other one occurs with/through the Output Capacitor and Load Resistor.
These poles appear in the frequency written below.

$$fp1 = \frac{G_{EA}}{2\pi \times C1 \times A_{EA}}$$

$$fp2 = \frac{1}{2\pi \times COUT \times RI}$$

Here, $G_{EA}$ is the trans-conductance of Error amplifier (typ: 220 μA/V).

Here, in this Control Loop, one zero becomes important. With the zero which occurs because of Phase compensation Capacitor C1 and Phase compensation Resistor R3, the Frequency below appears.

$$fz1 = \frac{1}{2\pi \times C1 \times R3}$$

Also, if Output Capacitor is big, and that ESR (RESR) is big, in this Control Loop, there are cases when it has an important, separate zero (ESR zero).
This ESR zero occurs due to ESR of Output Capacitor and Capacitance, and exists in the Frequency below.

$$fz_{ESR} = \frac{1}{2\pi \times COUT \times RESR} \qquad \text{(ESR zero)}$$

In this case, the 3rd pole determined with the 2nd Phase compensation Capacitor (C2) and Phase Correction Resistor (R3) is used in order to correct the ESR zero results in Loop Gain.
This pole exists in the frequency shown below.

$$fp3 = \frac{1}{2\pi \times C2 \times R3} \qquad \text{(Pole that corrects ESR zero)}$$

The target of Phase compensation design is to create a communication function in order to acquire necessary band and Phase margin.

Cross-over Frequency (band) at which Loop gain of Return Loop becomes "0" is important.
When Cross-over Frequency becomes low, Power supply Fluctuation Response, Load Response, etc worsens.
On the other hand, when Cross-over Frequency is too high, instability of the Loop can occur.
Tentatively, Cross-over Frequency is targeted to be made 1/20 or below of Switching Frequency.

Selection method of Phase Compensation constant is shown below.

1. Phase Compensation Resistor (R3) is selected in order to set to the desired Cross-over Frequency.
   Calculation of RC is done using the formula below.

$$R3 = \frac{2\pi \times COUT \times fc}{G_{EA} \times GCS} \times \frac{VOUT}{V_{FB}}$$

   Here, fc is the desired Cross-over Frequency. It is made about 1/20 and below of the Normal Switching Frequency (fs).

2. Phase compensation Capacitor (C1) is selected in order to achieve the desired phase margin.
   In an application that has a representative Inductance value (about several µH～20µH), by matching zero of compensation to 1/4 and below of the Cross-over Frequency, sufficient Phase margin can be acquired. C1 can be calculated using the following formula.

$$C1 > \frac{4}{2\pi \times R3 \times fc}$$

   RC is Phase compensation Resistor.

3. Examination whether the second Phase compensation Capacitor C2 is necessary or not is done.
   If the ESR zero of Output Capacitor exists in a place that is smaller than half of the Switching Frequency, a second Phase compensation Capacitor is necessary. In other words, it is the case wherein the formula below happens.

$$\frac{1}{2\pi \times COUT \times RESR} < \frac{fs}{2}$$

   In this case, add the second Phase compensation Capacitor C2, and match the frequency of the third pole to the Frequency fp3 of ESR zero.

   C2 is looked for using the following formula.

$$C2 = \frac{COUT \times RESR}{R3}$$

●**Evaluation Board BOM**

Below is a table with the build of materials. Part numbers and supplier references are provided.

| Item | Qty | Ref | Description | Manufacturer | Part Number |
|---|---|---|---|---|---|
| 1 | 1 | C1 | CAP, CER, 1210, 16 V, 20%, 47 µF | Murata | GRM32ER61C476ME15L |
| 2 | 1 | C2 | CAP, CER, 0603, NP0, 25 V, 5%, 6800 pF | TDK Corporation | C1608C0G1E682J |
| 3 | 1 | C3 | CAP, CER, 0603, X7R, 25 V, 20%, 10000 pF | TDK Corporation | C1608X7R1E103M |
| 4 | 1 | C4 | CAP, ALUM, SMD, 20%, 35 V, 33 µF | Panasonic Corp | EEE-FT1V330AR |
| 5 | 1 | C5 | CAP, CER, 0603, X7R, 50 V, 10%, 0.1 µF | AVX Corporation | 06035C104KAT2A |
| 6 | 1 | D1 | SBD, PMDS / SOD-106, 40 V, 3 A | ROHM Semiconductor | RB056L-40TE25 |
| 7 | 1 | L1 | INDUCTOR SMD 15UH 3.60A 100KHZ | Signal Transformers | SCRH105RY-150 |
| 8 | 1 | R1 | RES, SMD, 0805, 1/8 W, 5%, 120 kΩ | ROHM Semiconductor | MCR10EZPJ124 |
| 9 | 1 | R2 | RES, SMD, 0805, 1/8 W, 5%, 30 kΩ | ROHM Semiconductor | MCR10EZPJ303 |
| 10 | 1 | R3 | RES, SMD, 0603, 1/8 W, 5%, 10 kΩ | ROHM Semiconductor | MCR03EZPJ103 |
| 11 | 1 | R4 | RES, SMD, 0805, 1/8 W, 5%, 4.7 kΩ | ROHM Semiconductor | MCR10EZPJ472 |

*IC is not shown above. Either BD9673EFJ or BD9876EFJ will be used. Please check IC label on backside of PCB.

## Notes