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STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **ＢＤ９８８８Ｆ、ＢＤ９８８８ＦＶ**

FUNCTION
- 2ch control with Push-Pull
- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out
- Short circuit protection with over voltage
- Mode-selectable the operating or stand-by mode by stand-by pin
- Synchronous operating the other BD9888F or BD9888FV IC's
- BURST mode controlled by PWM and DC input
- Short circuit protection with voltage difference detection

○Absolute Maximum Ratings (Ta = 25℃)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply Voltage | VCC | 15 | V |
| Operating Temperature Range | Topr | -40～+90 | ℃ |
| Storage Temperature Range | Tstg | -55～+125 | ℃ |
| Power Dissipation | Pd | 600*1 (BD9888F) | mW |
| | | 850*2 (BD9888FV) | |
| Maximum Junction Temperature | Tjmax | +125 | ℃ |

*1 Pd derate at 6.0mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)
*2 Pd derate at 8.5mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○Recommended operating condition

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply voltage | VCC | 5.0～14.0 | V |
| CT oscillation frequency | fCT | 20～150 | kHz |
| BCT oscillation frequency | fBCT | 0.05～0.50 | kHz |

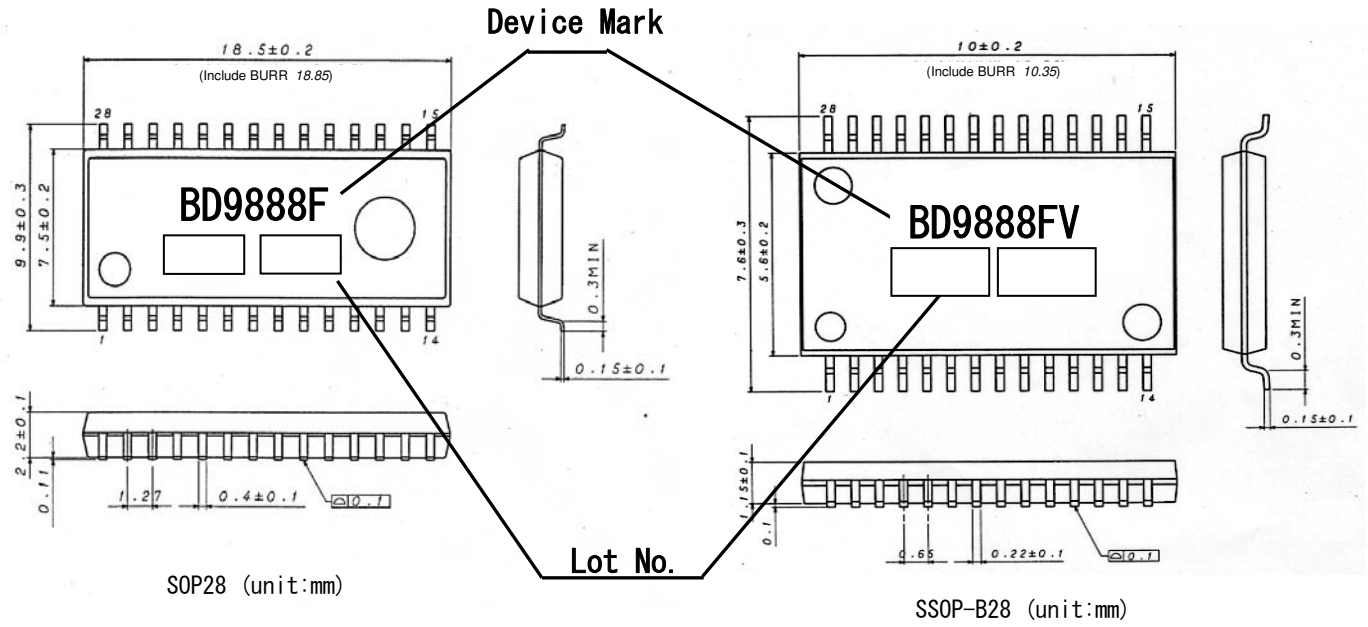
Status of this document
The Japanese version of this document is the official specification.
Please use the translation version of this document as a reference to expedite understanding of the official version.
If these are any uncertainty in translation version of this document, official version takes priority.

○Electric Characteristics (Ta=25℃, VCC=7V)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | | |
| ((WHOLE DEVICE)) | | | | | | |
| Operating current | Icc1 | — | 11.0 | 17.0 | mA | CT=0.5V |
| Stand-by current | Icc2 | — | 2 | 10 | μA | |
| ((OVER VOLTAGE DETECT)) | | | | | | |
| FB over voltage detect voltage | Vovf | 2.20 | 2.40 | 2.60 | V | |
| ((STAND BY CONTROL)) | | | | | | |
| Stand-by voltage H | VstH | 1.6 | — | VCC | V | System ＯＮ |
| Stand-by voltage L | VstL | -0.3 | — | 0.8 | V | System ＯＦＦ |
| Stand-by hysteresis | ⊿Vst | 0.08 | 0.18 | 0.28 | V | |
| ((TIMER LATCH)) | | | | | | |
| Timer Latch voltage | Vcp | 1.9 | 2.0 | 2.1 | V | |
| Timer Latch current | Icp | 0.5 | 1.0 | 1.5 | μA | |
| ((BURST MODE)) | | | | | | |
| BOSC Max voltage | VburH | 1.94 | 2.0 | 2.06 | V | $f_{BCT}$=0.2kHz |
| BOSC Min Voltage | VburL | 0.4 | 0.5 | 0.6 | V | $f_{BCT}$=0.2kHz |
| BOSC constant current | IBCT | 1.35/BRT | 1.5/BRT | 1.65/BRT | A | |
| BOSC frequency | fBCT | 266 | 280 | 294 | Hz | BRT=33kΩ、BCT=0.050μF |
| ((OSC BLOCK)) | | | | | | |
| OSC constant current | ICT | 1.35/RT | 1.5/RT | 1.65/RT | A | |
| OSC Max voltage | VoscH | 1.8 | 2.0 | 2.2 | V | $f_{CT}$=60kHz |
| OSC Min voltage | VoscL | 0.3 | 0.5 | 0.7 | V | $f_{CT}$=60kHz |
| MAX DUTY | MAXDUTY | 44 | 46.5 | 49 | % | $f_{CT}$=60kHz |
| Soft start current | Iss | 1.0 | 2.0 | 3.0 | μA | |
| IS COMP detect Voltage | Visc | 0.45 | 0.50 | 0.55 | V | |
| SS COMP detect voltage | Vss | 2.0 | 2.2 | 2.4 | V | |
| SRT ON resistance | RSRT | — | 200 | 400 | Ω | |
| ((UVLO BLOCK)) | | | | | | |
| Operating voltage | VuvloH | 4.100 | 4.300 | 4.500 | V | |
| Shut down voltage | VuvloL | 3.900 | 4.100 | 4.300 | V | |
| ((REG BLOCK)) | | | | | | |
| REG output voltage | VREG | 3.038 | 3.100 | 3.162 | V | |
| REG source current | IREG | 5.0 | — | — | mA | |
| VREF voltage | VREF | 1.225 | 1.250 | 1.275 | V | VREF=Open |
| ((FEED BACK BLOCK)) | | | | | | |
| IS threshold voltage | Vis | 1.225 | 1.250 | 1.275 | V | |
| VS threshold voltage | Vvs | 1.220 | 1.250 | 1.280 | V | |
| IS source current 1 | Iis1 | — | — | 1.5 | μA | DUTY=2.0V |
| IS source current 2 | Iis2 | 13.0 | 20.0 | 27.0 | μA | DUTY=0V、IS=0.5V |
| VS source current | Ivs | — | — | 1.0 | μA | |
| ((OUTPUT BLOCK)) | | | | | | |
| NAch output voltage H | VoutNAH | VCC-0.3 | VCC-0.1 | — | V | |
| NBch output voltage H | VoutNBH | VCC-0.3 | VCC-0.1 | — | V | |
| NAch output voltage L | VoutNAL | — | 0.1 | 0.3 | V | |
| NBch output voltage L | VoutNBL | — | 0.1 | 0.3 | V | |
| NAch output sink resistance | RsinkNA | — | 5 | 10 | Ω | Isink = 10mA |
| NAch output source resistance | RsourceNA | — | 8 | 16 | Ω | Isource = 10mA |
| NBch output sink resistance | RsinkNB | — | 5 | 10 | Ω | Isink = 10mA |
| NBch output source resistance | RsourceNB | — | 8 | 16 | Ω | Isource = 10mA |
| Drive output frequency | fOUT | 58.5 | 60.0 | 61.5 | KHz | RT=18kΩ、CT=395pF |
| ((COMP BLOCK)) | | | | | | |
| Under voltage detect | VCOMPL | 0.620 | 0.640 | 0.660 | V | |
| Voltage difference detect | ⊿VCOMP | 0.40 | 0.45 | 0.5 | V | \|$V_{COMPA}$-$V_{COMPB}$\| |

(This product is not designed to be radiation-resistant.)

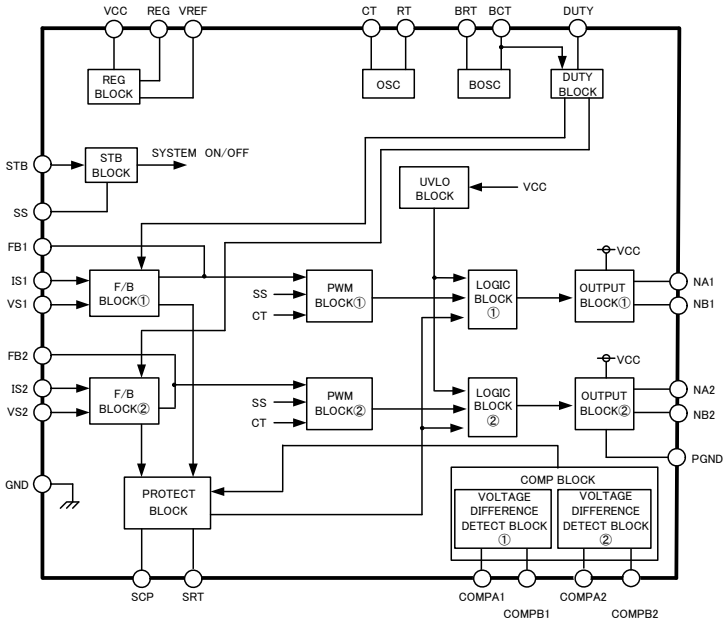
## ○Package Dimensions




SOP28 (unit:mm)

SSOP-B28 (unit:mm)

## ○Block Diagram




## ○Pin Description

| Pin No. | Pin Name | Function |
|---|---|---|
| 1 | DUTY | Control PWM mode and BURST mode |
| 2 | BRT | External resistor from BRT to GND for adjusting the BURST triangle oscillator |
| 3 | BCT | External capacitor from BCT to GND for adjusting the BURST triangle oscillator |
| 4 | RT | External resistor from SRT to RT for adjusting the triangle oscillator |
| 5 | SRT | External resistor from SRT to RT for adjusting the triangle oscillator |
| 6 | CT | External capacitor from CT to GND for adjusting the triangle oscillator |
| 7 | GND | GROUND |
| 8 | FB1 | Error amplifier output① |
| 9 | IS1 | Error amplifier input① |
| 10 | VS1 | Error amplifier input② |
| 11 | FB2 | Error amplifier output② |
| 12 | IS2 | Error amplifier input③ |
| 13 | VS2 | Error amplifier input④ |
| 14 | VREF | Reference voltage |
| 15 | COMPA1 | Voltage difference or under voltage detect for 1ch |
| 16 | STB | Stand-by switch |
| 17 | COMPB1 | Voltage difference or under voltage detect for 1ch |
| 18 | COMPA2 | Voltage difference or under voltage detect for 2ch |
| 19 | COMPB2 | Voltage difference or under voltage detect for 2ch. |
| 20 | REG | Internal regulator output |
| 21 | SS | External capacitor from SS to GND for Soft Start Control |
| 22 | SCP | External capacitor from SCP to GND for Timer Latch |
| 23 | NA2 | FET driver for 2ch |
| 24 | NB2 | FET driver for 2ch |
| 25 | PGND | Ground for FET drivers |
| 26 | NB1 | FET driver for 1ch |
| 27 | NA1 | FET driver for 1ch |
| 28 | Vcc | Supply voltage input |

○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and IC. Use adequate margins for steady state and transient characteristics.
2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within ±0.3V compared with the PGND pin.
6. BD9888F and BD9888FV incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
10. By STB voltage, BD9888F and BD9888FV are changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8～1.6).
11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
    This IC is a monolithic IC which (as shown is Fig-1) has $P^+$ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,
    - ○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
    - ○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

    Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.
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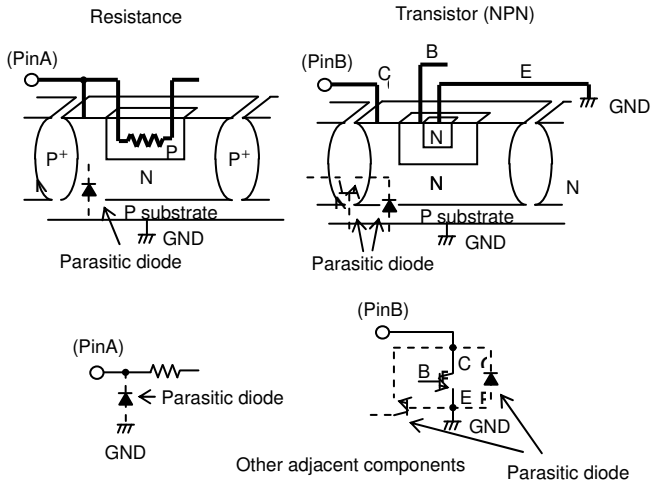


Fig-1 Simplified structure of a Bipolar IC

## Notes

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