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1 to 4-Cell Li-Ion Battery Manager For Application Processors

BD99954MWV, BD99954GW

■ General Description

BD99954 is a Battery Management LSI for 1-4 cell Lithium-Ion secondary battery, and available in a 40pin 0.40 mm pitch 5.0 mm x 5.0 mm QFN package and small 41-ball 0.4mm pitch 2.6mm x 3.0mm Wafer-Level CSP package which is designed to meet high degree demands for space-constraint equipment such as Low profile Notebook PC, Tablets and other applications.

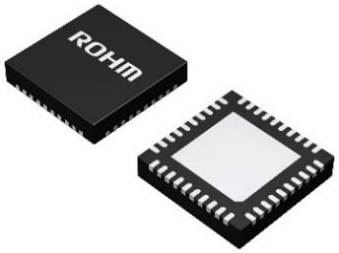
BD99954 provides a Dual-source Battery Charger, two port BC1.2 detection and a Battery Monitor with several alarm(INT#, PROCHOT#) outputs

■ Features

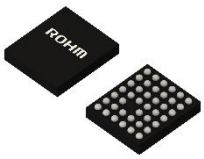
- **Dual-source Battery Charger**
  - High efficiency Step-Up/Down switching charger for 1-4 cell Li-Ion/Li-poly battery
  - Two separate input sources for USB-VBUS and DC adapter.
  - Two port BC1.2 detectors.
  - JEITA compliant charging profile
  - Programmable parameters for Preconditioning, Pre-charge current, and Fast-charge current
  - Programmable charging voltage
  - Programmable charge current
  - Programmable Switching Frequency: 600kHz to 1.2MHz
  - Support USB BCS 1.2, ACA, ID pin, OTG
  - USB-VBUS Over Voltage Protection
  - Over Voltage Battery Protection
  - Battery Short Circuit Detection
  - Power Path Management with charge pump gate driver
  - Flexibility power path control
  - Reverse Buck/Boost Option for USB/USB-PD
  - Bias voltage output for the external thermistor
  - PMON output
  - PROCHOT# output
  - Support Inhibit / Autonomous Charging
  - Battery Learn Function
  - Input Operating Range: 3.8V to 25V
- Voltage Measurement for Thermistor.
  - Bias voltage output for the external thermistor.
- SMBus Interface (Clock up friendly I2C) for Host communication
- Embedded OTPROM for initial settings

■ Packages

	Pitch	W	x D	x H
UQFN040V5050	0.4mm	5.0mm	x 5.0mm	x 1.0mm
UCSP55M3C 6 x 7balls	0.4mm	2.6mm	x 3.0mm	x 0.62mm



UQFN040V5050



UCSP55M3C

■ Applications

- Ultrabook
- Notebook PC
- Ultra-mobile PC
- Tablet PC

■ Structure

Silicon Monolithic Integrated Circuit

■ Line up matrix

Parts No.	Package
BD99954**MWV**	UQFN040V5050
BD99954**GW**	UCSP55M3C

Contents

Notation

Category	Notation	Description
Unit	V	Volt (Unit of voltage)
	A	Ampere (Unit of current)
	Ω, Ohm	Ohm (Unit of resistance)
	F	Farad (Unit of capacitance)
	deg., degree	degree Celsius (Unit of Temperature)
	Hz	Hertz (Unit of frequency)
	s (lower case)	second (Unit of time)
	Min	minute (Unit of time)
	b, bit	bit (Unit of digital data)
	B, byte	1 byte = 8 bits
Unit prefix	M, mega-, mebi-	2^{20} = 1,048,576 (used with “bit” or “byte”)
	M, mega-, million-	10^{6} = 1,000,000 (used with “Ω” or “Hz”)
	K, kilo-, kibi-	2^{10} = 1,024 (used with “bit” or “byte”)
	k, kilo-	10^{3} = 1,000 (used with “Ω” or “Hz”)
	m, milli-	10^{-3}
	μ, micro-	10^{-6}
	n, nano-	10^{-9}
	p, pico-	10^{-12}
Numeric value	xxh, xxH	Hexadecimal number. “x”: any alphanumeric of 0 to 9 or A to F.
	Xxb	Binary number; “b” may be omitted. “x”: a number, 0 or 1 “_” is used as a nibble (4-bit) delimiter. (e.g. “0011_0101b” = “35h”)
Address	#xxh	Address in a hexadecimal number. “x”: any alphanumeric of 0 to 9 or A to F.
Data	bit[n]	n-th single bit in the multi-bit data.
	bit[n:m]	Bit range from bit[n] to bit[m].
Signal level	“H”, High	High level (over V_{IH} or V_{OH}) of logic signal.
	“L”, Low	Low level (under V_{IL} or V_{OL}) of logic signal.
	“Z”, “Hi-Z”	High impedance state of 3-state signal.

Reference

Name	Reference Document	Release Date	Publisher
I2C-bus	“UM10204: I^2C-bus specification and user manual Rev. 4”	Feb. 13, 2012	NXP Semiconductors
SMBus	System Management Bus (SMBus) Specification 3.0	Dec. 20, 2014	SBS-IF
JEITA Profile	“A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook-type Personal Computers”	Apr. 10, 2007	JEITA
USB BC	“Battery Charging Specification Revision 1.2”	Dec. 7, 2010	USB.org
Smart Battery Charger	Smart Battery Charger Specification Revision 1.1	Dec. 11, 1998	SBS-IF
USB 2.0	Universal Serial Bus Specification Revision 2.0	Jul. 26, 2013	USB.org
USB 3.1	Universal Serial Bus Revision 3.1 Specification Rev. 1.0	Aug. 11, 2014	USB.org
USB PD	USB Power Delivery Specification Rev. 2.0 V1.0	Apr. 27, 2000	USB.org

1. Introduction

BD99954 is a Battery Manager IC for 1-4Cell Lithium-Ion / Lithium-Ion polymer secondary battery pack used in portable equipment such as Tablets, Ultra books or others.

BD99954 includes a Battery Charger, two port BC1.2 detection, a Battery Monitor for voltage, current, temperature and alarm(INT#, PROCHOT#) Controller. Figure 1-1 shows the Typical Application Circuit.

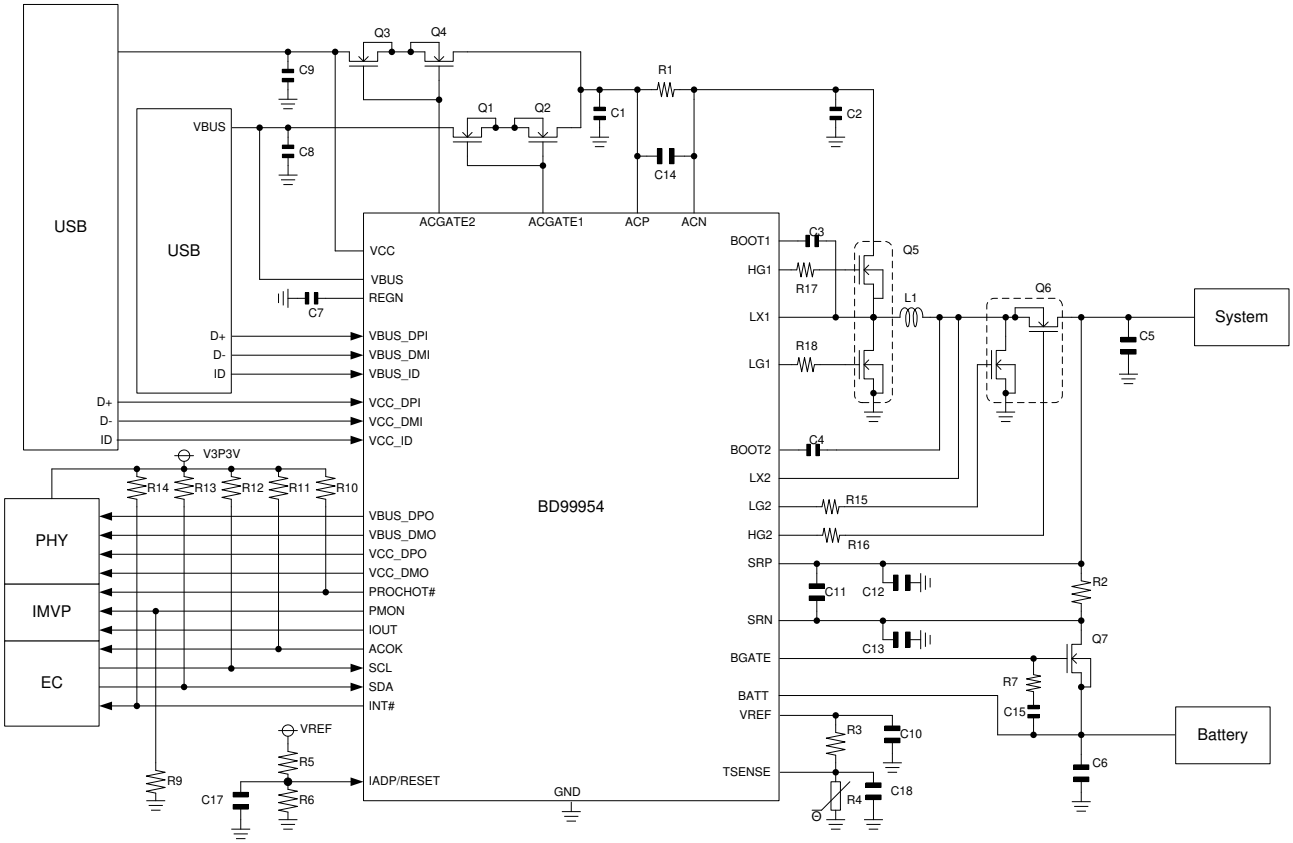


Figure 1-1 Block Diagram

2. Signal Description

Table 2-1 Signal Description

Pin No.	Ball No. [CSP]	Pin Name	Function
1	B2	VBUS	USB Power Supply
2	A2	VCC	DC Power Supply
3	D3	ACOK	AC adapter voltage detection open drain output.
4	A3	INT#	Interrupt for I2C
5	B3	PROCHOT#	Active low open drain output of “processor hot” indicator. The charger IC monitors events like adapter current, battery discharge current. Once any event in PROCHOT# profile is triggered, a minimum 10ms pulse is asserted.
6	A4	ACN	Input current sense resistor negative input.
7	A5	ACP	Input current sense resistor positive input.
8	B4	ACGATE1	Charge pump output to drive adapter input n-channel MOSFET s. The ACGATE1 voltage is 5V above VBUS during AC adapter insertion.
9	B5	ACGATE2	Charge pump output to drive adapter input n-channel MOSFET s. The ACGATE2 voltage is 5V above VCC during AC adapter insertion.
10	A6	IADP/RESET	Default Input Current Limit Setting pin and System resistor reset pin.
11	B6	VBUS_DMI	VBUS side USB D- Input / Output
12	C4	VBUS_DPI	VBUS side USB D+ Input / Output
13	C5	VBUS_DMO	VBUS side UDB D- Output / Input
14	C6	VBUS_DPO	VBUS side UDB D+ Output / Input
15	D5	VBUS_ID	VBUS side USB ID pin input
16	D6	VCC_DMI	VCC side USB D- Input / Output
17	D4	VCC_DPI	VCC side USB D+ Input / Output
18	E6	VCC_DMO	VCC side UDB D- Output / Input
19	F6	VCC_DPO	VCC side UDB D+ Output / Input
20	G6	VCC_ID	VCC side USB ID pin input
21	E5	SCL	SMBus Clock Input
22	F5	SDA	SMBus Data Input / Output
23	G5	PMON	Buffered total system power current output. Place a resistor between PMON pin and GND.
24	F4	IOUT	Buffered adapter or charge current output selectable with SMBus command.
25	G4	VREF	1.5V LDO Output
26	E3	TSENSE	Battery temperature monitor pin. Active low battery present input signal. LOW indicates battery is present, and HIGH indicates the battery is absent and the charging stop.
27	G3	BATT	Battery Voltage Input
28	F3	BGATE	Gate Control Output
29	G2	SRN	Charge current sense resistor negative input.
30	G1	SRP	Charge current sense resistor positive input.
31	F2	GND	Ground
32	F1	HG2	DC/DC Boost side High Side Gate Driver
33	E2	LX2	DC/DC Boost side Inductor Connection
34	E1	BOOT2	DC/DC Boost side Driver Voltage Output
35	D2	LG2	DC/DC Boost side Low Side Gate Driver
36	D1	LG1	DC/DC Buck side Low Side Gate Driver
37	C1	BOOT1	DC/DC Buck side Driver Voltage Output
38	C2	LX1	DC/DC Buck side Inductor Connection
39	B1	HG1	DC/DC Buck side High Side Gate Driver
40	A1	REGN	LDO Output

3. Pin Configuration

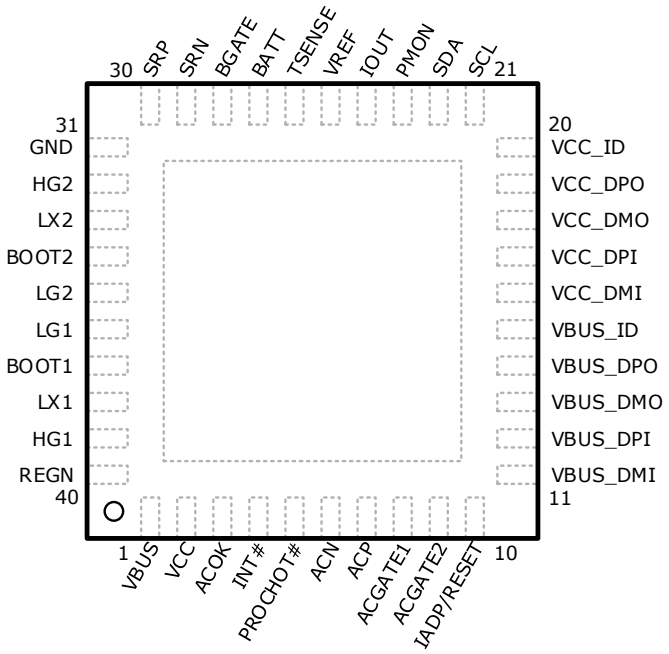


Figure 3-1 Pin Configuration in BD99954MWV (Top View)

	1	2	3	4	5	6
G	SRP	SRN	BATT	VREF	PMON	VCC_ID
F	HG2	GND	BGATE	IOUT	SDA	VCC_DPO
E	BOOT2	LX2	TSENSE	N/C	SCL	VCC_DMO
D	LG1	LG2	ACOK	VCC_DPI	VBUS_ID	VCC_DMI
C	BOOT1	LX1		VBUS_DPI	VBUS_DMO	VBUS_DPO
B	HG1	VBUS	PROCHOT#	ACGATE1	ACGATE2	VBUS_DMI
A	REGN	VCC	INT#	ACN	ACP	IADP/RESET

Figure 3-2 Pin Configuration in BD99954GW (Bottom View)

4. Absolute Maximum Rating

		Value
Voltage range (with respect to GND)	VBUS, VCC, SRN, SRP, ACN, ACP, BATT	-0.3 to 28V
	LX1, LX2	-2 to 28V
	ACGATE1, ACGATE2, BGATE, BOOT1, BOOT2, HG1, HG2	-0.3 to 32V
	LX1-BOOT1,LX2-BOOT2	-0.3 to 6V
	ACP-ACN, SRP-SRN	-0.3 to 0.3 V
	VBUS_DPI, VBUS_DMI, VBUS_ID, VBUS_DPO, VBUS_DMO, VCC_DPI, VCC_DMI, VCC_ID, VCC_DPO, VCC_DMO, ACOK, REGN, INT#, PROCHOT#, IOUT, PMON, SCL, SDA, LG1, LG2	-0.3 to 7.0 V
	TSENSE, IADP/RESET, VREF	-0.3 to 2.1 V
Junction temperature		150℃
Storage temperature		-50 to 150℃

5. Thermal Resistance (Note 1)

Parameter		Symbol	Thermal Resistance (Typ)			Unit
			1s(Note 4)	2s2p(Note5)	4s5p(Note7)	
	UQFN040V5050					
Junction to Ambient		θ_{JA}	113.6	24.5	-	°C/W
Junction to Top Characterization Parameter(Note 2)		Ψ_{JT}	8	3	-	°C/W
	UCSP55M3C					
Power	Dissipation(Note3)	θ_{JA}	-	-	0.97	W

*(Note 1)*Based on JESD51-2A(Still-Air) only BD99954MWV

*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Derate by 78.1mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board)

*(Note 4)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 5)*Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note6)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 6) This thermal via connects with the copper pattern of all layers..

*(Note 7)*Using a PCB board

Layer Number of Measurement Board	Material	Board Size
9 Layers	FR-4	63mm x 55mm x 1.6mmt

6. Recommended Operating Condition

	MIN	MAX	Unit
VBUS	3.8	25	V
VCC	3.8	25	V
BATT	0	19.2	V
IIN	-	16	A
ISYS	-	16	A
ICHARGE	-	16	A

Operating Temperature range	-30	85	℃

7. Function Descriptions

7.1. Block Diagram

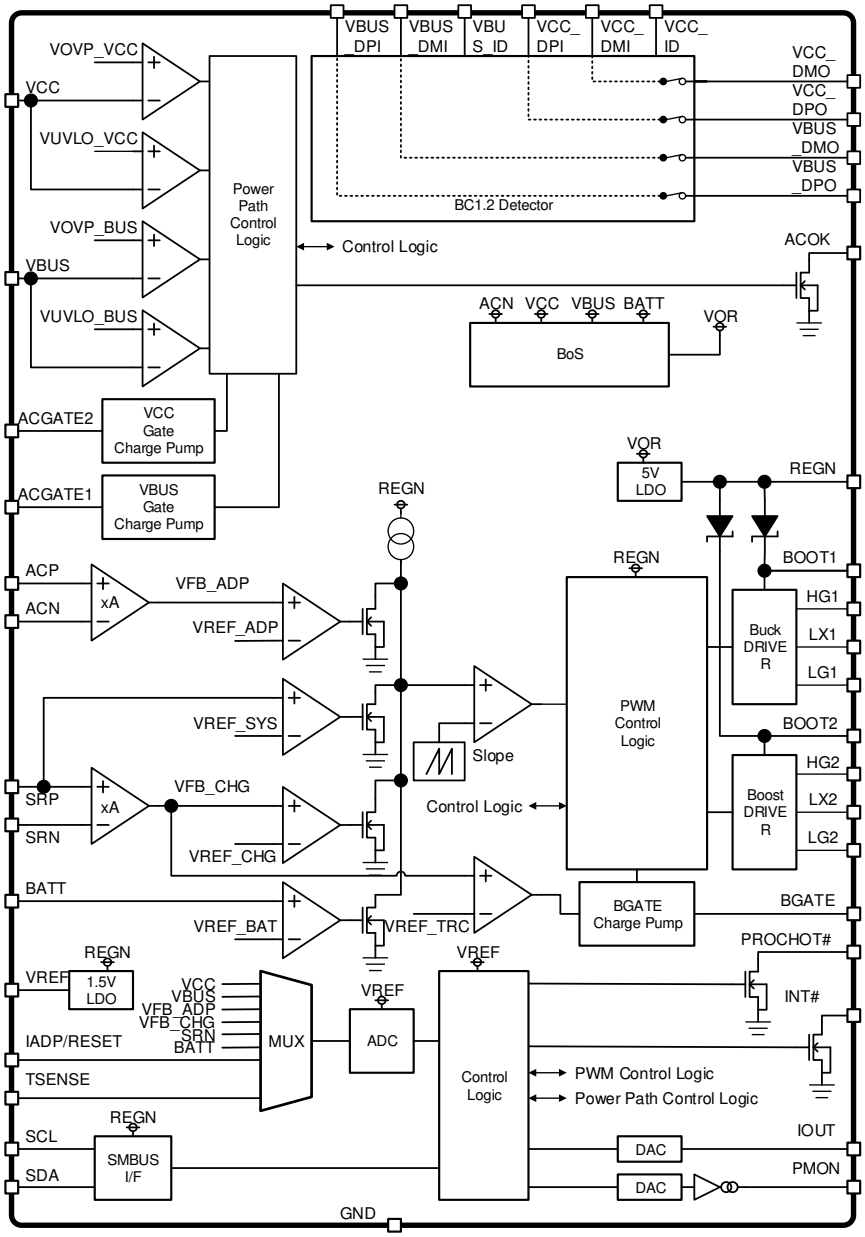


Figure 7-1 Block diagram

7.2. External Characteristics for Battery Charger

Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Adapter Standby Current 1	I_{ADP1}	-	1.0	1.5	mA	Charge Pump ON
Adapter Operating Current 2	I_{ADP2}	-	4.0	8.0	mA	Charge Pump ON Not Switching
Battery Standby Current (VBUS=VCC=0.0V)	I_{BATT1}	-	50.0	100.0	μA	BGATE Charge Pump ON REG0x7Ch[2:0]=5h
Battery Standby Current (VBUS=VCC=0.0V)	I_{BATT2}	-	25.0	50.0	μA	BGATE Charge Pump OFF Deep Sleep mode REG0x7Ch[2:0]=6h SDA=SCL=0V
Battery Standby Current (VBUS=VCC=0.0V)	I_{BATT3}	-	125	200	μA	BGATE Charge Pump ON PROCHOT only VSYS [1msec/S] REG0x7Ch[2:0]=2h
Battery Standby Current (VBUS=VCC=0.0V)	I_{BATT4}	-	150	290	μA	BGATE Charge Pump ON PROCHOT only VSYS [250μsec/S] REG0x7Ch[2:0]=1h
Battery Current (VBUS=VCC=0.0V)	I_{BATT5}	-	700	900	μA	BGATE Charge Pump ON with PROCHOT Monitored System voltage and Battery current REG0x7Ch[2:0]=0h
SMBus Operation Frequency	FSMB	10	-	400	kHz	
REGN Output Voltage	V_{REGN}	5.0	5.2	5.4	V	
REGN External output current	V_{REGN_LD}	10	-	-	mA	
REGN UVLO Voltage	V_{REGN_UVLO}	2.375	2.5	2.625	V	Detecting REGN falling edge
REGN UVLO Hysteresis Range	V_{REGN_UVLO}	50	100	200	mV	Detecting REGN rising edge
LDO Output Voltage	V_{REF}	1.455	1.5	1.55	V	IVREF=1mA
VREF UVLO release Voltage	V_{REF_UVLO}	1.35	1.40	1.45	V	Detecting VREF rising edge
VREF UVLO Hysteresis Range	$V_{REF\_UVLO\_hys}$	25	50	100	mV	Detecting VREF falling edge
<PMON>						
Power Monitor Amplifier Gain (IPMON)/(VACP×IACP + VBAT×IBAT)	G_{PMON}	-	16	-	μA/W	REG0x25h[2:0]=6h 6.25W Setting
		-	8	-	μA/W	REG0x25h[2:0]=5h 12.5W Setting
		-	4	-	μA/W	REG0x25h[2:0]=4h 25W Setting
		-	2	-	μA/W	REG0x25h[2:0]=3h 50W Setting
		-	1	-	μA/W	REG0x25h[2:0]=2h 100W Setting
		-	0.5	-	μA/W	REG0x25h[2:0]=1h 200W Setting
		-	0.25	-	μA/W	REG0x25h[2:0]=0h 400W Setting
	I_{PMON}	-5	-	+5	%	IPMON=50uA
PMON Maximum Current	$I_{PMONMAX}$	-	-	200	μA	
<IOUT>						
IADP Voltage Accuracy	G_{IADP}	-	20	-	V/V	(VIADP)/(VACP- VACN)
	V_{IOUT1}	802.8	819.2	835.6	mV	(VACP- VACN)=40.96mV
	V_{IOUT2}	393.2	409.6	426	mV	(VACP- VACN)=20.48mV
	V_{IOUT3}	174.1	204.8	235.5	mV	(VACP- VACN)=10.24mV
	V_{IOUT4}	81.92	102.4	122.9	mV	(VACP- VACN)=5.12mV
	V_{IOUT5}	-	51.2	-	mV	(VACP- VACN)=2.56mV
	V_{IOUT6}	-	25.6	-	mV	(VACP- VACN)=1.28mV
IDCHG Voltage Accuracy	G_{IDCHG}	-	16	-	V/V	(VIDCHG)/(VSRN- VSRP)
	V_{IDCHG1}	622.6	655.4	688.2	mV	(VSRN- VSRP)=40.96mV
	V_{IDCHG2}	298.2	327.7	357.2	mV	(VSRN- VSRP)=20.48mV
	V_{IDCHG3}	122.9	163.8	204.8	mV	(VSRN- VSRP)=10.24mV
	V_{IDCHG4}	41	81.9	122.9	mV	(VSRN- VSRP)=5.12mV

Note: Resister address refer to extended commands

7.3. DC Input & Over Voltage Protection (OVP)

7.3.1. Outline

- Dual-input for the battery charger source: USB VBUS and VCC
- 25V over voltage protection.
- One of two DC input selection (exclusive)
- Effective input is selected by the control registers, VCC as default.

7.3.2. Electrical Characteristics

Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
VCC Input Operating Range	V_{CCRNG}	3.8	-	25	V	
VCC UVLO Release Voltage	V_{CC_UVLO}	3.7	3.8	3.9	V	VCC rising
VCC UVLO Hysteresis Range	$V_{CC\_UVLO\_hys}$	80	130	180	mV	VCC falling
VCC OVP Detection Voltage	V_{CC_OVP}	25.0	25.5	26.0	V	VCC rising
VCC OVP Hysteresis Range	$V_{CC\_OVP\_hys}$	100	150	200	mV	VCC falling
USB Input Operating Range	V_{USBRNG}	3.8	-	25	V	
VBUS_UVLO Release Voltage	V_{BUS_UVLO}	3.7	3.8	3.9	V	VBUS rising
VBUS UVLO Hysteresis Range	$V_{BUS\_UVLO\_hys}$	80	130	180	mV	VBUS falling
VBUS OVP Detection Voltage	V_{BUS_OVP}	25.0	25.5	26	V	VBUS rising
VBUS OVP Hysteresis Range	$V_{BUS\_OVP\_hys}$	100	150	200	mV	VBUS falling
VACOK Output “L” Voltage	V_{OK_ON}	-	-	1.0	V	I(VACOK) =1mA
VACOK Leakage Current	I_{OKL}	-	-	1	µA	VACOK = 5V
VBUS Reverse Output turn-on Time	T_{VBUS_ON}	-	5	10	msec	
Voltage Output down-off Time	T_{VBUS_OFF}	-	1	5	µsec	

7.4. USB Detection

7.4.1. Outline

- USB Charger port detection and USB ID
- Supports USB BC 1.2, USB ACA, USB ID pin, USB OTG, and PD plug detection.
- Integrated analog switch supports USB HS (480Mbps).

7.4.2. Electrical Characteristics

Table 7-1 Electrical Characteristics for USB Detection

(Ta=25°C, BATT=3.6V, VBUS=5.0V)

Item	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
<USB Charger Detection>						
VDP_SRC voltage (output voltage for D+)	VDP_SRC	0.5	0.6	0.7	V	Io=0 to 200uA
VDM_SRC voltage (output voltage for D-)	VDM_SRC	0.5	0.6	0.7	V	Io=0 to 200uA
RCD resistance (D+ pull up resistance)	RCD	75	100	125	kΩ	
USB port un-detection resistance (Host D+ pull down resistance)	RHDP	100	-	-	kΩ	
VDAT_REF voltage (D+/D- detection voltage)	VDAT_REF	0.3	0.35	0.4	V	HDPR/HDML voltage rising
VLGC voltage (D+/D- detection voltage)	VLGC	1.2	1.4	1.6	V	HDPR/HDML voltage rising
D+ sink current	IDP_SINK	50	85	150	μA	V(HDPR) = 0.6V
D- sink current	IDM_SINK	50	85	150	μA	V(HDML) = 0.6V
<USB Switch (DP, DM)>						
Switch on-state resistance	RON_USBSW	-	5	10	Ω	VIN=3.3V or 0V
Switch off-state leakage current	IIOFF_USB	-3	-	3	μA	VIN=3.3V or 0V VBUS=OPEN
Switch capacitance	CSW	-	6	-	pF	USBSW ON
USB Switch start-up time	TUPUSB	-	-	1	ms	USBSW OFF→ON

(Ta=25°C, VBAT=3.6V, VBUS=5.0V)

Item	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
<USB ID>						
Pull-down detection resistance	RIDopen	1000	-	-	kΩ	USB ID removal detection
	RID1	-	797	-	kΩ	
	RID2	-	557	-	kΩ	
	RID3	-	440	-	kΩ	
	RID4	-	390	-	kΩ	
	RID5	-	287	-	kΩ	
	RID6	-	200	-	kΩ	
	RID7	-	180	-	kΩ	
	RID8	-	124	-	kΩ	
	RID9	-	102	-	kΩ	
	RID10	-	68	-	kΩ	
	RID11	-	47	-	kΩ	
	RID12	-	36.5	-	kΩ	
	RID13	-	1	-	kΩ	
	RID14	-	0	50	Ω	GND level detection
COMPH detection voltage ratio	RatioH	85	90	95	%	Ratio = 100xV(ID)/VCCIN [%] ID port voltage rising

Note: The pull-down resistance is designed in 5 % accuracy to comply with the standard of MCPC (Mobile Computing Promotion Consortium), except the 1kΩ resistor for RID_GND. The RID_GND resistance complies with the MHL (Mobile High-definition Link) standard in 20 % accuracy.

7.5. DC/DC Converter

7.5.1. - Outline

- Input Current Limit value setting: 96 mA to 16352 mA for VBUS and VCC
- Charger supply voltage anti-collapse control.
- Low power mode support
- Include thermal protection and shutdown

7.5.2. Electrical Characteristics

Table 7-2 Electrical Characteristics for DC/DC Converter
Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

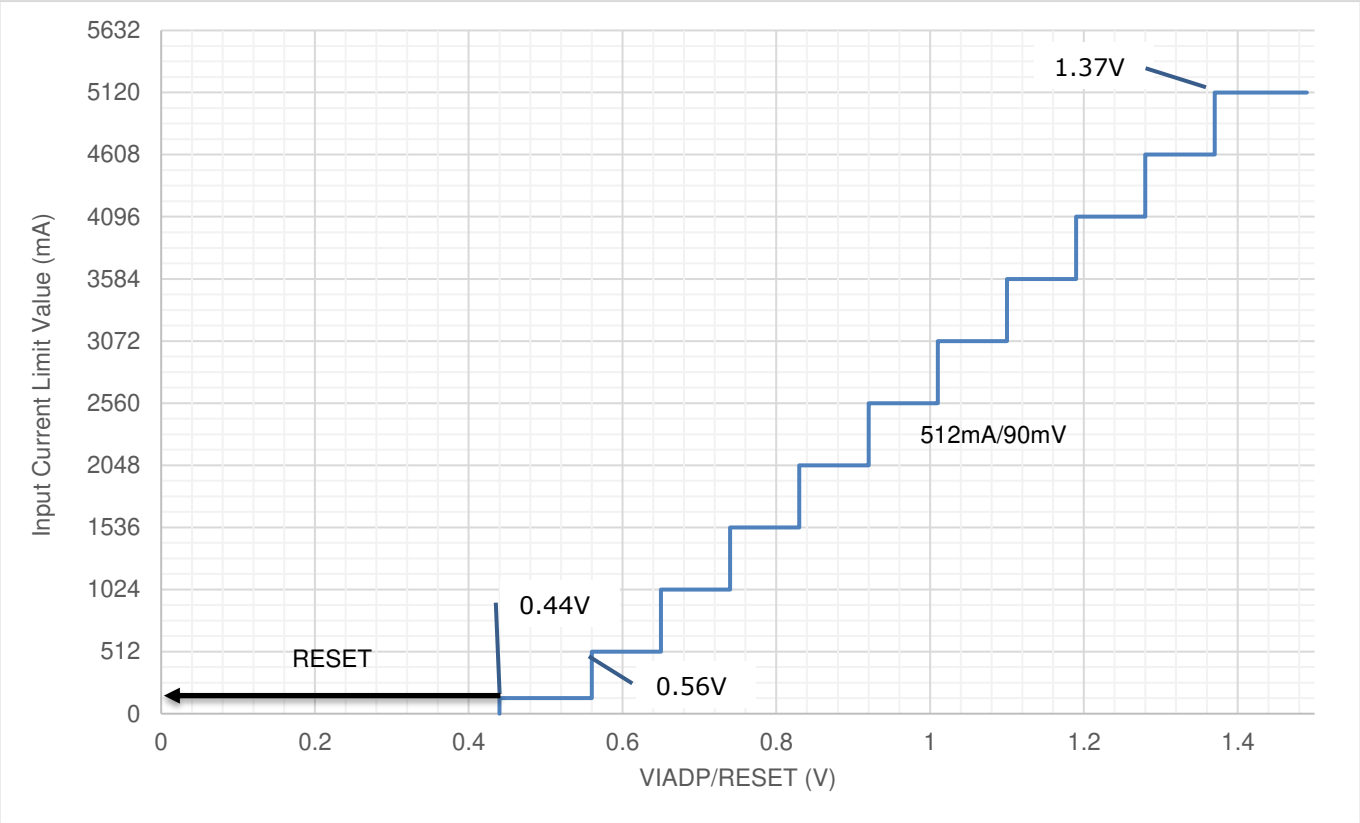
Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
<INPUT CURRENT>						
USB 500mA Current Accuracy	I_{USB500}	398	448	500	mA	REG0x07h/08h=01C0h
USB 900mA Current Accuracy	I_{USB900}	764	832	900	mA	REG0x07h/08h=0340h
BC1.2 1500mA Current Accuracy	$I_{USB1500}$	1380	1440	1500	mA	REG0x07h/08h=05A0h
USB-PD 3A Current Accuracy	$I_{USB3000}$	2824	2912	3000	mA	REG0x07h/08h=0B60h
USB-PD 5A Current Accuracy	$I_{USB5000}$	4792	4896	5000	mA	REG0x07h/08h=1320h
Input Current Setting Range	I_{ADPRNG}	96	-	16352	mA	REG0x07h or REG0x08h
Charge Current Setting LSB	I_{ADPLSB}	-	32	-	mA	
Input Current Accuracy (10mΩ current sense resistor)	I_{ADP1}	-2%	4096	+2%	mA	
	I_{ADP2}	-3%	2048	+3%	mA	
	I_{ADP3}	-5%	1024	+5%	mA	
	I_{ADP4}	-10%	512	+10%	mA	
IADP/RESET pin input Voltage range	$V_{ADPTRNG}$	0.1	-	1.4	V	
IADP/RESET pin Current setting Range	$I_{ADPTRNG}$	128	-	5120	mA	
IADP/RESET pin Current setting step	$I_{ADPSTEP}$	-	512	-	mA	
RESET Detection Voltage	Vreset_det	-	-	0.22	V	IADP/RESET voltage falling
RESET release Voltage	Vreset_rel	0.44	-	-	V	IADP/RESET voltage rising
RESET Detection duration time	T_{RESET}	100	-	-	µsec	
<MINIMUM SYSTEM VOLTAGE>						
Minimum System Voltage Setting Range	V_{MSVRNG}	2.560	-	19.2	V	VSYSREG_SET=2,560 ~ 19,200mV, 64mV steps.
Minimum System Voltage Setting LSB	V_{MSVLSB}	-	64	-	mV	
Minimum System Voltage accuracy	V_{MSV1}	-2.0%	3.072	+2.0%	V	REG0x11h=0C00h
	V_{MSV2}	-1.0%	6.144	+1.0%	V	REG0x11h=1800h
	V_{MSV3}	-2.0%	9.216	+2.0%	V	REG0x11h=2400h
	V_{MSV4}	-2.0%	12.288	+2.0%	V	REG0x11h=3000h
<Anti-Collapse Voltage>						
VBUS Anti-Collapse Threshold Voltage Range	V_{anti_VBUS}	3.84	-	25.0	V	REG0x0Dh
Anti-Collapse Threshold Voltage Accuracy	$V_{anti\_VBUS\_acc}$	-100	-	+100	mV	
VCC Anti-Collapse Threshold Voltage Range	V_{anti_VCC}	3.84	-	25.0	V	REG0x0Eh
Anti-Collapse Threshold Voltage Accuracy	$V_{anti\_VCC\_acc}$	-100	-	+100	mV	
<Switching Frequency>						
Switching Frequency 1	FOSC1	510	600	690	kHz	REG0x0Ch[3:2]=00b
Switching Frequency 2	FOSC2	770	860	950	kHz	REG0x0Ch[3:2]=01b
Switching Frequency 3	FOSC3	850	1000	1150	kHz	REG0x0Ch[3:2]=10b
Switching Frequency 4	FOSC4	1020	1200	1380	kHz	REG0x0Ch[3:2]=11b
<DRIVER>						
HRDV1 PMOS RON	R_{HDRV1P}	-	6.0	10.0	Ω	
HRDV1 NMOS RON	R_{HDRV1N}	-	0.7	1.3	Ω	
LRDV1 PMOS RON	R_{LDRV1P}	-	7.5	12.0	Ω	
LRDV1 NMOS RON	R_{LDRV1N}	-	0.9	1.4	Ω	
HRDV2 PMOS RON	R_{HDRV2P}	-	6.0	10.0	Ω	
HRDV2 NMOS RON	R_{HDRV2N}	-	0.7	1.3	Ω	
LRDV2 PMOS RON	R_{LDRV2P}	-	7.5	12.0	Ω	
LRDV2 NMOS RON	R_{LDRV2N}	-	0.9	1.4	Ω	

Note: Resister address refer to extended commands

7.5.3. Detailed IADP input current limit settings

- Input Current limit is set by external IADP/RESET pin.
- This function is enabled by VM_CTRL_SET.EXTIADPEN bit =1.
- Once the charger reset is released when this function is enabled, the corresponding input current value which depends on the IADP/RESET voltage will be stored to the SEL_ILIM_VAL register. And this is used as the input current limit. It can be overwritten through SMBus.

Table 7-3 IADP pin Input Current Limit settings



7.6. Charger

7.6.1. - Outline

- Supports battery insertion and removal detection.
- Controls the VSYS output voltage with a deeply discharged battery.
- JEITA compliant Battery Charging Profile with thermal control of the charging current and voltage settings by measuring the temperature from the external thermistor
- Supports battery supplement mode
- Automatic or manual control of the Watch Dog Timer (via software) while Pre–charging and Fast-charging

7.6.2. Electrical Characteristics

Table 7-4 Electrical Characteristics for Charger

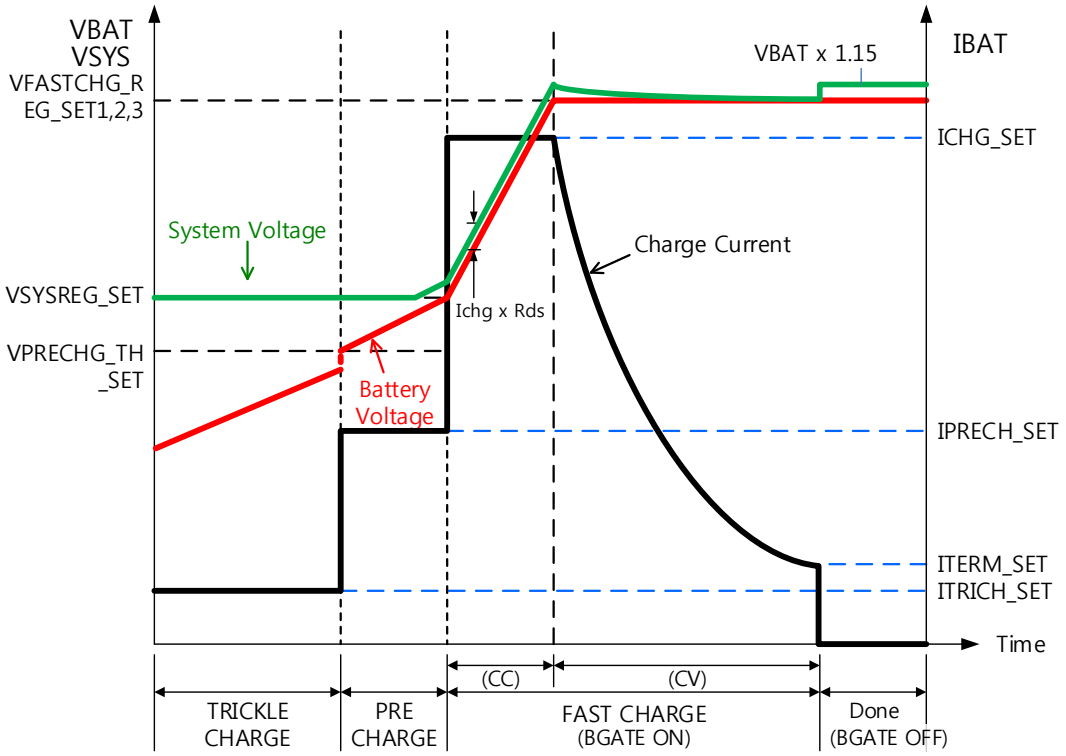
Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Battery Input Operating Range1	V_{BATRNG}	0.0	-	19.2	V	With Adapter Input
Battery Input Operating Range1	V_{BATRNG}	2.5	-	19.2	V	Without Adapter Input
<CHARGE VOLTAGE>						
Charge Voltage Setting Range	V_{CVRNG}	2.560	-	19.200	V	REG0x1A, REG0x1Bh or REG0x1Ch
Charge Voltage Setting LSB	V_{CVLSB}	-	16	-	mV	
Charge Voltage accuracy	V_{CV1S}	-0.5%	4.192	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=1060h
	V_{CV2S}	-0.5%	8.400	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=20D0h
	V_{CV3S}	-0.5%	12.592	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=3130h
	V_{CV4S}	-0.5%	16.800	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=41A0h
VBAT OVP Detection range	V_{OVPRNG}	2.56	-	19.2	V	REG0x1Dh
<CHARGE CURRENT>						
Charge Current Setting Range	I_{CHGRNG}	0	-	16384	mA	REG0x16h
Charge Current Setting LSB	I_{CHGLSB}	-	64	-	mA	
Charge Current accuracy (10mΩ current sense resistor, BATT > Minimum System Voltage)	I_{CHG1}	-2%	4096	+2%	mA	REG0x16h=1000h
	I_{CHG2}	-3%	2048	+3%	mA	REG0x16h=0800h
	I_{CHG3}	-5%	1024	+5%	mA	REG0x16h=0400h
	I_{CHG4}	-20%	256	+20%	mA	REG0x16h=0100h
	I_{CHG5}	-40%	128	+40%	mA	REG0x16h=0080h
Trickle Charge Current Setting Range	$I_{TRCCHGRNG}$	0	256	1024	mA	REG0x14h or REG0x15h
Trickle Charge Current Setting LSB	$I_{TRCCHGLSB}$	-	64	-	mA	
Maximum Trickle Charge Current (10mΩ current sense resistor, BATT < Minimum System Voltage)	I_{CHG6}	-	1024	-	mA	REG0x14h or REG0x15h
<Thermal Control>						
Battery Temperature Threshold HOT1	V_{TH_HOT1}	-	45	-	°C	OTP Programmable REG0x45h
Battery Temperature Threshold HOT2	V_{TH_HOT2}	-	50	-	°C	OTP Programmable REG0x44h
Battery Temperature Threshold HOT3	V_{TH_HOT3}	-	58	-	°C	OTP Programmable REG0x43h
Battery Temperature Threshold COLD1	V_{TH_COLD1}	-	10	-	°C	OTP Programmable REG0x42h
Battery Temperature Threshold COLD2	V_{TH_COLD2}	-	2	-	°C	OTP Programmable REG0x41h
Battery Temperature Measurement Acc	Tbat	-2	-	+2	°C	
Battery Open Detection Voltage	V_{TH_OPN}	-	V_{REF}*0.95	-	V	
<Battery Short Current Detection>						
Battery Short Current Detection	$I_{BATSHORT}$	0	-	25,000	mA	REG0x1Fh
Battery Short Current Duration time	$T_{BATSHORT}$	4	-	1020	msec	REG0x10h[15:8]
<Watchdog Timer>						
Pre Charging Time	T_{PRE}	13.0	14.5	16	min	
Fast Charging Time	T_{FAST}	196	218	240	min	
High Temperature Protection Time	T_{HTPRO}	108	120	132	min	Over 58°C
Charging Termination Delay Time	T_{TOPOFF}	13	15	17	sec	

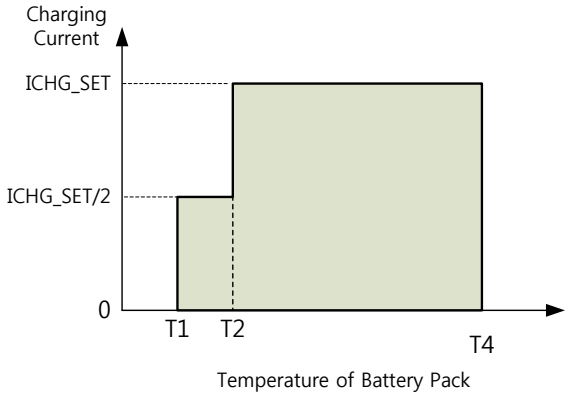
Note: Resister address refer to extended commands

7.6.3. Battery Charging Profile

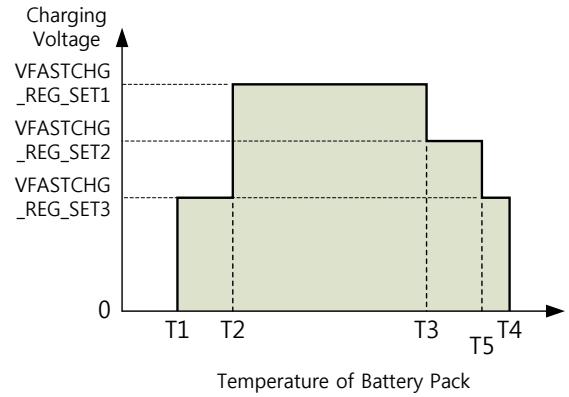
Figure 7-5 Battery Charging Profile



The charging current is controlled by the battery temperature measured from the external thermistor.
In the low-temperature condition, the charging current is reduced to a half of the setting value (ICHG_SET).



The charging voltage is also **reduced by the temperature** as **set by** the **control registers, VFASTCHG_REG_SET1/2/3**.



7.7. Reverse DC/DC Converter

7.7.1. Outline

- Charger provides a voltage output (Reverse Buck/Boost) via VBUS or/and VCC when an USB OTG device is connected.

7.7.2. Electrical Characteristics

Table 7-6 Electrical Characteristics for Reverse Buck/Boost

Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
<OUTPUT CURRENT Limit>						
Output Current Limit Setting Range	$I_{RADPRNG}$	0	4096	8128	mA	REG0x09h
Output Current Limit Setting LSB	$I_{RADPLSB}$	-	32	-	mA	
Output Current Limit Accuracy (10mΩ current sense resistor)	I_{RADP1}	-2%	4096	+2%	mA	REG0x09h=1000h
	I_{RADP2}	-3%	2048	+3%	mA	REG0x09h=0800h
	I_{RADP3}	-5%	1024	+5%	mA	REG0x09h=0400h
	I_{RADP4}	-10%	512	+10%	mA	REG0x09h=0200h
<Output VOLTAGE>						
Output Voltage Setting 1	V_{ROUT1}	4.95	5.0	5.05	V	REG0x19h=1380h
Output Voltage Setting 2	V_{ROUT2}	5.15	5.2	5.25	V	REG0x19h=1440h
Output Voltage Setting 3	V_{ROUT3}	8.91	9.0	9.09	V	REG0x19h=2340h
Output Voltage Setting 4	V_{ROUT4}	11.88	12.0	12.12	V	REG0x19h=2F00h
Output Voltage Setting 5	V_{ROUT5}	19.8	20.0	20.2	V	REG0x19h=4E40h
Output Voltage Setting Range	$V_{ROUTRNG}$	4.032	-	22.016	V	REG0x19h
Output Voltage Setting LSB	$V_{ROUTLSB}$	-	64	-	mV	
VBUS Buck/Boost Output Short Circuit Protection.	V_{R}scp	-	VBUS_UVLO VCC_UVLO	-	V	
VBUS Buck/Boost OVP Voltage	V_{R}ovp	-	V_{ROUT} x 1.1	-	V	
VBUS Buck/Boost OVP Detection Hysteresis Range	V_{R}ovp_hys	-	V_{ROUT} x 1.05	-	mV	

Note: Resister address refer to extended commands

7.8. 12-bit ADC

7.8.1. Outline

- 12-bit Successive Approximation Register A/D Converter
- Input Voltage range: 2.0 to 19.2V (BATT)
- Input Voltage range: 2.0 to 25V (VBUS, VCC, ACP, SRP)
- Input Voltage range: 0.1 to 1.4V (TSENSE)
- Input Voltage range: 0.1 to 1.4V (IADP/RESET)
- Current monitor range: 0.3 to 16.384A (IACP)
- Current monitor range: 0.3 to 25A (IBAT)

7.8.2. Electrical Characteristics

Table 7-7 Electrical Characteristics for 12-bit SAR-ADC

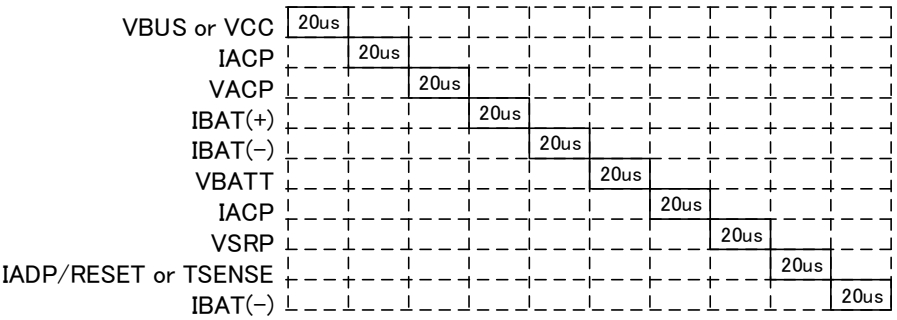
(Unless otherwise specified, Ta=25°C, VREF=1.5V)

Parameter	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
<12-bit SAR ADC>						
Resolution	RES	-	-	12	bit	
Conversion Period	TCONV	-	20	-	µs	
Gain Error 1	Gerr1	−1.1	-	+1.1	%	BATT,VBUS,VCC,ACP, SRP=5V and 15V
Gain Error 2	Gerr2	−1.1	-	+1.1	%	TSENSE,IADP/RESET =0.5V and 1.0V
Gain Error 3	Gerr3	−1.1	-	+1.1	%	IACP,IBAT=1.5A and 8A
VOffset error	Voffset	-110		110	mV	
IOffset error	Ioffset	-110	-	110	mA	

7.8.3. Functions

SAR-ADC measures the 10 following factors by time sharing. These factors can be disabled by SMBus command.
The actual value and the 2-sample moving average value are read by SMBus command.

#	Factor	Conversion Period	Conversion Interval
1	VBUS or VCC	20us	VBUS 400us VCC 400us
2	IACP	20us	200us
3	VACP	20us	200us
4	IBAT(+)	20us	200us
5	IBAT(-)	20us	200us
6	VBATT	20us	200us
7	IACP	20us	200us
8	VSRP	20us	200us
9	IADP/RESET or TSENSE	20us	IADP/RESET 200us TSENSE 1s
10	IBAT(-)	20us	200us



The power calculation of PMON is carried out from IACP, VACP, IBAT, VBATT.

PACP = IACP * VACP
PBAT = IBAT * VBATT
PMON = PACP + PBATT

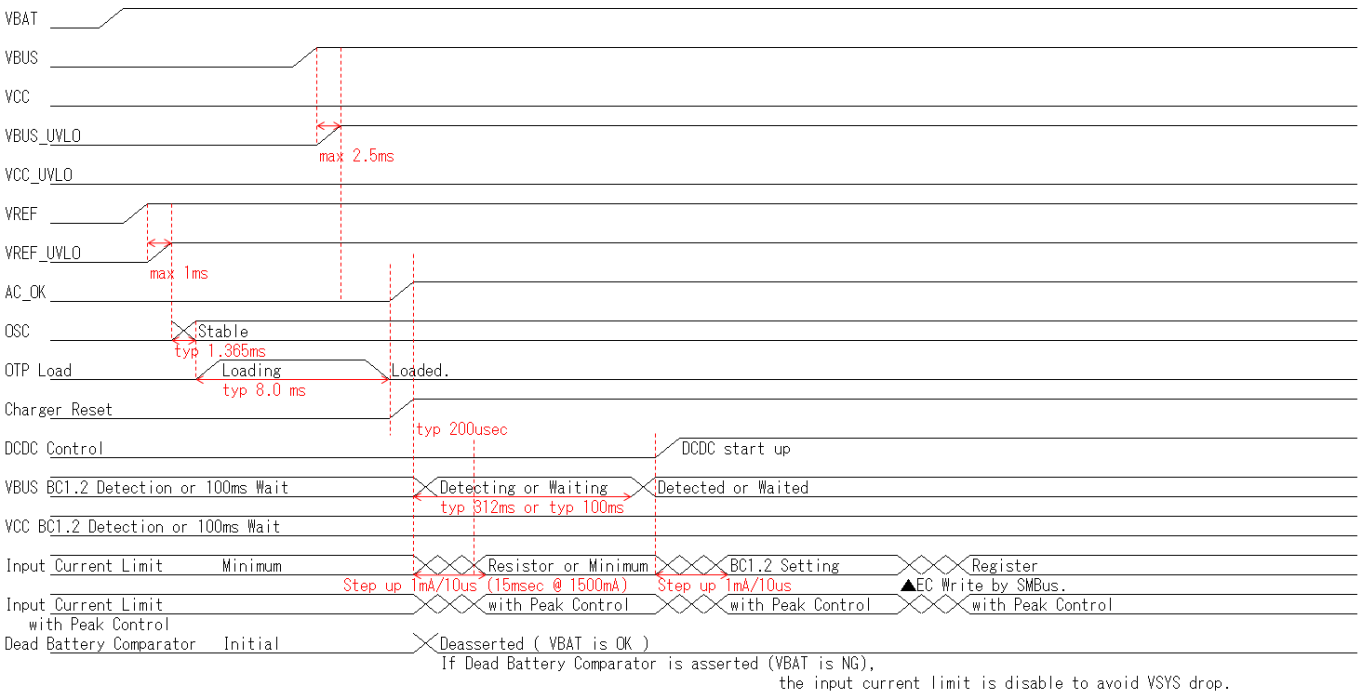
PMON power change can be observed when the value is stable longer than the “Conversion Interval”, 200us.

7.9. Power On

Whenever BD99954 receives power from the adapter or battery, BD99954 wakes up and starts loading data from the OTP. After OTP loading is completed, BD99954 is in standby position.

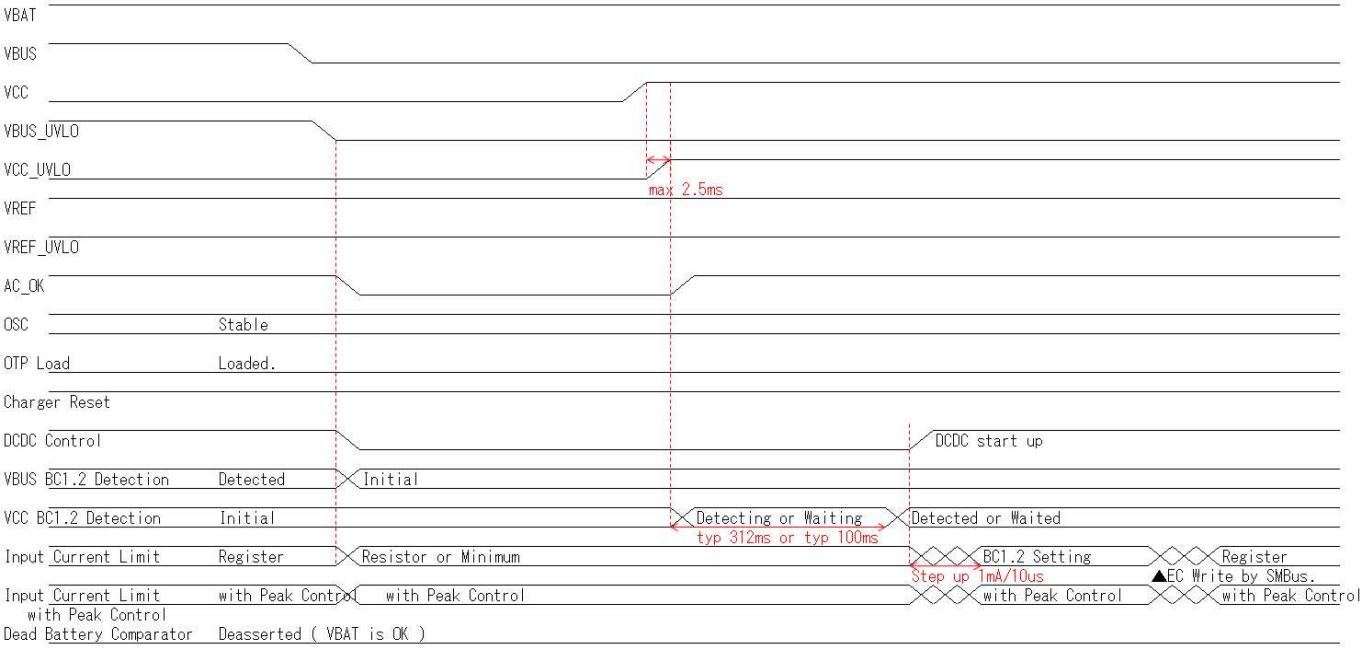
7.9.1. VBAT power on and VBUS/VCC plugged-in

At the first VBAT power on, BD99954 starts OTP loading. And when VBUS or VCC is eventually plugged in, BD99954sserts ACOK and starts the BC1.2 Detection sequence. After the BC1.2 Detection is completed, BD99954 limits the input current, reflects the BC1.2 setting and starts charging.



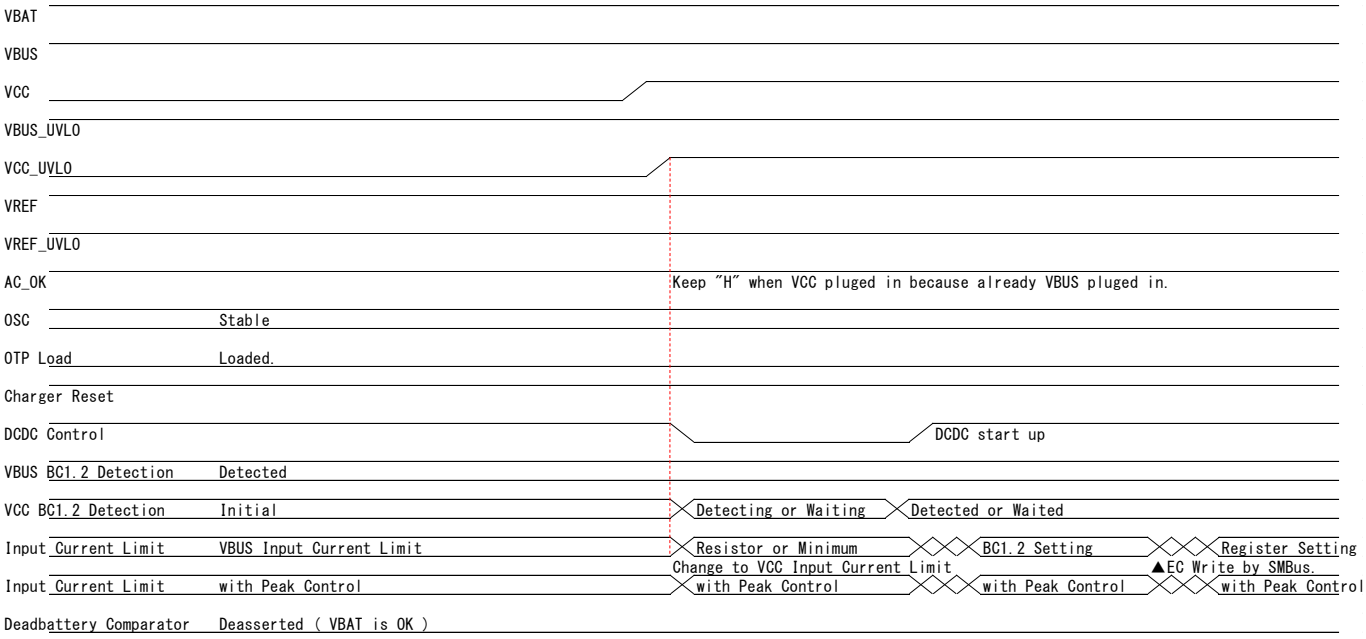
7.9.2. VBUS/VCC plugged-off

When VBUS plugged off, BD99954 deasserts AC_OK and limits input current as IADP external pin or minimum setting (it is programmable). And then VBUS or VCC plugged in again, BD99954sserts AC_OK and starts BC1.2 detection.



7.9.3. VBUS and VCC plugged in

When VBUS plugged in and then VCC plugged in, BD99954 selects VBUS or VCC with priority setting. If VCC is 1st priority (programmable), BD99954 changes power source from VBUS to VCC. If VBUS is 1st priority BD99954 keeps power source VBUS. Each case AC_OK keeps “H”.



8. Control Specification

BD99954 has several control registers to set configurations or to sense the hardware status for the internal function operations. Host is able to write to or read from the control registers via SMBus (friendly I2C).

8.1. SMBus Communication

BD99954 operates in slave mode on the SMBus and supports Layer 2 communication protocol.

8.1.1. SMBus Slave Address

Slave Address for the BD99954 is 0001_001.

The register address is set by “Slave Address”. The “Slave Address” is also used as the start address of contiguous addressing for multiple write or read access.

8.2. SMBus Protocols

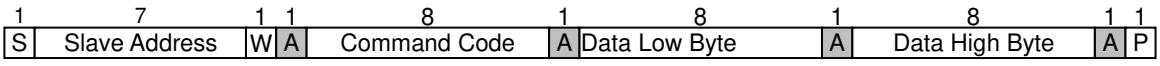
The following is a description of the various SMBus protocols. BD99954 supports the protocols defined in this section. BD99954 does not support all the protocols defined in the SMBus Specification. The results returned by such a device to a protocol it does not support is undefined.
Below is a key to the protocol diagrams in this section. Not all protocol elements will be presented in every command. For instance, not all packets are required to include the packet error code.

S	Start Condition
Sr	Repeated Start Condition
Rd	Read (bit value of 1)
Wr	Write (bit value of 0)
x	Shown under a field indicates that that field is required to have the value of ‘x’
A	Acknowledge (this bit position may be‘0’ for an ACK)
N	Acknowledge (this bit position may be‘1’ for a NACK)
P	Stop Condition
PEC	Packet Error Code
	Master (SMBus Host) to Slave
	Slave (SMBus Device) to Master

BD99954 supports following protocols.
- ✧ Write Word
- ✧ Read Word

8.2.1. Write Word

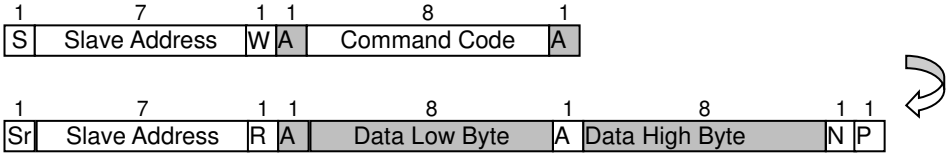
The first byte of a Write Word access is the command code. The next are the high data byte and low data byte to be written. In this example the master asserts the slave device address followed by the write bit. The device acknowledges and the master delivers the command code. The slave again acknowledges before the master sends the data bytes. The slave acknowledges each byte, and the entire transaction is finished with a STOP condition.
BD99954 does not support PEC.



SMBus Write Word

8.2.2. Read Word

Reading data is slightly more complicated than writing data. First the host must write a command to the slave device. Then it must follow that command with a repeated START condition to denote a read from that device's address. The slave then returns one high and low byte of data.
Note that there is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer. BD99954 does not support PEC.



SMBus Read Word

8.2.3. SMBus Communication Timing Waveforms and Timing Specification

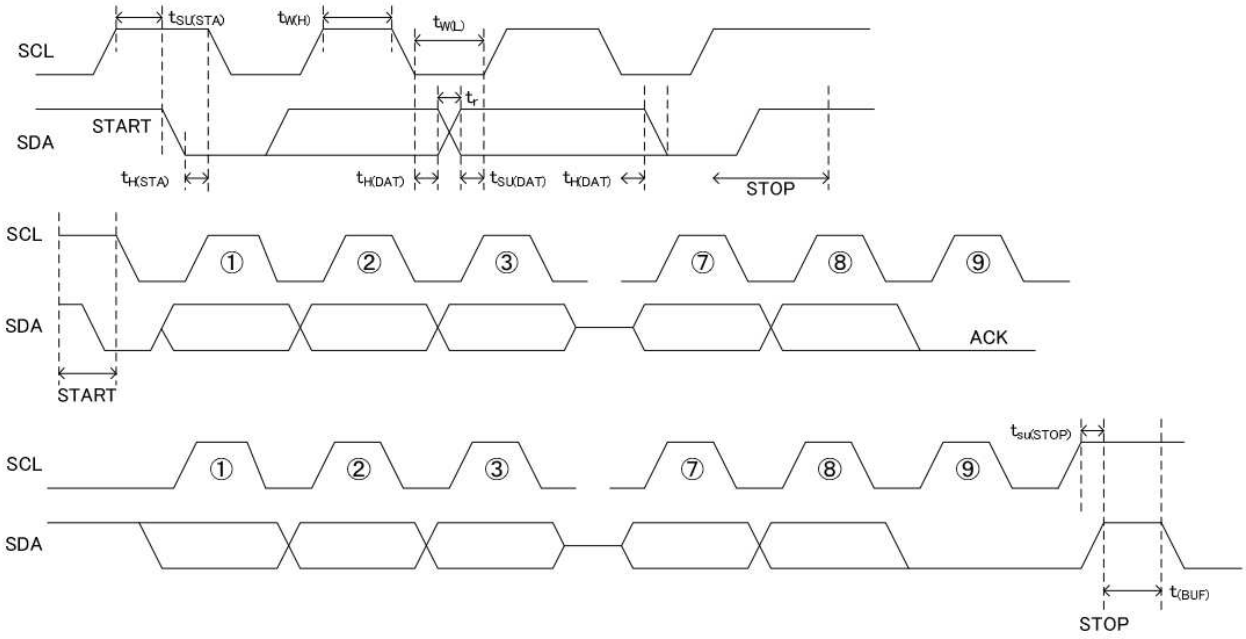


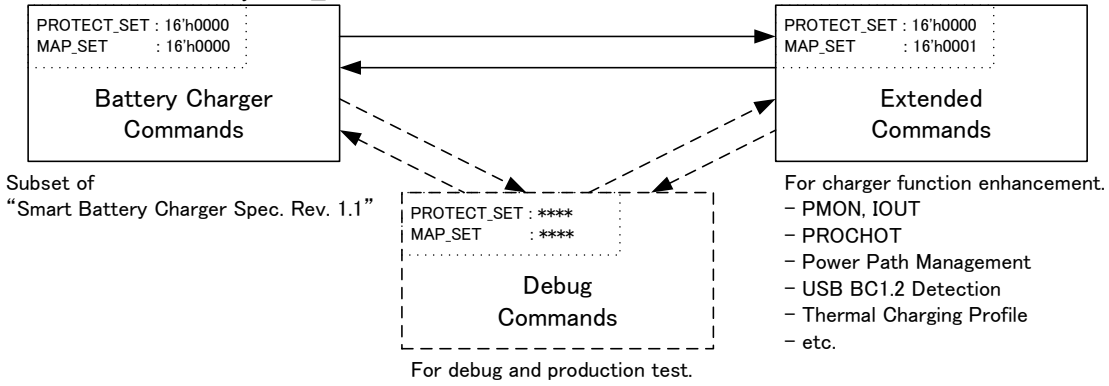
Table 8-1 Electrical Characteristics for SMBus Timing Specification
(Unless otherwise specified, Ta=25°C, VREF=1.5V)

Parameter	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
<SMBus>						
SMBus Frequency	F_{SMBus}	10	-	400	kHz	
SDA/SCL Input Low Voltage	V_{INL}	0.0	-	0.8	V	
SDA/SCL Input High Voltage	V_{INH}	2.1	-	5.5	V	
SDA Hold Time from SCL	$T_{H(DAT)}$	250	-	-	ns	
SDA Setup Time from SCL	$T_{SU(DAT)}$	300	-	-	ns	
Start Condition Hold Time from SCL	$T_{H(STA)}$	4	-	-	µs	
Start Condition Setup Time from SCL	$T_{SU(STA)}$	4.7	-	-	µs	
Stop Condition Setup Time from SCL	$T_{SU(STOP)}$	4	-	-	µs	
Bus Free Time	T_{BUF}	4.7	-	-	µs	

8.3. Command Code

BD99954 has 3 command maps, "Battery Charger Commands", "Extended Commands" and "Debug Commands". All commands are addressed within 00h ~ 7Fh address area. And 80h ~ FFh address is a mirror of 00h ~ 7Fh.

"Battery Charger Commands" is a subset of "Smart Battery Charger Specification Revision 1.1."
"Extended Commands" is for charger function enhancement.
"Debug Commands" are used for debug purpose or in production test.
These are selectable by MAP_SET command.



8.3.1. Battery Charger Commands

Following is a table of "Battery Charger Commands" which BD99954 supports. "Battery Charger Commands" is subset of "Smart Battery Charger Specification Revision 1.1."
Note: Reserved command should not be accessed. If accessed, operation is not guaranteed.

Code	Command	Protocols	Byte Size	Description
14h	ChargingCurrent	Read/Write Word	2	The Battery, System Host or other master device sends the desired charging rate (mA). This command is a mirror of ICHG_SET command of the extended command.
15h	ChargingVoltage	Read/Write Word	2	The Battery, System Host or other master device sends the desired charging voltage to the Smart Battery Charger (mV). This command is a mirror of VFASTCHG_REG_SET1 command of the extended command.
3Ch	IBUS_LIM_SET	Read/Write Word	2	VBUS Input Current Limit Setting. This command is a mirror of IBUS_LIM_SET command of the extended command.
3Dh	ICC_LIM_SET	Read/Write Word	2	VCC Input Current Limit Setting. This command is a mirror of ICC_LIM_SET command of the extended command.
3Eh	PROTECT_SET	Read/Write Word	2	Access Un-protect Setting for Address 3Fh This command is a mirror of PROTECT_SET command of the extended command.
3Fh	MAP_SET	Read/Write Word	2	Change Command Code Map. This command is a mirror of MAP_SET command of the extended command.

8.3.2. Extended Commands

Following is a table of "Extended Commands" which BD99954 supports. "Extended Commands" is for charger function enhancement.

Note: Reserved command should not be accessed. If accessed, operation is not guaranteed.

Code	Command	Protocols	Byte Size	Description
00h	CHGSTM_STATUS	Read Word	2	Charger State Machine Status
01h	VBAT/VSYS_STATUS	Read Word	2	VBAT and VSYS Status
02h	VBUS/VCC_STATUS	Read Word	2	VBUS and VCC Status
03h	CHGOP_STATUS	Read Word	2	Charger Operation Status
04h	WDT_STATUS	Read Word	2	Charger WDT and Thermal WDT Status
05h	CUR_ILIM_VAL	Read Word	2	Actual Input Current Limit
06h	SEL_ILIM_VAL	Read Word	2	Selected Input Current Limit
07h	IBUS_LIM_SET	Read/Write Word	2	VBUS Input Current Limit Setting
08h	ICC_LIM_SET	Read/Write Word	2	VCC Input Current Limit Setting
09h	IOTG_LIM_SET	Read/Write Word	2	OTG Output Current Limit Setting
0Ah	VIN_CTRL_SET	Read/Write Word	2	VBUS and VCC Control Setting
0Bh	CHGOP_SET1	Read/Write Word	2	Charger Operation Control Setting 1
0Ch	CHGOP_SET2	Read/Write Word	2	Charger Operation Control Setting 2
0Dh	VBUSCLPS_TH_SET	Read/Write Word	2	VBUS Collapse Detect Threshold Voltage Setting
0Eh	VCCCLPS_TH_SET	Read/Write Word	2	VCC Collapse Detect Threshold Voltage Setting
0Fh	CHGWDT_SET	Read/Write Word	2	Charger WDT Setting
10h	BATTWDT_SET	Read/Write Word	2	Battery temperature and Battery short current WDT Setting
11h	VSYSREG_SET	Read/Write Word	2	VSYS Regulation Setting
12h	VSYSVAL_THH_SET	Read/Write Word	2	VSYS Valid Threshold High Setting (Hysteresis)
13h	VSYSVAL_THL_SET	Read/Write Word	2	VSYS Valid Threshold Low Setting (Hysteresis)
14h	ITRICH_SET	Read/Write Word	2	Trickle-charge Current Setting
15h	IPRECH_SET	Read/Write Word	2	Pre-charge Current Setting
16h	ICHG_SET	Read/Write Word	2	Fast-charge Current Setting
17h	ITERM_SET	Read/Write Word	2	Charge Termination Current Setting
18h	VPRECHG_TH_SET	Read/Write Word	2	Pre-charge Voltage Threshold Setting
19h	VRBOOST_SET	Read/Write Word	2	Reverse Buck Boost Voltage Setting
1Ah	VFASTCHG_REG_SET1	Read/Write Word	2	Fast Charge Voltage Regulation Setting 1
1Bh	VFASTCHG_REG_SET2	Read/Write Word	2	Fast Charge Voltage Regulation Setting 2 (Hot 1)
1Ch	VFASTCHG_REG_SET3	Read/Write Word	2	Fast Charge Voltage Regulation Setting 3 (Hot 2)
1Dh	VRECHG_SET	Read/Write Word	2	Re-charge Battery Voltage Setting
1Eh	VBATOVP_SET	Read/Write Word	2	Battery Over Voltage Protection Setting
1Fh	IBATSHORT_SET	Read/Write Word	2	Battery Short Current Protection Setting
20h	PROCHOT_CTRL_SET	Read/Write Word	2	PROCHOT# pin Control Setting
21h	PROCHOT_ICRIT_SET	Read/Write Word	2	Peak Input Current Threshold Setting for PROCHOT#
22h	PROCHOT_INORM_SET	Read/Write Word	2	Average Input Current Threshold Setting for PROCHOT#
23h	PROCHOT_IDCHG_SET	Read/Write Word	2	Dis-charge Current Threshold Setting for PROCHOT#
24h	PROCHOT_VSYS_SET	Read/Write Word	2	VSYS Voltage Threshold Setting for PROCHOT#
25h	PMON_IOUT_CTRL_SET	Read/Write Word	2	PMON and IOUT Output Control Setting
26h	PMON_DACIN_VAL	Read Word	2	PMON DAC Input Value
27h	IOUT_DACIN_VAL	Read Word	2	IOUT DAC Input Value
28h	VCC_UCD_SET	Read/Write Word	2	BC1.2 Charger Detector on the VCC side Setting
29h	VCC_UCD_STATUS	Read Word	2	BC1.2 Charger Detect Status on the VCC side
2Ah	VCC_IDD_STATUS	Read Word	2	ID Detect Status on the VCC side
2Bh	VCC_UCD_FCTRL_SET	Read/Write Word	2	BC1.2 Charger Detector on the VCC side Manual Control Setting
2Ch	VCC_UCD_FCTRL_EN	Read/Write Word	2	BC1.2 Charger Detector on the VCC side Manual Control Enable
2Dh	(reserved)	-	-	-
2Eh	(reserved)	-	-	-
2Fh	(reserved)	-	-	-
30h	VBUS_UCD_SET	Read/Write Word	2	BC1.2 Charger Detector on the VBUS side Setting
31h	VBUS_UCD_STATUS	Read Word	2	BC1.2 Charger Detect Status on the VBUS side
32h	VBUS_IDD_STATUS	Read Word	2	ID Detect Status
33h	VBUS_UCD_FCTRL_SET	Read/Write Word	2	BC1.2 Charger Detector on the VBUS side Manual Control Setting

Code	Command	Protocols	Byte Size	Description
34h	VBUS_UCD_FCTRL_EN	Read/Write Word	2	BC1.2 Charger Detector on the VBUS side Manual Control Enable
35h	(reserved)	-	2	-
36h	(reserved)	-	-	-
37h	(reserved)	-	-	-
38h	CHIP_ID	Read Word	2	Chip ID
39h	CHIP_REV	Read Word	2	Chip Revision
3Ah	IC_SET1	Read/Write Word	2	1-Cell mode setting, ACP discharge control and ACOK control setting.
3Bh	IC_SET2	Read/Write Word	2	IC Setting Register for debug and production test.
3Ch	SYSTEM_STATUS	Read Word	2	System Power-on Status
3Dh	SYSTEM_CTRL_SET	Read/Write Word	2	Software reset and re-load OTP
3Eh	PROTECT_SET	Read/Write Word	2	Access Un-protect Setting for Address FCh and FEh
3Fh	MAP_SET	Read/Write Word	2	Change Command Code Map to Debug Command Code Map
40h	VM_CTRL_SET	Read/Write Word	2	SAR-ADC Measurement Control Setting
41h	THERM_WINDOW_SET1	Read/Write Word	2	JEITA Temperature Window Setting 1
42h	THERM_WINDOW_SET2	Read/Write Word	2	JEITA Temperature Window Setting 2
43h	THERM_WINDOW_SET3	Read/Write Word	2	JEITA Temperature Window Setting 3
44h	THERM_WINDOW_SET4	Read/Write Word	2	JEITA Temperature Window Setting 4
45h	THERM_WINDOW_SET5	Read/Write Word	2	JEITA Temperature Window Setting 5
46h	IBATP_TH_SET	Read/Write Word	2	Battery Current (Charge) Interrupt Threshold Setting
47h	IBATM_TH_SET	Read/Write Word	2	Battery Current (Dis-charge) Interrupt Threshold Setting
48h	VBAT_TH_SET	Read/Write Word	2	Battery Voltage Interrupt Threshold Setting
49h	THERM_TH_SET	Read/Write Word	2	Battery Temperature Interrupt Threshold Setting
4Ah	IACP_TH_SET	Read/Write Word	2	Input Current (between ACP-ACN) Interrupt Threshold Setting
4Bh	VACP_TH_SET	Read/Write Word	2	Input Voltage (ACP) Interrupt Threshold Setting
4Ch	VBUS_TH_SET	Read/Write Word	2	VBUS Voltage Interrupt Threshold Setting
4Dh	VCC_TH_SET	Read/Write Word	2	VCC Voltage Interrupt Threshold Setting
4Eh	VSYS_TH_SET	Read/Write Word	2	VSYS Voltage Interrupt Threshold Setting
4Fh	EXTIADP_TH_SET	Read/Write Word	2	IADP (Input current Limit setting pin) Voltage Interrupt Threshold Setting
50h	IBATP_VAL	Read Word	2	Battery Current (Charge) Measurement Value
51h	IBATP_AVE_VAL	Read Word	2	Battery Current (Charge) Measurement Average Value
52h	IBATM_VAL	Read Word	2	Battery Current (Dis-charge) Measurement Value
53h	IBATM_AVE_VAL	Read Word	2	Battery Current (Dis-charge) Measurement Average Value
54h	VBAT_VAL	Read Word	2	Battery Voltage Measurement Value
55h	VBAT_AVE_VAL	Read Word	2	Battery Voltage Measurement Average Value
56h	THERM_VAL	Read/Write Word	2	Temperature Measurement Value
57h	VTH_VAL	Read Word	2	Thermistor Measurement Voltage Value
58h	IACP_VAL	Read Word	2	Input Current (between ACP-ACN) Measurement Value
59h	IACP_AVE_VAL	Read Word	2	Input Current (between ACP-ACN) Measurement Average Value
5Ah	VACP_VAL	Read Word	2	Input Voltage (ACP) Measurement Value
5Bh	VACP_AVE_VAL	Read Word	2	Input Voltage (ACP) Measurement Average Value
5Ch	VBUS_VAL	Read Word	2	VBUS Voltage Measurement Value
5Dh	VBUS_AVE_VAL	Read Word	2	VBUS Voltage Measurement Average Value
5Eh	VCC_VAL	Read Word	2	VCC Voltage Measurement Value
5Fh	VCC_AVE_VAL	Read Word	2	VCC Voltage Measurement Average Value
60h	VSYS_VAL	Read Word	2	VSYS Voltage Measurement Value
61h	VSYS_AVE_VAL	Read Word	2	VSYS Voltage Measurement Average Value
62h	EXTIADP_VAL	Read Word	2	IADP (Input current Limit setting pin) Voltage Measurement Value
63h	EXTIADP_AVE_VAL	Read Word	2	IADP (Input current Limit setting pin) Voltage Measurement Average Value
64h	VACPCLPS_TH_SET	Read/Write Word	2	VACP Collapse Detect Threshold Voltage Setting
65h	(reserved)	-	-	-
66h	(reserved)	-	-	-
67h	(reserved)	-	-	-
68h	INT0_SET	Read/Write Word	2	1st Level Interrupt Setting
69h	INT1_SET	Read/Write Word	2	2nd Level Interrupt Setting 1 (VBUS)
6Ah	INT2_SET	Read/Write Word	2	2nd Level Interrupt Setting 2 (VCC)

Code	Command	Protocols	Byte Size	Description
6Bh	INT3_SET	Read/Write Word	2	2nd Level Interrupt Setting 3 (Battery)
6Ch	INT4_SET	Read/Write Word	2	2nd Level Interrupt Setting 4 (VSYS)
6Dh	INT5_SET	Read/Write Word	2	2nd Level Interrupt Setting 5 (Charger)
6Eh	INT6_SET	Read/Write Word	2	2nd Level Interrupt Setting 6 (Charger)
6Fh	INT7_SET	Read/Write Word	2	2nd Level Interrupt Setting 7 (SAR-ADC)
70h	INT0_STATUS	Read/Write Word	2	1st Level Interrupt Status
71h	INT1_STATUS	Read/Write Word	2	2nd Level Interrupt Status 1 (VBUS)
72h	INT2_STATUS	Read/Write Word	2	2nd Level Interrupt Status 2 (VCC)
73h	INT3_STATUS	Read/Write Word	2	2nd Level Interrupt Status 3 (Battery)
74h	INT4_STATUS	Read/Write Word	2	2nd Level Interrupt Status 4 (VSYS)
75h	INT5_STATUS	Read/Write Word	2	2nd Level Interrupt Status 5 (Charger)
76h	INT6_STATUS	Read/Write Word	2	2nd Level Interrupt Status 6 (Charger)
77h	INT7_STATUS	Read/Write Word	2	2nd Level Interrupt Status 7 (SAR-ADC)
78h	REG0	Read/Write Word	2	Reserved Register 0 (for future use)
79h	REG1	Read/Write Word	2	Reserved Register 1 (for future use)
7Ah	OTPREG0	Read/Write Word	2	Input current limit degradation setting.
7Bh	OTPREG1	Read/Write Word	2	Reserved OTP-loaded Register 1 (for future use)
7Ch	SMBREG	Read/Write Word	2	Power Save Mode Setting.
7Dh	(reserved)	-	-	-
7Eh	(reserved)	-	-	-
7Fh	DEBUG_MODE_SET	Read/Write Word	2	Debug Mode Setting

8.3.3. Debug Commands

Following is a table of "Debug Commands" which BD99954 supports. "Debug Commands" is used for debug purpose or in production test.

Note: Reserved command should not be accessed. If accessed, operation is not guaranteed.