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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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2.7V to 5.5V Input, 4A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9A400MUV

General Description

BD9A400MUV is a synchronous buck switching regulator with built-in low on-resistance power MOSFETs. It is capable of providing current up to 4A.The SLLM™ control provides excellent efficiency characteristics in light-load conditions which make the product ideal for equipment and devices that demand minimal standby power consumption. The oscillating frequency is high at 1MHz using a small value of inductance. It is a current mode control DC/DC converter and features high-speed transient response. Phase compensation can also be set easily.

Features

- Synchronous Single DC/DC Converter.
- SLLM™ (Simple Light Load Mode) Control.
- Over Current Protection.
- Short Circuit Protection.
- Thermal Shutdown Protection.
- Under Voltage Lockout Protection.
- Adjustable Soft start Function.
- Power Good Output.
- VQFN016V3030 Package (Backside Heat Dissipation)

Applications

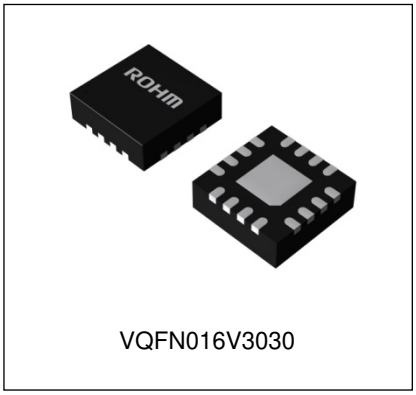
- Step-Down Power Supply for DSPs, FPGAs, Microprocessors, etc.
- Laptop PCs/ Tablet PCs/ Servers.
- LCD TVs.
- Storage Devices (HDDs/SSDs).
- Printers, OA Equipment.
- Entertainment Devices.
- Distributed Power Supply, Secondary Power Supply.

Key Specifications

- Input Voltage Range: 2.7V to 5.5V
- Output Voltage Range: 0.8V to V_{PVIN}×0.7V
- Average Output Current: 4A(Max)
- Switching Frequency: 1MHz(Typ)
- High-Side MOSFET On-Resistance: 60mΩ (Typ)
- Low-Side MOSFET On-Resistance: 60mΩ (Typ)
- Standby Current: 0μA (Typ)

Package

	W(Typ) x D(Typ) x H(Max)
VQFN016V3030	3.00mm x 3.00mm x 1.00mm



Typical Application Circuit

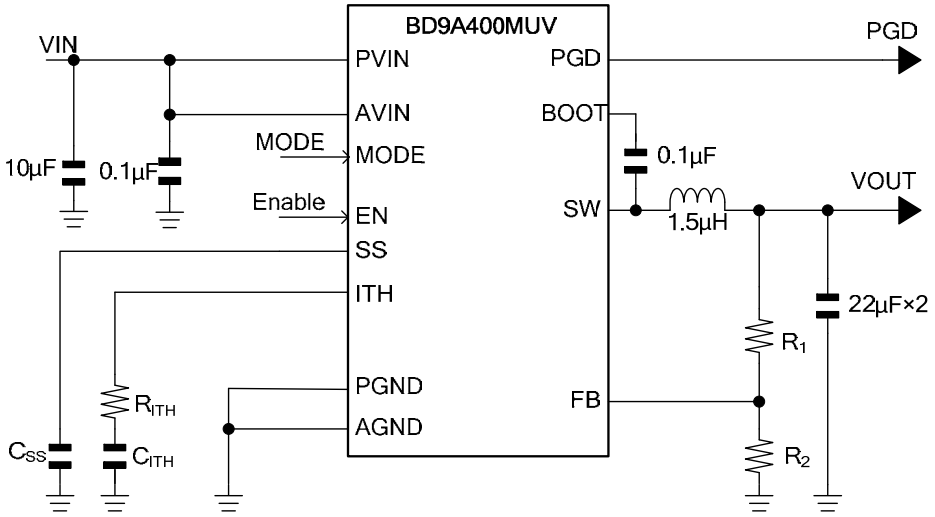


Figure 1. Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

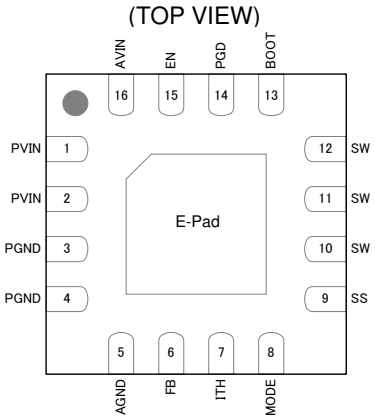


Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Function
1, 2	PVIN	Power supply terminals for the switching regulator. These terminals supply power to the output stage of the switching regulator. Connecting a 10µF ceramic capacitor is recommended.
3, 4	PGND	Ground terminals for the output stage of the switching regulator.
5	AGND	Ground terminal for the control circuit.
6	FB	An inverting input node for the gm error amplifier. See page 23 for how to calculate the resistance of the output voltage setting.
7	ITH	An input terminal for the gm error amplifier output and the output switch current comparator. Connect a frequency phase compensation component to this terminal. See page 24 for how to calculate the resistance and capacitance for phase compensation.
8	MODE	Turning this terminal signal Low (0.2V or lower) forces the device to operate in the fixed frequency PWM mode. Turning this terminal signal High (0.8V or higher) enables the SLLM control and the mode is automatically switched between the SLLM control and fixed frequency PWM mode.
9	SS	Terminal for setting the soft start time. The rise time of the output voltage can be specified by connecting a capacitor to this terminal. See page 23 for how to calculate the capacitance.
10, 11, 12	SW	Switch nodes. These terminals are connected to the source of the high-side MOSFET and drain of the low-side MOSFET. Connect a bootstrap capacitor of 0.1µF between these terminals and BOOT terminals. In addition, connect an inductor of 1.5µH considering the direct current superimposition characteristic.
13	BOOT	Connect a bootstrap capacitor of 0.1µF between this terminal and SW terminals. The voltage of this capacitor is the gate drive voltage of the high-side MOSFET.
14	PGD	A “Power Good” terminal, an open drain output. Use of pull up resistor is needed. See page 18 for how to specify the resistance. When the FB terminal voltage reaches within ±7% of 0.8V (Typ), the internal Nch MOSFET turns off and the output turns High.
15	EN	Turning this terminal signal low (0.8V or lower) forces the device to enter the shutdown mode. Turning this terminal signal high (2.0V or higher) enables the device. This terminal must be terminated.
16	AVIN	Supplies power to the control circuit of the switching regulator. Connecting a 0.1µF ceramic capacitor is recommended.
-	E-Pad	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using multiple vias provides excellent heat dissipation characteristics.

Block Diagram

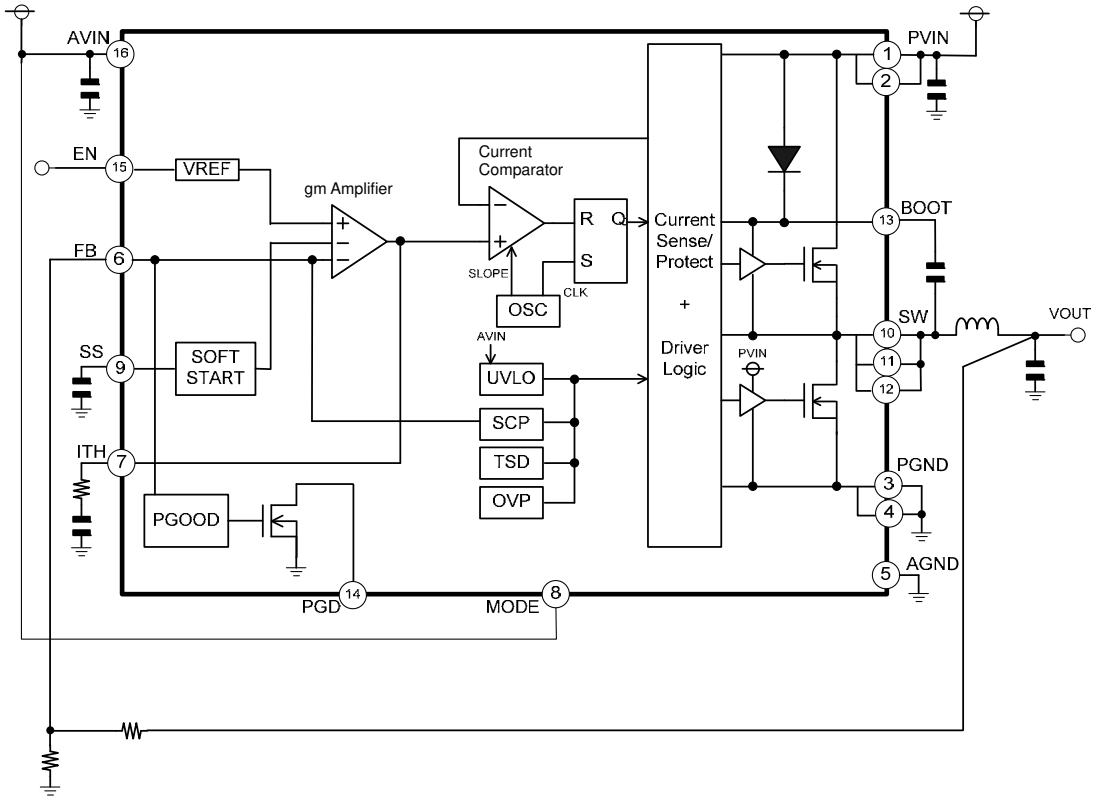


Figure 3. Block Diagram

Description of Blocks

1. VREF
   The VREF block generates the internal reference voltage.

2. UVLO
   The UVLO block is for under voltage lockout protection. It will shut down the IC when the VIN falls to 2.45V (Typ) or lower. The threshold voltage has a hysteresis of 100mV (Typ).

3. SCP
   After the soft start is completed and when the feedback voltage of the output voltage has fallen below 0.4V (Typ) for 1msec (Typ), the SCP stops the operation for 16msec (Typ) and subsequently initiates restart.

4. OVP
   Over voltage protection function (OVP) compares FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage exceeds 0.88V (Typ) it turns MOSFET of output part MOSFET off. After output voltage drop it returns with hysteresis.

5. TSD
   The TSD block is for thermal protection. The thermal protection circuit shuts down the device when the internal temperature of IC rises to 175°C (Typ) or higher. Thermal protection circuit resets when the temperature falls. The circuit has a hysteresis of 25°C (Typ).

6. SOFT START
   The Soft Start circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current. A built-in soft start function is provided and a soft start is initiated in 1msec (Typ) when the SS terminal is open.

7. gm Amplifier
   The gm Amplifier block compares the reference voltage with the feedback voltage of the output voltage. The error and the ITH terminal voltage determine the switching duty. A soft start is applied at startup. The ITH terminal voltage is limited by the internal slope voltage.

8. Current Comparator
   The Current Comparator block compares the output ITH terminal voltage of the error amplifier and the slope block signal to determine the switching duty. In the event of over current, the current that flows through the high-side MOSFET is limited at each cycle of the switching frequency.

9. OSC
   This block generates the oscillating frequency.

10. DRIVER LOGIC
    This block is a DC/DC driver. A signal from current comparator is applied to drive the MOSFETs.

11. PGOOD
    When the FB terminal voltage reaches 0.8V (Typ) within ±7%, the Nch MOSFET of the built-in open drain output turns off and the output turns high.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{PVIN}, V_{AVIN}	-0.3 to +7	V
EN Voltage	V_{EN}	-0.3 to +7	V
MODE Voltage	V_{MODE}	-0.3 to +7	V
PGD Voltage	V_{PGD}	-0.3 to +7	V
Voltage from GND to BOOT	V_{BOOT}	-0.3 to +14	V
Voltage from SW to BOOT	ΔV_{BOOT}	-0.3 to +7	V
FB Voltage	V_{FB}	-0.3 to +7	V
ITH Voltage	V_{ITH}	-0.3 to +7	V
SW Voltage	V_{SW}	-0.3 to V_{PVIN} + 0.3	V
Allowable Power Dissipation(Note 1)	Pd	2.66	W
Operating Temperature Range	Topr	-40 to 85	°C
Storage Temperature Range	Tstg	-55 to 150	°C

(Note 1) When mounted on a 70mm x 70mm x 1.6mm 4-layer glass epoxy board (copper foil area: 70 mm x 70 mm)
Derate by 21.3mW when operating above 25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{PVIN}, V_{AVIN}	2.7	-	5.5	V
Output Current(Note 2)	I_{OUT}	-	-	4	A
Output Voltage Range	V_{RANGE}	0.8	-	V_{PVIN} × 0.7	V

(Note 2) Pd,ASO should not be exceeded.

Electrical Characteristics (Unless otherwise specified Ta = 25°C, VAVIN = VPVIN = 5V, VEN = 5V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
AVIN PIN						
Standby Supply Current	I_{STB}	-	0	10	µA	EN= GND
Operating Supply Current	I_{CC}	-	350	500	µA	I_{OUT}= 0mA Non-switching
UVLO Detection Voltage	V_{UVLO1}	2.35	2.45	2.55	V	V_{IN} falling
UVLO Release Voltage	V_{UVLO2}	2.425	2.55	2.7	V	V_{IN} rising
ENABLE						
EN Threshold Voltage High	V_{ENH}	2.0	-	-	V	
EN Threshold Voltage Low	V_{ENL}	-	-	0.8	V	
EN Input Current	I_{EN}	-	5	10	µA	EN= 5V
MODE						
MODE Threshold Voltage	V_{MODEH}	0.2	0.4	0.8	V	
MODE Input Current	I_{MODE}	-	10	20	µA	MODE= 5V
Reference Voltage, Error Amplifier						
FB Terminal Voltage	V_{FB}	0.792	0.8	0.808	V	
FB Input Current	I_{FB}	-	0	1	µA	FB= 0.8V
ITH Sink Current	I_{THSI}	10	20	40	µA	FB= 0.9V
ITH Source Current	I_{THSO}	10	20	40	µA	FB= 0.7V
Soft Start Time	T_{SS}	0.5	1.0	2.0	ms	With internal constant
Soft Start Current	I_{SS}	0.9	1.8	3.6	µA	
SWITCHING FREQUENCY						
Switching Frequency	F_{OSC}	800	1000	1200	kHz	
POWER GOOD						
Falling (Fault) Voltage	V_{PGDFF}	87	90	93	%	OUTPUT voltage falling
Rising (Good) Voltage	V_{PGDRG}	90	93	96	%	OUTPUT voltage rising
Rising (Fault) Voltage	V_{PGDRF}	107	110	113	%	OUTPUT voltage rising
Falling (Good) Voltage	V_{PGDFG}	104	107	110	%	OUTPUT voltage falling
PGD Output Leakage Current	I_{LKPGD}	-	0	5	µA	PGD= 5V
Power Good ON Resistance	R_{PGD}	-	100	200	Ω	
Power Good Low Level Voltage	P_{GDVL}	-	0.1	0.2	V	I_{PGD}= 1mA
SWITCH MOSFET						
High Side FET ON Resistance	R_{ONH}	-	60	120	mΩ	BOOT – SW= 5V
Low Side FET ON Resistance	R_{ONL}	-	60	120	mΩ	
High Side Output Leakage Current	R_{ILH}	-	0	10	µA	Non-switching
Low Side Output Leakage Current	R_{ILL}	-	0	10	µA	Non-switching
SCP						
Short Circuit Protection Detection Voltage	V_{SCP}	0.28	0.4	0.52	V	

Typical Performance Curves

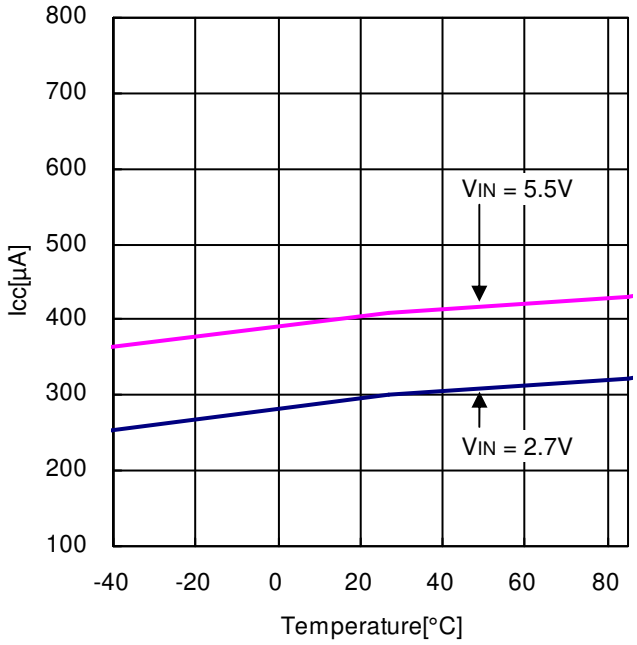


Figure 4. Operating Current vs Temperature

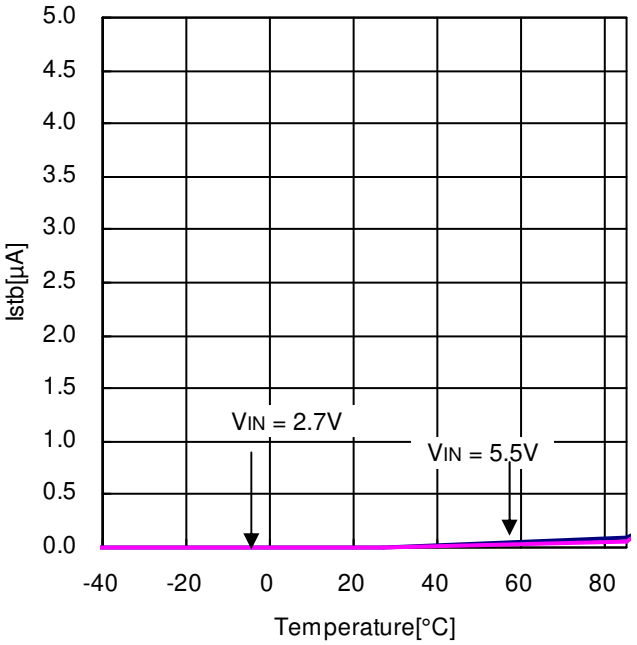


Figure 5. Stand-by Current vs Temperature

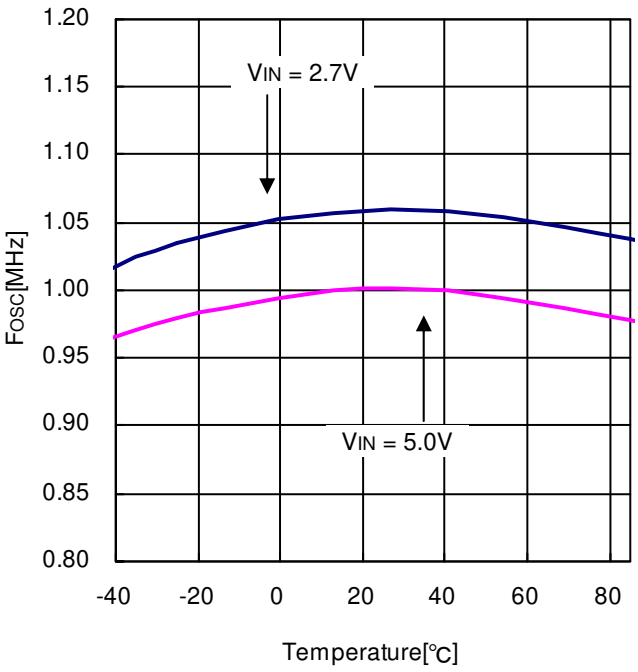


Figure 6. Switching Frequency vs Temperature

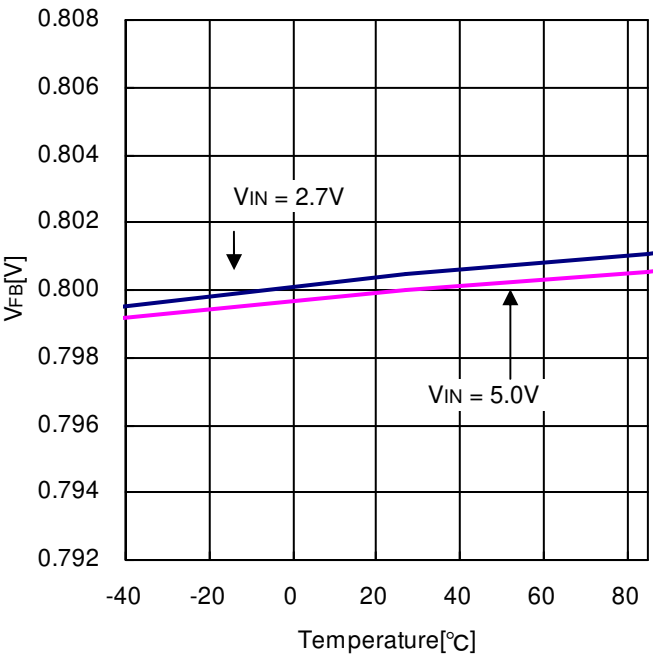


Figure 7. FB Voltage Reference vs Temperature

Typical Performance Curves - continued

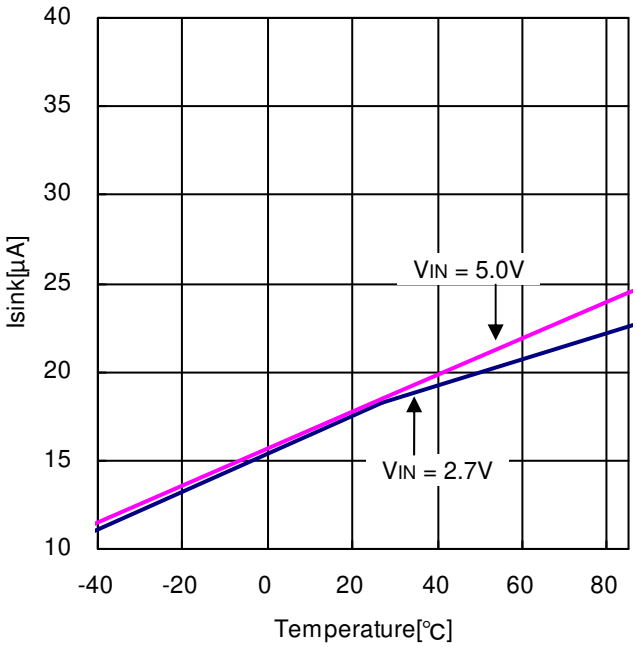


Figure 8. ITH Sink Current vs Temperature

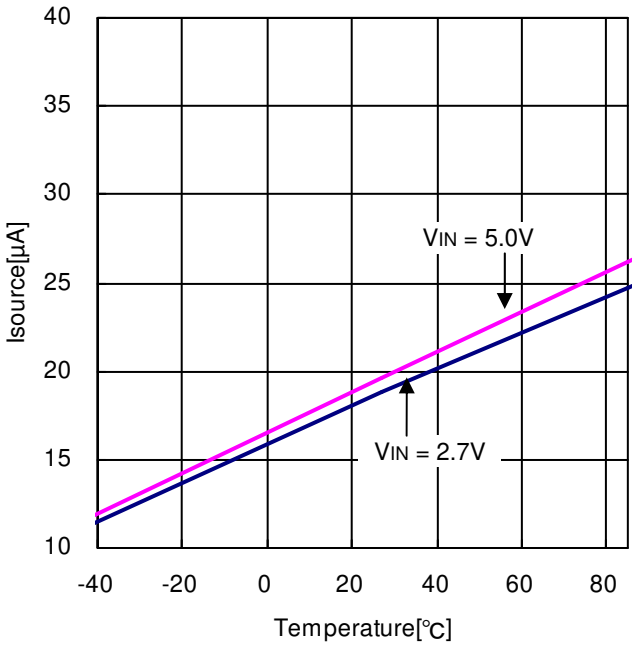


Figure 9. ITH Source Current vs Temperature

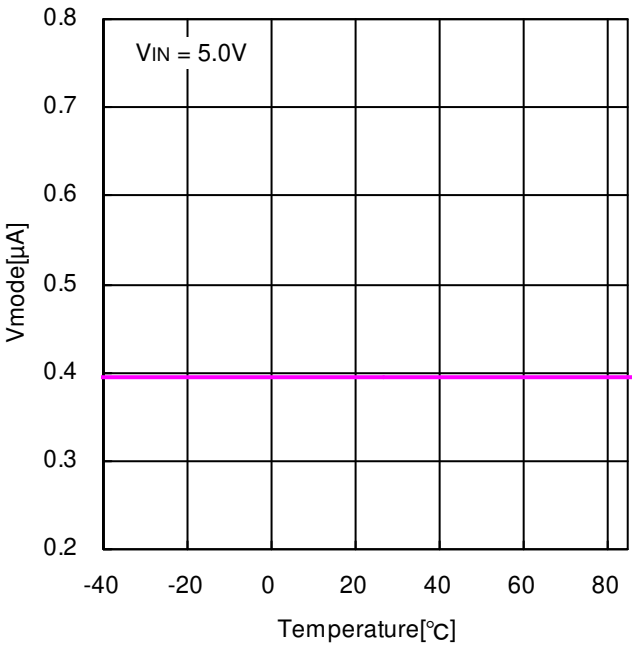


Figure 10. Mode Threshold vs Temperature

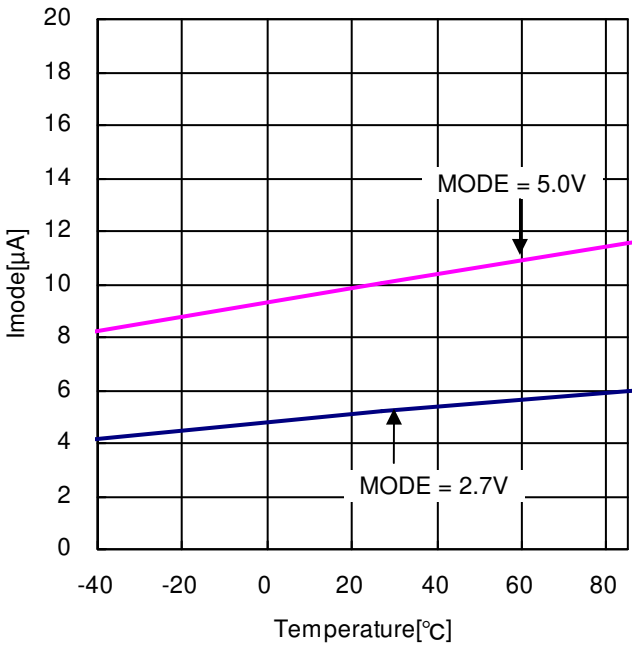


Figure 11. Mode Input Current vs Temperature

Typical Performance Curves - continued

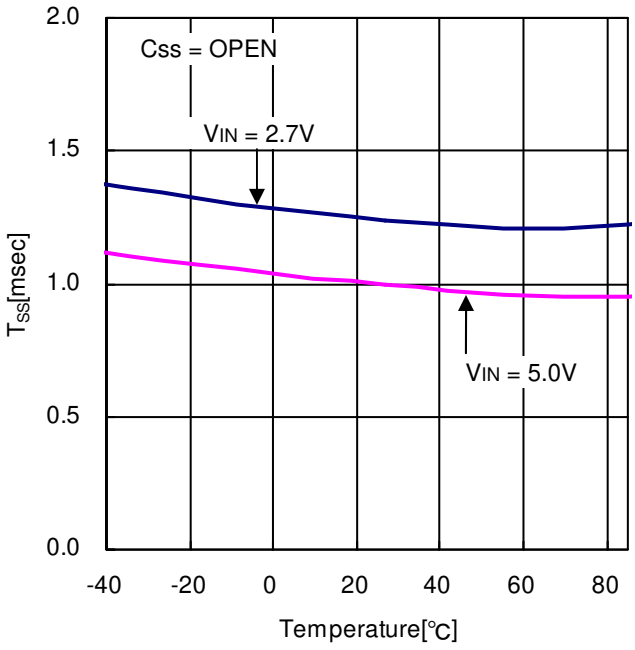


Figure 12. Soft Start Time vs Temperature

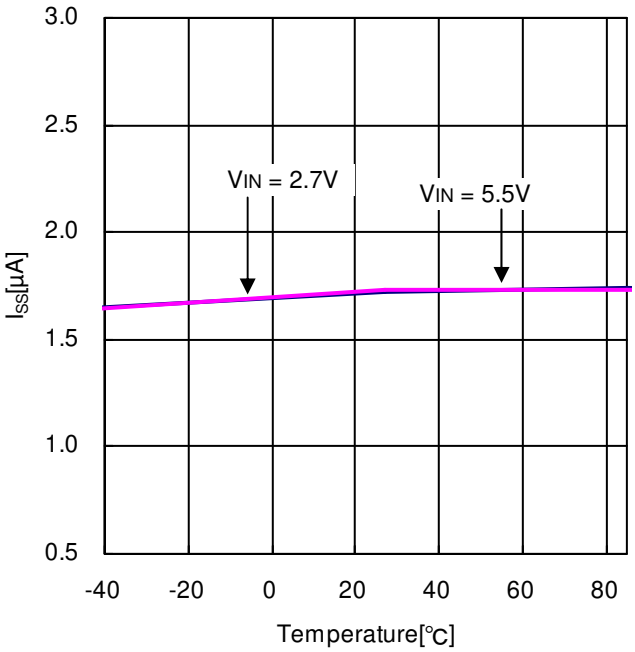


Figure 13. Soft Start Terminal Current vs Temperature

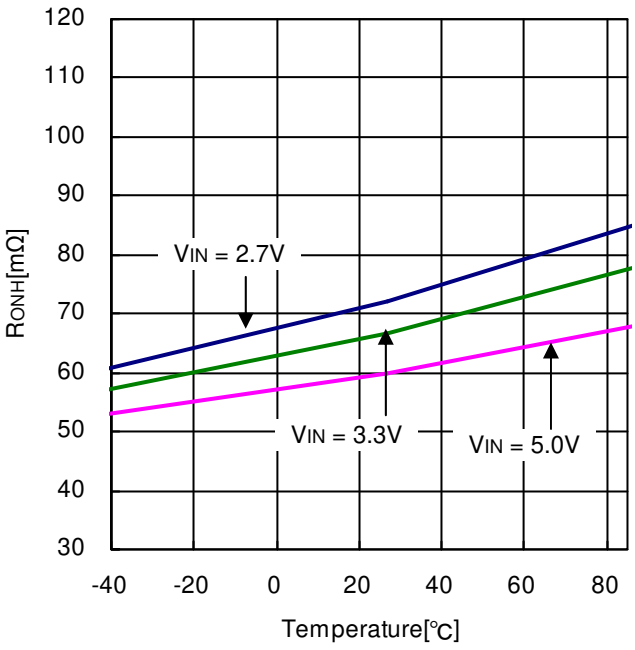


Figure 14. High side FET ON-Resistance vs Temperature

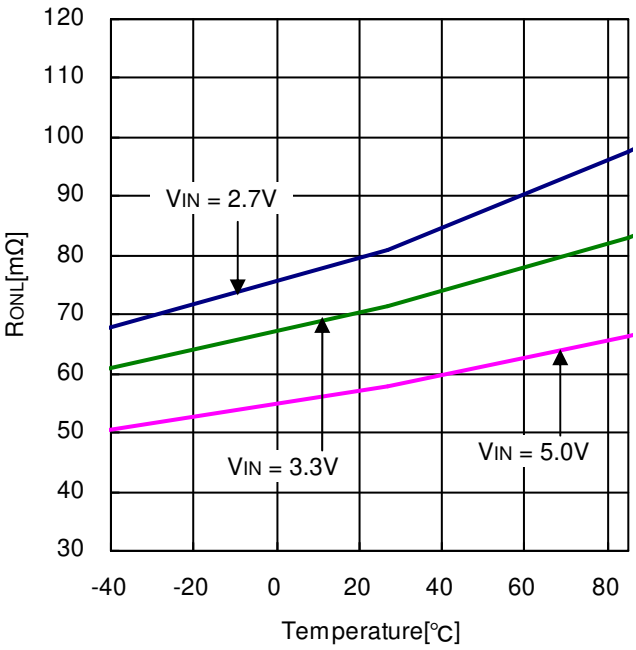


Figure 15. Low side FET ON-Resistance vs Temperature

Typical Performance Curves - continued

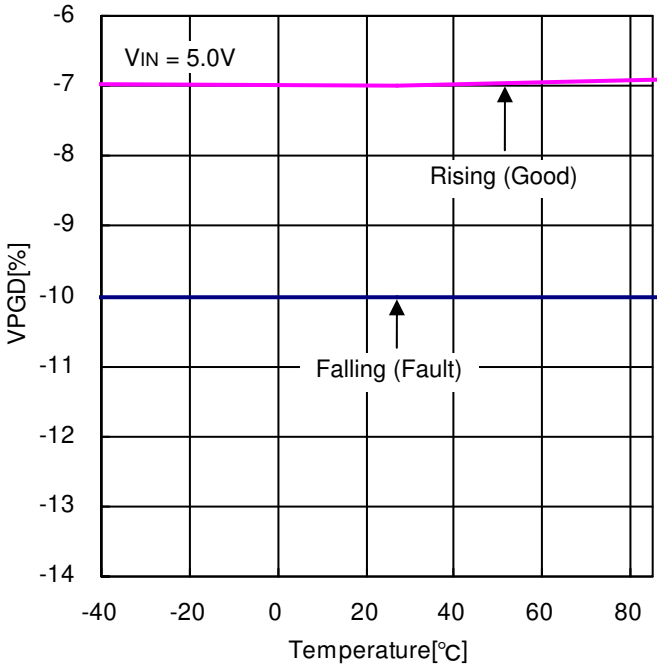


Figure 16. PGD Voltage vs Temperature

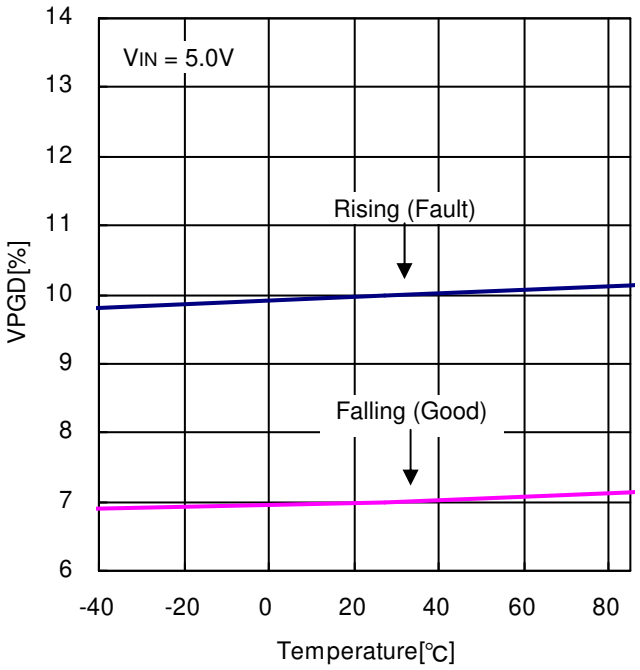


Figure 17. PGD Voltage vs Temperature

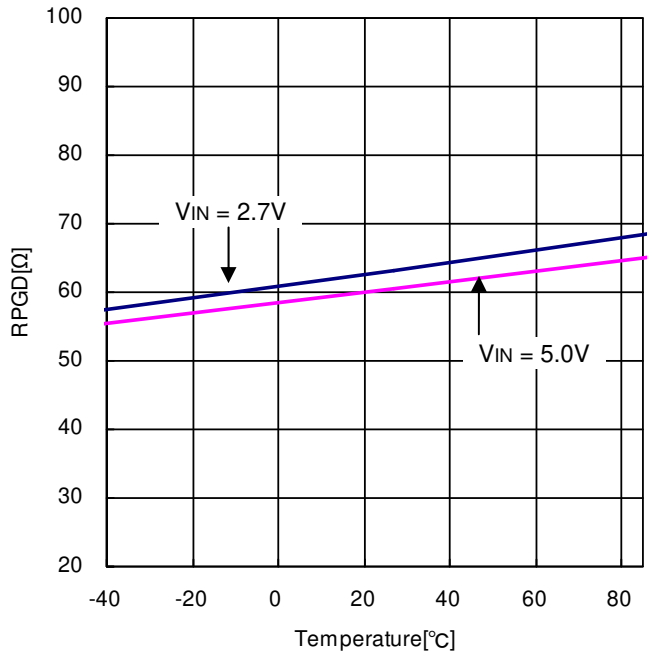


Figure 18. PGD ON-Resistance vs Temperature

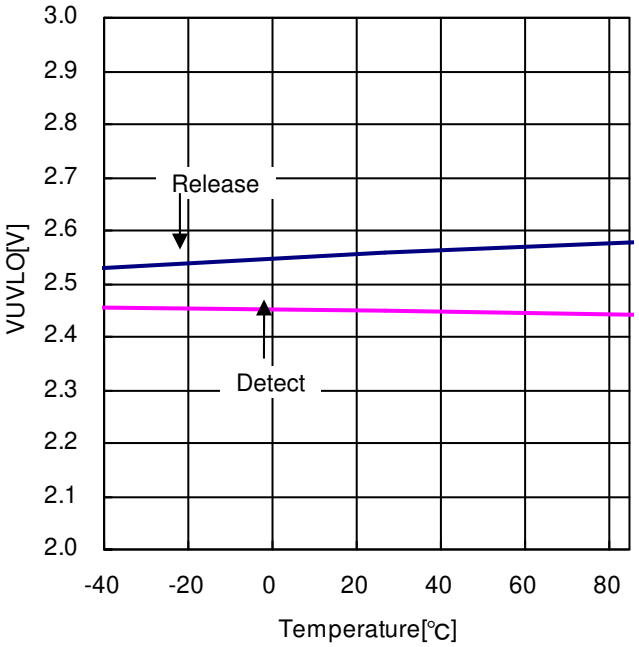


Figure 19. UVLO Threshold vs Temperature

Typical Performance Curves - continued

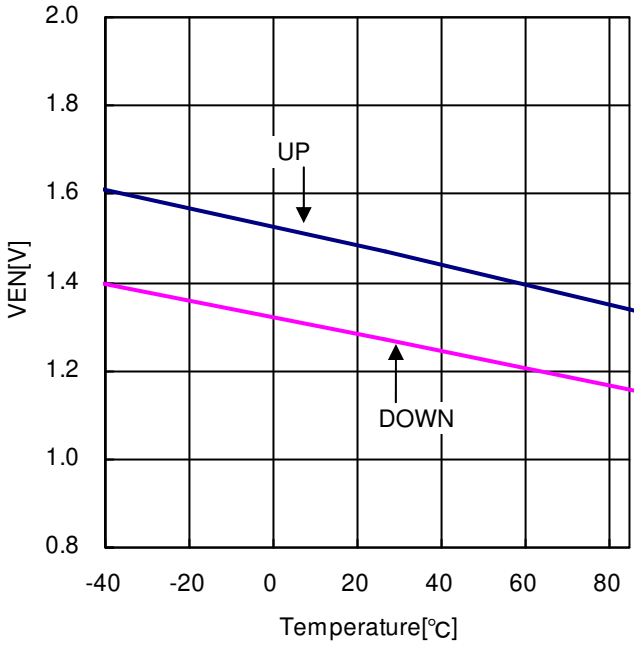


Figure 20. EN Threshold vs Temperature

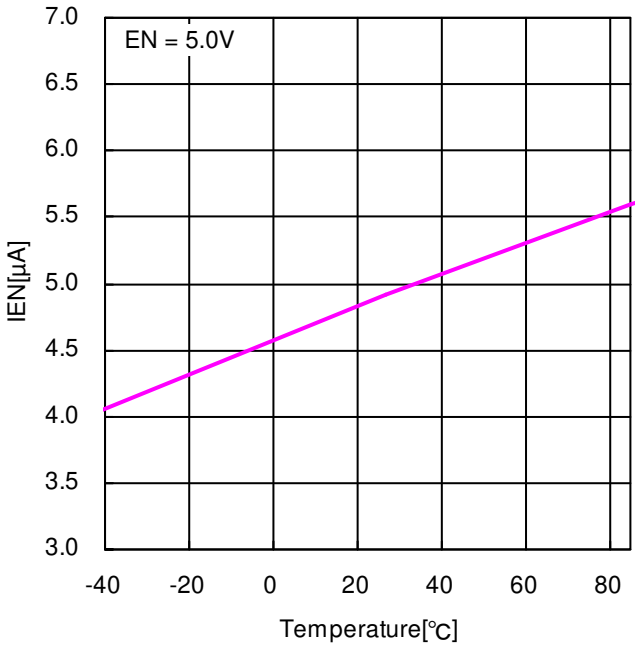


Figure 21. EN Input Current vs Temperature

Typical Performance Curves (Application)

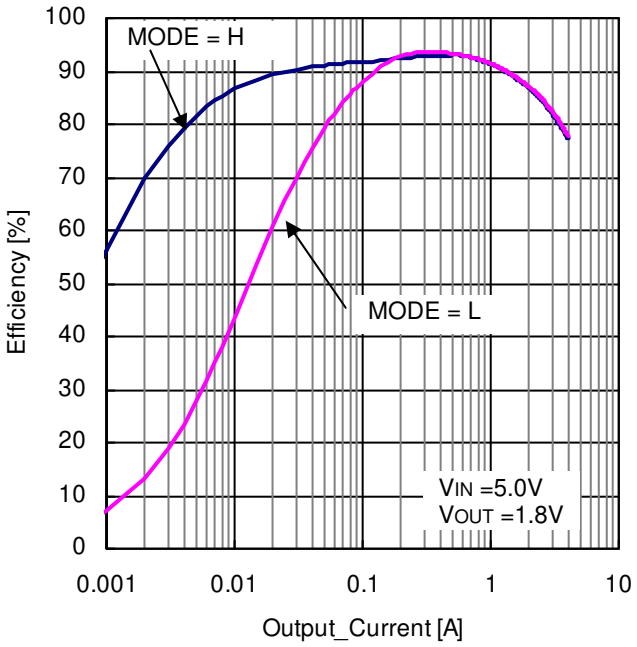


Figure 22. Efficiency vs Load Current
(VIN=5V, VOUT=1.8V, L=1.5µH)

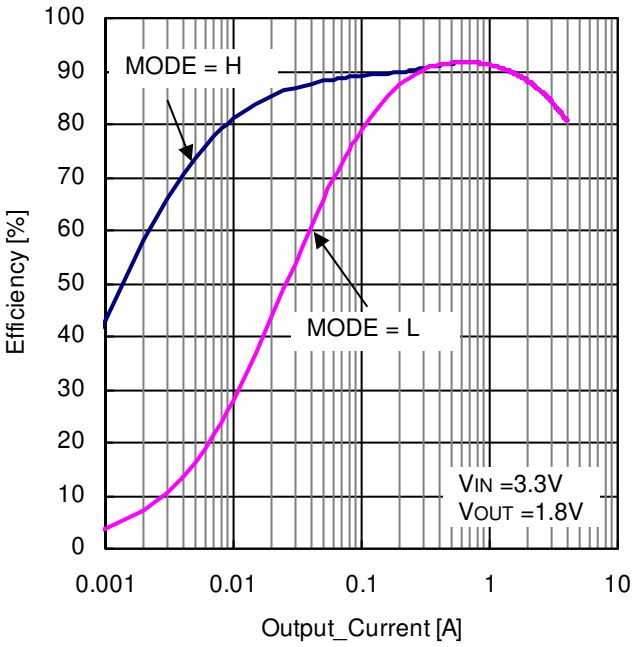


Figure 23. Efficiency vs Load Current
(VIN=3.3V, VOUT=1.8V, L=1.5µH)

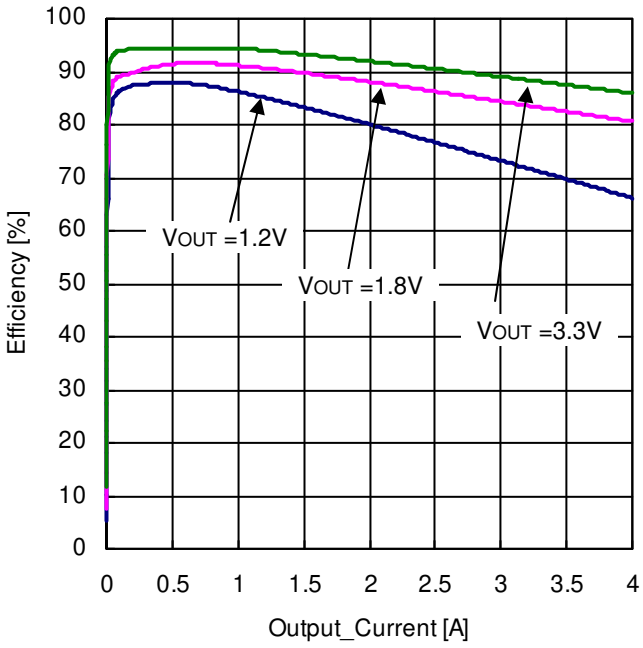


Figure 24. Efficiency vs Load Current
(VIN = 5.0V, MODE = 5.0V, L=1.5µH)

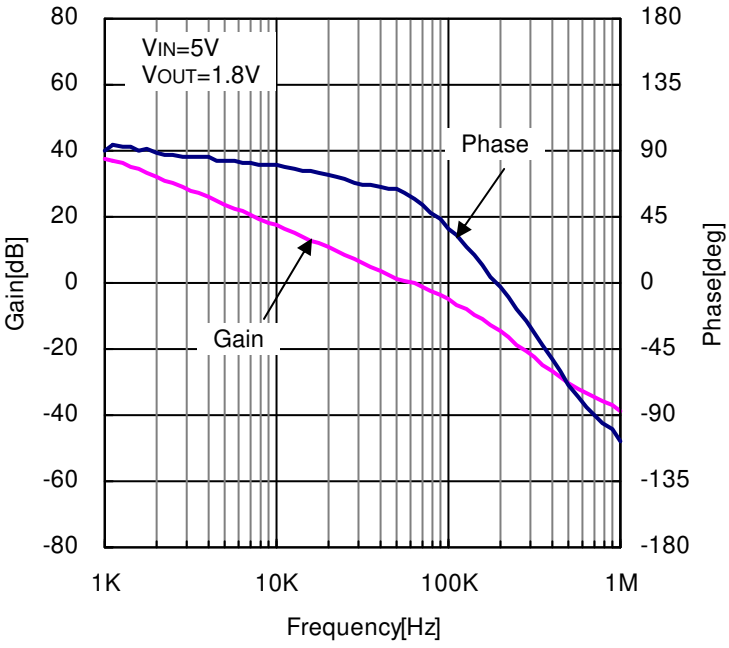


Figure 25. Closed Loop Response
(VIN=5V, VOUT=1.8V, IOUT=1A, L=1.5µH, C_{OUT}=Ceramic 44µF)

Typical Performance Curves (Application) - continued

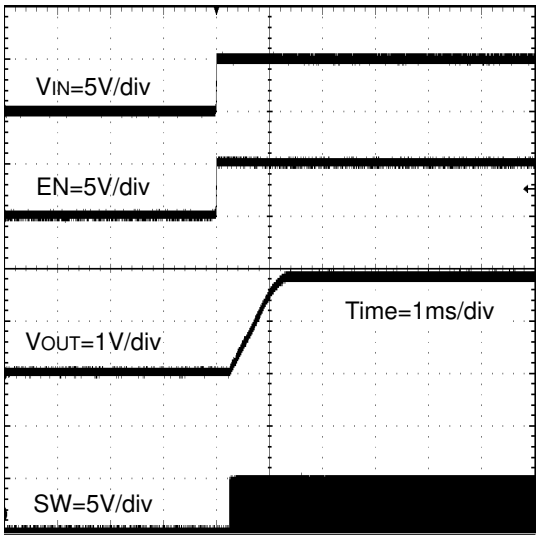


Figure 26. Power Up (V_{IN} = EN)

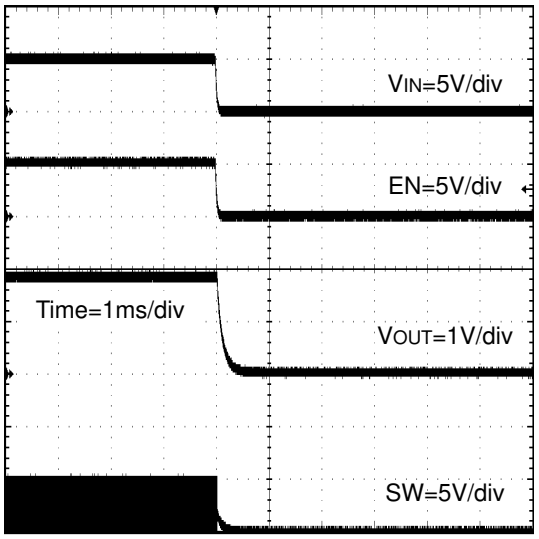


Figure 27. Power Down (V_{IN} = EN)

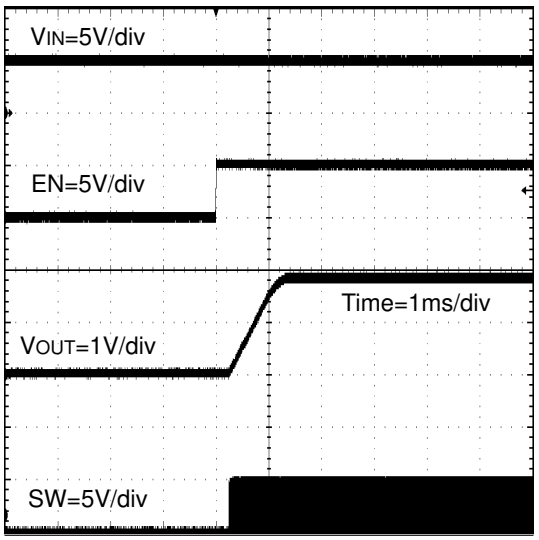


Figure 28. Power Up (EN = 0V→5V)

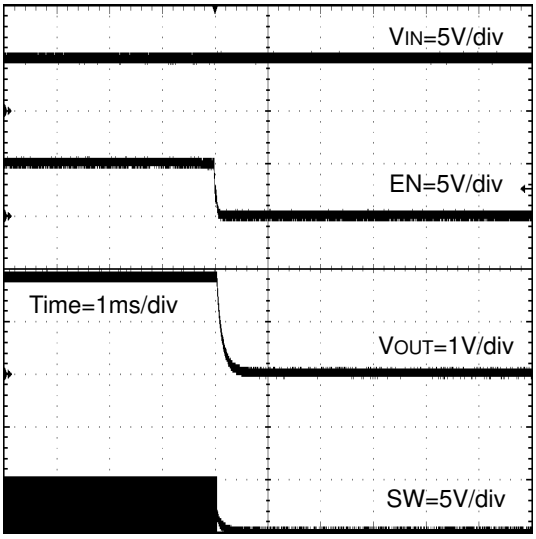


Figure 29. Power Down (EN = 5V→0V)

Typical Performance Curves (Application) - continued

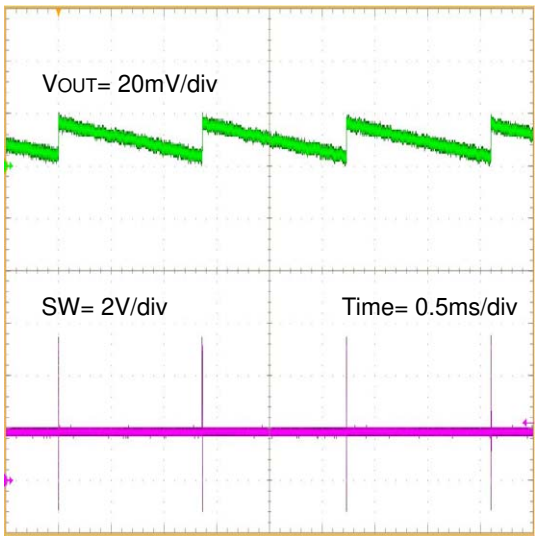


Figure 30. Output Ripple
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0A)

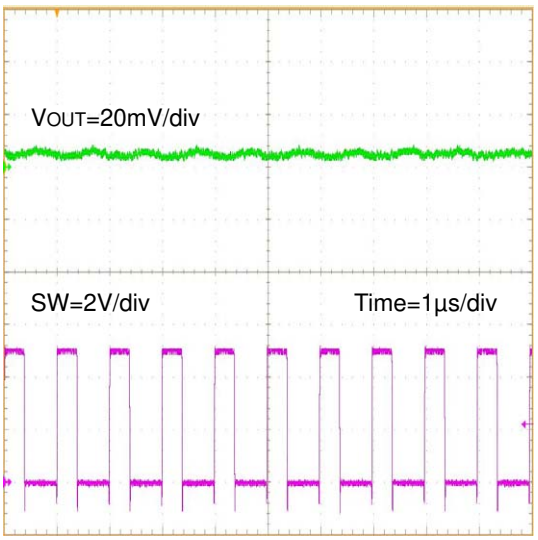


Figure 31. Output Ripple
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 4A)

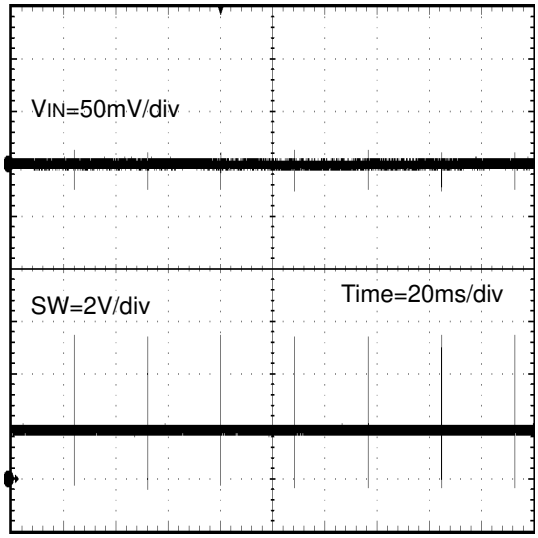


Figure 32. Input Ripple
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0A)

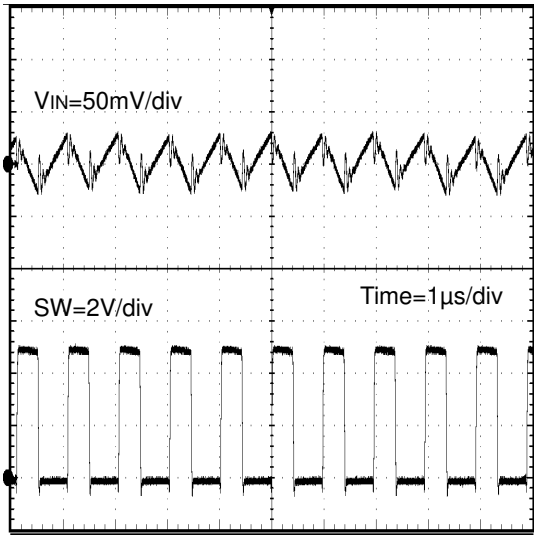


Figure 33. Input Ripple
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 4A)

Typical Performance Curves (Application) - continued

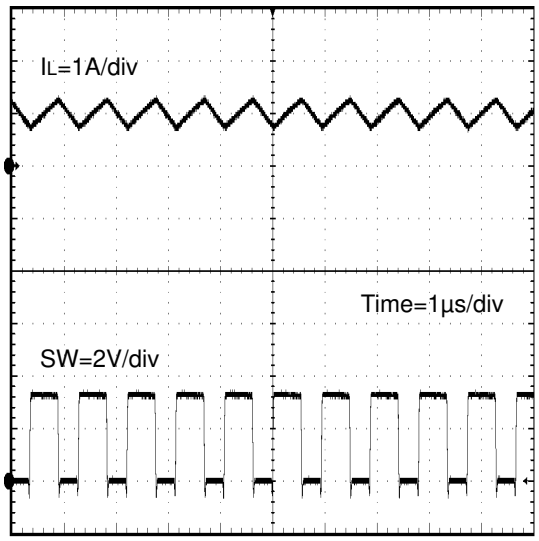


Figure 34. Switching Waveform
(V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 1A, L=1.5µH)

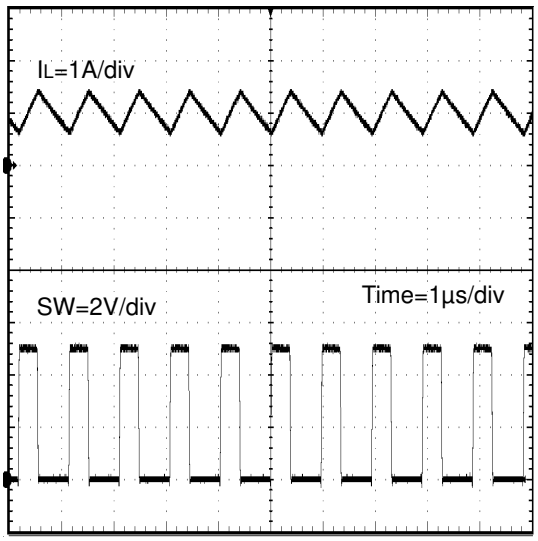


Figure 35. Switching Waveform
(V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 1A, L=1.5µH)

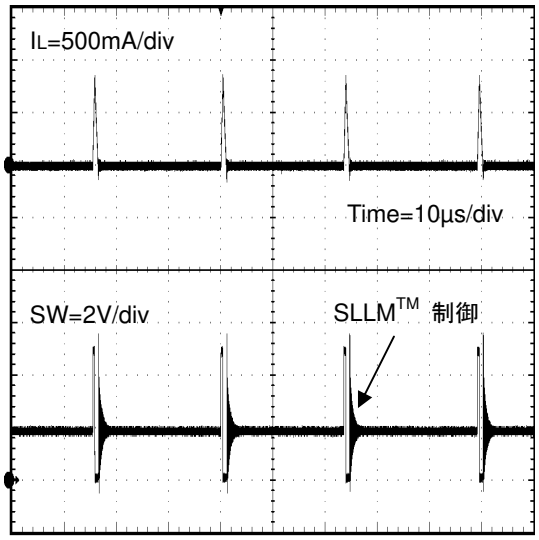


Figure 36. Switching Waveform with SLLM™
(V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 30mA, L=1.5µH)

Typical Performance Curves (Application) - continued

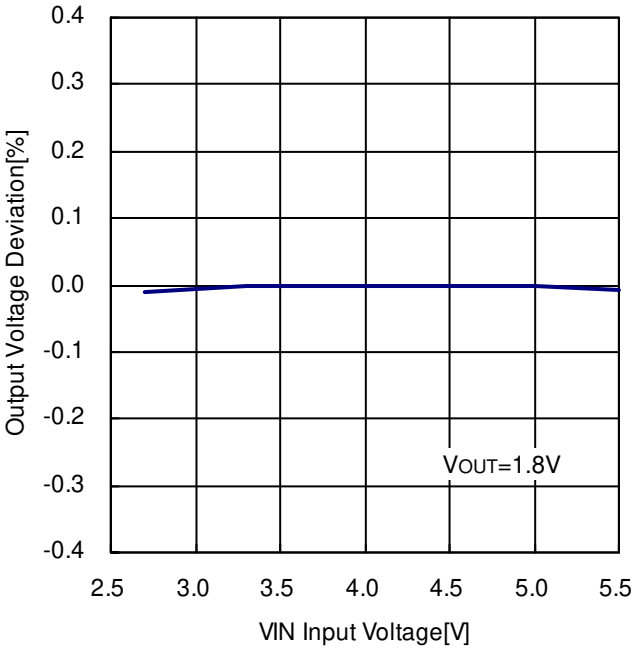


Figure 37. Line Regulation vs Input Voltage

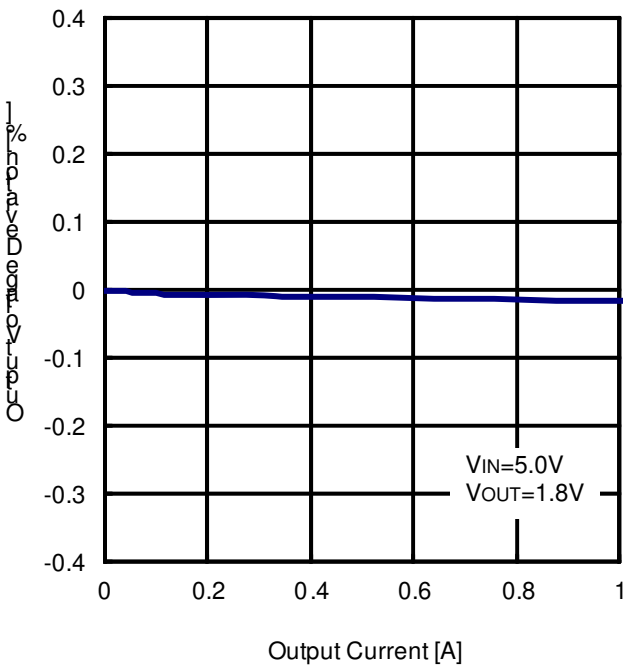


Figure 38. Load Regulation vs Load Current

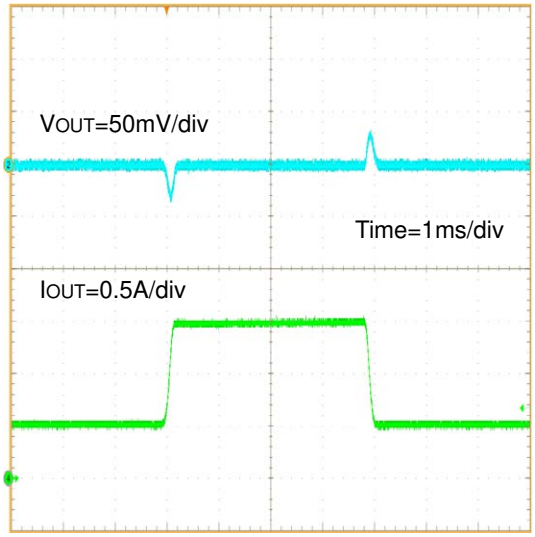


Figure 39. Load Transient Response IOUT=1A to 3A load step
(VIN=5V, VOUT=1.8V, COUT=Ceramic 44µF)

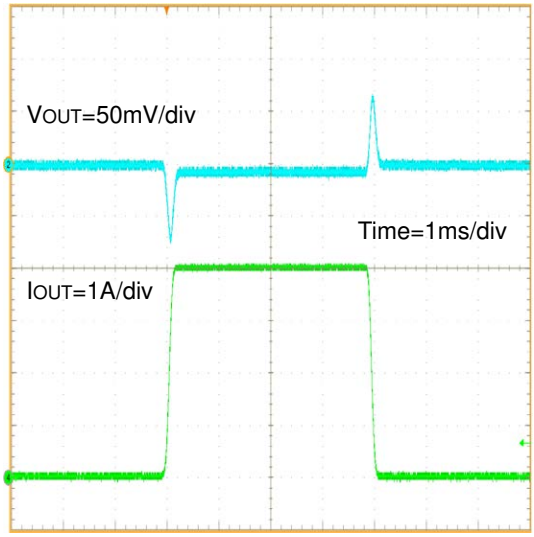


Figure 40. Load Transient Response IOUT=0A to 4A
(VIN=5V, VOUT=1.8V, COUT=Ceramic 44µF)

1. Function Explanations
   (1) DC/DC converter operation

BD9A400MUV is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM (Simple Light Load Mode) control for lighter load to improve efficiency.

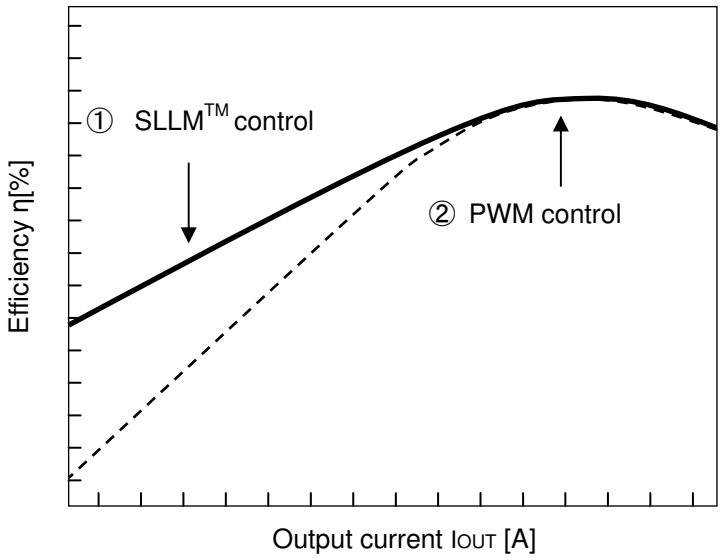


Figure 41. Efficiency (SLLM™ control and PWM control)

①SLLM™ control

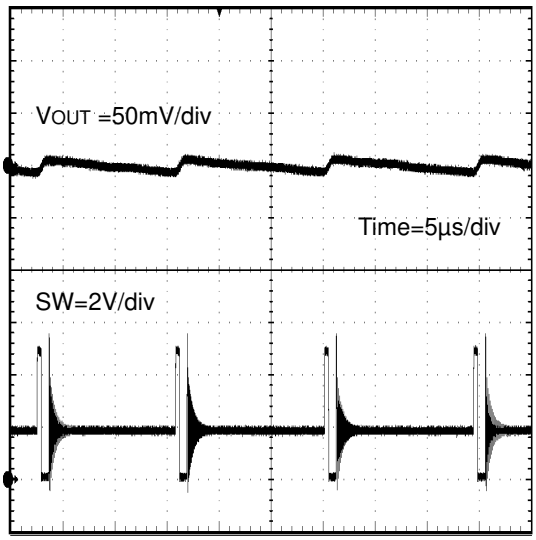


Figure 42. SW Waveform (SLLM™ control)
(V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 50mA)

②PWM control

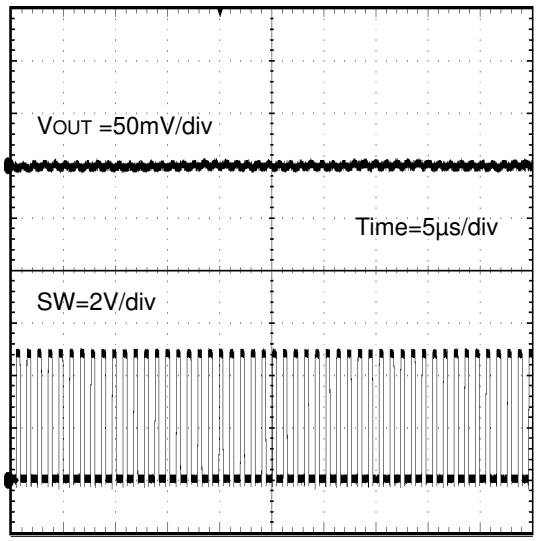


Figure 43. SW Waveform (PWM control)
(V_{IN} = 5.0V, V_{OUT} = 1.8V, I_{OUT} = 1A)

(2) Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When the EN terminal voltage is 2.0V or higher, the internal circuit is activated and the IC starts up. To enable shutdown control with the EN terminal, the shutdown interval (Low level interval of EN) must be set to 100µs or longer.

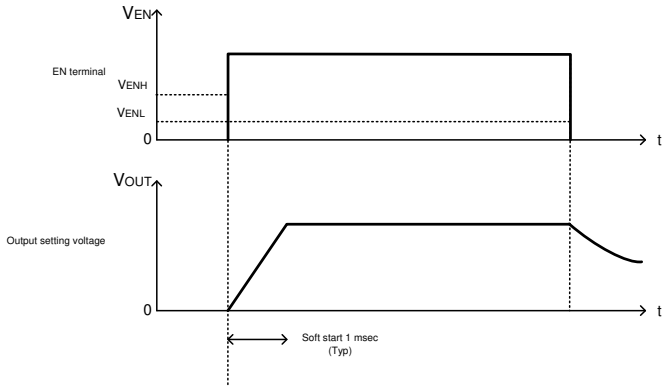


Figure 44. Start Up and Down with Enable

(3) Power Good

When the output voltage reaches outside ±10% of the voltage setting, the open drain N-ch MOSFET internally connected to the PGD terminal turns on and the PGD terminal is pulled down with an impedance of 100Ω (Typ). A hysteresis of 3% applies to resetting. Connecting a pull up resistor (10kΩ to 100kΩ) is recommended.

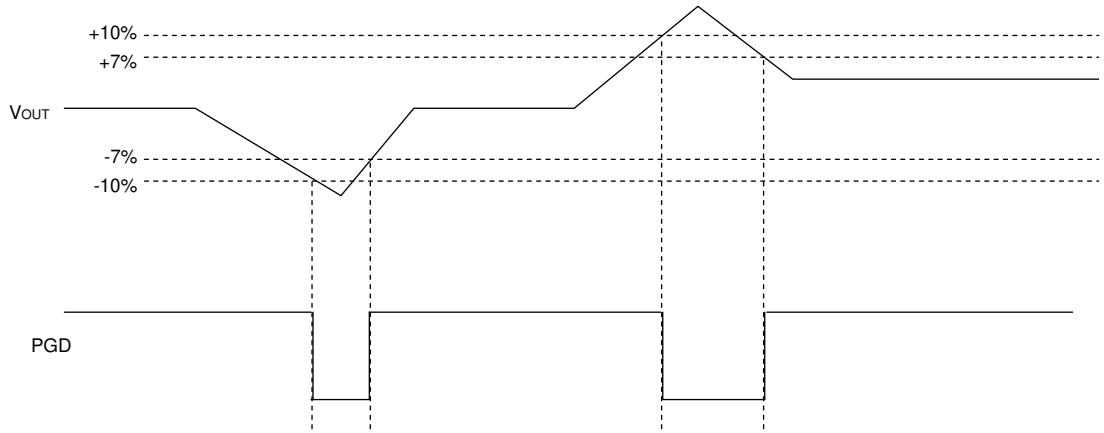


Figure 45. PGD Timing Chart

2. Protection

The protective circuits are intended for prevention of damage caused by unexpected accidents. Do not use them for continuous protective operation.

(1) Short Circuit Protection (SCP)
The short circuit protection block compares the FB terminal voltage with the internal reference voltage VREF. When the FB terminal voltage has fallen below 0.4V (Typ) and remained there for 1msec (Typ), SCP stops the operation for 16msec (Typ) and subsequently initiates a restart.

EN Terminal	FB Terminal	Short Circuit Protection	Short Circuit Protection Operation
2.0V or higher	＜0.4V(Typ)	Enabled	ON
	＞0.4V(Typ)		OFF
0.8V or lower	-	Disabled	OFF

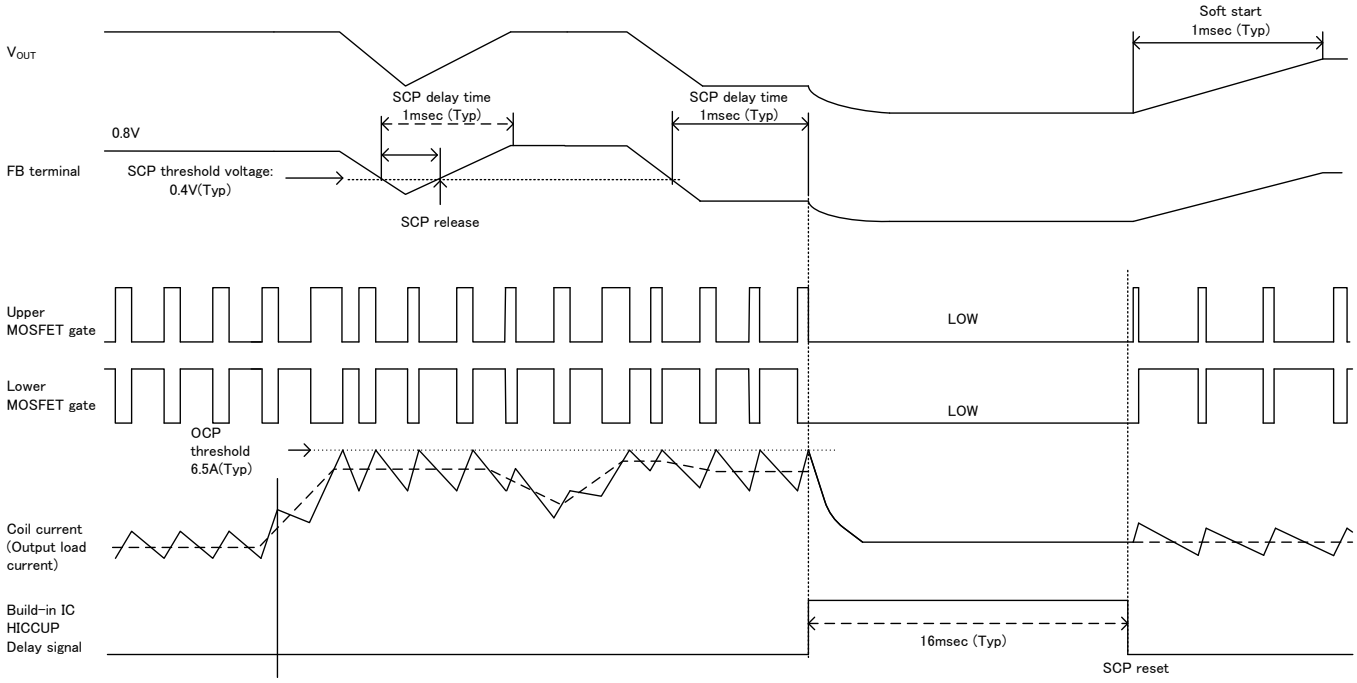


Figure 46. Short Circuit Protection (SCP) timing chart

(2) Under Voltage Lockout Protection (UVLO)
The Under Voltage Lockout Protection circuit monitors the AVIN terminal voltage.
The operation enters standby when the AVIN terminal voltage is 2.45V (Typ) or lower.
The operation starts when the AVIN terminal voltage is 2.55V (Typ) or higher.

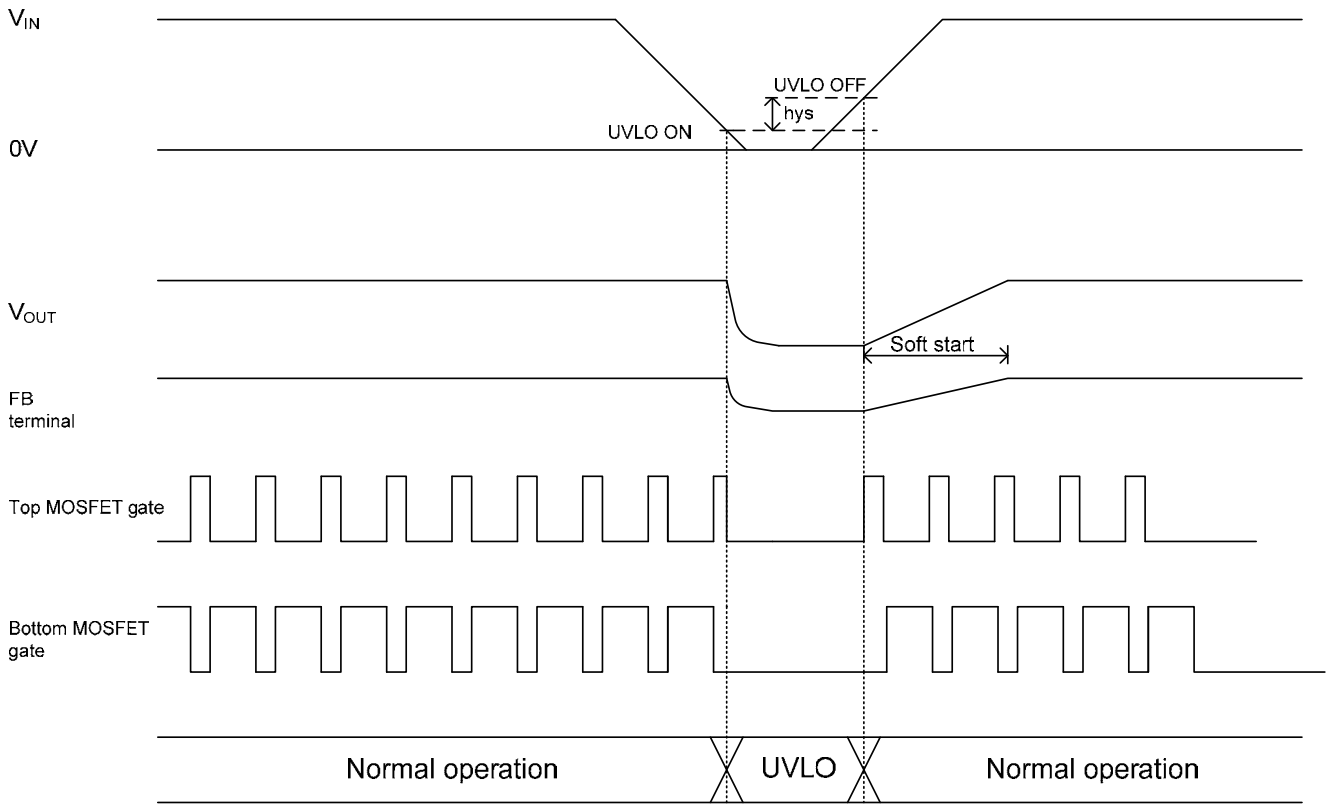


Figure 47. UVLO Timing Chart

(3) Thermal Shutdown
When the chip temperature exceeds Tj = 175°C, the DC/DC converter output is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding Tjmax = 150°C. It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.

(4) Over Current Protection
The Over Current Protection function operates by using the current mode control to limit the current that flows through the high-side MOSFET at each cycle of the switching frequency. The designed over current limit value is 6.5A (Typ).

(5) Over Voltage Protection (OVP)
Over voltage protection function (OVP) compares FB terminal voltage with internal standard voltage VREF and when FB terminal voltage exceeds 0.88V (Typ) it turns MOSFET of output part MOSFET off. After output voltage drop it returns with hysteresis.

Application Example

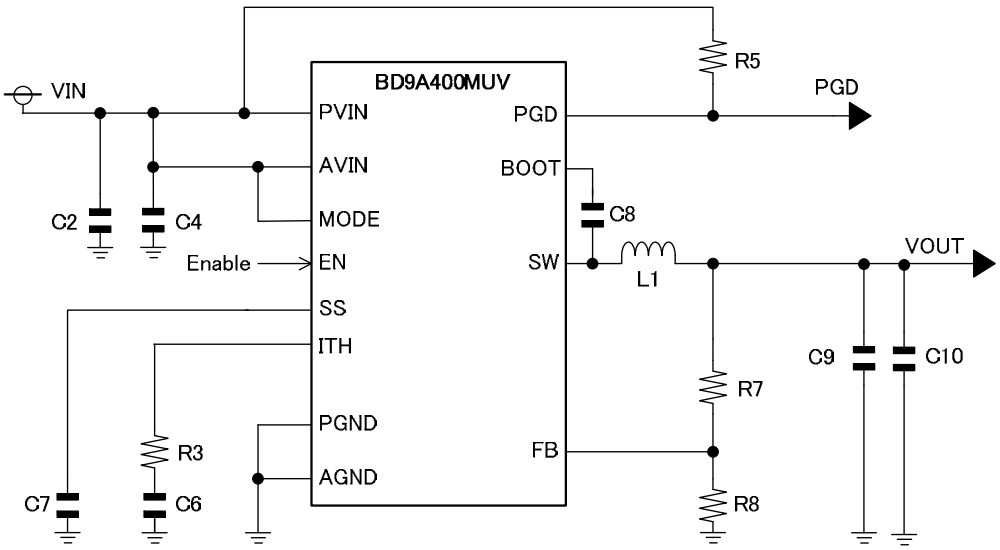


Figure 48. Application Circuit

Table 1. Recommended Component Values

Reference Designator	Output Voltage					Description
	1.1V	1.2V	1.5V	1.8V	3.3V	
R3	8.2kΩ	8.2kΩ	9.1kΩ	9.1kΩ	18kΩ	-
R5	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	-
R7	10kΩ	10kΩ	16kΩ	30kΩ	75kΩ	-
R8	27kΩ	20kΩ	18kΩ	24kΩ	24kΩ	-
C2	10µF	10µF	10µF	10µF	10µF	10V, X5R, 3216
C4	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF	25V, X5R, 1608
C6	2700pF	2700pF	2700pF	2700pF	2700pF	-
C7	0.01µF	0.01µF	0.01µF	0.01µF	0.01µF	-
C8	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF	-
C9	22µF	22µF	22µF	22µF	22µF	10V, X5R, 3225
C10	22µF	22µF	22µF	22µF	22µF	10V, X5R, 3225
L1	1.5µH	1.5µH	1.5µH	1.5µH	1.5µH	TOKO, FDSD0630

Selection of Components Externally Connected

1. Output LC Filter Constant
   The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. BD9A400MUV is returned to the IC and IL ripple current flowing through the inductor for SLLM™ control. This feedback current, Inductance value is the behavior of the best when the 1.5µH. Therefore, the inductor to use is recommended 1.5µH.

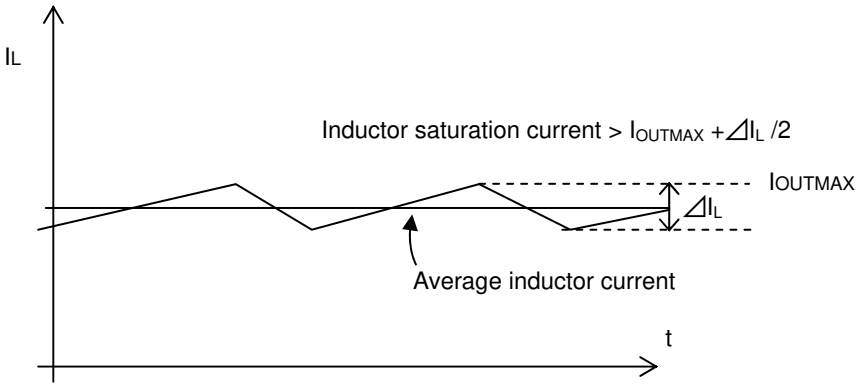


Figure 49. Waveform of current through inductor

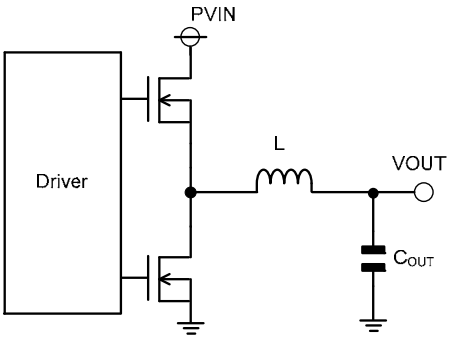


Figure 50. Output LC filter circuit

Computation with VIN = 5V, VOUT = 1.8V, L=1.5µH, and the switching frequency F_{OSC} = 1MHz, the method is as below.

Inductor ripple current ΔIL

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times L} = 748[\mathrm{mA}]$$

The saturation current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current ΔIL.

The output capacitor COUT affects the output ripple voltage characteristics. The output capacitor COUT must satisfy the required ripple voltage characteristics.

The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}})[\mathrm{V}]$$

R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.
With COUT = 44µF, RESR = 10mΩ the output ripple voltage is calculated as

$$\Delta V_{RPL} = 0.5236 \times (10m + \frac{1}{(8 \times 44\mu \times 1MHz)}) = 9.6\,[\mathrm{mV}]$$

*Be careful of total capacitance value, when additional capacitor CLOAD is connected in addition to output capacitor COUT. Use maximum additional capacitor CLOAD(max.) condition which satisfies the following method.

$$Maximum\ starting\ inductor\ ripple\ current\ IL_{START} < Over\ Current\ limit\ 4.8A(min)$$

Maximum starting inductor ripple current ILSTART can be expressed in the following method.

$$IL_{START} = Maximum\ starting\ output\ current(I_{OMAX}) + Charge\ current\ to\ output\ capacitor(I_{CAP}) + \frac{\Delta I_L}{2}$$

Charge current to output capacitor I_{CAP} can be expressed in the following method.

$$I_{CAP} = \frac{(C_{OUT} + C_{LOAD}) \times V_{OUT}}{T_{SS}} [A]$$

Computation with V_{IN} = 5V, V_{OUT} = 3.3V, L = 1.5µH, switching frequency F_{OSC}= 800kHz (min.), Output capacitor C_{OUT} = 44µF, Soft Start time T_{SS} = 0.5ms (min.), load current during soft start I_{OSS} = 3A the method is as below.

$$C_{LOAD}(max) < \frac{(4.8 - I_{OSS} - \Delta I_L/2) \times T_{SS}}{V_{OUT}} - C_{OUT} = 157.9 [\mu F]$$

If the value of C_{LOAD} is large, and cannot meet the above equation,

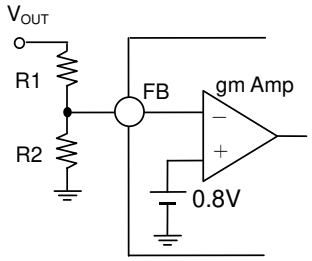
$$C_{LOAD}(max) < \frac{(4.8 - I_{OSS} - \Delta I_L/2) \times V_{FB}}{V_{OUT} \times I_{SS}} \times C_{SS} - C_{OUT}$$

Adjust the value of the capacitor C_{SS} to meet the above formula.
(Refer to the following items (3) Soft Start Setting equation of time T_{SS} and soft-start value of the capacitor to be connected to the C_{SS}.)

Computation with V_{IN} = 5V, V_{OUT} = 3.3V, L = 1.5µH, load current during soft start I_{OSS} = 3A, switching frequency F_{OSC}= 800kHz (min.), Output capacitor C_{OUT} = 44µF, V_{FB} = 0.792V(max.), I_{SS} = 3.6µA(max.), A capacitor connected to the C_{SS} if you want to connect the C_{LOAD} = 220µF is the following equation.

$$C_{SS} > \frac{V_{OUT} \times I_{SS}}{(4.8 - I_{OSS} - \Delta I_L/2) \times V_{FB}} \times (C_{LOAD} + C_{OUT}) = 2.97 [nF]$$

2. Output Voltage Setting
The output voltage value can be set by the feedback resistance ratio.



$$V_{OUT} = \frac{R1 + R2}{R2} \times 0.8 [V]$$

Figure 51. Feedback Resistor Circuit

3. Soft Start Setting
Turning the EN terminal signal high activates the soft start function. This causes the output voltage to rise gradually while the current at startup is placed under control. This allows the prevention of output voltage overshoot and inrush current. The rise time depends on the value of the capacitor connected to the SS terminal.

$$T_{SS} = (C_{SS} \times V_{FB})/I_{SS}$$

T_{SS} : Soft Start Time

C_{SS} : Capacitor connected to Soft Start Time Terminal

V_{FB} : FB Terminal Voltage (0.8V (Typ))

I_{SS} : Soft Start Terminal Source Current (1.8µA(Typ))

with $C_{SS} = 0.01$µF,

$$T_{SS} = (0.010[\mu F] \times 0.8[V])/1.8[\mu A]$$
$$= 4.44[msec]$$

Turning the EN terminal signal high with the SS terminal open (no capacitor connected) or with the terminal signal high causes the output voltage to rise in 1msec (Typ).

4. Phase Compensation Component

A current mode control buck DC/DC converter is a one-pole, one-zero system. One poles are formed by an error amplifier and load and the one zero point is added by phase compensation. The phase compensation resistor R_{ITH} determines the crossover frequency F_{CRS} where the total loop gain of the DC/DC converter is 0dB. A high value crossover frequency F_{CRS} provides a good load transient response characteristic but inferior stability. Conversely, a low value crossover frequency F_{CRS} greatly stabilizes the characteristics but the load transient response characteristic is impaired.

(1) Selection of Phase Compensation Resistor R_{ITH}

The Phase Compensation Resistance R_{ITH} can be determined by using the following equation.

$$R_{ITH} = \frac{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} [\Omega]$$

V_{OUT} : Output Voltage[V]

F_{CRS}: Crossover Frequency[Hz]

C_{OUT} : Output Capacitance[F]

V_{FB} : Feedback Reference Voltage (0.8V (Typ))

G_{MP} : Current Sense Gain (13A/V (Typ))

G_{MA} : Error Amplifier Trans conductance (260μA /V(Typ))

(2) Selection of Phase Compensation Capacitance C_{ITH}

For stable operation of the DC/DC converter, zero for compensation cancels the phase delay due to the pole formed by the load.

The phase compensation capacitance C_{ITH} can be determined by using the following equation.

$$C_{ITH} = \frac{C_{OUT} \times V_{OUT}}{R_{ITH} \times I_{OUT}} [F]$$

(3) Loop stability

To ensure the stability of the DC/DC converter, make sure that a sufficient phase margin is provided. A phase margin of at least 45º in the worst conditions is recommended.

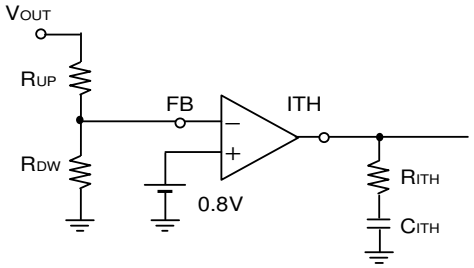


Figure 52. Phase Compensation Circuit

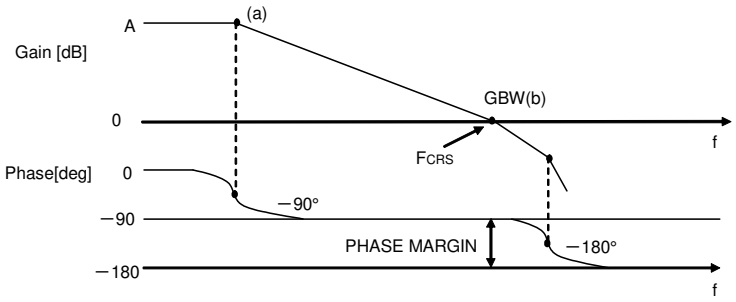


Figure 53. Bode Plot

PCB Layout Design

In the buck DC/DC converter, a large pulse current flows into two loops. The first loop is the one into which the current flows when the high-side FET is turned on. The flow starts from the input capacitor C_{IN}, runs through the FET, inductor L and output capacitor C_{OUT} and back to GND of C_{IN} via GND of C_{OUT}. The second loop is the one into which the current flows when the low-side FET is turned on. The flow starts from the low-side FET, runs through the inductor L and output capacitor C_{OUT} and back to GND of the low-side FET via GND of C_{OUT}. Route these two loops as thick and as short as possible to allow noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors directly to the GND plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

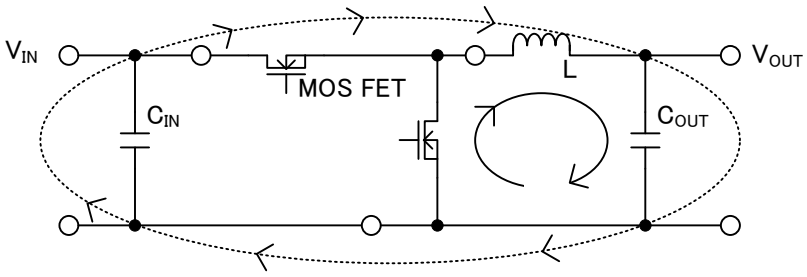
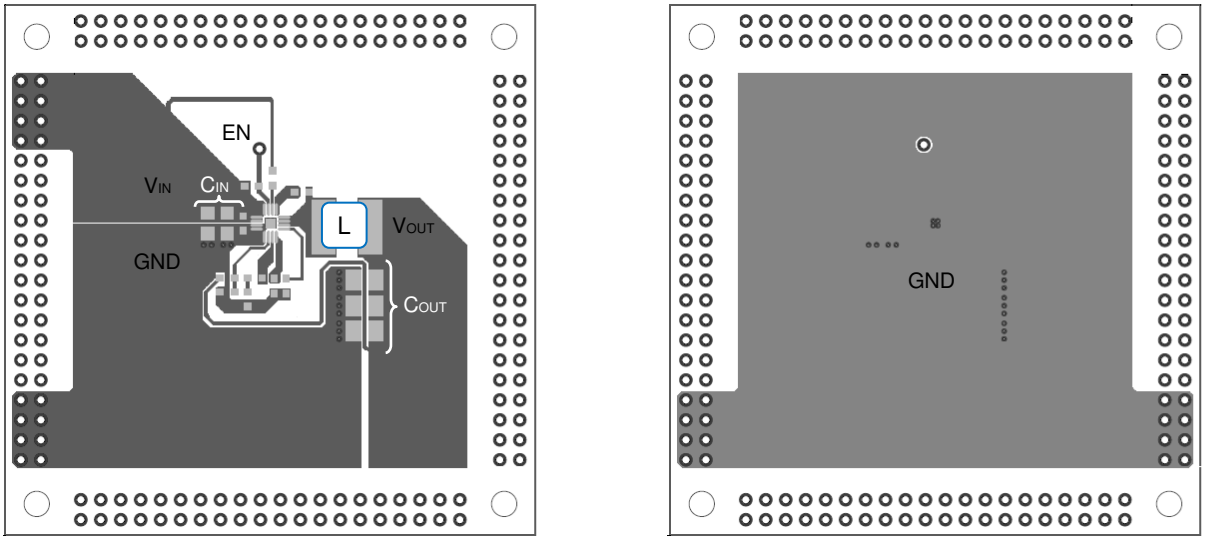


Figure 54. Current Loop of Buck DC/DC Converter

Accordingly, design the PCB layout considering the following points.

- Connect an input capacitor as close as possible to the IC PVIN terminal on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the GND node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Provide lines connected to FB and ITH far from the SW nodes.
- Place the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.



Top Layer Bottom Layer

Figure 55. Example of evaluation board layout