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2.7V to 5.5V Input ,3A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9B331GWZ

General Description

ROHM's high efficiency switching regulator, BD9B331GWZ, is a step-down converter designed to produce a low voltage output of 0.6V~3.3V from a 2.7V~5.5V power supply line. It offers high efficiency in all load ranges by automatic PFM/PWM adjustment. It employs an On time control system to provide faster transient response to sudden change in load.

Features

- Fast transient response with On time control system.
- High efficiency for all load range with synchronous rectifier (Nch/Nch FET) and adaptive PFM/PWM system.
- Adjustable Soft-start function.
- Thermal and UVLO protection.
- Short-circuit current protection with pulse count
- Shutdown function.

Applications

Power supply for LSI including SoC, DSP, Micro computer and ASIC

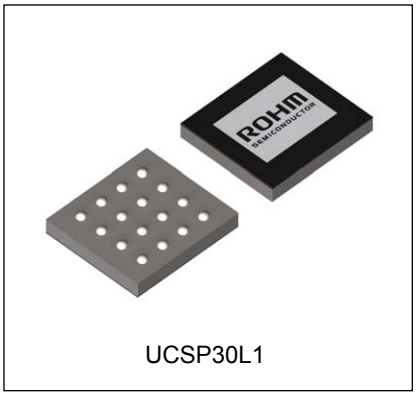
- Laptop PC / Tablet PC / Server
- LCD TV, Storage Devices (HDD / SSD)
- Printer
- Amusement
- Secondary power supply

Key Specifications

- Input Voltage Range: 2.7V to 5.5V
- Output Voltage Range: 0.6V to PVcc × 0.8V
- Output Current: 3.0A (Max)
- Switching Frequency: 1.3MHz(Typ)
- High Side FET ON Resistance: 23mΩ(Typ)
- Low Side FET ON Resistance: 23mΩ(Typ)
- Standby Current: 0μA (Typ)
- Operating Temperature Range: -40°C to +85°C

Package(s)

	W(Typ) x D(Typ) x H(Max)
UCSP30L1:	1.98mm x 1.80mm x 0.33mm



UCSP30L1

Typical Application Circuit(s)

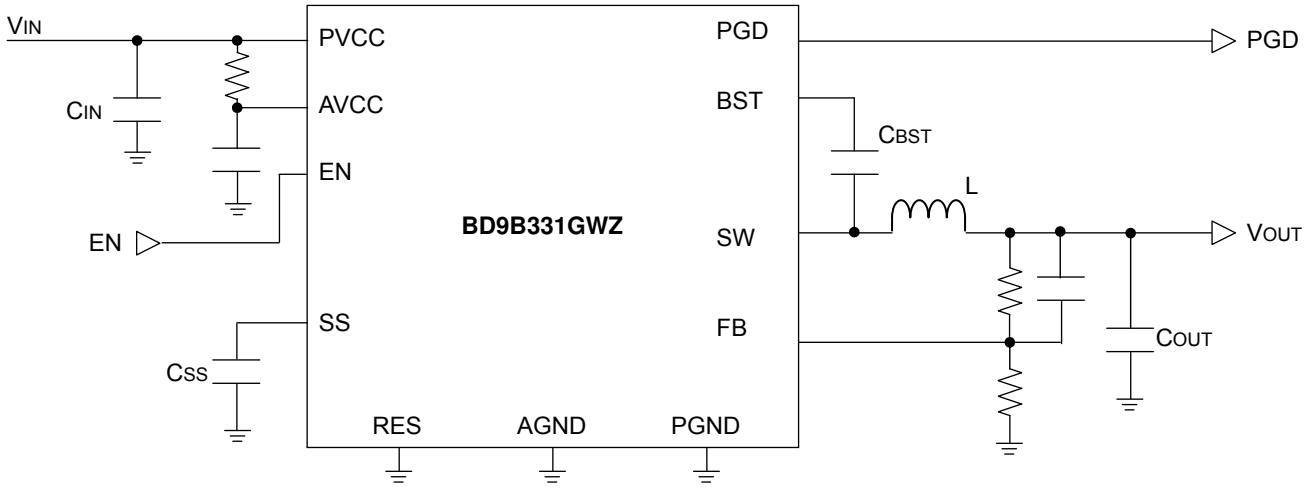


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration (BOTTOM VIEW)

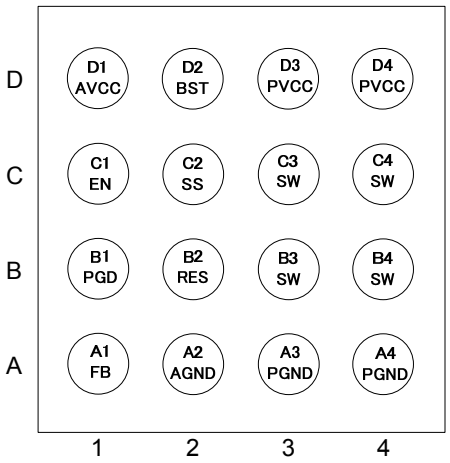


Figure 2. Pin Configuration

Pin Description(s)

Pin No	Symbol	Function	Pin No	Symbol	Function
A1	FB	Output feedback pin	C1	EN	Enable pin（High active）
A2	AGND	Ground pin	C2	SS	Soft start capacitor connection pin
A3	PGND	Power ground pin	C3	SW	Switch pin
A4	PGND	Power ground pin	C4	SW	Switch pin
B1	PGD	Power good open drain pin	D1	AVCC	Power supply input pin
B2	RES	Reserved pin (Connect to Ground)	D2	BST	Bootstrap pin
B3	SW	Switch pin	D3	PVCC	Power supply input pin
B4	SW	Switch pin	D4	PVCC	Power supply input pin

Block Diagram(s)

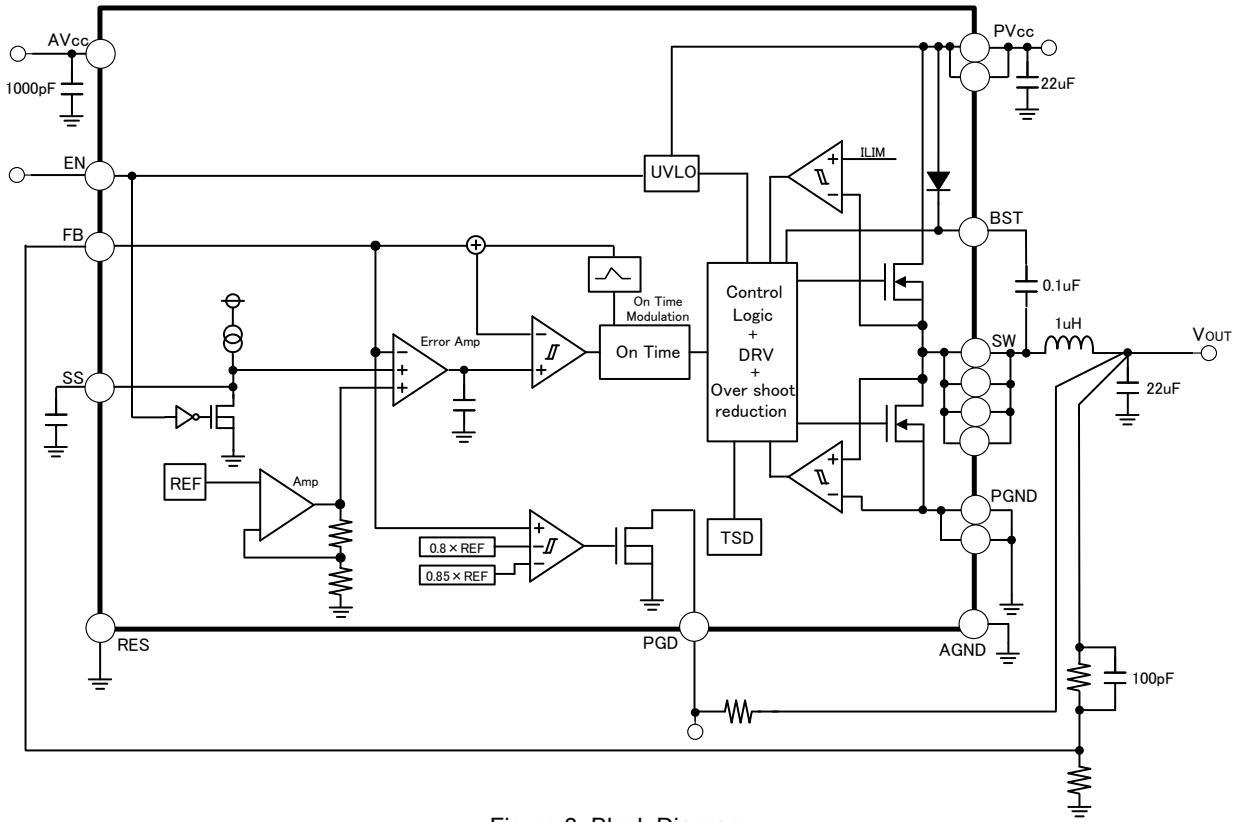


Figure 3. Block Diagram

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
AVCC / PVCC Voltage	AVCC / PVCC	-0.3 to +7 (Note 1)	V
EN Voltage	VEN	-0.3 to +7 (Note 1)	V
BST Voltage	VBST	-0.3 to +13	V
BST_SW Voltage	VBST-SW	-0.3 to +7	V
SW Voltage	Vsw	-0.3 to PVcc+0.3	V
SS/FB/PGD/ Voltage	VSS/ VFB VPGD	-0.3 to +7	V
Power Dissipation	Pd	0.81 (Note 2)	W
Operating temperature range	Topr	-40 to +85	°C
Storage temperature range	Tstg	-55 to +150	°C
Maximum junction temperature	Tjmax	+150	°C

(Note 1) Pd,and Tj=150°C should not be exceeded.
(Note 2) Derate by 6.5mW/°C when operating above Ta=25°C.
When mounted on a board 63mm × 55mm × 1.6mm glass-epoxy board, 9 layer.(Refer to page.16)

Recommended Operating Ratings (Ta=-40 to 85℃)

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	AVCC	2.7	5.0	5.5	V
	PVCC	2.7	5.0	5.5	V
EN Voltage	VEN	0	AVCC	5.5	V
Output voltage Range	VOUT	0.6	-	PVCC × 0.8	V
SW average output current	ISW	-	-	3(Note 3)	A

(Note 3) Pd, ASO should not be exceeded

Electrical Characteristics (Unless otherwise specified AVCC=PVCC=5V, EN=AVCC Ta=25°C)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Supply						
AVcc and PVcc voltage range	VIN	2.7	-	5.5	V	
Standby current	ISTB	-	-	3	μA	EN=GND
Active current	ICC	-	150	200	μA	
UVLO detection voltage	VUVLOTH	2.38	2.50	2.62	V	AVCC falling
UVLO hysteresis	VUVLOHYS	40	50	60	mV	
Enable						
EN low voltage	VENL	GND	-	0.5	V	Standby mode
EN high voltage	VENH	1.5	-	AVcc	V	Active mode
EN input current	IEN	-	3	6	μA	VEN=5V
Power GOOD						
PG threshold voltage	VPGTH	-20%	-15%	-10%	V	VFB-15% (Typ)
PG hysteresis voltage	VPGHYS	-25%	-20%	-15%	V	VFB-20% (Typ)
PG detect delay time	PDELAY	6	15	25	μs	
Open drain output resistance	RPG	50	100	200	Ω	VFB <VPGTH
PG leakage current	IPL	-	-	1	μA	VPG=5V
Power Switch						
High side FET ON resistance	RONH	-	23	50	mΩ	PVCC=5V
Low side FET ON resistance	RONL	-	23	50	mΩ	PVCC=5V
On time	TON	-	230	-	ns	VIN=3.3V,VOUT=0.9V, PWM
Soft Start						
Soft start time	TSS	-	1	-	ms	
Soft start current	ISS	0.5	1.2	1.8	μA	
Output						
Output feedback threshold voltage	VFB	0.591	0.600	0.609	V	

Typical Performance Curves

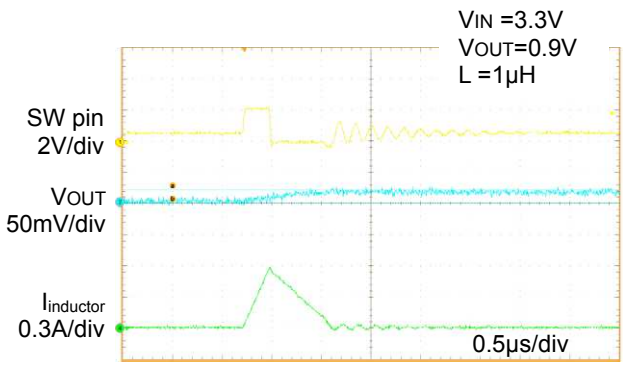


Figure 4. PFM operation, load 0mA

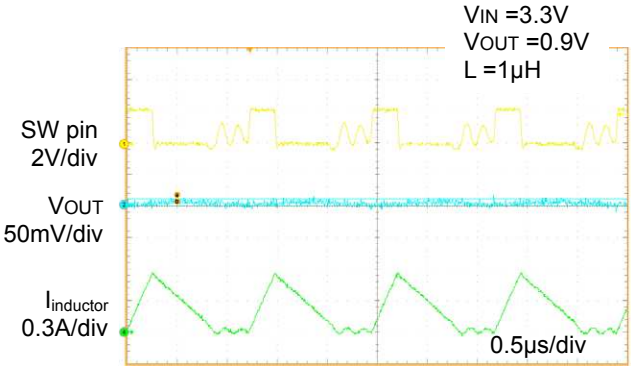


Figure 5. PFM operation, load 100mA

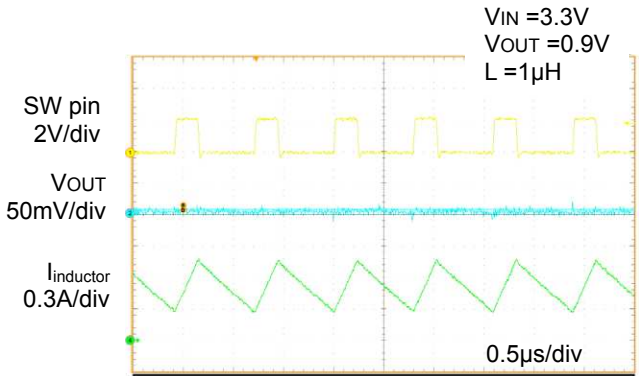


Figure 6. PWM operation, load 500mA

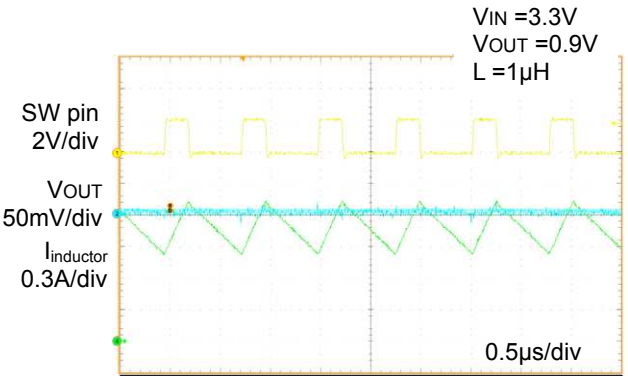


Figure 7. PWM operation, load 1000mA

Typical Performance Curves - continued

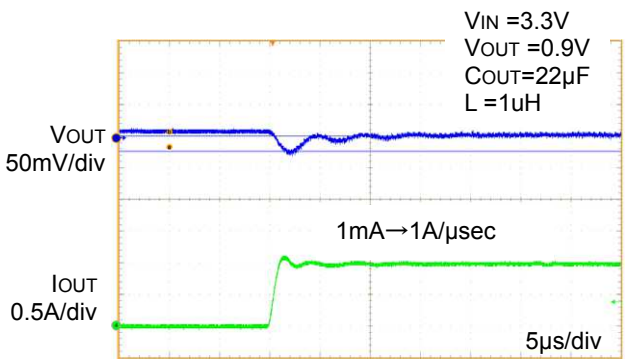


Figure 8. Load rise response

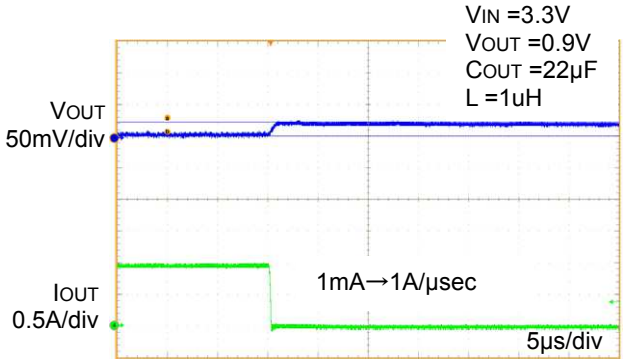


Figure 9. Load fall response

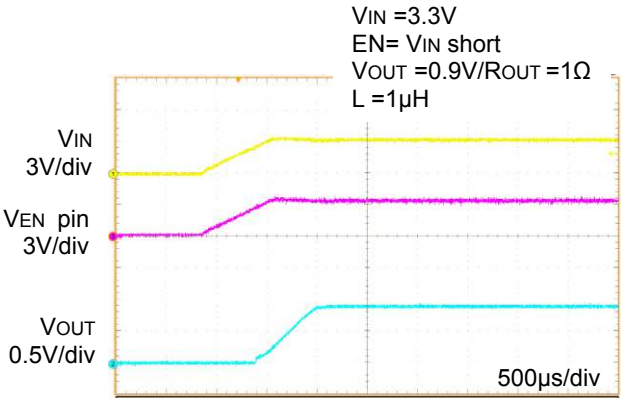


Figure 10. Start up (with VIN UVLO)

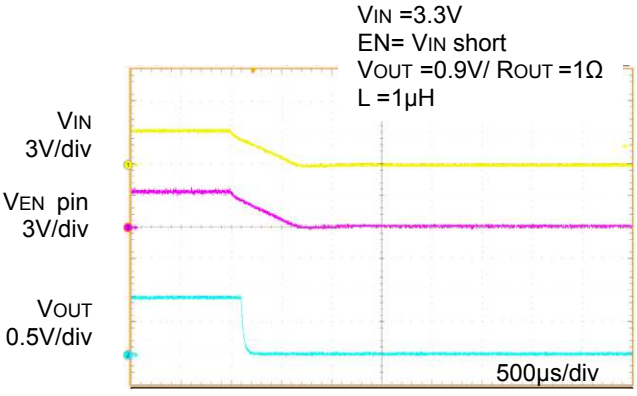


Figure 11. Shutdown (with VIN UVLO)

Typical Performance Curves - continued

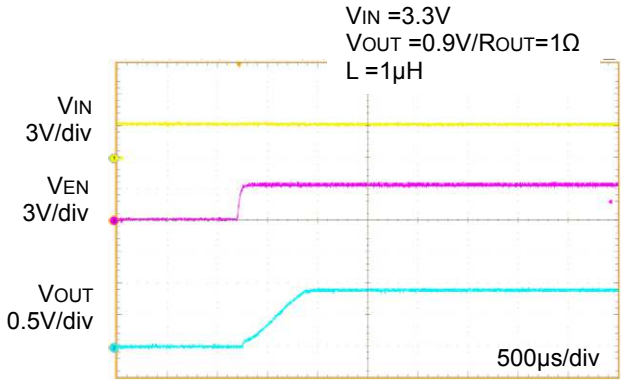


Figure 12. Start up (with EN)

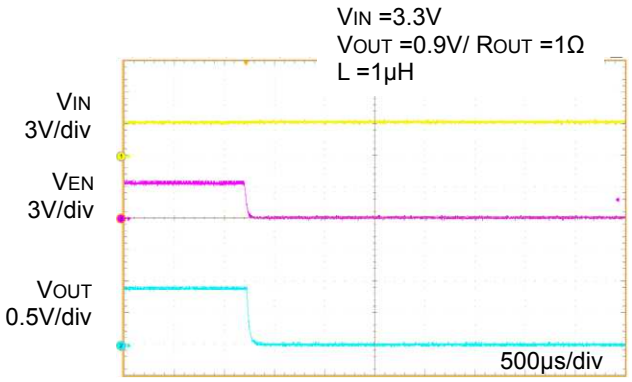


Figure 13. Shutdown (with EN)

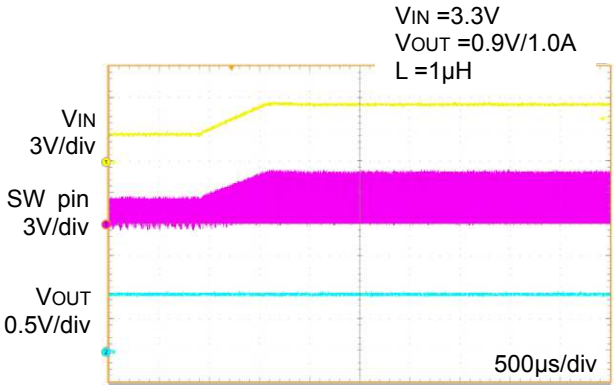


Figure 14. VIN variation 2.9V→5.5V

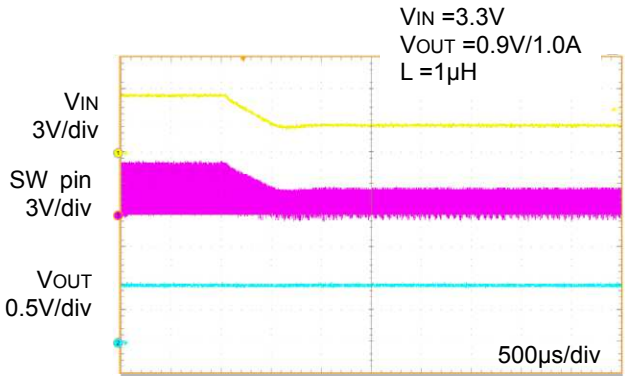


Figure 15. VIN variation 5.5V→2.9V

Typical Performance Curves - continued

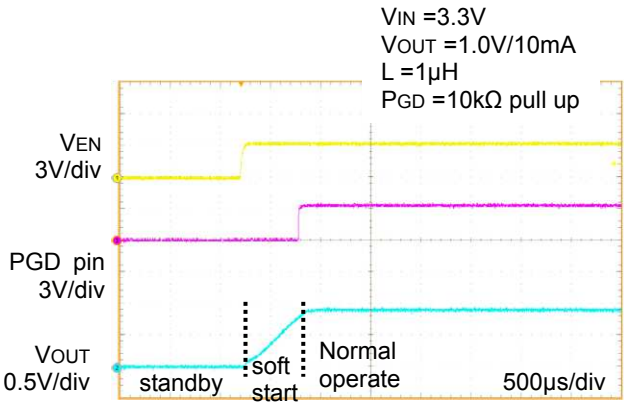


Figure 16. Power Good (Start up)

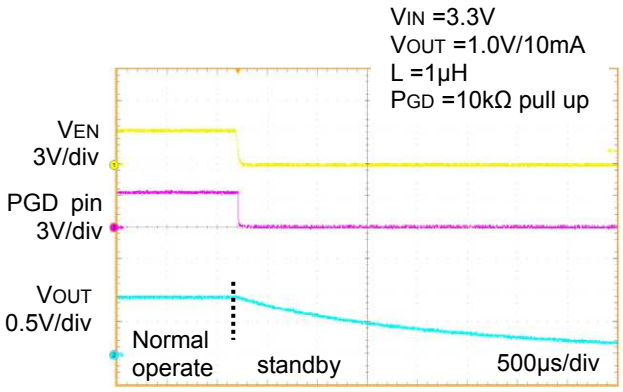


Figure 17. Power Good (Shutdown)

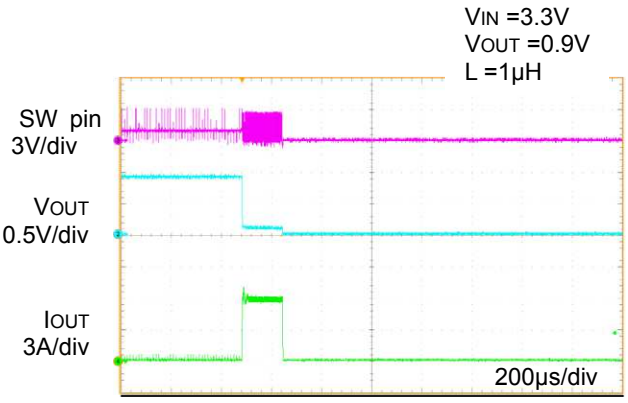


Figure 18. Output ground fault

Typical Performance Curves - continued

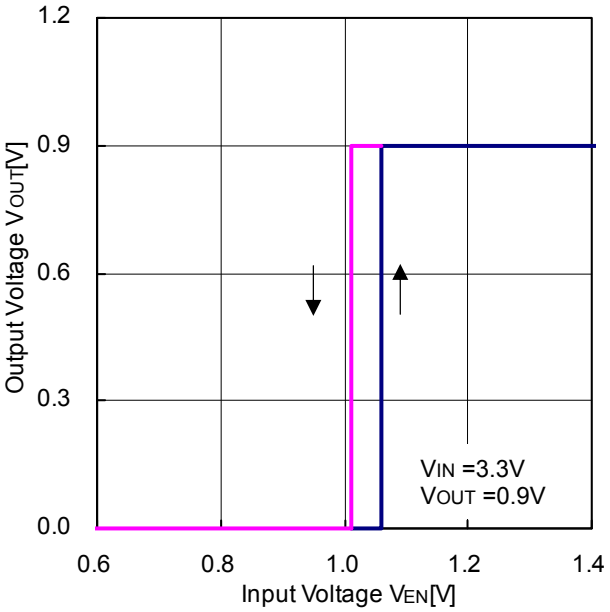


Figure 19. VEN start up

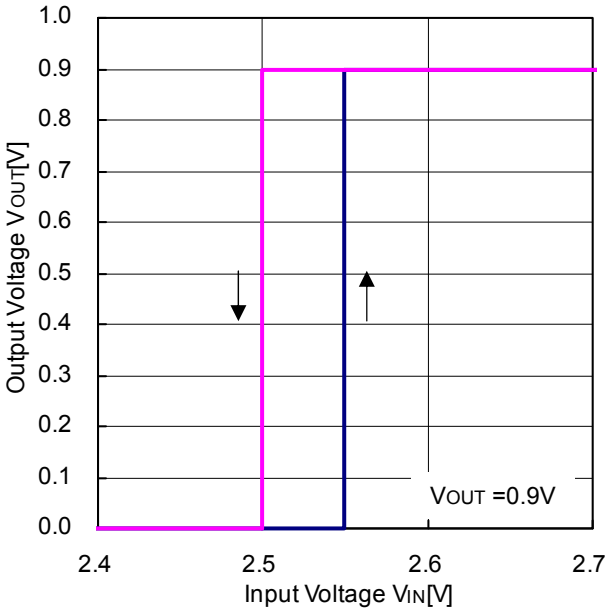


Figure 20. VIN start up

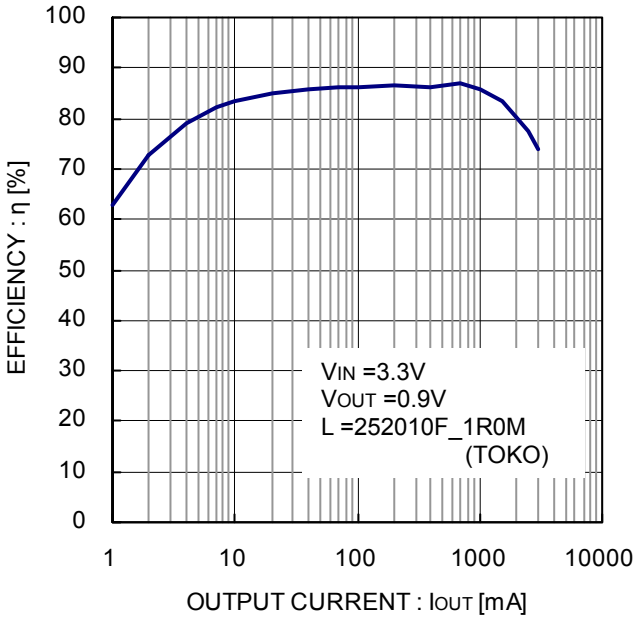


Figure 21. Efficiency

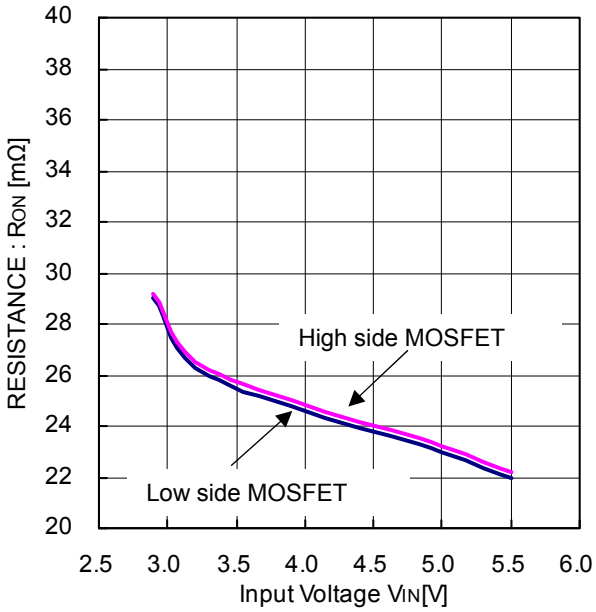


Figure 22. Power MOS On resistor

Typical Performance Curves - continued

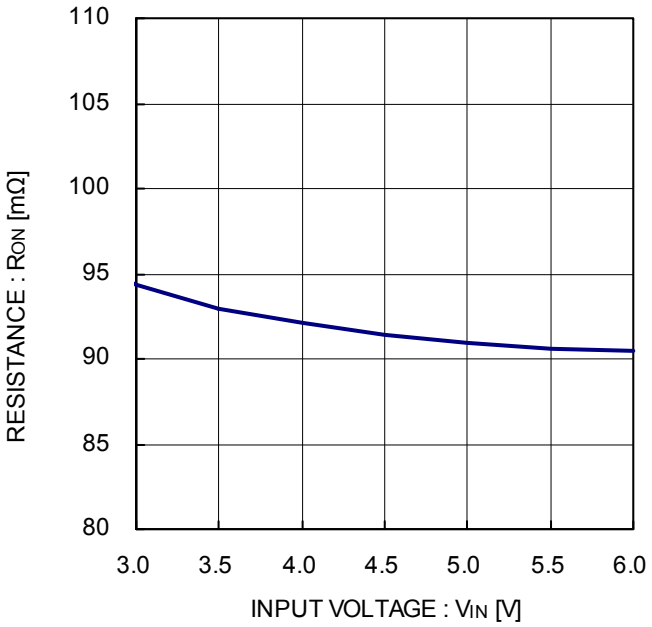


Figure 23. Power Good MOS On resistor

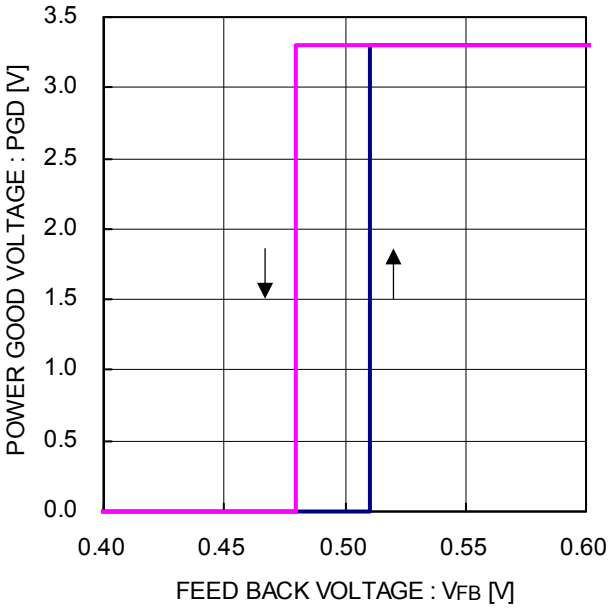


Figure 24. Power Good voltage/hysteresis

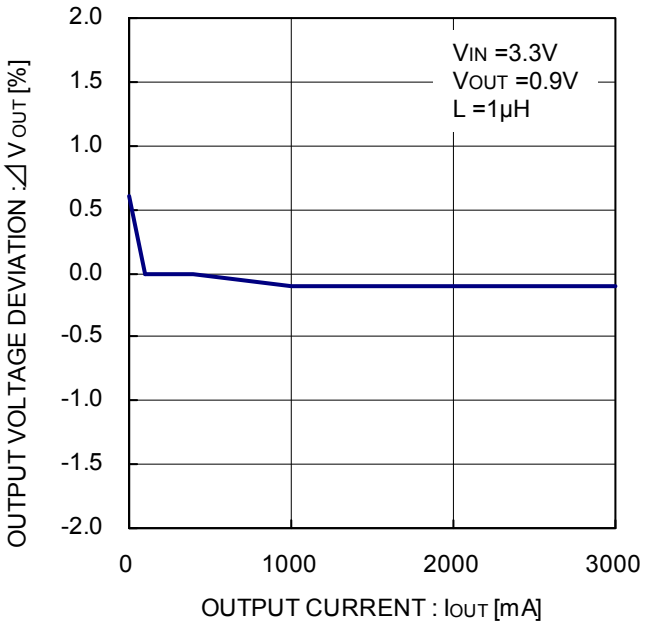


Figure 25. Output variation (Load regulation)

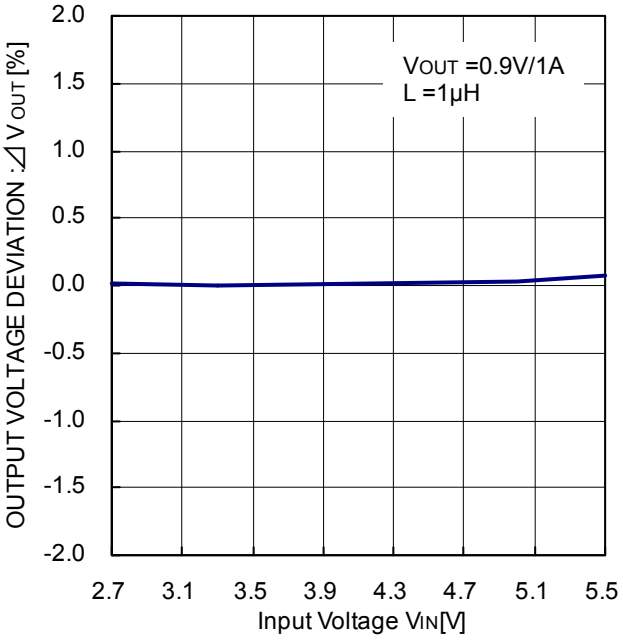


Figure 26. Output variation (Line regulation)

Typical Performance Curves - continued

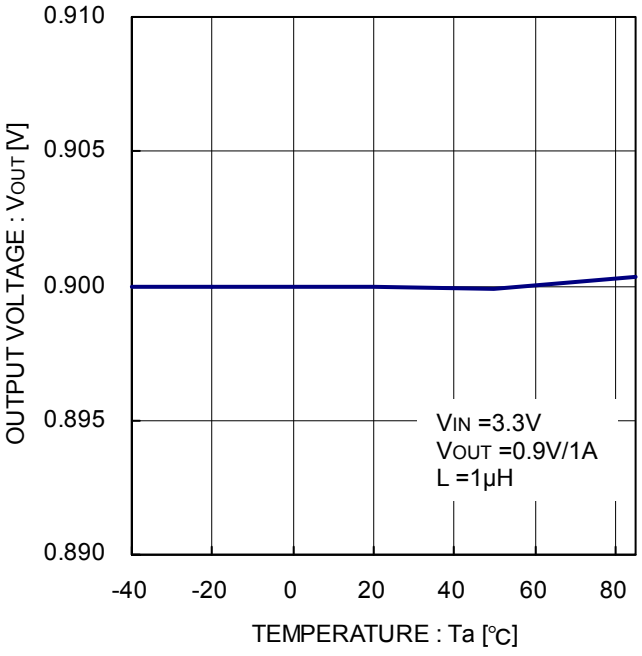


Figure 27. Output variation (ambient temperature)

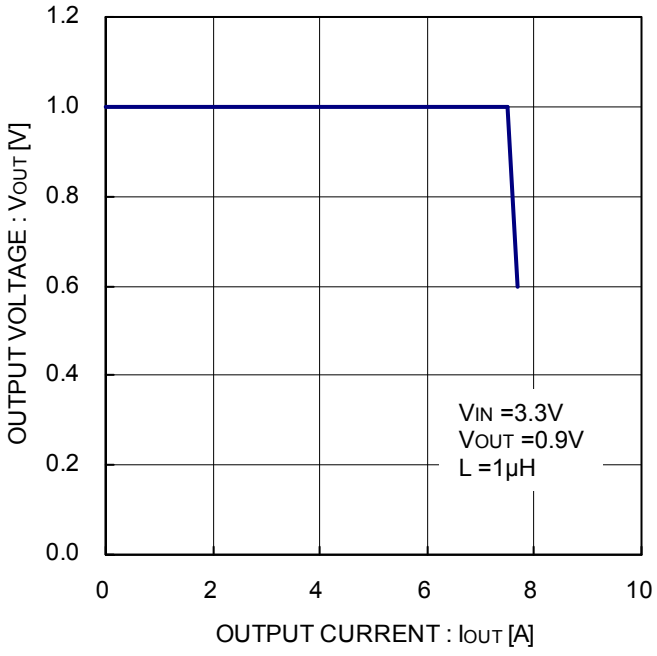


Figure 28. OCP detection current

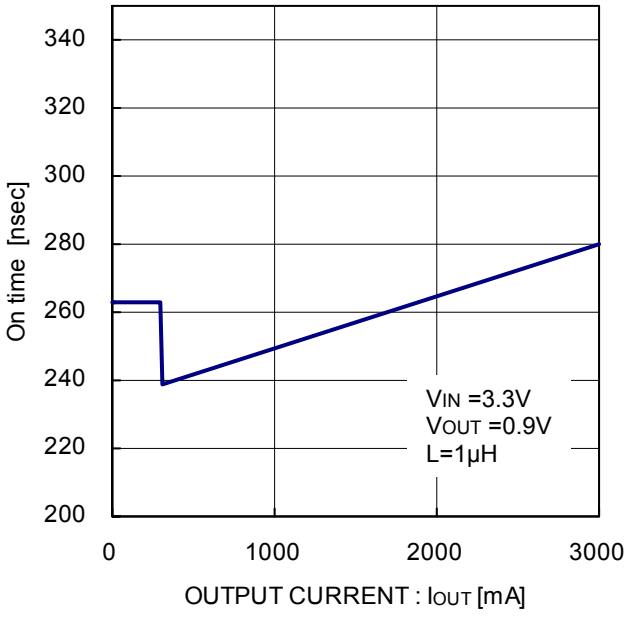


Figure 29. On time v.s. OUTPUT CURRENT

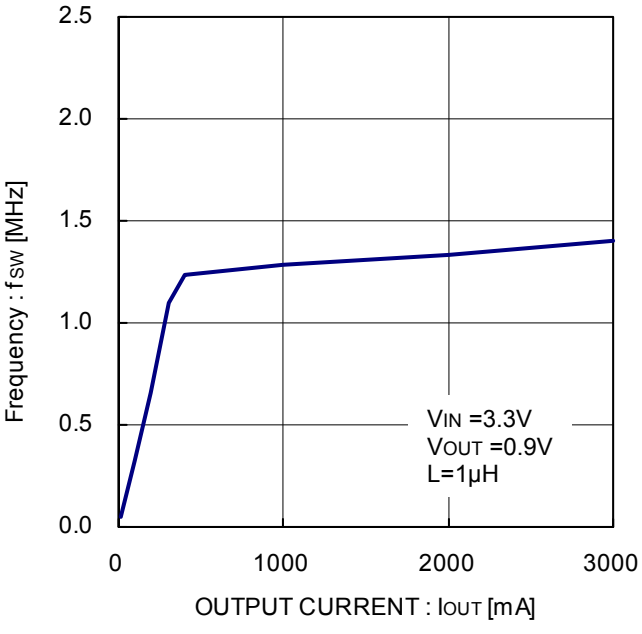


Figure 30. Frequency v.s. OUTPUT CURRENT

Application Information

Operation

BD9B331GWZ is a buck synchronous rectification switching regulator capable of high speed transient response by implementing a constant On Time system as its hysteresis control. General hysteresis control systems need a certain ripple to give an output voltage. Furthermore, a high ESR output capacitor is needed to maintain appropriate switching control.
BD9B331GWZ has a ripple implanted system at output detection which keeps a normal switching operation even if a low ESR output capacitor is used. This feature also resolved a weakness of a regular hysteresis control, which is, to keep a steady frequency from a variation of frequencies.
When operating with light loads, BD9B331GWZ reduce switching loss and attain high efficiency by utilizing a pulse skip system.

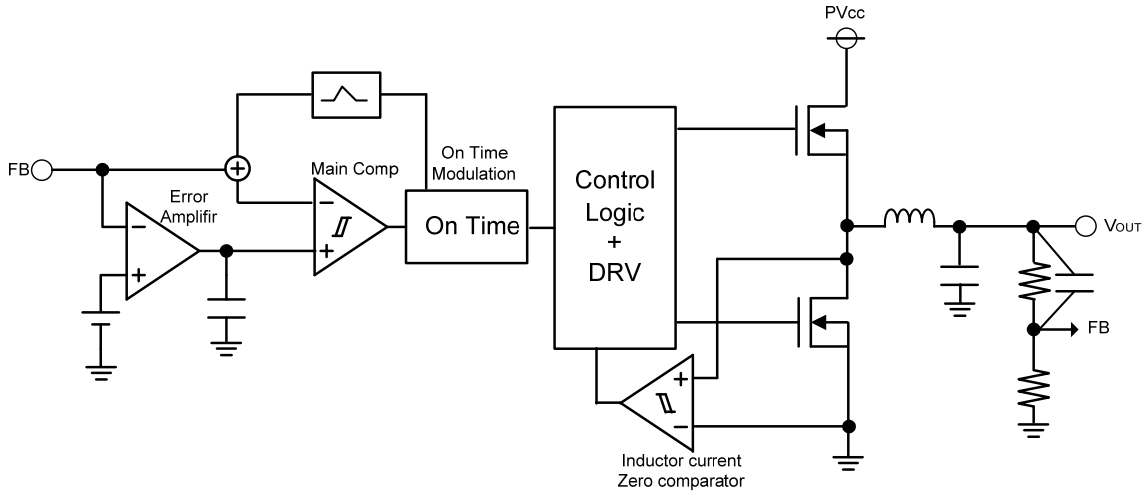


Figure 31. Constant on time system block diagram

Description of Operations

・Soft Start Function

When EN terminal is shifted to “High”, it activates a soft-start function which gradually raises the output voltage while limiting the current at startup. This prevents an overshoot in output voltage by preventing startup in-rush current.

$$T_{SS} = \frac{(C_{SS} \times V_{FB})}{I_{SS}} [\text{sec}]$$

where :

T_{SS} is Soft - start time

C_{SS} is Capacitor connected to Soft - start pin

V_{FB} is FB Voltage 0.6V (Typ)

I_{SS} is Source current at Soft - start pin 1.2 μA (Typ)

Ex) When Css = 0.01 μF

$$T_{SS} = (0.01[\mu A] \times 0.6\ [V]) / 1.2\ [\mu A]$$
$$= 5.0\ [\text{msec}]$$

If EN terminal is shifted to “High” when capacitor Css is not connected, SS pin is OPEN or in “High” condition, the output voltage will rise in 1msec(Typ).

・Shutdown Function

With EN terminal shifted to “Low”, the device turns to Standby Mode. All functional blocks including reference voltage circuit, internal oscillator and drivers are turned OFF. Circuit current during standby is 0μA (Typ).

・UVLO Function

UVLO detects whether the input voltage is sufficient to secure a desired IC output voltage. A hysteresis width of 50mV (Typ) is provided to prevent output chattering.

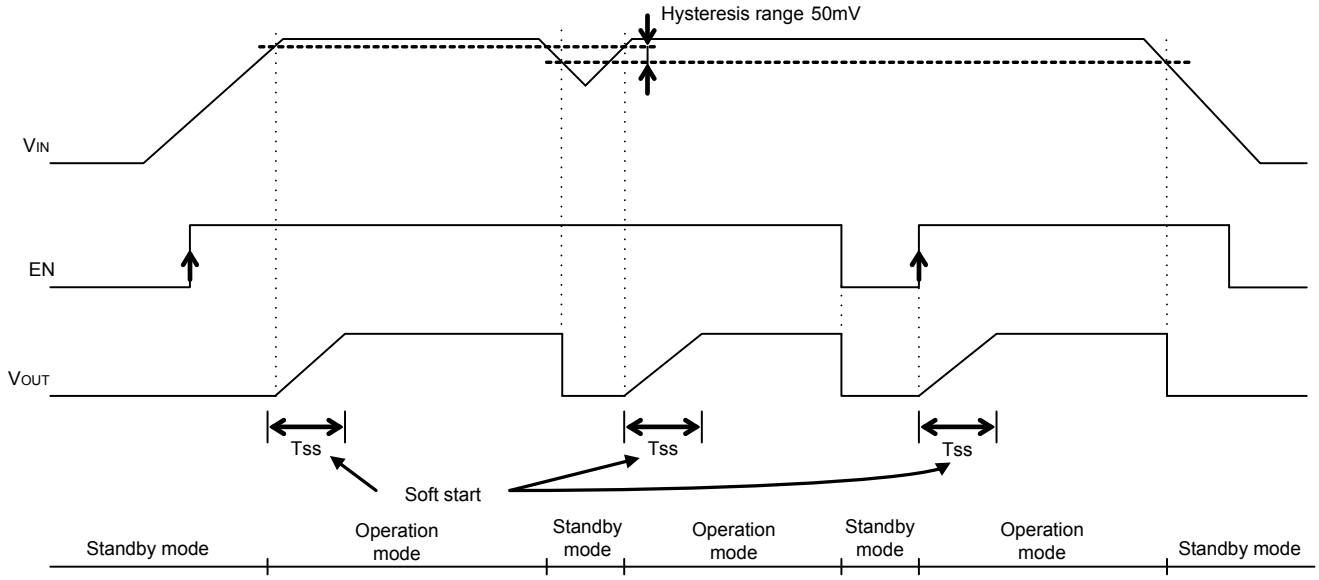


Figure 32. Soft Start, Shutdown, UVLO timing chart

・Power-good function

When FB terminal voltage falls below 80%(0.48V) of the internal reference voltage, an open drain MOS which is internally connected to PGD terminal turns ON. This event pulls down the PGD terminal with a 100Ω(Typ) impedance.

When FB terminal voltage reaches 85%(0.51V) of the internal reference voltage, PGD terminal will enter a high impedance state after 15μsec delay. This terminal is an open drain output so a pull up resistor is needed for proper operation.

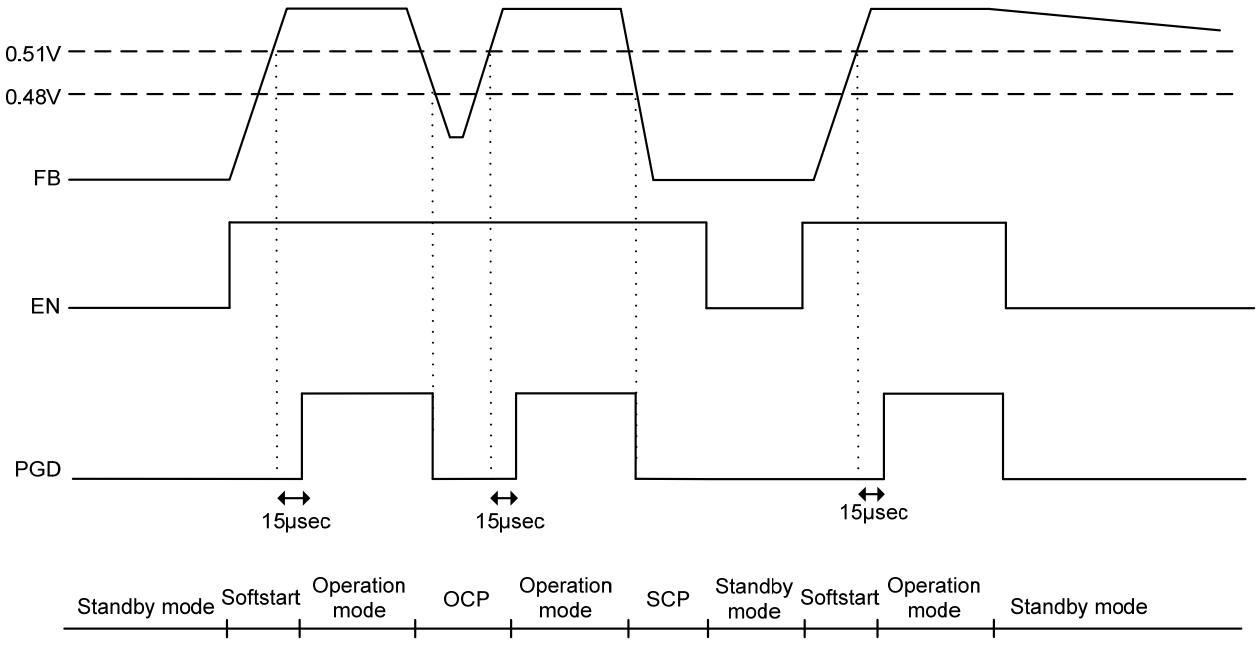


Figure 33. Power-good timing chart

・Over Current Protection Function(OCP) / Pulse Count Short-Circuit Protection (SCP)

Over current detection circuit is operating when the high side MOS is ON. When over current is detected, On/Off duty will be controlled to decrease the output voltage. If over current is still present 512 counts after output voltage falls below 80% of the set voltage (Power Good error), the output will be latched in OFF state to prevent IC damage. Output is returned by resetting EN or releasing UVLO again.

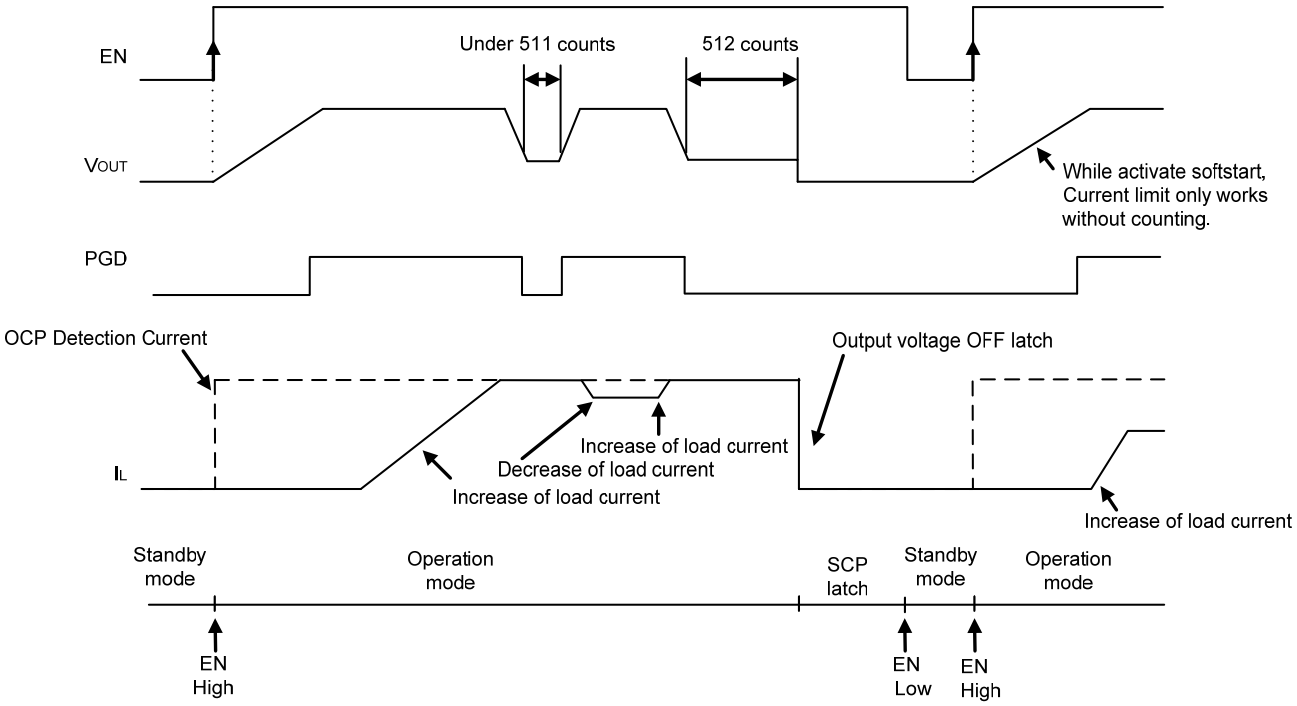


Figure 34. Over current protection/short-circuit protection function timing chart

・Over Short Reduction(load responsiveness characteristic improvement function)

Output voltage rises when load current is decreased rapidly. Normally, Low side power MOS is kept on turning ON and the gradient of coil current $\triangle I_L$ will be $\triangle I_L$ = -Vo/L. At this point, if slew rate, $\triangle I_{OUT}$, of load current I_{OUT} will be $\triangle I_{OUT} > \triangle I_L$, excess current will be charged and output voltage will keep on rising (Fig.35 dotted line waveform). When the output voltage is set to a low value, $\triangle I_L$ will be small and output voltage will increase significantly. BD9B331GWZ operates over shoot reduction when the Low side power MOS is kept ON after twice the PWM pulse width. Vf voltage is generated to the SW terminal by turning off the HG-LG and applying I_L through the body diode of the Low side MOS. This makes $\triangle I_L$ =(-Vf-V_{OUT})/L and reduces the rise in output voltage by controlling excess current not to be charged to output capacitor.

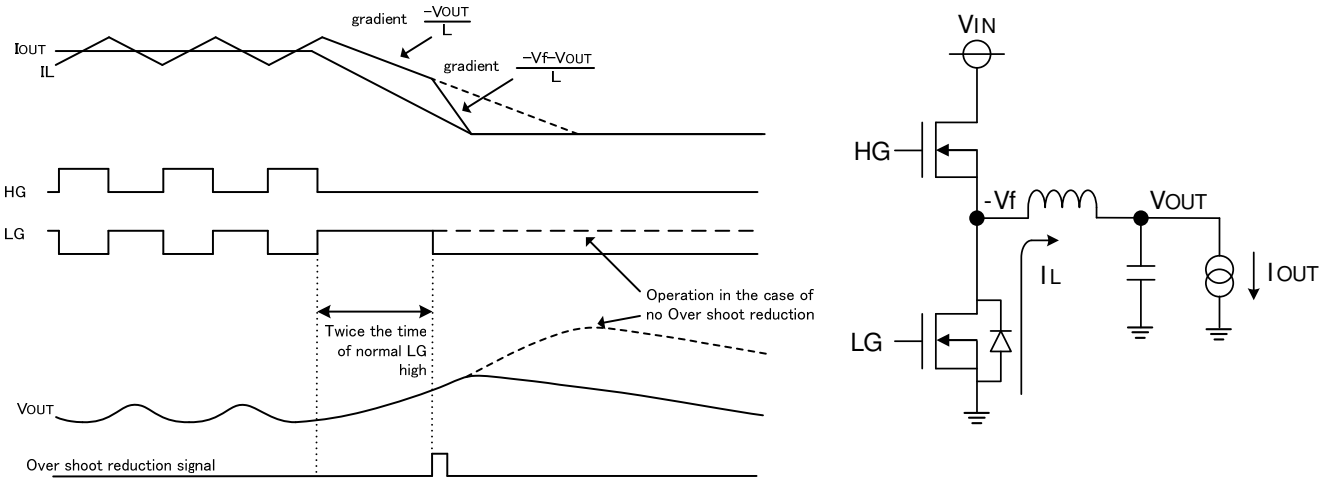


Figure 35. Over short reduction timing chart

Switching Regulator Efficiency

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100\ [\%] = \frac{P_{OUT}}{P_{IN}} \times 100\ [\%] = \frac{P_{OUT}}{P_{OUT} + P_{D\alpha}} \times 100\ [\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors $P_D\alpha$ as follows:

Dissipation factors:
1) ON resistance dissipation of inductor and FET : PD (I^2R)
2) Gate charge/discharge dissipation : PD (Gate)
3) Switching dissipation : PD (SW)
4) ESR dissipation of capacitor : PD (ESR)
5) Operating current dissipation of IC : PD (IC)

1) $P_D(I^2R) = {I_{OUT}}^2 \times (R_{COIL} + R_{ON})$

where :
R_{COIL} is DC resistance of inductor
R_{ON} is ON resistance of FET
I_{OUT} is Output current

2) $P_D(Gate) = Cqs \times f \times V^2$

where :
Cqs is Gate capacitance of FET
f is Switching frequency
V is Gate driving voltage of FET

3) $P_D(SW) = \frac{{V_{IN}}^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$

where :
C_{RSS} is Reverse transfer capacitance of FET
I_{DRIVE} is Peak current of gate

4) $P_D(ESR) = {I_{RMS}}^2 \times ESR$

where :
I_{RMS} is Ripple current of capacitor
ESR is Equivalent series resistance

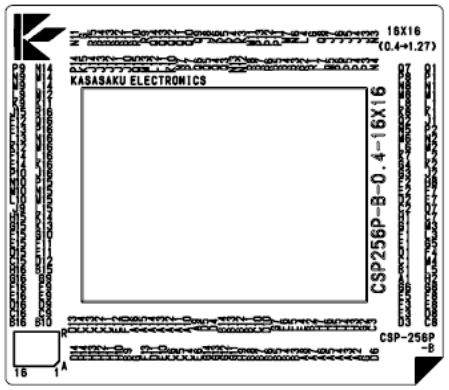
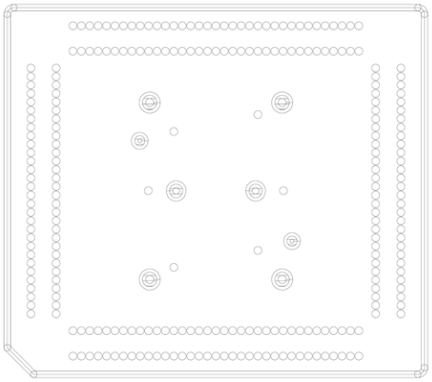
5) $P_D(IC) = V_{IN} \times I_{CC}$

where :
I_{CC} is Circuit current

Power Dissipation (Pd)

As for power dissipation, an estimate of heat reduction characteristics and internal power consumption of IC are shown, so please use these for reference. Since power dissipation changes substantially depending on the implementation conditions (board size, board thickness, metal wiring rate, number of layers and through holes, etc.), it is recommended to measure Pd on a set board. Exceeding the power dissipation of IC may lead to deterioration of the original IC performance, such as reduction in current capability. Therefore, be sure to prepare sufficient margin within power dissipation for usage.

○Measurement conditions

		Evaluation board
Layout of Board for Measurement		  Top Layer (Top View) Bottom Layer (Bottom View)
Measurement State		With board implemented (Wind speed 0 m/s)
Board Material		Glass epoxy resin (9 layers)
Board Size		63 mm x 55 mm x 1.6 mm
Wiring Rate	Top layer	Metal (GND) wiring rate: Approx. 81.6%
	Bottom layer	Metal (GND) wiring rate: Approx. 82.3%
Copper Foil Thickness		Outer layer L1,L9 : 27μm Inner layer L8 : 27μm,L2~L7 : 18μm
Through Hole		Diameter 0.1mm x 256 holes Diameter 0.6mm x 266 holes
Power Dissipation		0.81W
Thermal Resistance		θJA =153.8°C/W

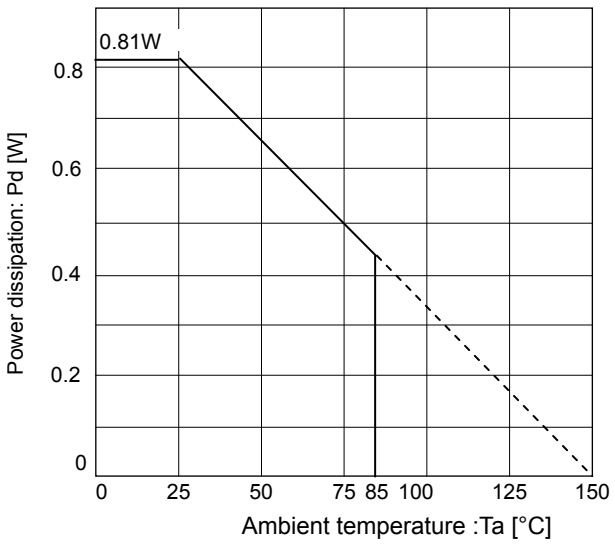


Figure 36. Power dissipation (BD9B331GWZ)

$$P = I_{OUT}{}^2 \times R_{ON}$$
$$R_{ON} = D \times R_{ONH} + (1 - D) R_{ONL}$$

Where :

D is ON duty (= VOUT/VIN)

R_{ONH} is ON resistance of High side MOS FET

R_{ONL} is ON resistance of Low side MOS FET

I_{OUT} is Output current

Ex) VIN = 5V, VOUT = 1V, RONH = 23mΩ, RONL = 23mΩ, IOUT = 3A

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{1}{5} = 0.2$$
$$R_{ON} = 0.2 \times 0.023 + (1 - 0.2) \times 0.023$$
$$= 0.023\ [\Omega]$$
$$P = 3^2 \times 0.023 = 0.207\ [\mathrm{W}]$$

Thermal design must be carried out with sufficient margin allowed with consideration on the dissipation above.

External Component Selection

1. Inductor (L)

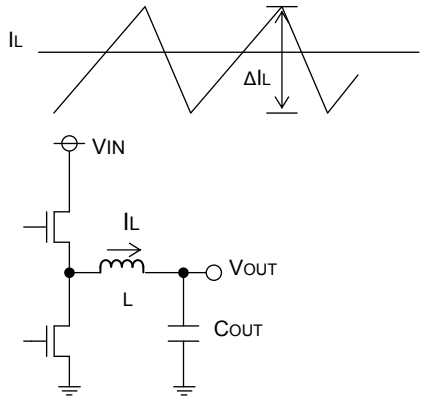


Figure 37. Output ripple current

The inductance has great influence on the output ripple current. As seen in the equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f}[\mathrm{A}] \quad \cdots \quad (1)$$

Where :
f is Switching frequency
I_L is Output ripple current

Efficiency is affected as the dissipation factor, $P_D(I^2R)$, P_D(Gate), P_D(SW), changes with respect to the coil value and PFM frequency dependence on ripple current.
BD9B331GWZ is designed to have least dissipation in PFM and PWM, both about L = 0.47µH to 1µH.

※Current flow that exceeds the coil rating brings the coil into magnetic saturation, which may lead to lower efficiency. Select an inductor with an adequate margin so that the peak current does not exceed the rated current of the coil. In addition, select a coil with a low resistance component (DCR, ACR) to lessen coil dissipation and improve efficiency.

2. Output Capacitor (COUT)

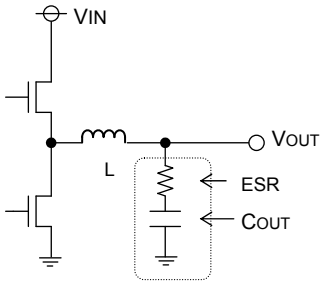


Figure 38. Output capacitor

Output capacitor should be selected with the consideration on the stability region and the equivalent series resistance required for smooth ripple voltage.

Output ripple voltage is determined by the equation (2) :

$$\Delta V_{OUT} = \Delta I_L \times ESR[\mathrm{V}] \quad \cdots \quad (2)$$

Where :
ESR is Equivalent series resistance of COUT
ΔI_L is output ripple current

※The capacitor rating must allow a sufficient margin with respect to the output voltage. A 22µF to 100µF ceramic capacitor is recommended. A capacitor with low ESR is recommended order to reduce output ripple.

Maximum value of COUT must be considered as a large current is needed to charge COUT to VOUT set point during boot-up. This current may trigger over current protection (OCP) and cause a normal boot-up failure.

$$C_{OUT} > \frac{T_{SS} \times I_{OCP}}{V_{OUT}}[\mathrm{F}] \quad \cdots \quad (3)$$

Where :
T_{SS} is Soft start time (refer to Page12)
I_{OCP} is Over current detection(min) about 6.5A

3. Input Capacitor (CIN)

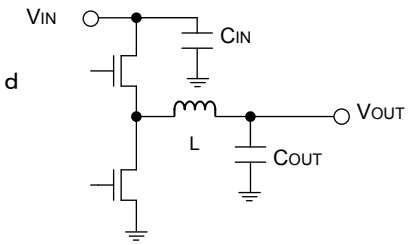


Figure 39. Input capacitor

Input capacitor must be a low ESR capacitor with a capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (4):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \text{ [A]} \quad \cdots \quad (4)$$

<Worst case> $I_{RMS(max)}$

$$V_{IN} = 2 \times V_{OUT}\ ,\ I_{RMS} = \frac{I_{OUT}}{2}$$

Ex) BD9B331GWZ when V_{IN}=5.5V, V_{OUT}=2.75V, I_{OUTmax}=3A

$$I_{RMS} = 3 \times \frac{\sqrt{2.75 \times (5.5 - 2.75)}}{5.5} = 1.5 \text{ [A}_{RMS}\text{]}$$

4. Feedback Capacitor

Generally, in fixed ON time control (hysteresis control), sufficient ripple voltage in FB voltage is needed to operate comparator stably. This IC is designed to respond to low ESR output capacitor, such as ceramic capacitor, by injecting a ripple to the feedback voltage. In order to inject appropriate ripple, a feedback capacitor of 100pF to 200pF is recommended.

5. Output Voltage Determination

The output voltage VOUT is determined by the equation (5):

$$V_{OUT} = \left(\frac{R_2}{R_1} + 1 \right) \times V_{FB} \quad \cdots \quad (5)$$

Where :

V_{FB} is FB terminal voltage(0.6V Typ.)

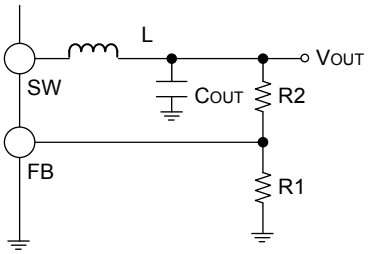


Figure 40. Output voltage setting resistor

With R1 and R2 adjusted, the output voltage may be determined as required.

(Output voltage setting range is 0.6V to PVcc × 0.8 V)

Use about 100kΩ resistor for R1 and R2 to consider loss at the PFM.

6. Bootstrap capacitor

Bootstrap capacitor CBOOT shall be 0.1μF. Connect a bootstrap capacitor between SW pin and BOOT pin.
For capacitance of Bootstrap capacitor, take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 0.047μF.

Recommended Part Circuit

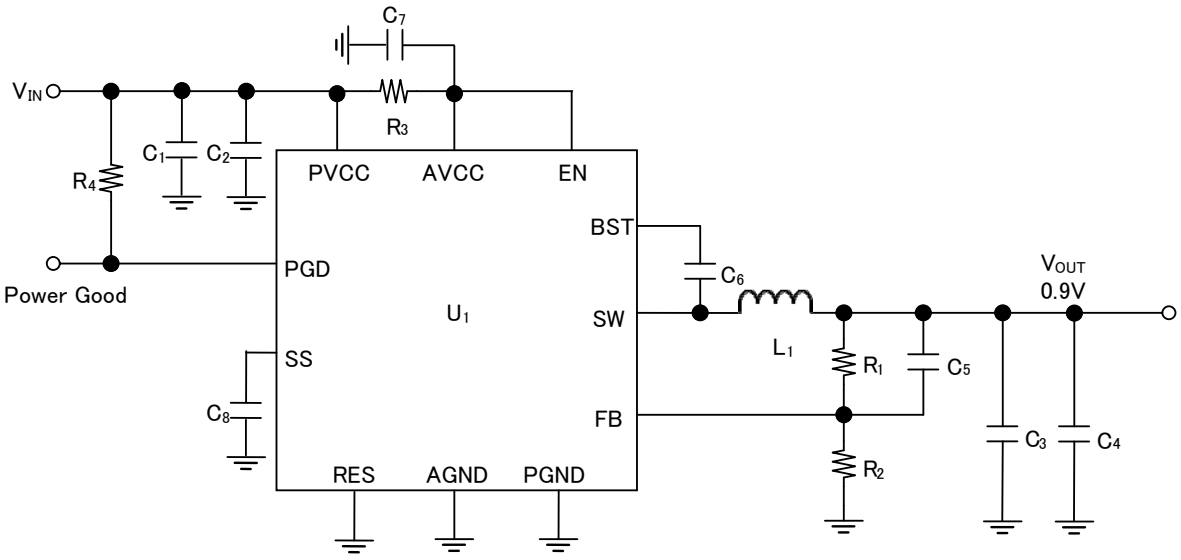


Figure 41. Recommended part circuit

●EN
Provide control signal externally when controlling the output via enable terminal.
●RES
Connect to ground.
●R4
Pull-up resistor for Power Good function.
Keep PGD open or connect it to ground when Power Good function is not in use.

●Recommendation parts list

Part No	Value	Manufacturer	Part number	Size(mm)
U1	-	ROHM	BD9B331GWZ	1.98*1.80*0.33
L1	1.0μH	TOKO	DFE252010F-1R0M	2520
C1	22μF(Note 4)	MURATA	GRM219 Series 10V	2012
C2	-	-	-	-
C3	22μF	MURATA	GRM188 Series 4V	1608
C4	-	-	-	-
C5	100pF	MURATA	GRM033 Series	0603
C6	0.1uF	MURATA	GRM033 Series	0603
C7	1000pF	ROHM	MCR006 Series	0603
C8	-	-	-	-
R1	100kΩ	ROHM	MCR006 Series	0603
R2	200kΩ	ROHM	MCR006 Series	0603
R3	100Ω	ROHM	MCR006 Series	0603
R4	100kΩ	ROHM	MCR006 Series	0603

(Note 4) For capacitance of input capacitor, take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 8μF.

※Evaluation using the actual machine must be done for above constant is only a value on our evaluation board.

PCB Layout Design

In the step-down DC/DC converter, a large pulse current flows into two loops. The first loop is the one into which the current flows when the High-Side FET is turned ON. The flow starts from the input capacitor CIN, runs through the FET, inductor L and output capacitor COUT and back to GND of CIN via GND of COUT. The second loop is the one into which the current flows when the Low-Side FET is turned on. The flow starts from the Low-Side FET, runs through the inductor L and output capacitor COUT and back to GND of the Low-Side FET via GND of COUT. Route these two loops as thick and as short as possible to allow noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors directly to the GND plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

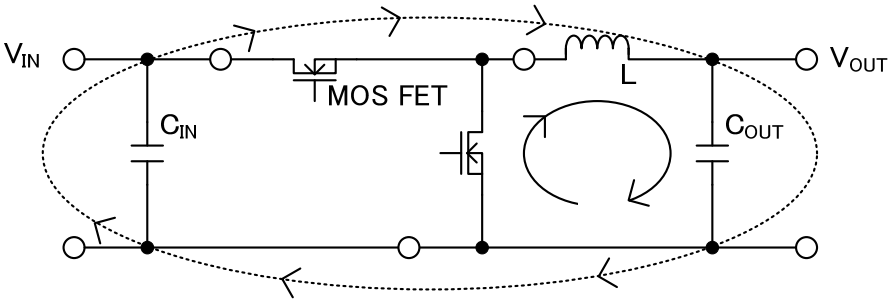


Figure 42. Current Loop of Buck Converter

Accordingly, design the PCB layout considering the following points.

- Connect an input capacitor as close as possible to the IC PVCC terminal on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the GND node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Provide lines connected to FB far from the SW nodes.
- Place the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.

An example of PCB layout

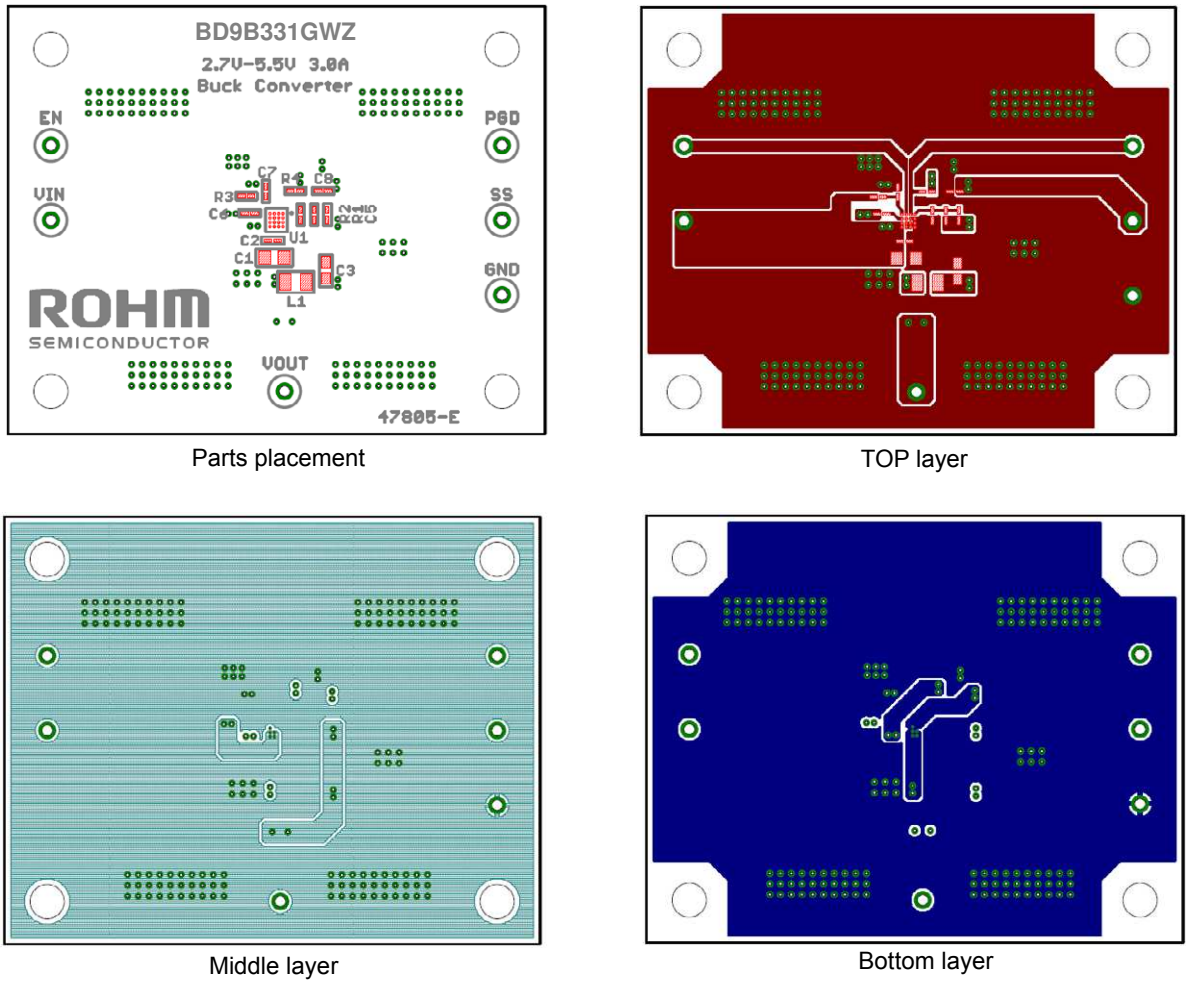


Figure 43. An example of PCB layout

I/O equivalent circuit(s)

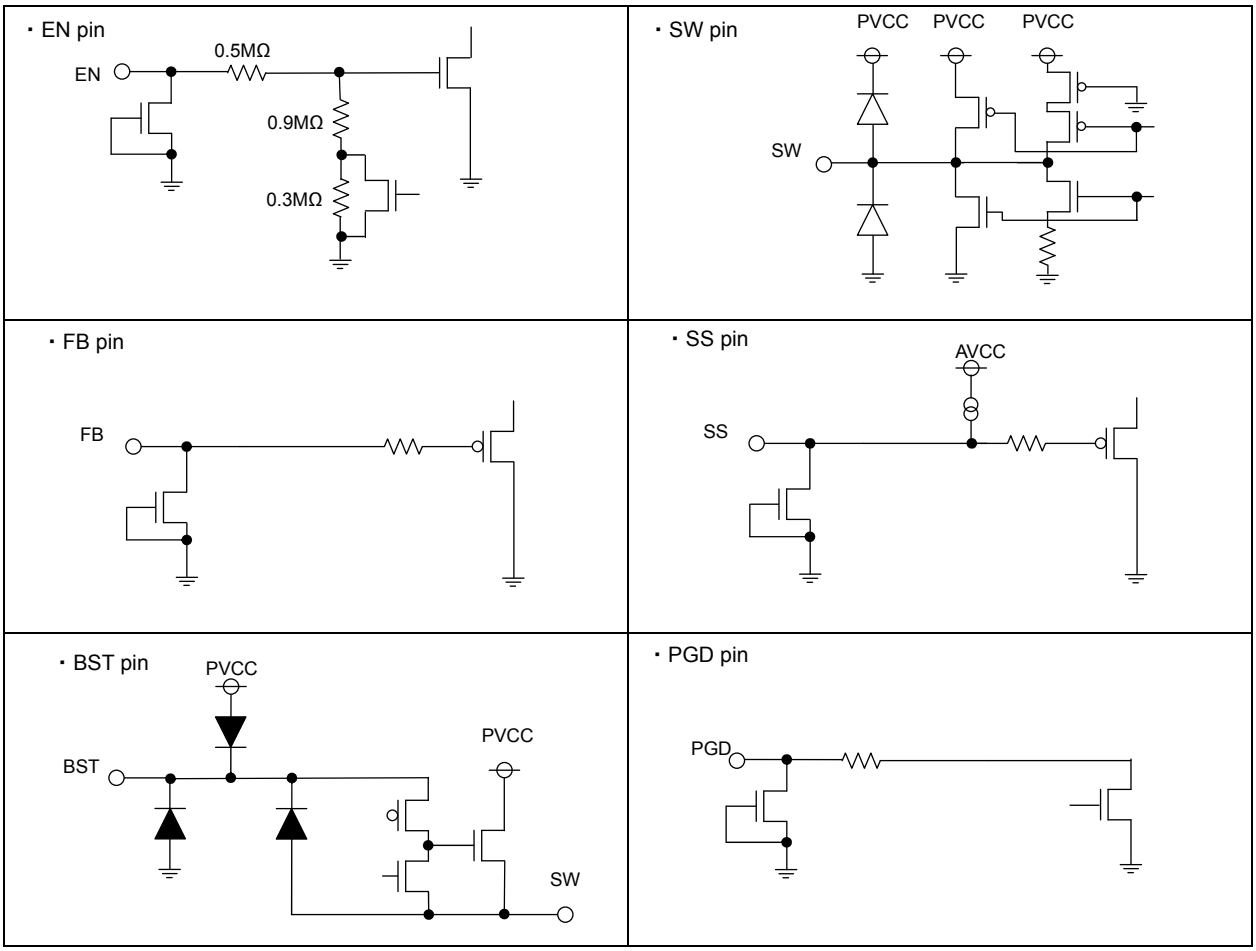


Figure 44. I/O equivalence circuit

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

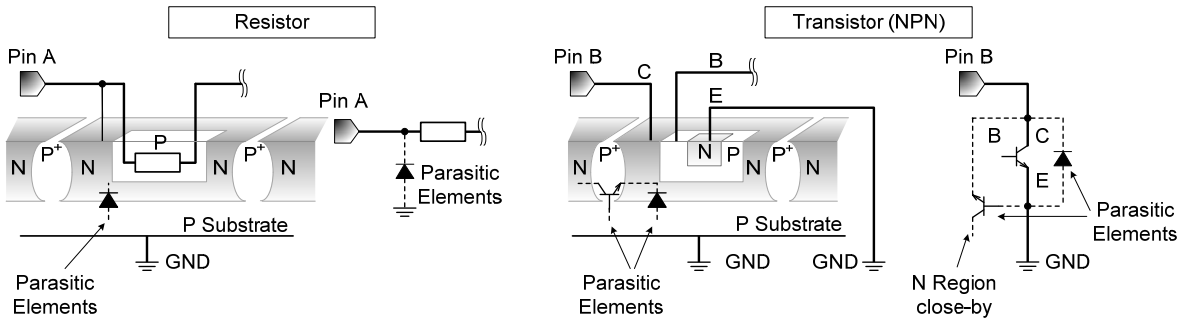


Figure 45. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the TJ falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

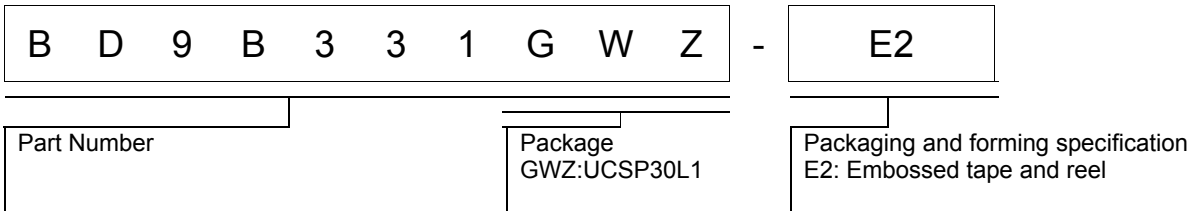
16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

17. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information



Marking Diagrams