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2.7V to 5.5V Input, 4.0A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9B400MUV

General Description

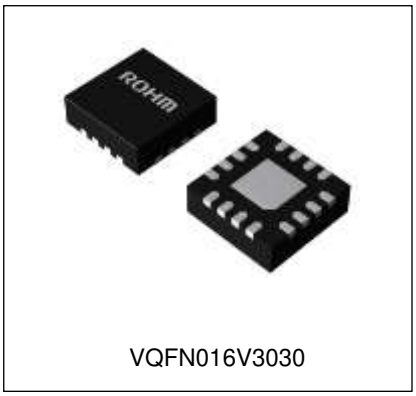
BD9B400MUV is a synchronous buck switching regulator with built-in low on-resistance power MOSFETs. This IC, which is capable of providing current up to 4A, features fast transient response by employing constant on-time control system. It offers high oscillating frequency at low inductance. With its original constant on-time control method which operates low consumption at light load, this product is ideal for equipment and devices that demand minimal standby power consumption.

Key Specifications

- Input Voltage Range: 2.7V to 5.5V
- Output Voltage Range: 0.8 V to V_{PVIN} x 0.8 V
- Maximum Operating Current: 4A (Max)
- Switching Frequency: 2MHz/1MHz (Typ)
- High-Side MOSFET ON Resistance: 30mΩ (Typ)
- Low-Side MOSFET ON Resistance: 30mΩ (Typ)
- Standby Current: 0μA (Typ)

Package(s)

	W (Typ) x D (Typ) x H (Max)
VQFN016V3030	3.00 mm x 3.00 mm x 1.00 mm



VQFN016V3030

Features

- Synchronous Single DC/DC Converter
- Constant on-time control suitable to Deep-SLLM
- Over Current Protection
- Short Circuit Protection
- Thermal Shutdown Protection
- Under Voltage Lockout Protection
- Adjustable Soft Start
- Power Good Output
- VQFN016V3030 Package (backside heat dissipation)

Applications

- Step-down Power Supply for DSPs, FPGAs, Microprocessors, etc.
- Laptop PCs/Tablet PCs/Servers
- LCD TVs
- Storage Devices (HDDs/SSDs)
- Printers, OA Equipment
- Entertainment Devices
- Distributed Power Supply, Secondary Power Supply

Typical Application Circuit

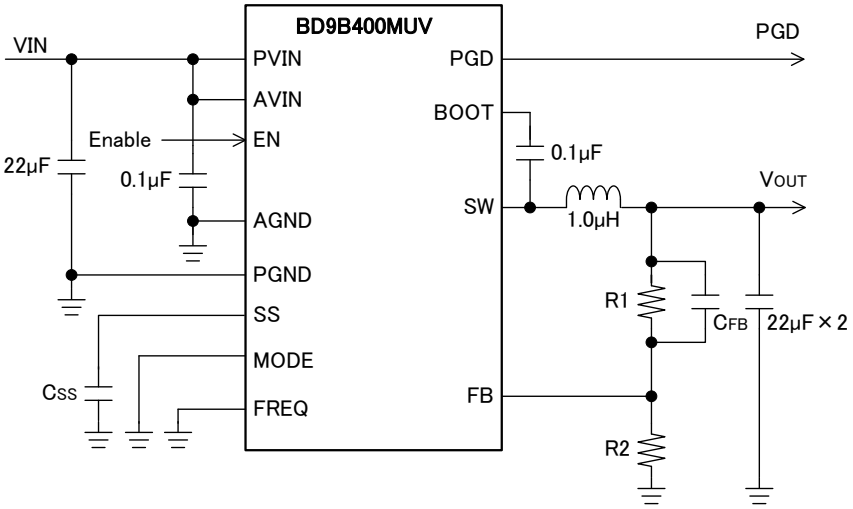


Figure 1. Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration(s)

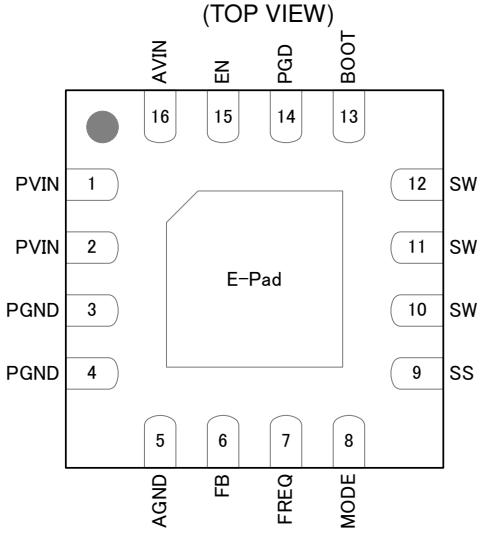


Figure 2. Pin Assignment

Pin Description(s)

Pin No.	Pin Name	Function
1, 2	PVIN	Power supply terminals for the switching regulator. These terminals supply power to the output stage of the switching regulator. Connecting a 22µF ceramic capacitor is recommended.
3, 4	PGND	Ground terminals for the output stage of the switching regulator.
5	AGND	Ground terminal for the control circuit.
6	FB	An inverting input node for the error amplifier and main comparator. See page 22 for how to calculate the resistance of the output voltage setting.
7	FREQ	Terminal for setting switching frequency. Connecting this terminal to ground makes switching to operate constant on-time corresponding to 2.0MHz. Connecting this terminal to AVIN makes switching to operate constant on-time corresponding to 1.0MHz. Please fix this terminal to AVIN or ground in operation.
8	MODE	Terminal for setting switching control mode. Connecting this terminal to AVIN forces the device to operate in the fixed frequency PWM mode. Connecting this terminal to ground enables the Deep-SLLM control and the mode is automatically switched between the Deep-SLLM control and fixed frequency PWM mode. Please fix this terminal to AVIN or ground in operation.
9	SS	Terminal for setting the soft start time. The rise time of the output voltage can be specified by connecting a capacitor to this terminal. See page 23 for how to calculate the capacitance.
10, 11, 12	SW	Switch nodes. These terminals are connected to the source of the High-Side MOSFET and drain of the Low-Side MOSFET. Connect a bootstrap capacitor of 0.1 µF between these terminals and BOOT terminal. In addition, connect an inductor of 0.47µH to 1µH (FREQ=L), 1µH to 1.5µH (FREQ=H) considering the direct current superimposition characteristic.
13	BOOT	Terminal for bootstrap. Connect a bootstrap capacitor of 0.1 µF between this terminal and SW terminals. The voltage of this terminal is the gate drive voltage of the High-Side MOSFET.
14	PGD	A “Power Good” terminal, an open drain output. Use of pull up resistor is needed. See page 17 for how to specify the resistance. When the FB terminal voltage reaches more than 80% of 0.8 V, the internal Nch MOSFET turns off and the output turns High.
15	EN	Enable terminal. Turning this terminal signal Low (0.8V or lower) forces the device to enter the shutdown mode. Turning this terminal signal High (2.0V or higher) enables the device. This terminal must be terminated.
16	AVIN	Terminal for supplying power to the control circuit of the switching regulator. Connecting a 0.1µF ceramic capacitor is recommended. This terminal must be connected to PVIN.
-	E-Pad	A backside heat dissipation exposed pad. Connecting to the internal PCB ground plane by using multiple vias provides excellent heat dissipation characteristics.

Block Diagram(s)

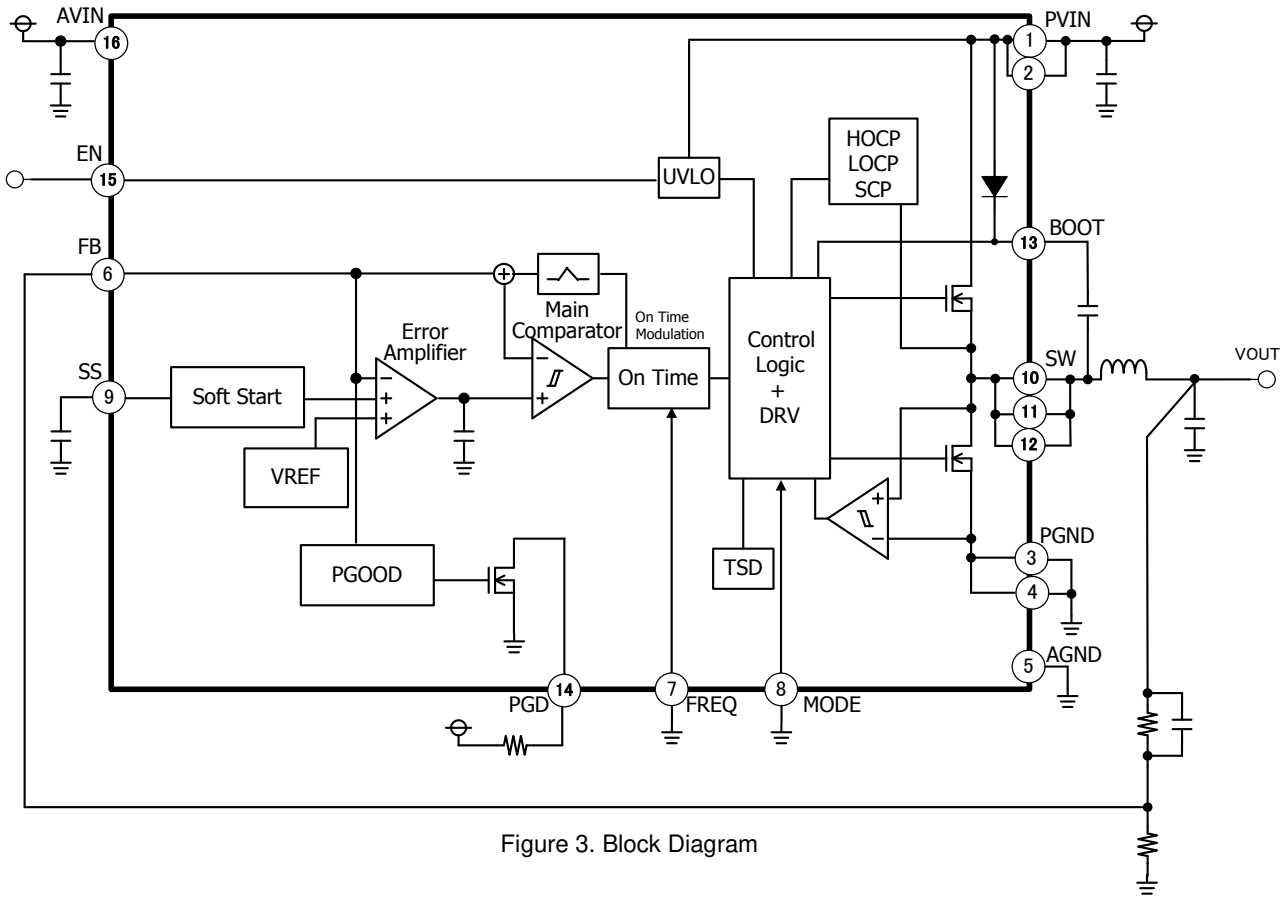


Figure 3. Block Diagram

Description of Block(s)

- VREF
  The VREF block generates the internal reference voltage.

- UVLO
  The UVLO block is for Under Voltage lockout protection. It will shut down the IC when VIN falls to 2.45 V (Typ) or lower. The threshold voltage has a hysteresis of 100mV (Typ).

- TSD
  The TSD block is for thermal protection. The thermal protection circuit shuts down the device when the internal temperature of IC rises to 175°C (Typ) or higher. Thermal protection circuit resets when the temperature falls. The circuit has a hysteresis of 25°C (Typ).

- Soft Start
  The Soft Start circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current. A built-in soft start function is provided and a soft start is initiated in 1msec (Typ) when the SS terminal is open.

- Control Logic + DRV
  This block is a DC/DC driver. A signal from On Time is applied to drive the MOSFETs.

- PGOOD
  When the FB terminal voltage reaches more than 80% of 0.8 V, the Nch MOSFET of the built-in open drain output turns off and the output turns High.

- HOCP/LOCP/SCP
  After soft start is completed and in condition where output voltage is below 70% (Typ) of voltage setting, it counts the number of times of which current flowing in High side FET or Low side FET reaches over current limit. When 512 times is counted it stops operation for 1m sec (Typ) and re-operates. Counting is reset when output voltage is above 80% (Typ) of voltage setting or when EN, UVLO, SCP function is re-operated.

- Error Amplifier
  Adjusts Main Comparator input to make internal reference voltage equal to FB terminal voltage.

- Main Comparator
  Main comparator compares Error Amplifier output and FB terminal voltage. When FB terminal voltage becomes low it outputs High and reports to the On Time block that the output voltage has dropped below control voltage.

- On Time
  This is a block which creates On Time. Requested On Time is created when Main Comparator output becomes High. On Time is adjusted to restrict frequency change even with I/O voltage change.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{PVIN}, V_{AVIN}	-0.3 to +7	V
EN Terminal Voltage	V_{EN}	-0.3 to +7	V
MODE Terminal Voltage	V_{MODE}	-0.3 to +7	V
FREQ Terminal Voltage	V_{FREQ}	-0.3 to +7	V
PGD Terminal Voltage	V_{PGD}	-0.3 to +7	V
Voltage from GND to BOOT	V_{BOOT}	-0.3 to +14	V
Voltage from SW to BOOT	ΔV_{BOOT}	-0.3 to +7	V
FB Terminal Voltage	V_{FB}	-0.3 to +7	V
SW Terminal Voltage	V_{SW}	-0.3 to V_{PVIN} + 0.3	V
Output Current	I_{OUT}	4.5	A
Operating Temperature Range	Topr	-40 to 85	°C
Storage Temperature Range	Tstg	-55 to 150	°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN016V3030				
Junction to Ambient	θ_{JA}	189.0	57.5	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	23	10	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air)
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 4)*Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(NOTE 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers..

Recommended Operating Conditions (Ta= -40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{PVIN}, V_{AVIN}	2.7	-	5.5	V
Output Current *(Note 6)*	I_{OUT}	-	-	4	A
Output Voltage Range	V_{RANGE}	0.8	-	V_{PVIN} × 0.8	V

(Note 6) Pd, ASO should not be exceeded

Electrical Characteristics (Unless otherwise specified Ta=25°C, V_{AVIN} = V_{PVIN} = 5V, V_{EN} = 5V, V_{MODE} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
AVIN pin						
Standby Supply Current	I_{STB}	-	0	10	µA	EN=GND
Operating Supply Current	I_{CC}	-	45	80	µA	FREQ=AVIN, I_{OUT}=0mA Non switching
UVLO Detection Threshold	V_{UVLO1}	2.35	2.45	2.55	V	V_{IN} falling
UVLO Release Threshold	V_{UVLO2}	2.425	2.55	2.7	V	V_{IN} rising
UVLO Hysteresis	$V_{UVLOHYS}$	50	100	200	mV	
Enable						
EN Input High Level Voltage	V_{ENH}	2.0	-	-	V	
EN Input Low Level Voltage	V_{ENL}	-	-	0.8	V	
EN Input Current	I_{EN}	-	5	10	µA	EN=5V
Reference Voltage, Error Amplifier						
FB Terminal Voltage	V_{FB}	0.792	0.8	0.808	V	
FB Input Bias Current	I_{FB}	-	-	1	µA	FB=0.8V
Internal Soft Start Time	T_{SS}	0.5	1.0	2.0	ms	SS terminal is open
Soft Start Terminal Current	I_{SS}	0.5	1.0	2.0	µA	
Control						
FREQ Input High Level Voltage	V_{FRQH}	V_{AVIN}-0.3	-	-	V	
FREQ Input Low Level Voltage	V_{FRQL}	-	-	0.3	V	
MODE Input High Level Voltage	V_{MODEH}	V_{AVIN}-0.3	-	-	V	
MODE Input Low Level Voltage	V_{MODEL}	-	-	0.3	V	
On time1	ONT1	96	120	144	ns	V_{OUT}=1.2V, FREQ=GND
On time2	ONT2	192	240	288	ns	V_{OUT}=1.2V, FREQ=AVIN
Power Good						
Power Good Rising Threshold	V_{PGDH}	75	80	85	%	FB rising, V_{PGDH}=FB/VFBx100
Power Good Falling Threshold	V_{PGDL}	65	70	75	%	FB falling, V_{PGDL}=FB/VFBx100
Output Leakage Current	I_{LKPGD}	-	0	5	µA	PGD=5V
Power Good On Resistance	R_{PGD}	-	100	200	Ω	
Power Good Low Level Voltage	P_{GDVL}	-	0.1	0.2	V	I_{PGD}=1mA
SW						
High Side FET On Resistance	R_{ONH}	-	30	60	mΩ	BOOT - SW = 5 V
Low Side FET On Resistance	R_{ONL}	-	30	60	mΩ	
High Side Output Leakage Current	R_{ILH}	-	0	10	µA	No switching
Low Side Output Leakage Current	R_{ILL}	-	0	10	µA	No switching

Typical Performance Curves

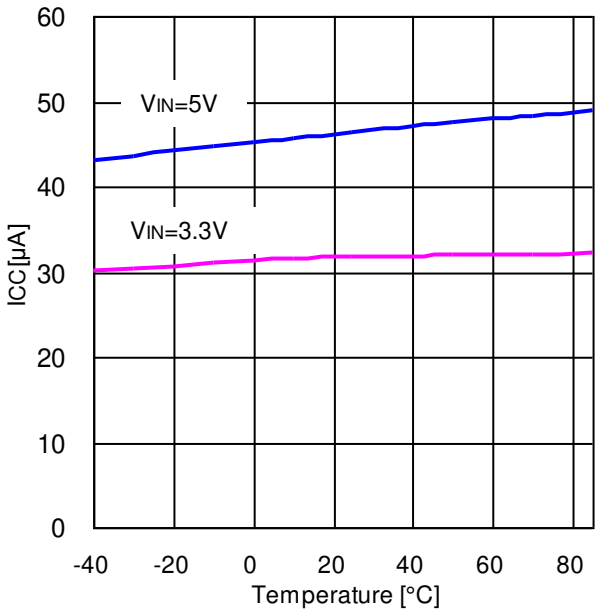


Figure 4. Operating Supply Current vs Temperature

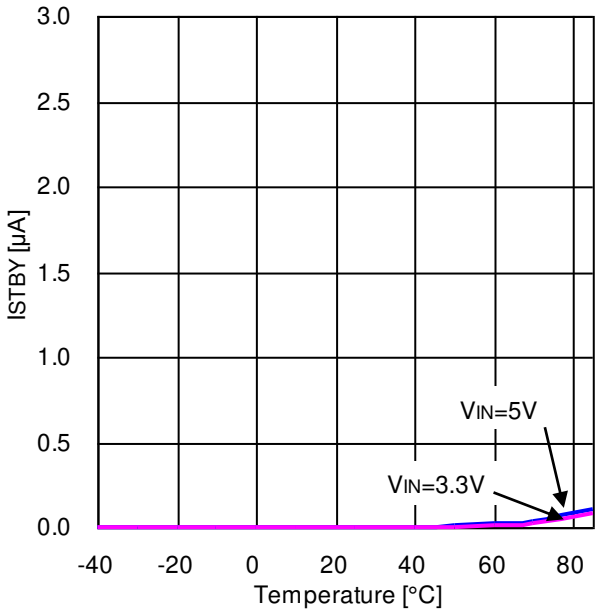


Figure 5. Stand-by Supply Current vs Temperature

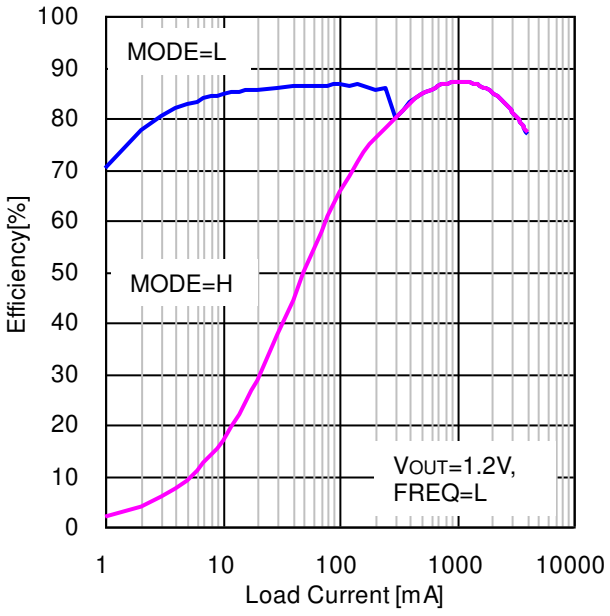


Figure 6. Efficiency vs Load Current
(VIN=5V, VOUT=1.2V, L=1.0µH, FREQ=L)

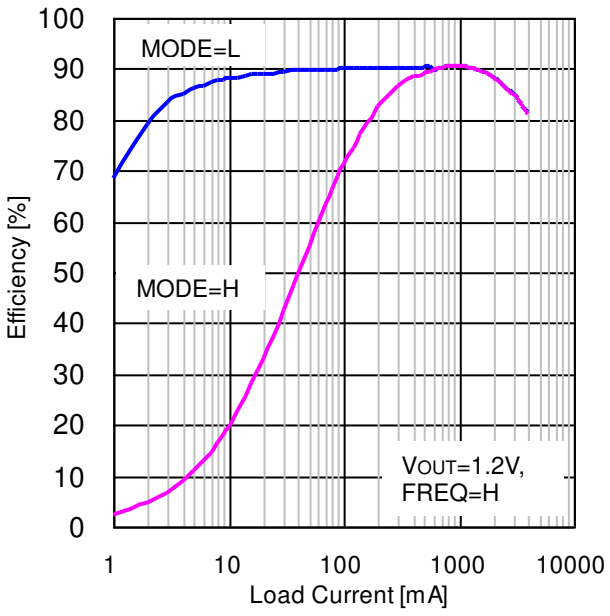


Figure 7. Efficiency vs Load Current
(VIN=5V, VOUT=1.2V, L=1.0µH, FREQ=H)

Typical Performance Curves - continued

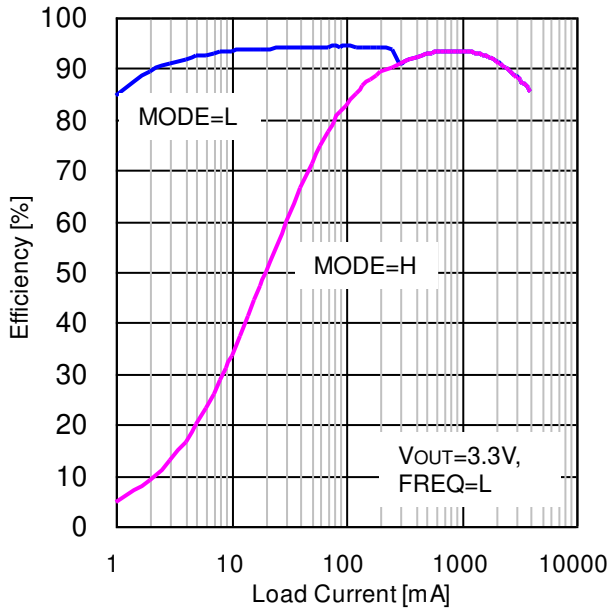


Figure 8. Efficiency vs Load Current
(VIN=5V, VOUT=3.3V, L=1.0µH, FREQ=L)

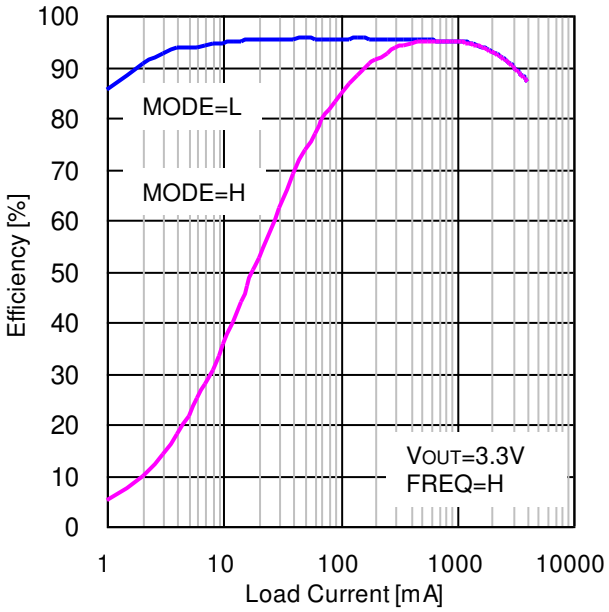


Figure 9. Efficiency vs Load Current
(VIN=5V, VOUT=3.3V, L=1.0µH, FREQ=H)

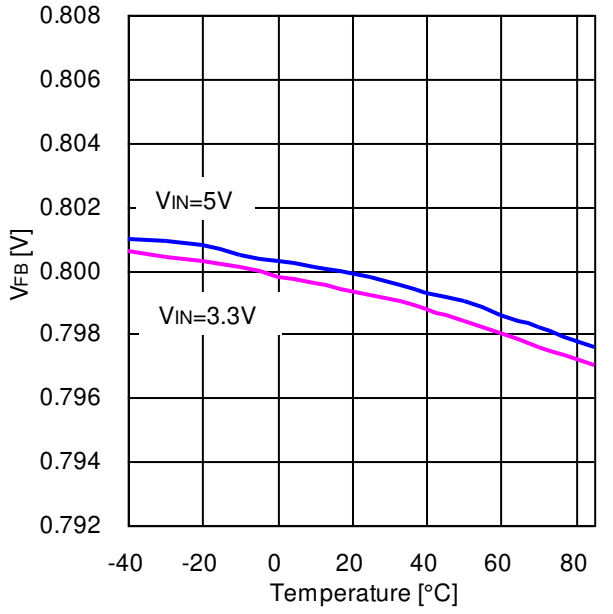


Figure 10. FB Voltage vs Temperature

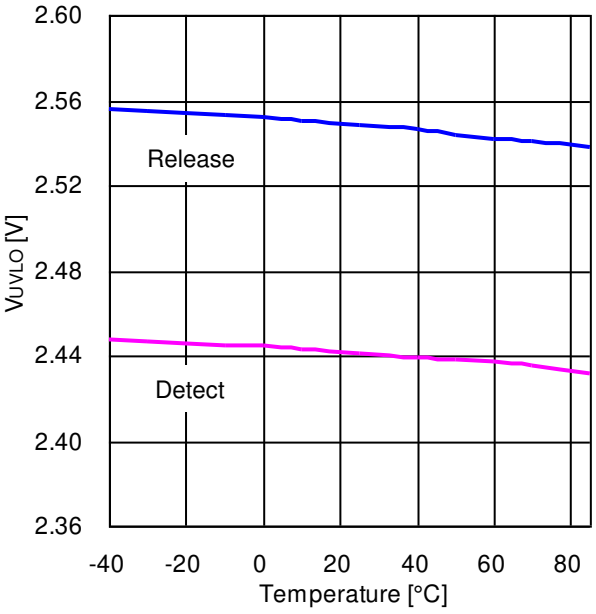


Figure 11. UVLO Threshold vs Temperature

Typical Performance Curves - continued

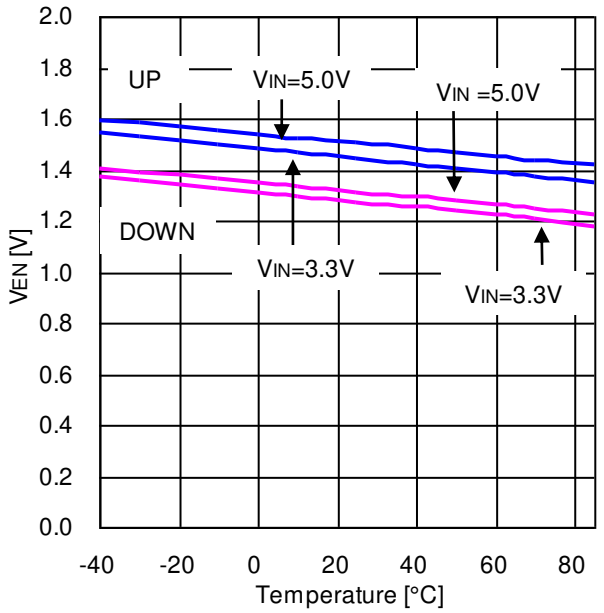


Figure 12. EN Threshold vs Temperature

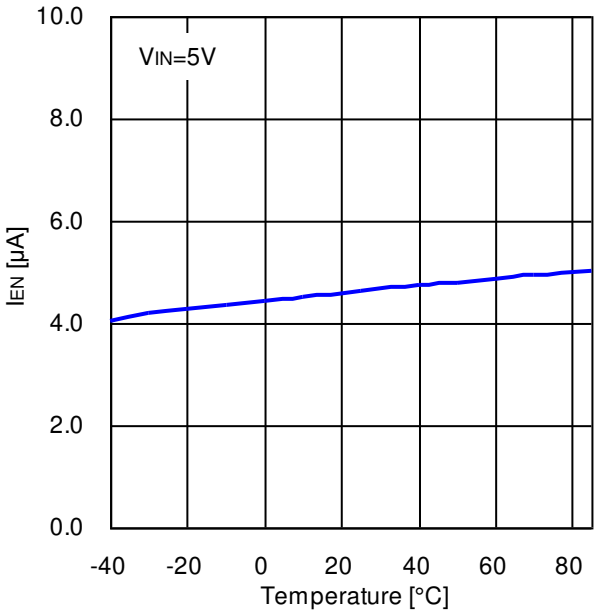


Figure 13. EN Input Current vs Temperature

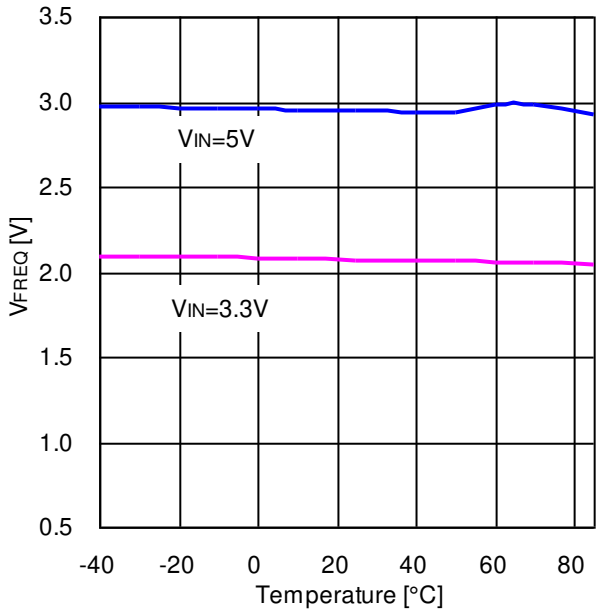


Figure 14. FREQ Threshold vs Temperature

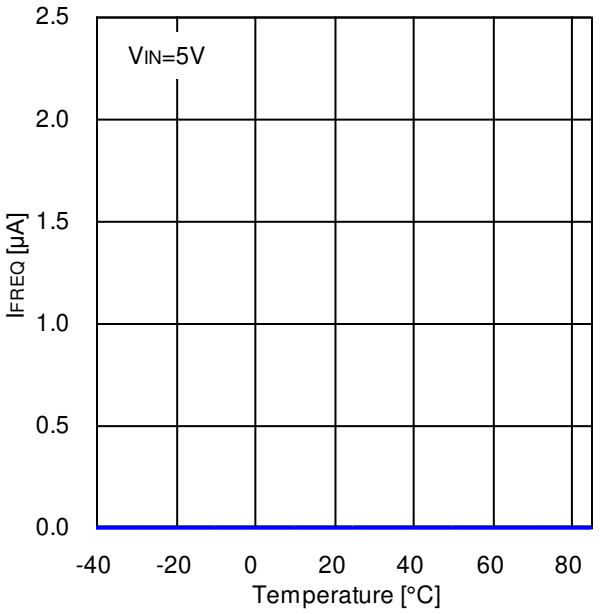


Figure 15. FREQ Input Current vs Temperature

Typical Performance Curves - continued

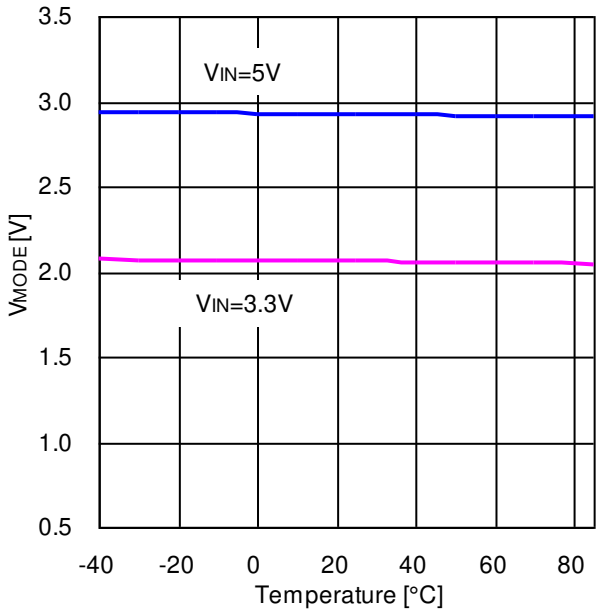


Figure 16. MODE Threshold Voltage vs Temperature

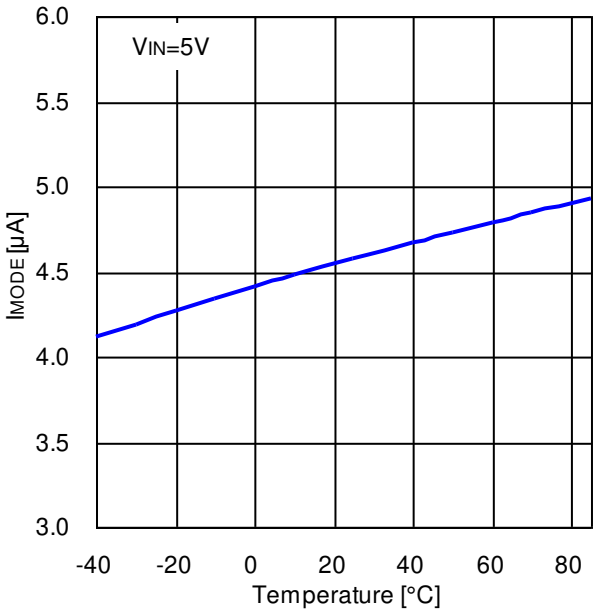


Figure 17. MODE Input Current vs Temperature

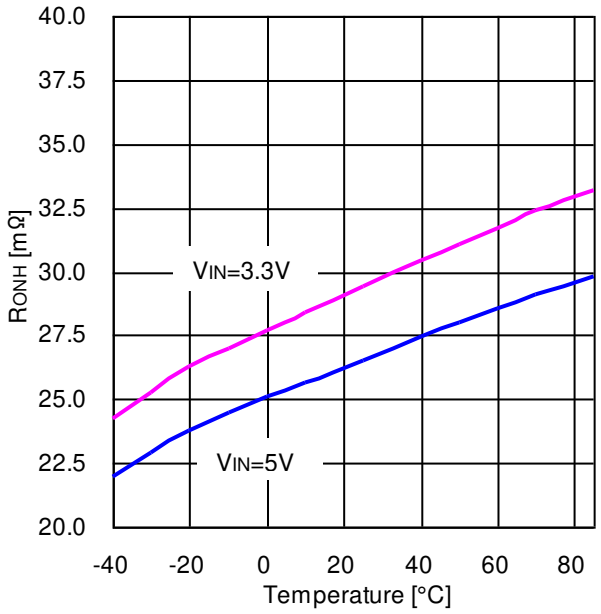


Figure 18. High Side ON-Resistance vs Temperature

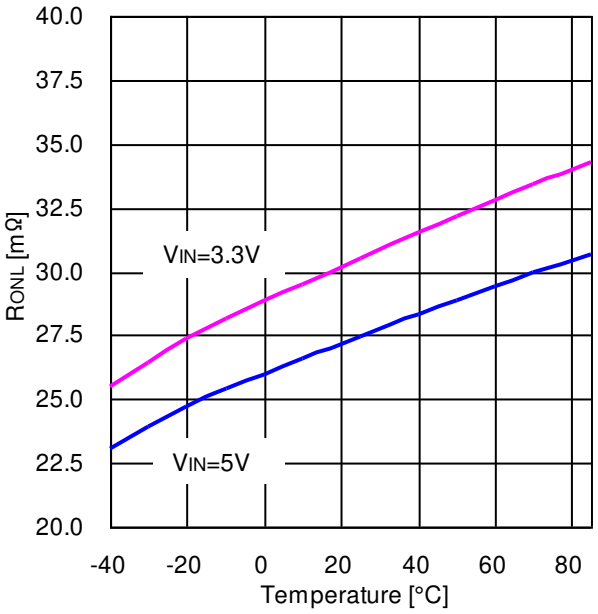


Figure 19. Low Side ON-Resistance vs Temperature

Typical Performance Curves - continued

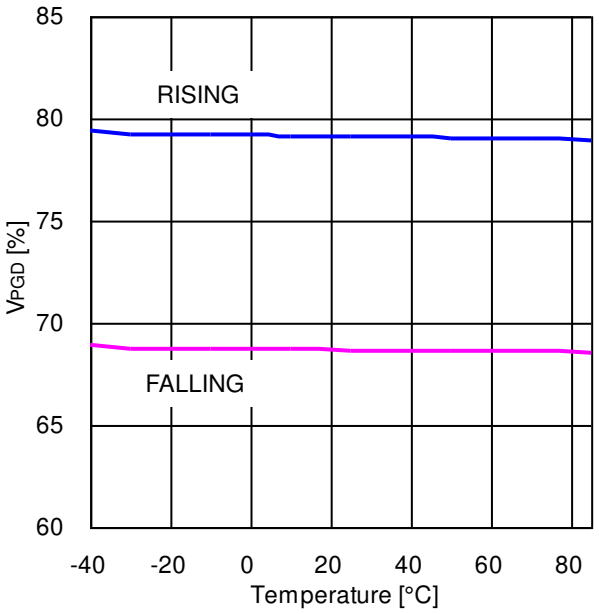


Figure 20. PGD Threshold vs Temperature

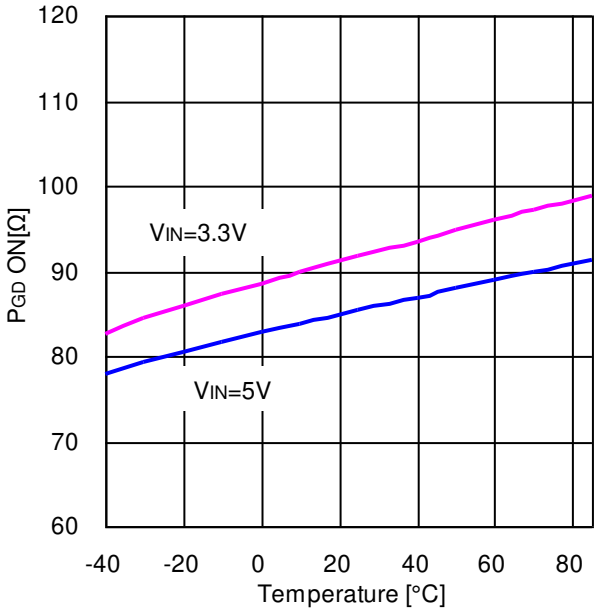


Figure 21. PGD ON-Resistance vs Temperature

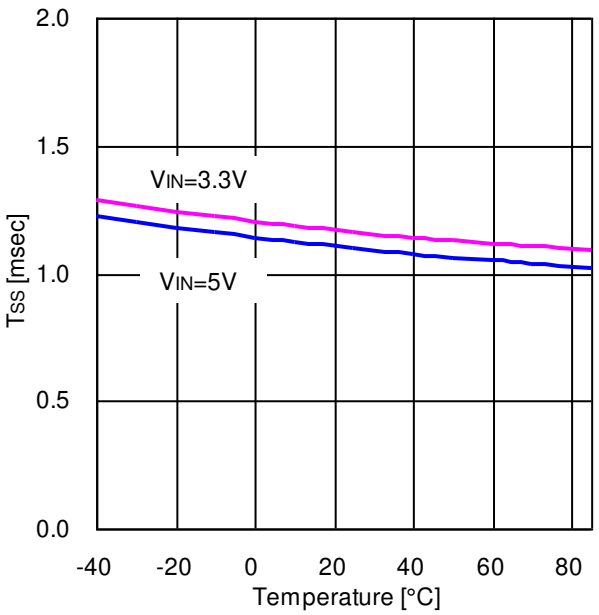


Figure 22. Soft Start Time vs Temperature

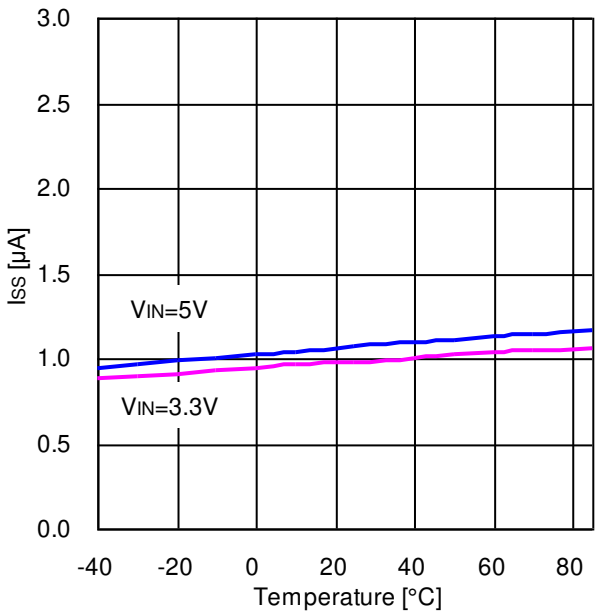


Figure 23. SS Terminal Current vs Temperature

Typical Performance Curves - continued

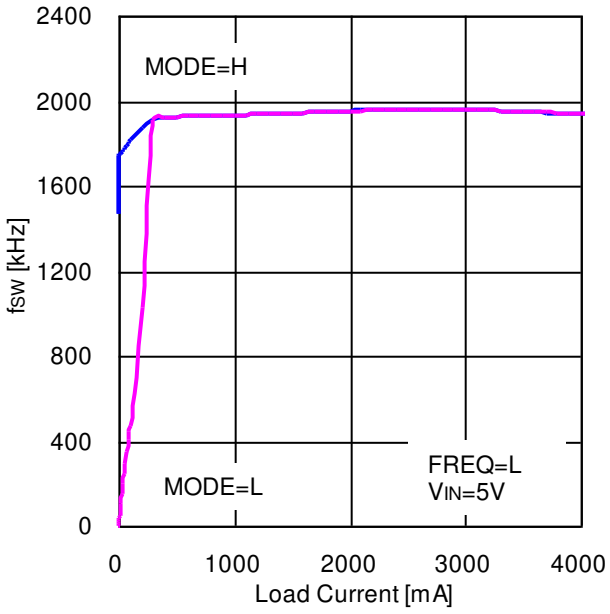


Figure 24. Switching Frequency vs Load Current

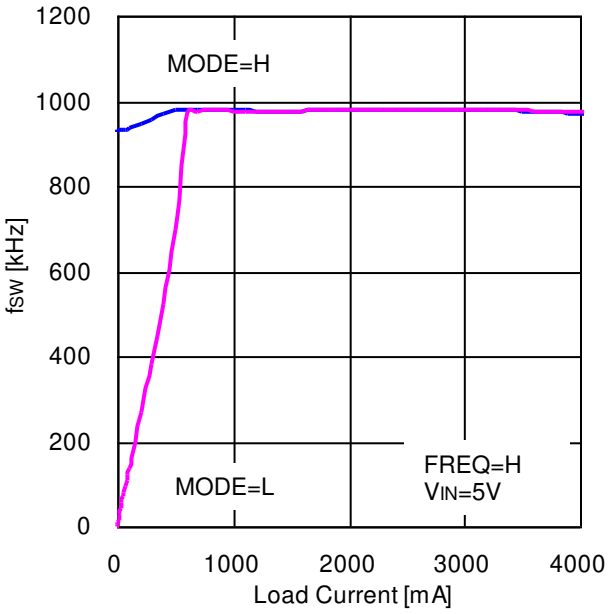


Figure 25. Switching Frequency vs Load Current

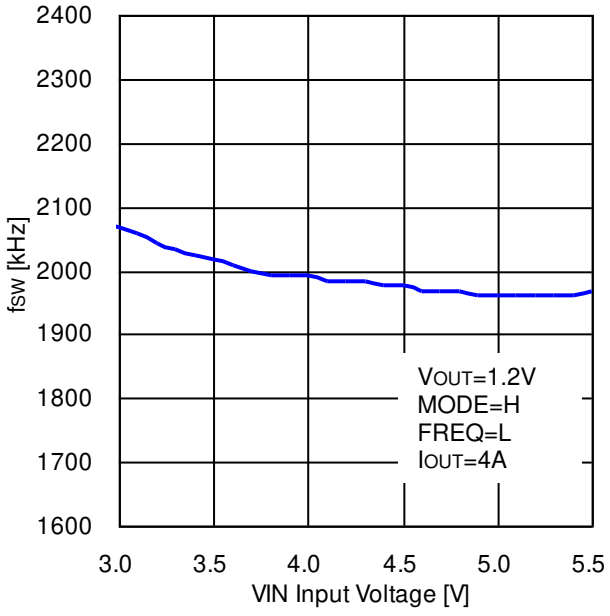


Figure 26. Switching Frequency vs Input Voltage

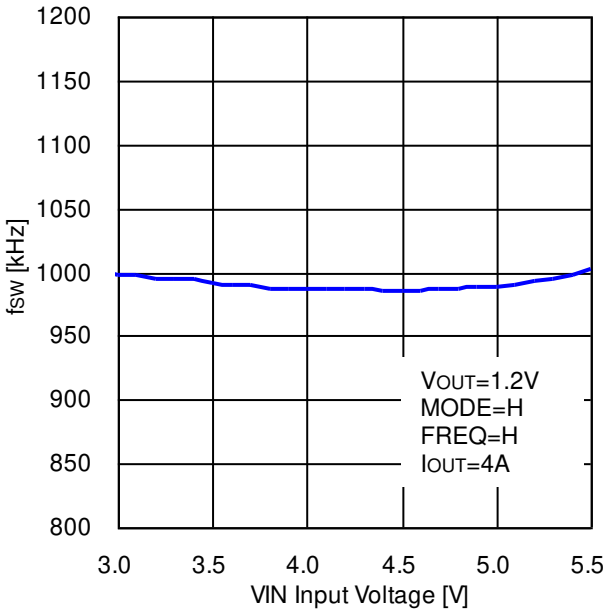


Figure 27. Switching Frequency vs Input Voltage

Typical Performance Curves - continued

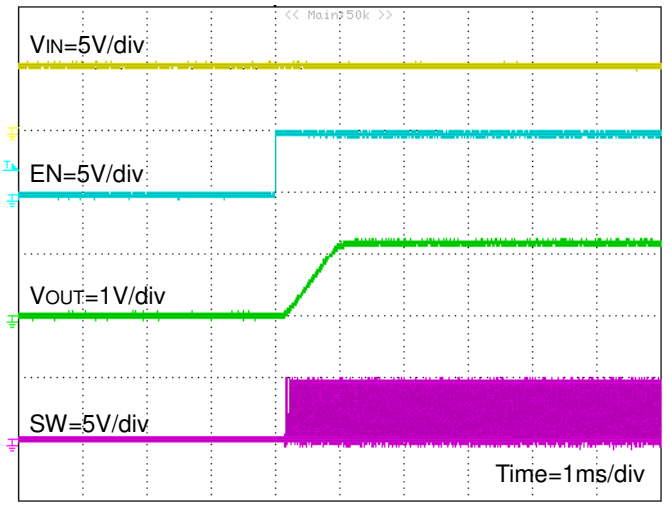


Figure 28. Power Up Waveform with EN
(FREQ=H, RLOAD=0.3Ω)

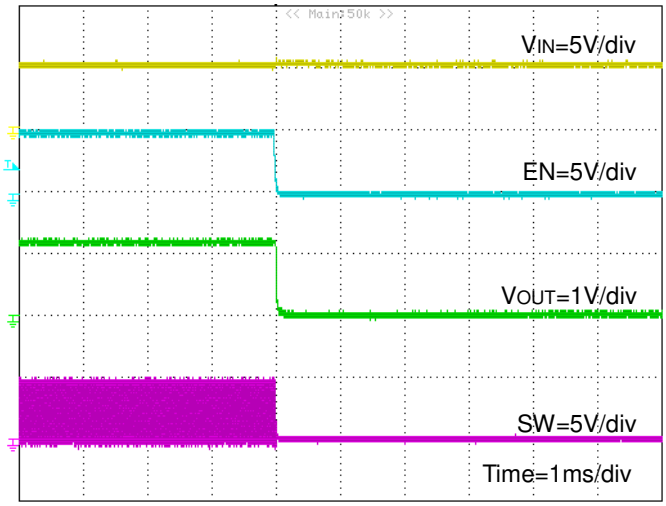


Figure 29. Power Down Waveform with EN
(FREQ=H, RLOAD=0.3Ω)

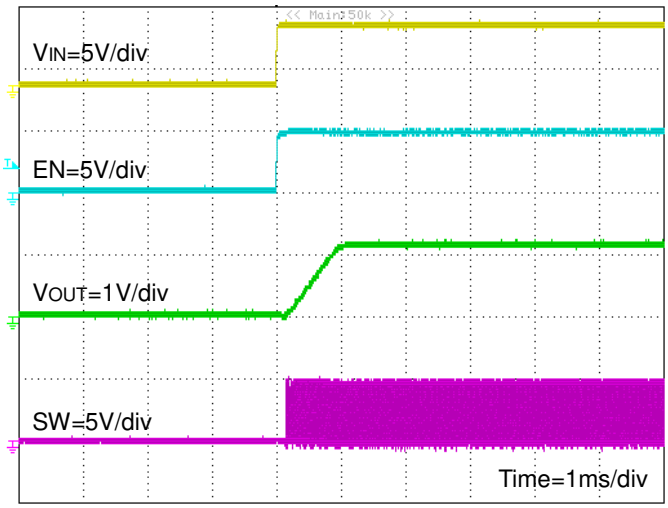


Figure 30. Power Up Waveform with VIN
(FREQ=H, RLOAD=0.3Ω)

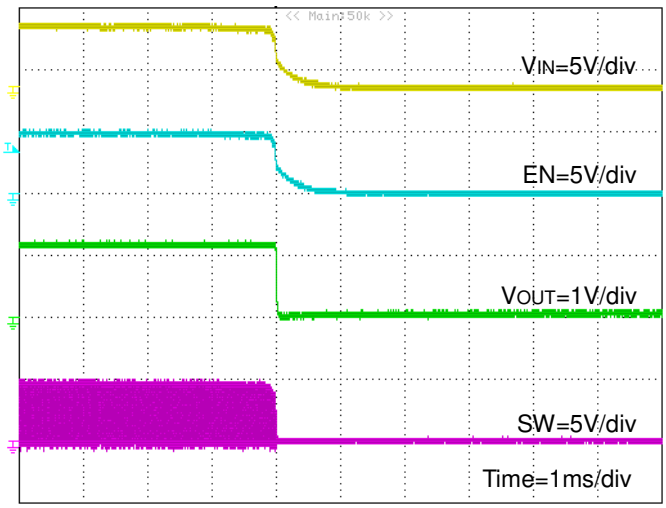


Figure 31. Power Down Waveform with VIN
(FREQ=H, RLOAD=0.3Ω)

Typical Performance Curves - continued

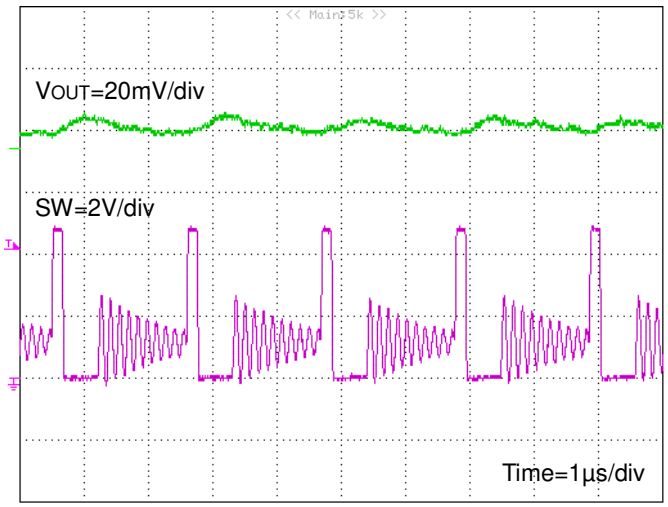


Figure 32. Switching Waveform
(VIN=5V, VOUT=1.2V, FREQ=L, IOUT=0.1A)

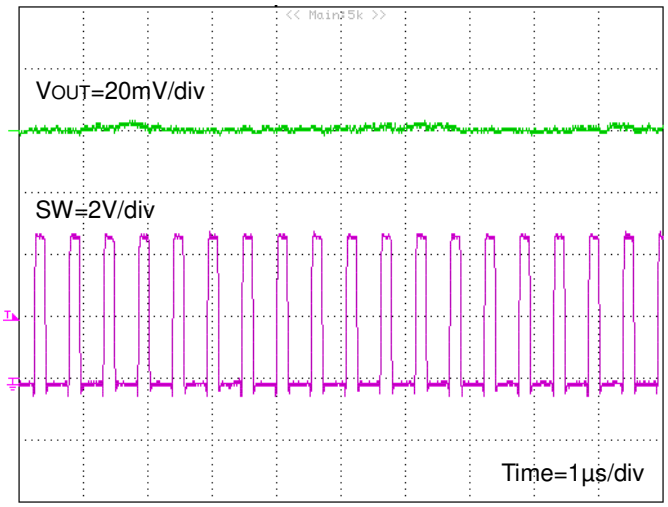


Figure 33. Switching Waveform
(VIN=5V, VOUT=1.2V, FREQ=L, IOUT=4A)

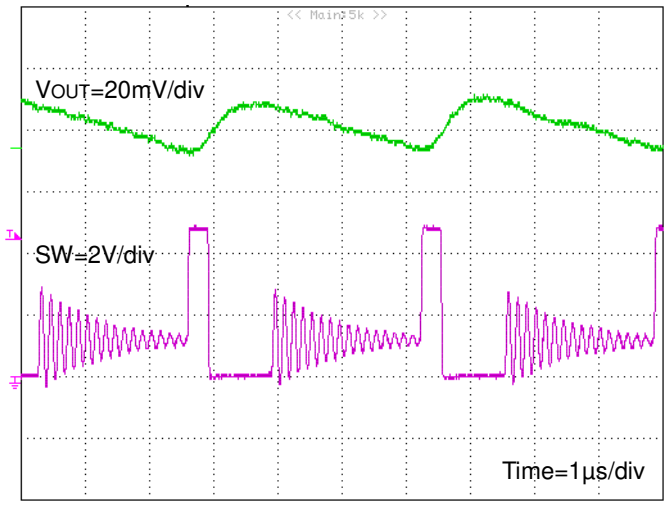


Figure 34. Switching Waveform
(VIN=5V, VOUT=1.2V, FREQ=H, IOUT=0.2A)

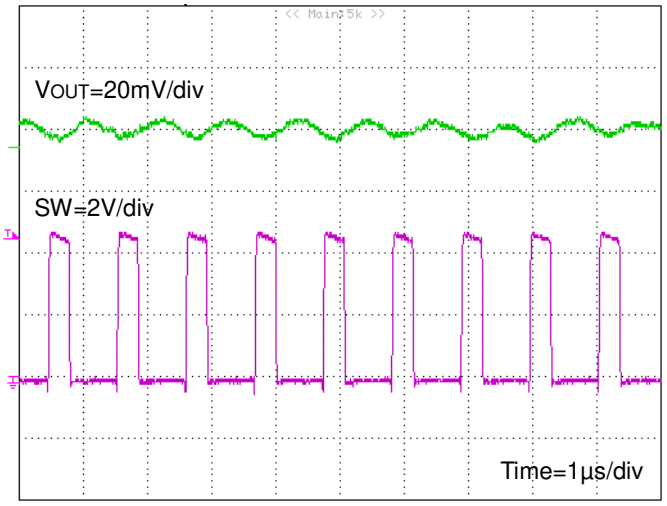


Figure 35. Switching Waveform
(VIN=5V, VOUT=1.2V, FREQ=H, IOUT=4A)

Typical Performance Curves - continued

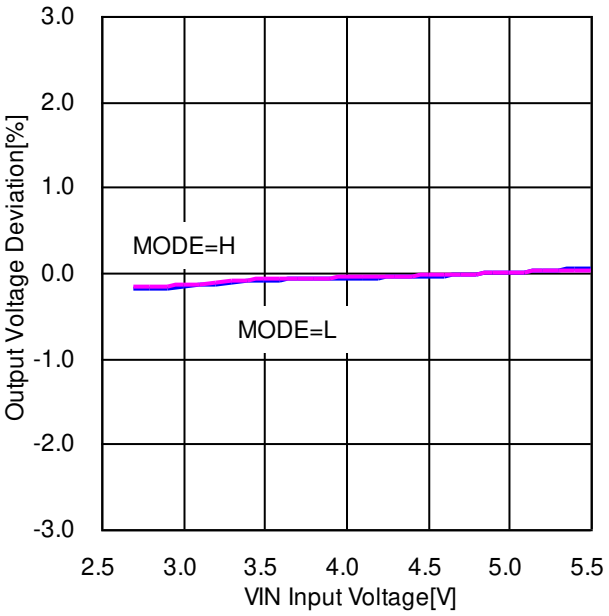


Figure 36. Line Regulation
(VOUT=1.2V, L=1.0µH, FREQ=H, IOUT=4A)

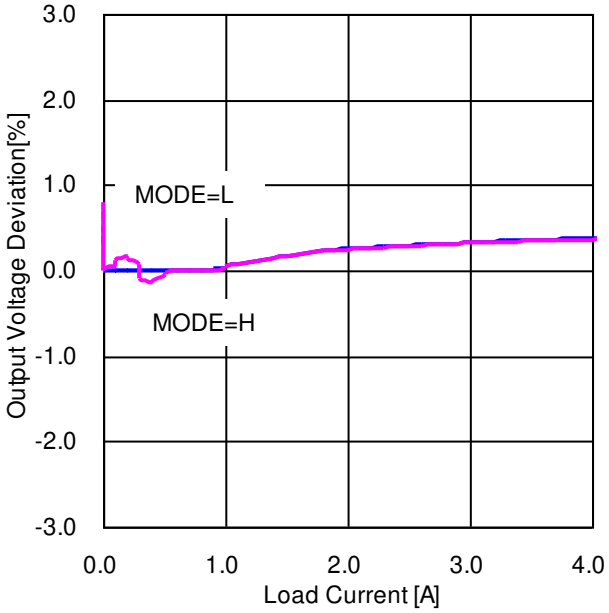


Figure 37. Load Regulation
(VIN=5V, VOUT=1.2V, L=1.0µH, FREQ=H)

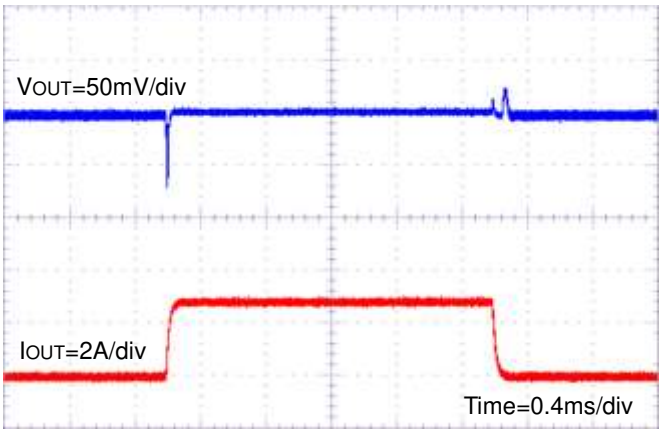


Figure 38. Load Transient Response IOUT=0.1A to 3A
(VIN=5V, VOUT=1.2V, FREQ=L, MODE=L, COUT=Ceramic 44µF)

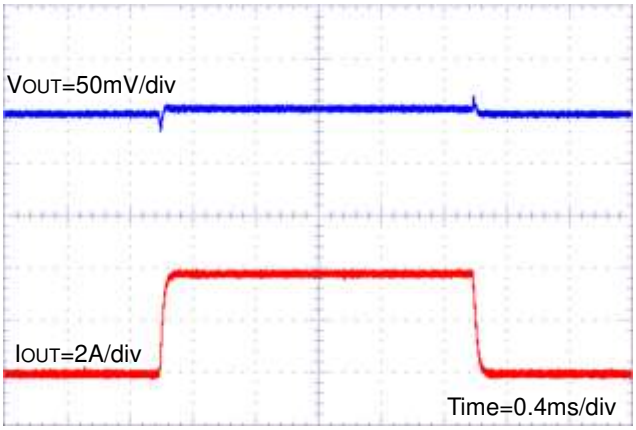


Figure 39. Load Transient Response IOUT=0.1A to 4A
(VIN=5V, VOUT=1.2V, FREQ=L, MODE=H, COUT=Ceramic 44µF)

Function explanation(s)

1. Basic Operation

(1) DC/DC Converter operation

BD9B400MUV is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing constant on-time control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes Deep-SLLM (Deep_Simple Light Load Mode) control for lighter load to improve efficiency.

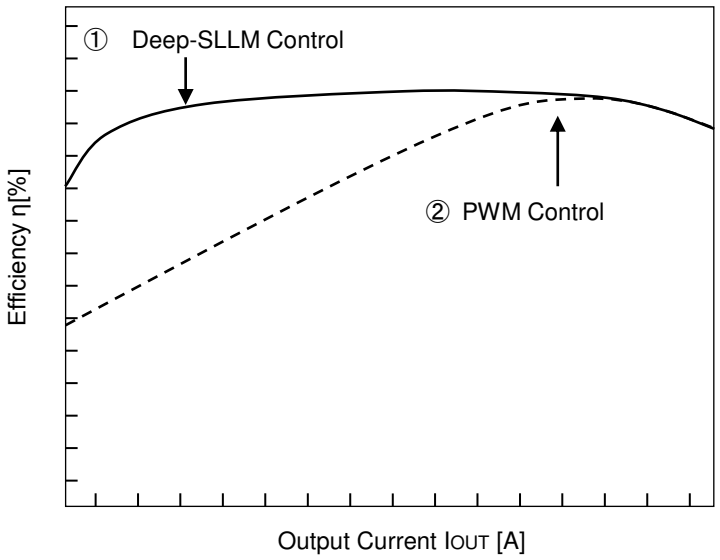


Figure 40. Efficiency (Deep-SLLM Control and PWM Control)

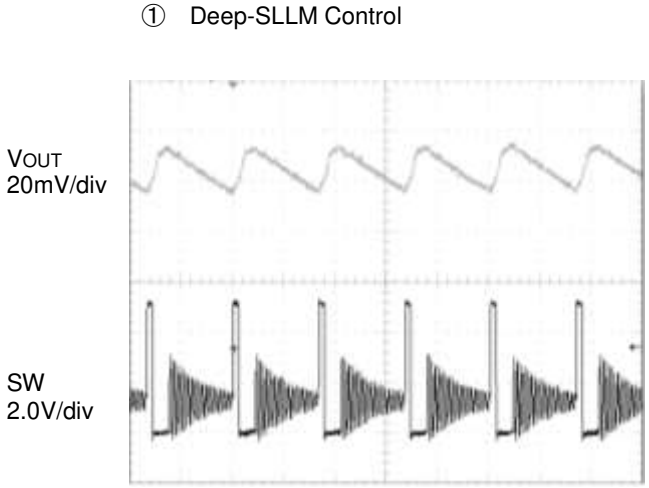


Figure 41. Switching Waveform at Deep-SLLM Control
(V_{IN}=5.0V, V_{OUT}=1.2V, I_{OUT}=100mA)

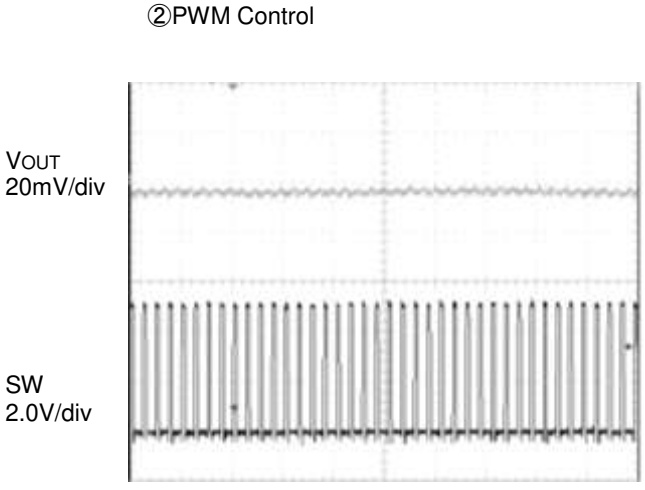


Figure 42. Switching Waveform at PWM Control
(V_{IN}=5.0V, V_{OUT}=1.2V, I_{OUT}=4A)

(2) Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When VEN reaches 2.0 V(Typ), the internal circuit is activated and the IC starts up. To enable shutdown control with the EN terminal, the shutdown interval (Low level interval of EN) must be set to 100 µs or longer. Startup by EN must be at the same time or after the input of power supply voltage.

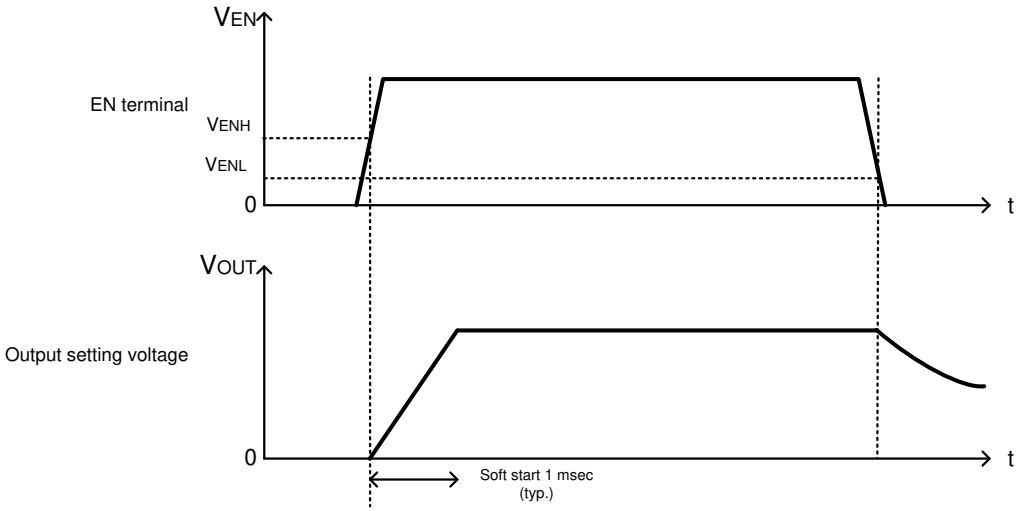


Figure 43. Start Up and Down with Enable

(3) Power Good

When the output voltage reaches more than 80% of the voltage setting, the open drain NMOSFET, internally connected to the PGD terminal, turns off and the PGD terminal turns to Hi-z condition. Also when the output voltage falls below 70% of voltage setting, the open drain NMOS FET turns on and PGD terminal pulls down with 100Ω. Connecting a pull up resistor (10KΩ to 100KΩ) is recommended.

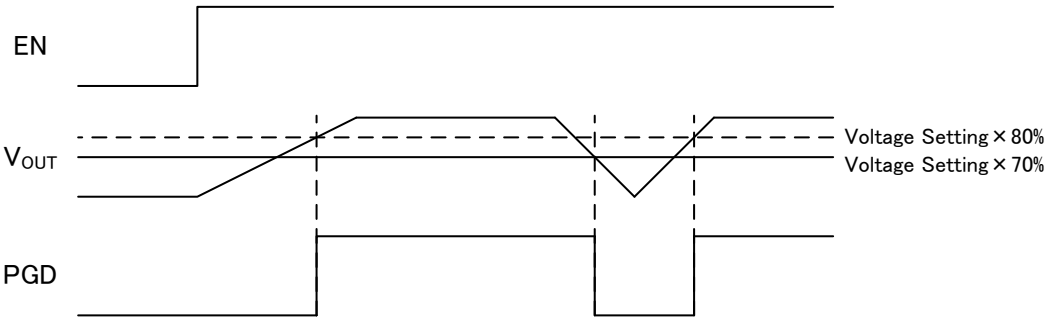


Figure 44. Power Good Timing Chart

(4) Soft Start

When EN terminal is turned High, Soft Start operates and output voltage gradually rises. With the Soft Start Function, over shoot of output voltage and rush current can be prevented. Rising time of output voltage when SS terminal is open is 1msec (Typ). Capacitor connected to SS terminal makes rising time more than 1msec. Please refer to page 23 for the method of setting rising time.

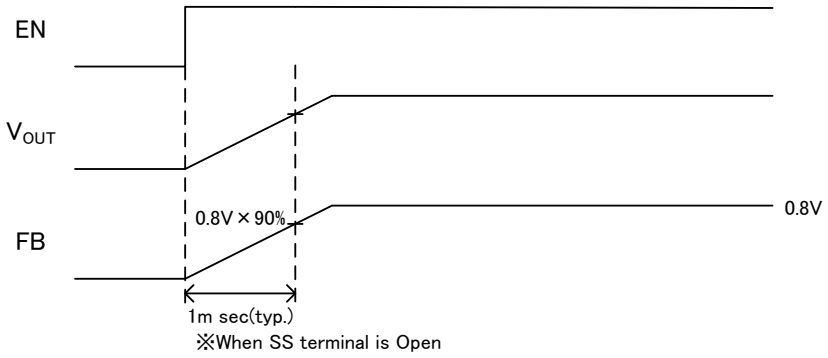


Figure 45. Soft Start Timing Chart

2. Protection

The protective circuits are intended for prevention of damage caused by unexpected accidents. Do not use them for continuous protective operation

(1) Over Current Protection (OCP) / Short Circuit Protection (SCP)

Setting (Typ) of over current protection are 7A (lower MOSFET) and 9.5A (upper MOSFET). When OCP is triggered, over current protection is realized by restricting On / Off Duty of current flowing in upper and lower MOSFET by each switching cycle. Also, if Over current protection operates 512 cycles in a condition where FB terminal voltage reaches below 70% of internal standard voltage, Short Circuit protection (SCP) operates and stops switching for 1msec (Typ) before it initiates restart. However, during startup, Short circuit protection will not operate even if the IC is still in the SCP condition.

Table 1. Over Current Protection / Short Circuit Protection Function

EN terminal	PGD	Startup	Over current protection	Short circuit protection
More than 2.0V	L	While start up	Valid	Invalid
		Startup completed	Valid	Valid
	H	*	Valid	Invalid
Less than 0.8V	*	*	Invalid	Invalid

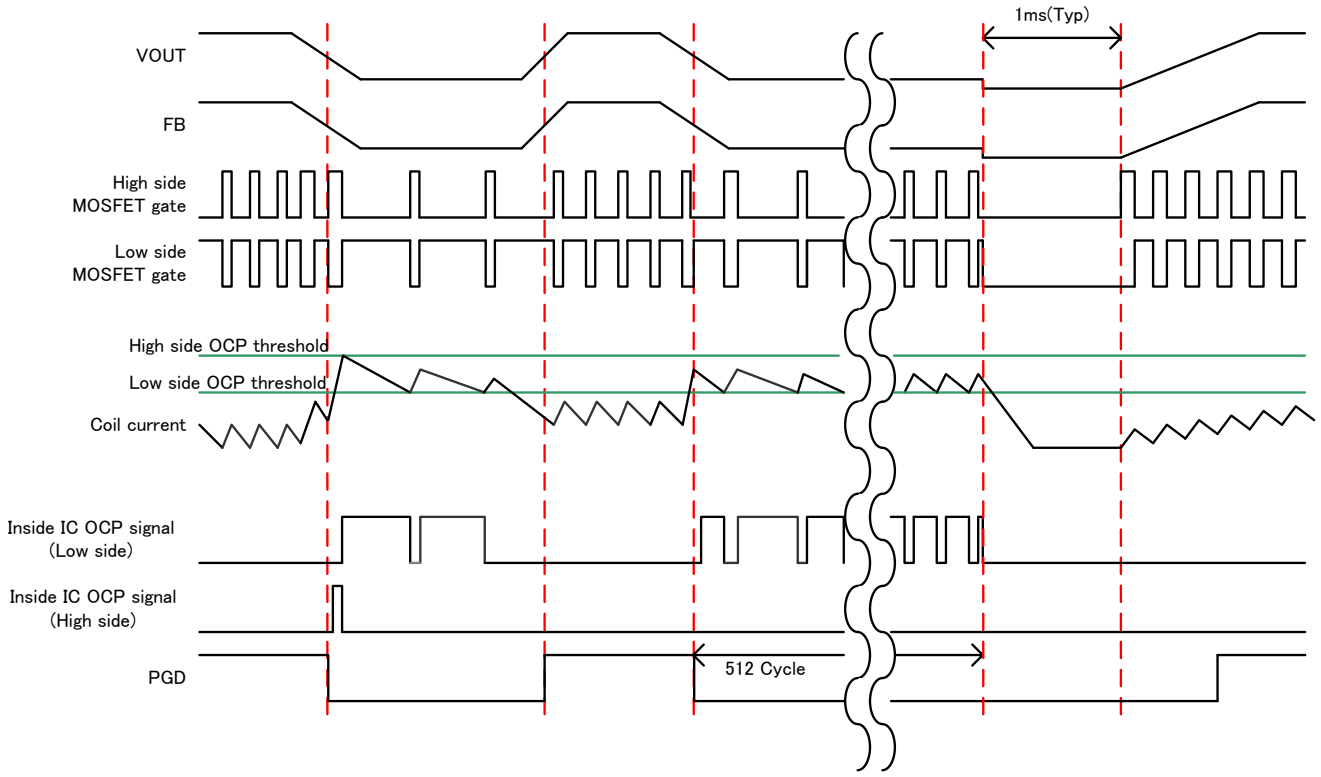


Figure 46. Short Circuit Protection (SCP) Timing Chart

(2) Under Voltage Lockout Protection (UVLO)

The Under Voltage Lockout Protection circuit monitors the AVIN terminal voltage.
The operation enters standby when the AVIN terminal voltage is 2.45V (Typ) or lower.
The operation starts when the AVIN terminal voltage is 2.55V (Typ) or higher.

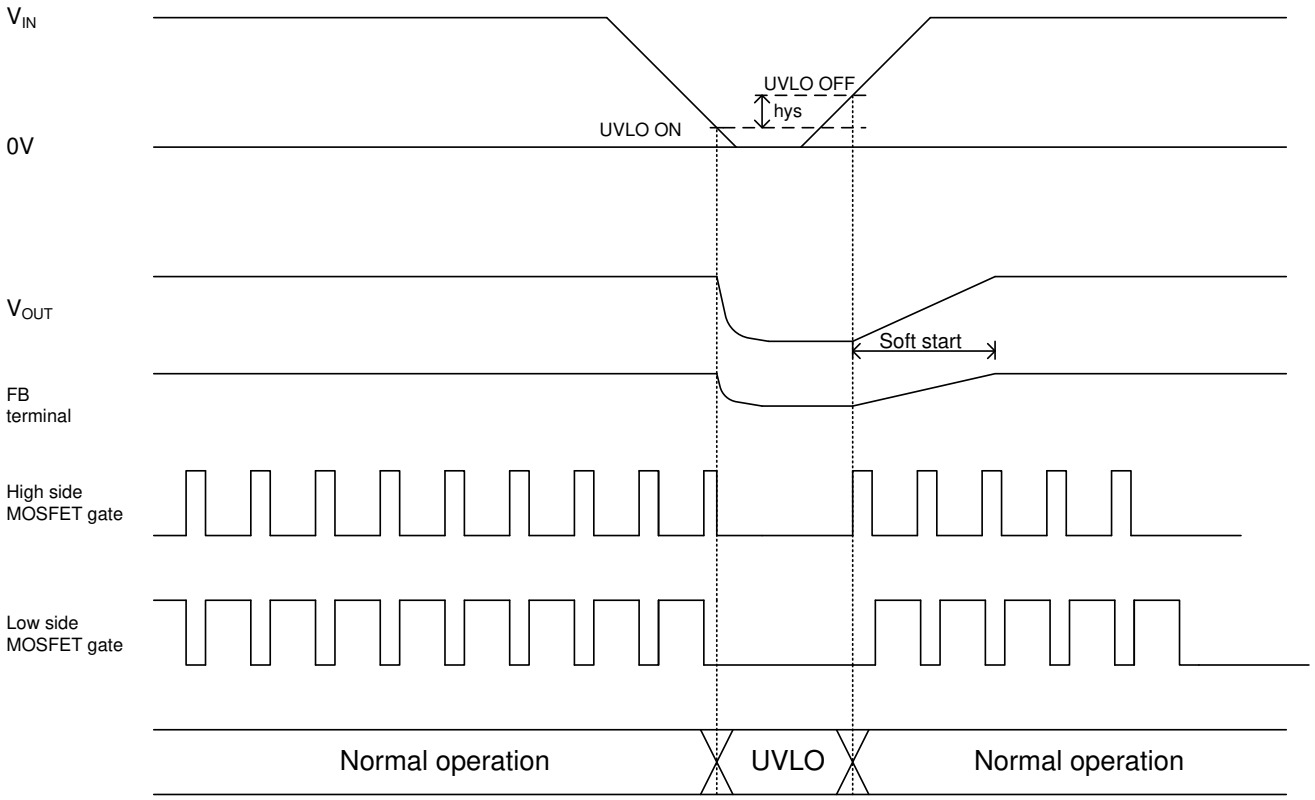


Figure 47. UVLO Timing Chart

(3) Thermal Shutdown

When the chip temperature exceeds Tj=175°C (Typ), the DC/DC converter output is stopped. The circuits are automatically restored to normal operation when the chip temperature falls. It has a hysteresis of 25°C (Typ). The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding Tjmax=150°C. It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.

Application Example(s)

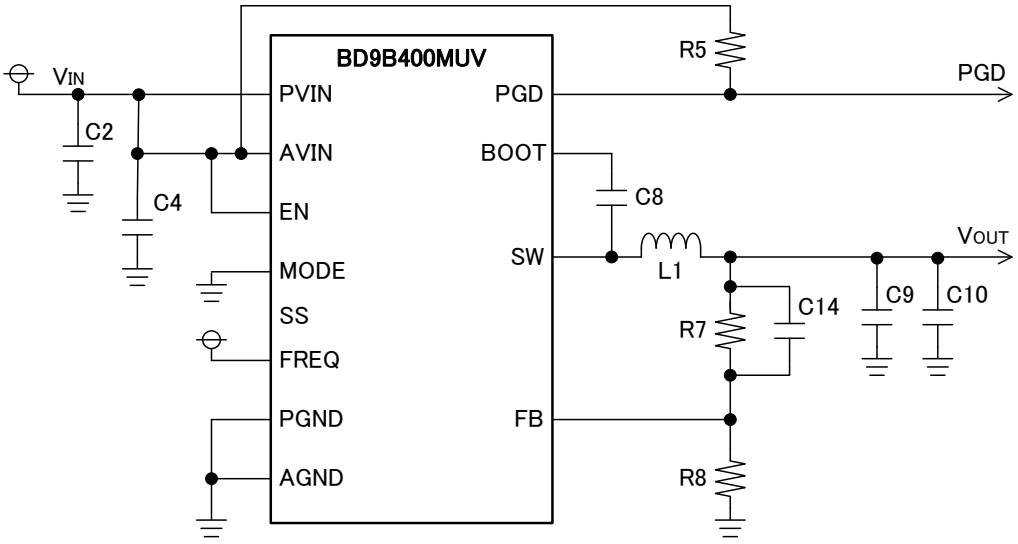


Figure 48. Application Circuit

Table 2. Recommended Component Values (V_{IN}=5V, FREQ=H)

Reference Designator	V_{OUT}					Description
	1.0V	1.2V	1.5V	1.8V	3.3V	
R5	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	-
R7	51kΩ	75kΩ	160kΩ	150kΩ	75kΩ	-
R8	200kΩ	150kΩ	180kΩ	120kΩ	24kΩ	-
C2*(Note 7)*	22µF	22µF	22µF	22µF	22µF	10V, X5R, 3216
C4	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF	25V, X5R, 1608
C8*(Note 8)*	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF	-
C9	22µF	22µF	22µF	22µF	22µF	6.3V, X5R, 3225
C10	22µF	22µF	22µF	22µF	22µF	6.3V, X5R, 3225
C14	120pF	120pF	150pF	150pF	180pF	-
L1	1.0µH	1.0µH	1.0µH	1.0µH	1.0µH	TOKO, FDSD0630

Table 3. Recommended Component Values (V_{IN}=5V, FREQ=L)

Reference Designator	V_{OUT}					Description
	1.0V	1.2V	1.5V	1.8V	3.3V	
R5	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	-
R7	51kΩ	75kΩ	160kΩ	150kΩ	75kΩ	-
R8	200kΩ	150kΩ	180kΩ	120kΩ	24kΩ	-
C2*(Note 7)*	22µF	22µF	22µF	22µF	22µF	10V, X5R, 3216
C4	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF	25V, X5R, 1608
C8*(Note 8)*	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF	-
C9	22µF	22µF	22µF	22µF	22µF	6.3V, X5R, 3225
C10	22µF	22µF	22µF	22µF	22µF	6.3V, X5R, 3225
C14	100pF	100pF	120pF	120pF	120pF	-
L1	1.0µH	1.0µH	1.0µH	1.0µH	1.0µH	TOKO, FDSD0630

(Note 7) For capacitance of input capacitor take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 10µF.

(Note 8) For capacitance of bootstrap capacitor take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 0.047µF.

※Evaluation using the actual machine must be done for above constant is only a value on our evaluation board.

Selection of Components Externally Connected

1. Output LC Filter Constant

In order to supply a continuous current to the load, the DC/DC converter requires an LC filter for smoothing the output voltage. It is recommended to use inductors of values 0.47µH to 1.0µH when FREQ=L or 1.0µH to 1.5µH at FREQ=H.

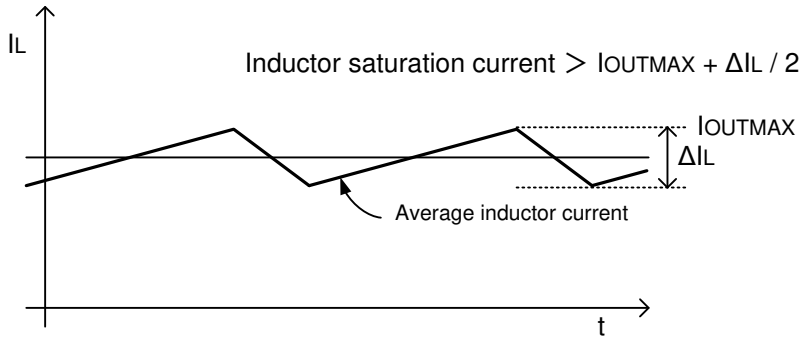


Figure 49. Waveform of current through inductor

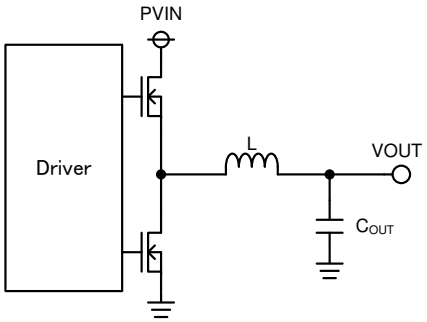


Figure 50. Output LC filter circuit

Inductor ripple current ΔIL

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{SW} \times L} = 912\ [\mathrm{mA}]$$

Where:
VIN= 5V
VOUT= 1.2V
L=1.0µH
fSW=1MHz (switching frequency)

The saturation current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current ΔIL.

The output capacitor COUT affects the output ripple voltage characteristics. The output capacitor COUT must satisfy the required ripple voltage characteristics.

The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}})[\mathrm{V}]$$

where RESR is the Equivalent Series Resistance (ESR) of the output capacitor.

* The capacitor rating must allow a sufficient margin with respect to the output voltage.
The output ripple voltage can be decreased with a smaller ESR.
A ceramic capacitor of about 22 µF to 47 µF is recommended.

*Be careful of total capacitance value, when additional capacitor CLOAD is connected in addition to output capacitor COUT.
Use maximum additional capacitor CLOAD (Max) condition which satisfies the following condition.

$$Maximum\,starting\ inductor\ bottom\ ripple\ current\ IL_{START}$$
$$< Low\ side\ FET\ Over\ Current\ limit\ 4.5A(min)$$

Maximum starting inductor ripple bottom current ILSTART can be expressed using the following equation.

$$IL_{START} = Maximum\ starting\ output\ current(I_{OMAX}) + Charge\ current\ to\ output\ capacitor(I_{CAP}) - \frac{\Delta I_L}{2}$$

Charge current to output capacitor I_{CAP} can be expressed using the following equation.

$$I_{CAP} = \frac{(C_{OUT} + C_{LOAD}) \times V_{OUT}}{T_{SS}} [A]$$

For example, given V_{IN}= 5V, V_{OUT}= 3.3V, L= 1.5µH, switching frequency f_{SW}= 1.2MHz(Max), Output capacitor C_{OUT}= 44µF, Soft Start time T_{SS}= 0.5ms(Min), and load current during soft start I_{OSS}= 4A, maximum C_{LOAD} can be computed using the following equation.

$$C_{LOAD}(max) < \frac{(4.5 - I_{OSS} + \Delta I_L/2) \times T_{SS}}{V_{OUT}} - C_{OUT} = 78.9 [\mu F]$$

If the value of C_{LOAD} is large, and cannot meet the above equation, adjust the value of the capacitor C_{SS} to meet the condition below.

$$C_{LOAD}(max) < \frac{(4.5 - I_{OSS} + \Delta I_L/2) \times V_{FB}}{V_{OUT} \times I_{SS}} \times C_{SS} - C_{OUT}$$

(Refer to the following items (3) Soft Start Setting equation of time T_{SS} and soft-start value of the capacitor to be connected to the C_{SS}.)

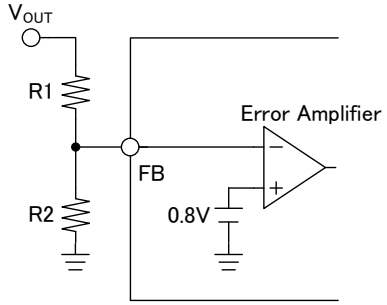
For example, given V_{IN} = 5V, V_{OUT} = 3.3V, L = 1.5µH, load current during soft start I_{OSS} = 4A, switching frequency f_{SW} = 1.2MHz (Max), Output capacitor C_{OUT} = 44µF, V_{FB} = 0.792V(Max), I_{SS} = 3.6µA(Max), with C_{LOAD} = 220uF, capacitor C_{SS} is computed as follows.

$$C_{SS} > \frac{V_{OUT} \times I_{SS}}{(4.5 - I_{OSS} + \Delta I_L/2) \times V_{FB}} \times (C_{LOAD} + C_{OUT}) = 2710 [pF]$$

※C_{LOAD} has an effect on the stability of the DC/DC converter.
To ensure the stability of the DC/DC converter, make sure that a sufficient phase margin is provided.

2. Output Voltage Setting

The output voltage value can be set by the feedback resistance ratio.
For stable operation, it is recommended to use feedback resistance R1 of more than 20kΩ.



$$V_{OUT} = \frac{R1 + R2}{R2} \times 0.8 [V]$$

$$R2 = \frac{0.8}{V_{OUT} - 0.8} \times R1 [\Omega]$$

Figure 51. Feedback Resistor Circuit

3. Soft Start Setting

Turning the EN terminal signal High activates the soft start function. This causes the output voltage to rise gradually while the current at startup is placed under control. This allows the prevention of output voltage overshoot and inrush current. The rise time depends on the value of the capacitor connected to the SS terminal.

$$T_{SS} = (C_{SS} \times V_{FB}) / I_{SS}$$

$$C_{SS} = (I_{SS} \times T_{SS}) / V_{FB}$$

T_{SS} : Soft Start Time

C_{SS} : Capacitor connected to Soft Start Time Terminal

V_{FB} : FB Terminal Voltage(0.8V (Typ))

I_{SS} : Soft Start Terminal Source Current (1.0μA(Typ))

with $C_{SS} = 0.01$ [μF],

$$T_{SS} = (0.01\ [\mu F] \times 0.8\ [V]) / 1.0\ [\mu F]$$

$$= 8.0\ [msec]$$

Turning the EN terminal signal High with the SS terminal open or with the terminal signal High (no capacitor connected) causes the output voltage to rise in 1msec (Typ).

4. FB Capacitor

Generally, in fixed ON time control (hysteresis control), sufficient ripple voltage in FB voltage is needed to operate comparator stably. Regarding this IC, by injecting ripple voltage to FB voltage inside IC it is designed to correspond to low ESR output capacitor. Please set the FB capacitor within the range of the following expression to inject an appropriate ripple.

$$\frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})}{f_{SW} \times 7.65 \times 10^{3}} < C_{FB} < \frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})}{f_{SW} \times 3.3 \times 10^{3}}$$

V_{IN} : Input Voltage

V_{OUT} : Output Voltage

f_{SW} : Switching Frequency

PCB Layout Design

In the step-down DC/DC converter, a large pulse current flows into two loops. The first loop is the one into which the current flows when the High-Side FET is turned ON. The flow starts from the input capacitor CIN, runs through the FET, inductor L and output capacitor COUT and back to GND of CIN via GND of COUT. The second loop is the one into which the current flows when the Low-Side FET is turned on. The flow starts from the Low-Side FET, runs through the inductor L and output capacitor COUT and back to GND of the Low-Side FET via GND of COUT. Route these two loops as thick and as short as possible to allow noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors directly to the GND plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

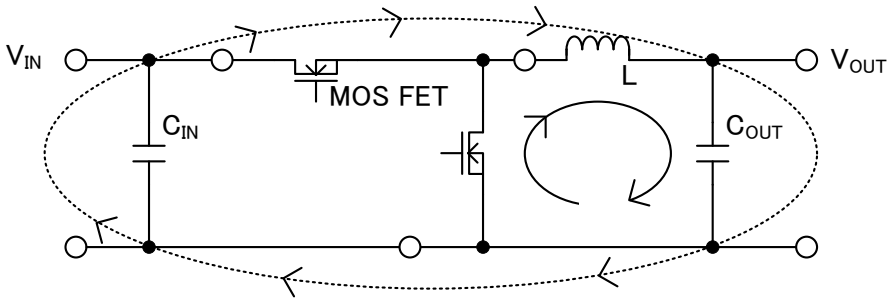
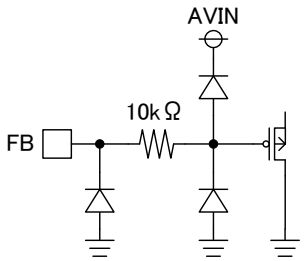
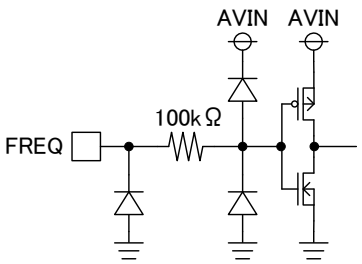
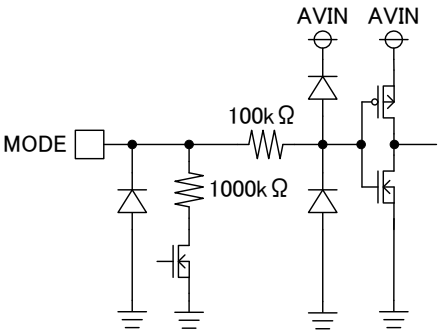
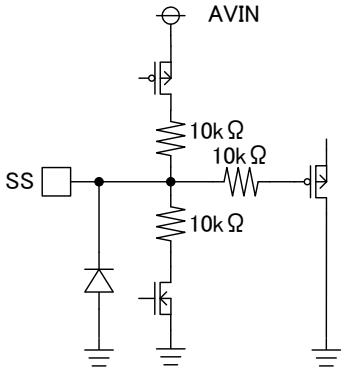
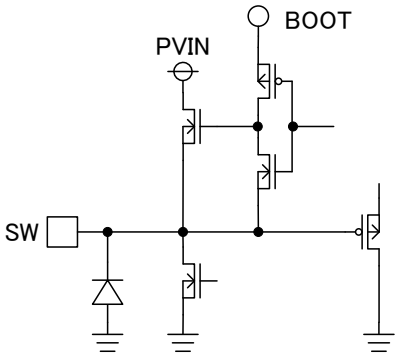
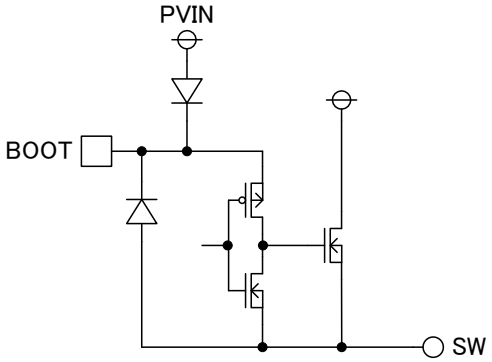


Figure 52. Current Loop of Buck Converter

Accordingly, design the PCB layout considering the following points.

- Connect an input capacitor as close as possible to the IC PVIN terminal on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the GND node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Provide lines connected to FB far from the SW nodes.
- Place the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.

I/O equivalence circuit(s)

6. FB	7. FREQ
	
8. MODE	**9. SS**
	
10.11.12. SW	**13. BOOT**
	
14. PGD	**15. EN**