Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

7.0V to 36V Input, 1.0 A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9E101FJ-LB

General Description

This is the product guarantees long time support in Industrial market.

BD9E101FJ-LB is a synchronous buck switching regulator with built-in power MOSFETs. It is capable of an output current of up to 1.0A. It is a current mode control DC/DC converter and features high-speed transient response. Phase compensation can also be set easily.

Features

- Long Time Support Product for Industrial Applications.
- Synchronous single DC/DC converter.
- Over-Current Protection.
- Short Circuit Protection.
- Thermal Shutdown Protection.
- Undervoltage Lockout Protection.
- Soft Start.
- SOP-J8 package.

Applications

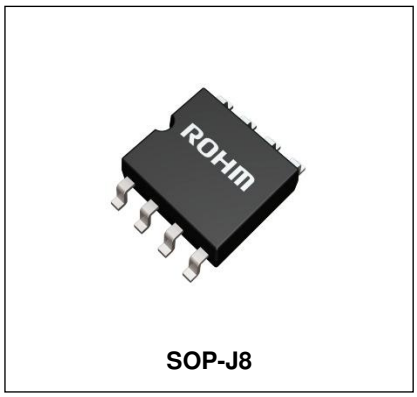
- Industrial Equipment.
- Power supply for FA's industrial device using 24V bass.
- Consumer applications such as home appliance. Distribution type power supply system for 12V, and 24V.

Key Specifications

- Input Voltage Range: 7.0V to 36V
- Output Voltage Range: 1.0V to $V_{IN} \times 0.7V$
- Output Current: 1.0A (Max)
- Switching Frequency: 570kHz (Typ)
- High-Side MOSFET ON-Resistance: 300mΩ (Typ)
- Low-Side MOSFET ON-Resistance: 300mΩ (Typ)
- Standby Current: 0μA (Typ)

Package

	W (Typ) x D (Typ) x H (Max)
SOP-J8	4.90mm x 6.00mm x 1.65mm



SOP-J8

Typical Application Circuit

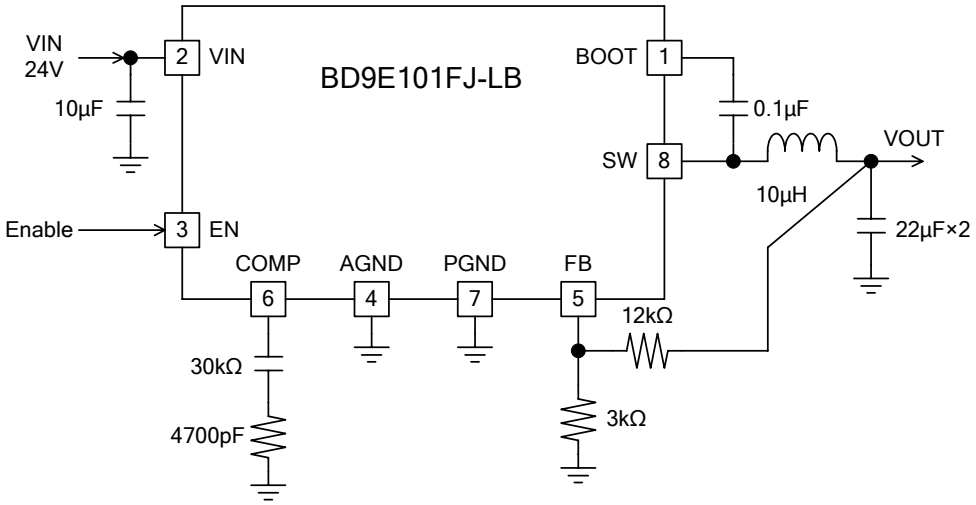


Figure 1. Application circuit

Pin Configuration

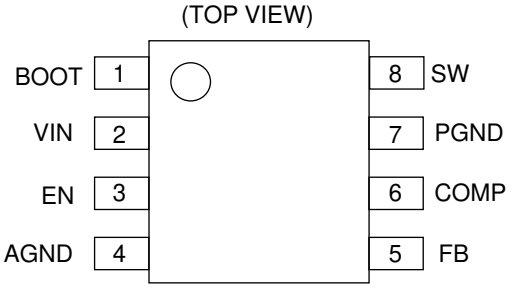


Figure 2. Pin assignment

Pin Description(s)

Pin No	Pin Name	Description
1	BOOT	Connect a bootstrap capacitor of 0.1µF between this terminal and SW terminal. The voltage of this capacitor is the gate drive voltage of the high-side MOSFET.
2	VIN	Power supply terminal for the switching regulator and control circuit. Connecting a 10µF ceramic capacitor is recommended.
3	EN	Turning this terminal signal low-level (0.8V or lower) forces the device to enter the shut down mode. Turning this terminal signal high-level (2.5V or higher) enables the device. This terminal must be terminated.
4	AGND	Ground terminal for the control circuit.
5	FB	Inverting input node for the gm error amplifier. See page 22 on how to calculate the resistance of the output voltage setting.
6	COMP	Input terminal for the gm error amplifier output and the output switch current comparator. Connect a frequency phase compensation component to this terminal. See page 23 on how to calculate the resistance and capacitance for phase compensation.
7	PGND	Ground terminal for the output stage of the switching regulator.
8	SW	Switch node. This terminal is connected to the source of the high-side MOSFET and drain of the low-side MOSFET. Connect a bootstrap capacitor of 0.1µF between this terminal and BOOT terminal. In addition, connect an inductor considering the direct current superimposition characteristic.

Block Diagram

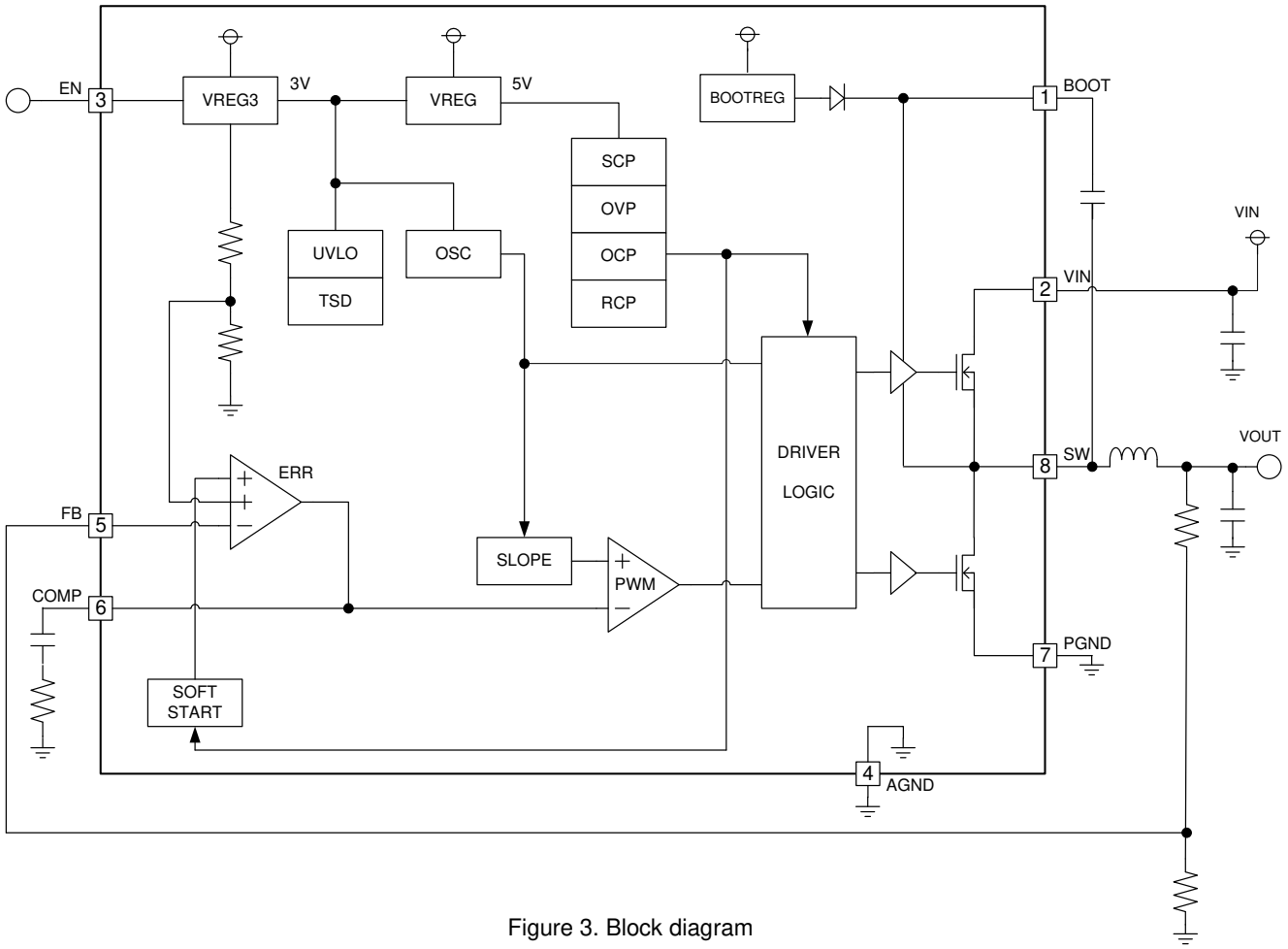


Figure 3. Block diagram

Description of Block

- VREG3
  Block creating internal reference voltage 3V (Typ).

- VREG
  Block creating internal reference voltage 5V (Typ).

- BOOTREG
  Block creating gate drive voltage.

- TSD
  This is the thermal shutdown block. Thermal shutdown circuit shuts down the whole system if temperature exceeds 175°C (Typ). When the temperature decreases, it returns to normal operation with hysteresis of 25°C (Typ).

- UVLO
  This is the under voltage lock-out block. IC shuts down when VIN is under 6.4V (Typ). The threshold voltage has a hysteresis of 200mV (Typ).

- ERR
  This circuit compares the feedback voltage at the output to the reference voltage. The output of this circuit is the COMP terminal voltage and this determines the switching duty. Also, because of soft start during start-up, COMP terminal voltage is controlled by internal slope voltage.

- OSC
  Block generating oscillation frequency.

- SLOPE
  This circuit creates a triangular wave from generated clock in OSC. The voltage converted from current sense signal of high side MOSFET and the triangular wave is sent to PWM comparator.

- PWM
  This block determines the switching duty by comparing the output COMP terminal voltage of error amplifier and output of SLOPE block.

- DRIVER LOGIC
  This is the DC/DC driver block. Input to this block is signal from PWM and output drives the MOSFETs.

- SOFT START
  This circuit prevents the overshoot of output voltage and In-rush current by forcing the output voltage to rise slowly, thus, avoiding surges in current during start-up.

- OCP
  This block limits the current flowing in high side MOSFET for each cycle of switching frequency during over-current.

- RCP
  This block limits the current flowing in low side MOSFET for each cycle of switching frequency during over-current.

- SCP
  The short circuit protection block compares the FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage has fallen below 0.85V (Typ) and remained in that state for 1.0msec (Typ), SCP activates and stops the operation for 16msec (Typ) and subsequently initiates a restart.

- OVP
  Over voltage protection function (OVP) compares FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage exceeds 1.30V (Typ), it turns output MOSFETs off. When output voltage drops until it reaches the hysteresis, it will return to normal operation.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}	-0.3 to +40	V
EN Input Voltage	V_{EN}	-0.3 to +40	V
Voltage from GND to BOOT	V_{BOOT}	-0.3 to +45	V
Voltage from SW to BOOT	ΔV_{BOOT}	-0.3 to +7	V
FB Input Voltage	V_{FB}	-0.3 to +7	V
COMP Input Voltage	V_{COMP}	-0.3 to +7	V
SW Input Voltage	V_{SW}	-0.5 to VIN + 0.3	V
Allowable Power Dissipation	Pd	0.67 (Note 1)	W
Operating Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) Derating in done 5.36 mW/°C for operating above Ta≧25°C (Mount on 1-layer 70.0mm x 70.0mm x 1.6mm board)

Caution1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution2: Reliability is decreased at junction temperature greater than 125°C.

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	V_{IN}	7.0	-	36	V
Output Current	I_{OUT}	0	-	1.0	A
Output Voltage Range	V_{RANGE}	1.0 (Note 2)	-	V_{IN} × 0.7	V

(Note 2) Please use it in I/O voltage setting of which output pulse width does not become 150nsec (Typ) or less. See the page 22 for how to calculate the resistance of the output voltage setting.

Electrical Characteristics (Unless otherwise specified V_{IN}=24V V_{EN}=3V Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply Current in Operating	I_{OPR}	-	1.5	2.5	mA	V_{FB} = 1.1V No switching
Supply Current in Standby	I_{STBY}	-	0	10	μA	V_{EN} = 0V
Reference Voltage	V_{FB}	0.98	1.00	1.02	V	
FB Input Current	I_{FB}	-1	0	1	μA	V_{FB} = 0V
Switching frequency	F_{OSC}	484	570	656	KHz	
Maximum Duty ratio	Maxduty	85	90	95	%	
High-side FET on-resistance	R_{ONH}	-	300	-	mΩ	I_{SW} = 100mA
Low-side FET on-resistance	R_{ONL}	-	300	-	mΩ	I_{SW} = 100mA
Over Current limit	I_{LIMIT}	-	3.0	-	A	
UVLO detection voltage	V_{UVLO}	6.1	6.4	6.7	V	V_{IN} falling
UVLO hysteresis voltage	$V_{UVLOHYS}$	100	200	300	mV	
EN high-level input voltage	V_{ENH}	2.5	-	V_{IN}	V	
EN low-level input voltage	V_{ENL}	-	-	0.8	V	
EN Input current	I_{EN}	2.1	4.2	8.4	μA	V_{EN} = 3V
Soft Start time	T_{SS}	1.5	3.0	6.0	msec	EN rising to FB=0.85V

- V_{FB} : FB Input Voltage. V_{EN} : EN Input Voltage.
- Pd should not be exceeded.

Typical Performance Curves

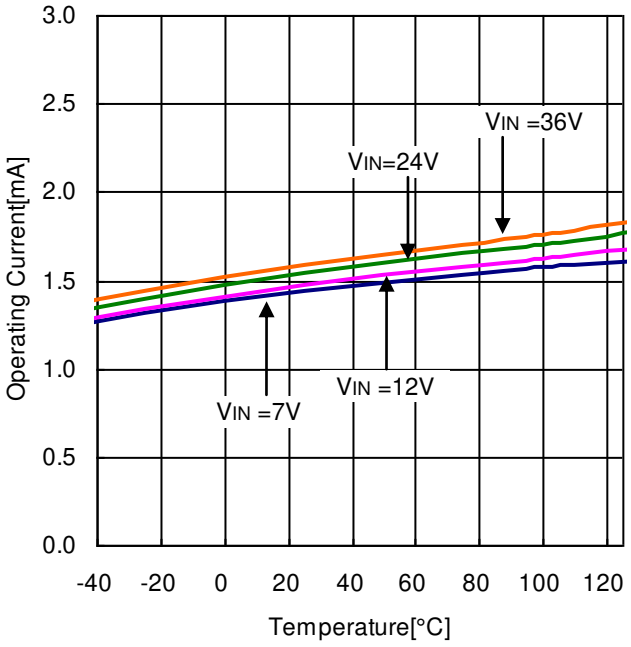


Figure 4. Operating Current vs Junction Temperature

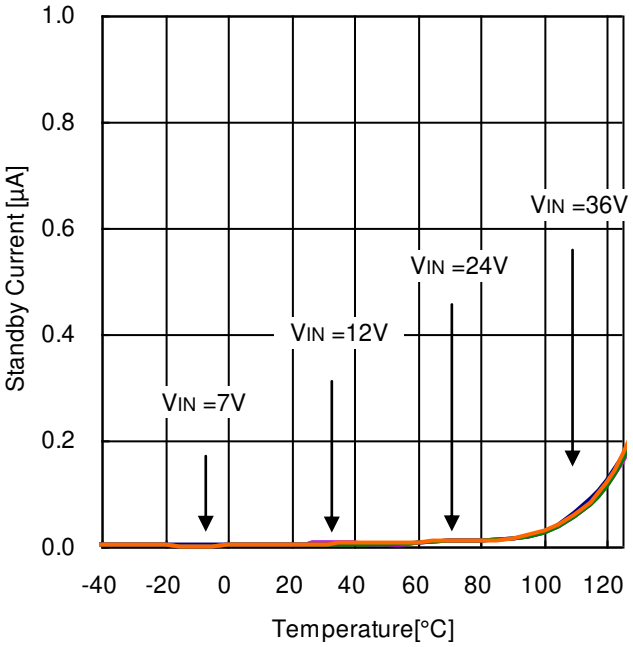


Figure 5. Stand-by Current vs Junction Temperature

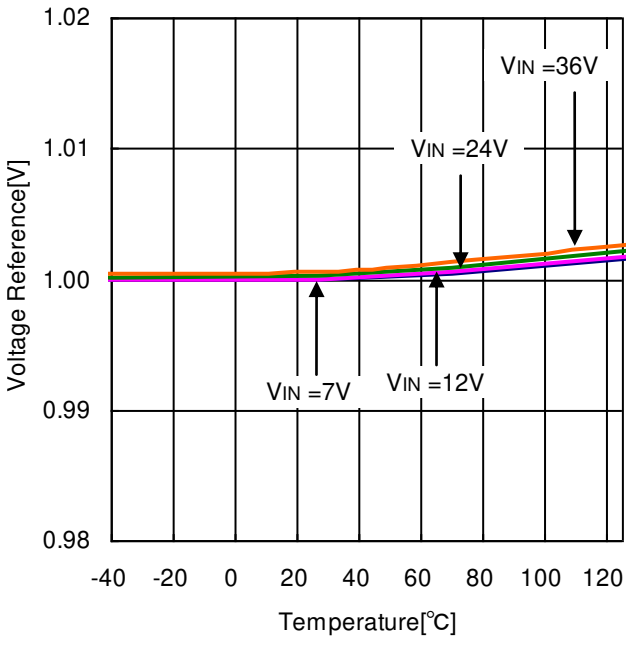


Figure 6. FB Voltage Reference vs Junction Temperature

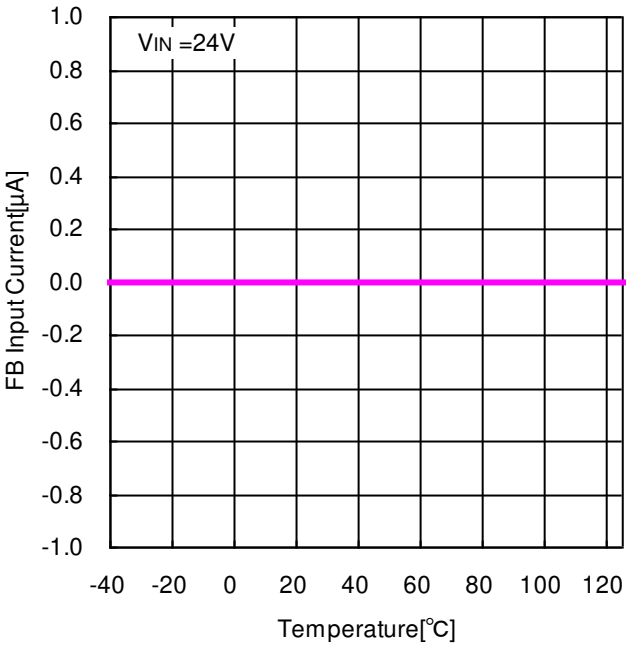


Figure 7. FB Input Current vs Junction Temperature

Typical Performance Curves - continued

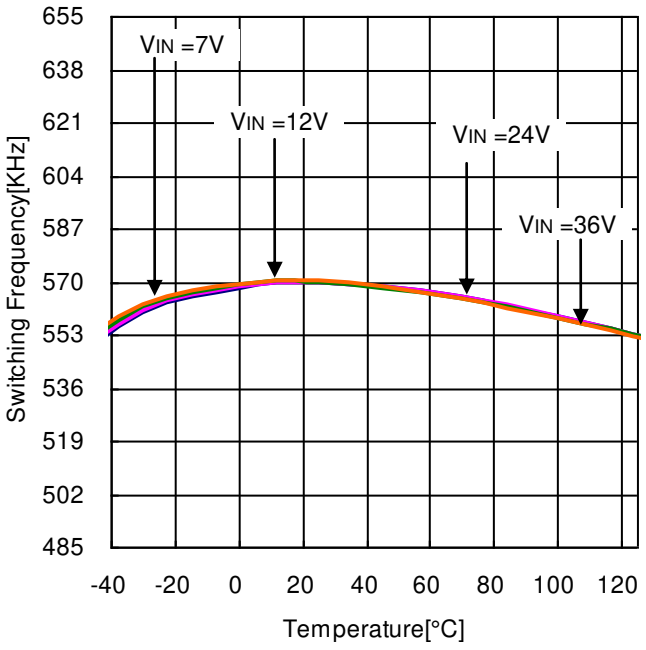


Figure 8. Switching Frequency vs Junction Temperature

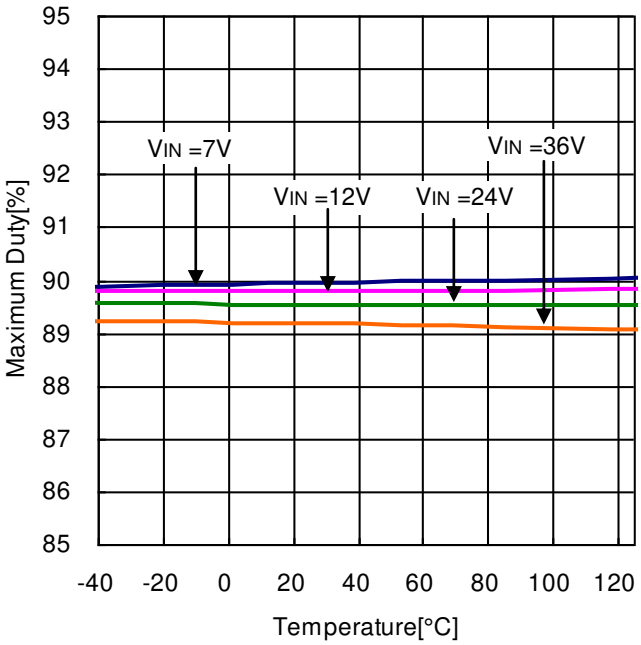


Figure 9. Maximum Duty vs Junction Temperature

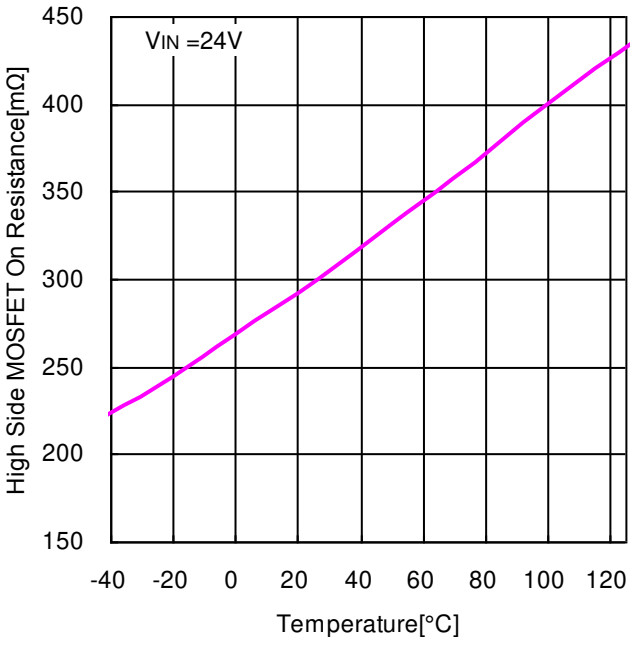


Figure 10. High Side MOSFET ON - Resistance vs Junction Temperature

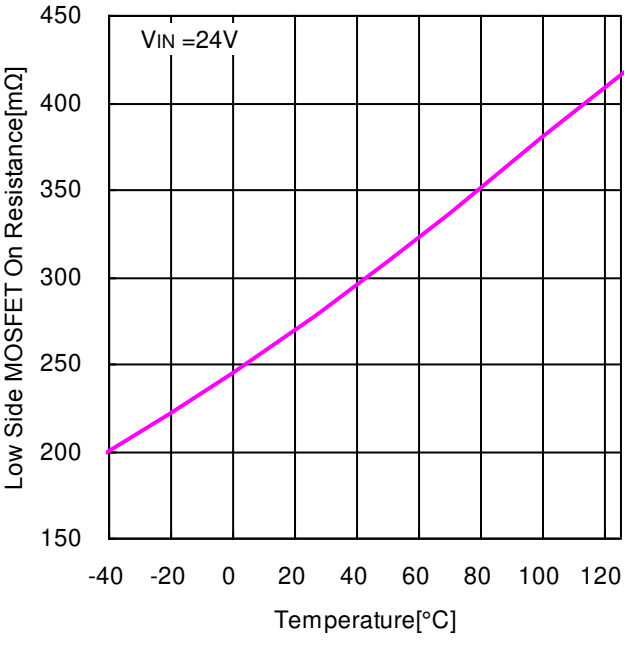


Figure 11. Low Side MOSFET ON -Resistance vs Junction Temperature

Typical Performance Curves - continued

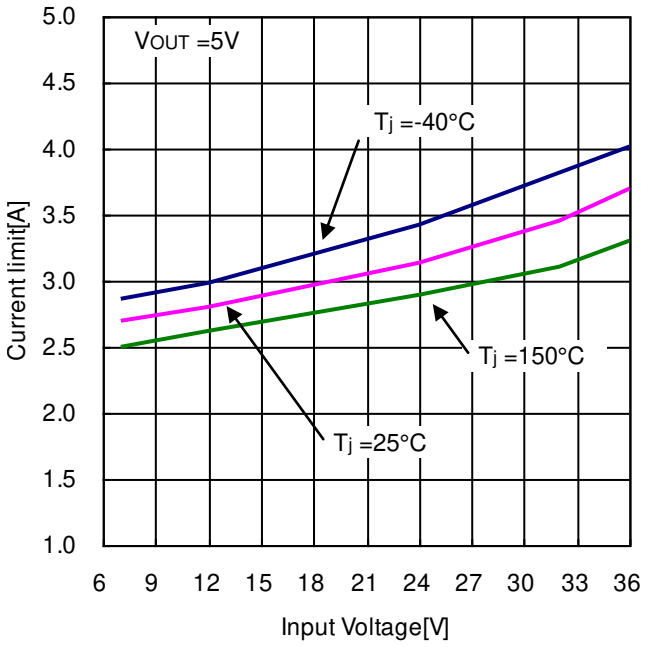


Figure 12. Current Limit vs Input Voltage

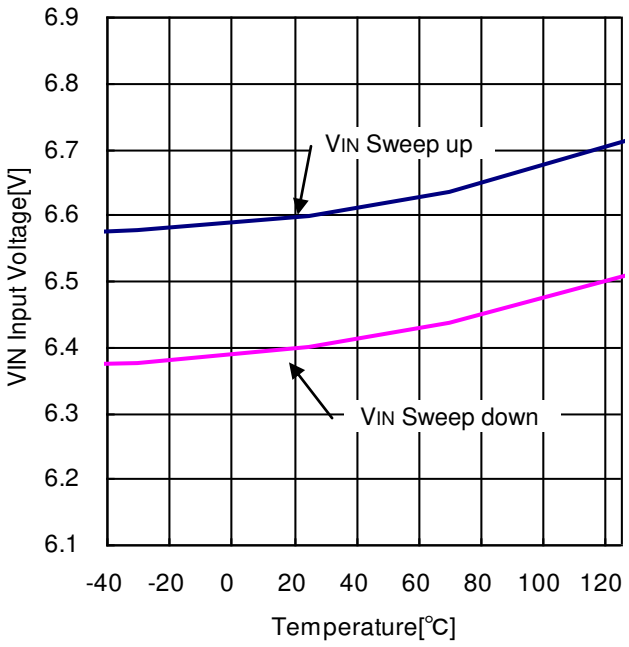


Figure 13. UVLO Threshold vs Junction Temperature

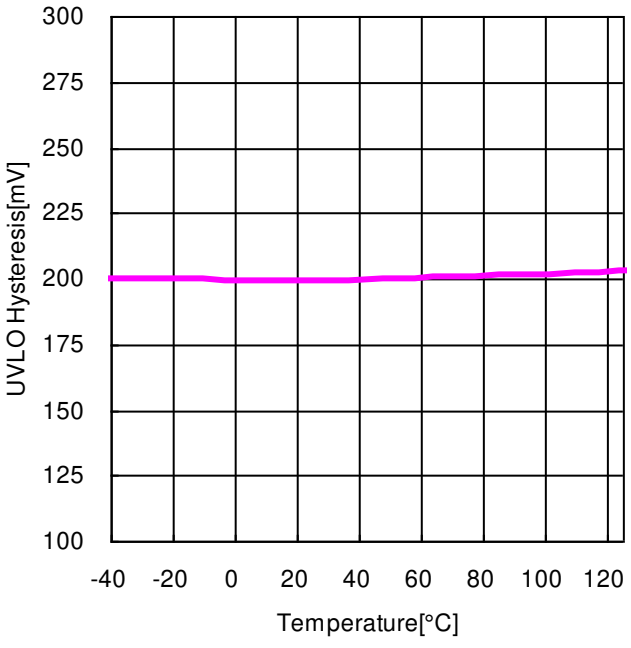


Figure 14. UVLO Hysteresis vs Junction Temperature

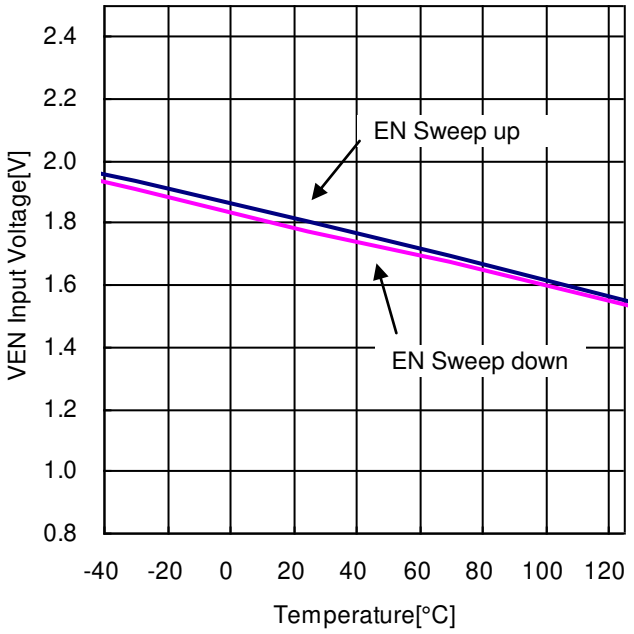


Figure 15. EN Threshold vs Junction Temperature

Typical Performance Curves - continued

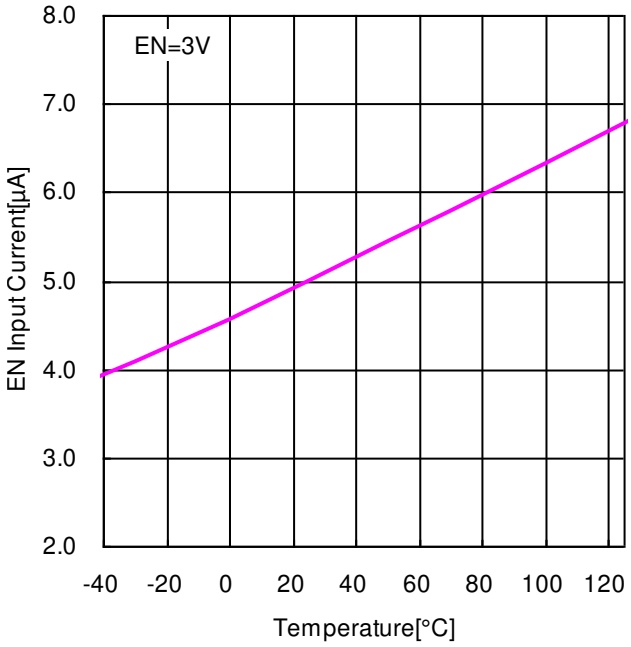


Figure 16. EN Input Current vs Junction Temperature

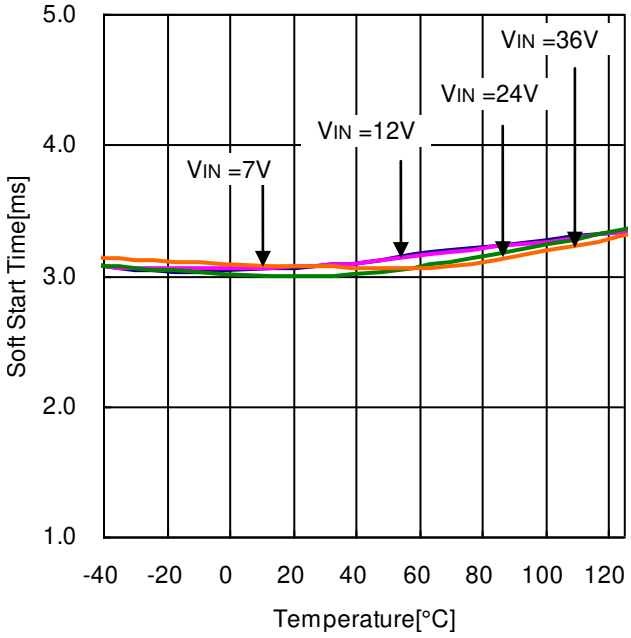


Figure 17. Soft Start Time vs Junction Temperature

Typical Performance Curves - continued

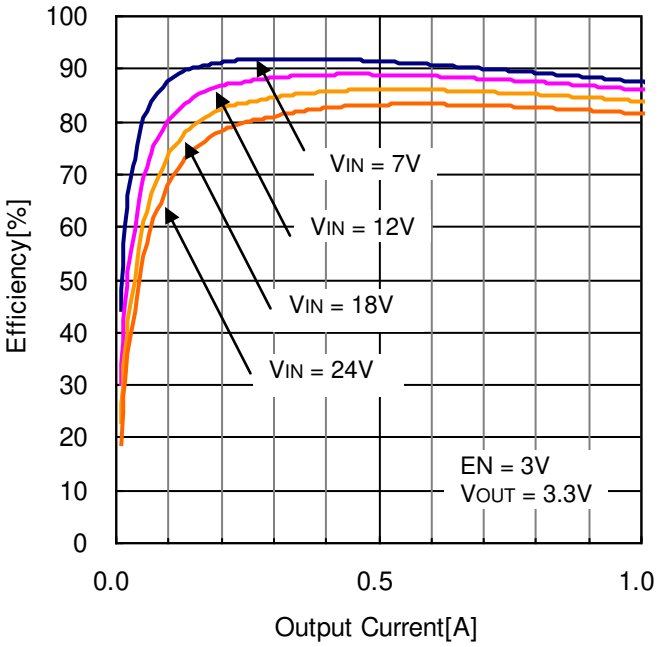


Figure 18. Efficiency vs Output Current
(VOUT = 3.3V, L=10µH)

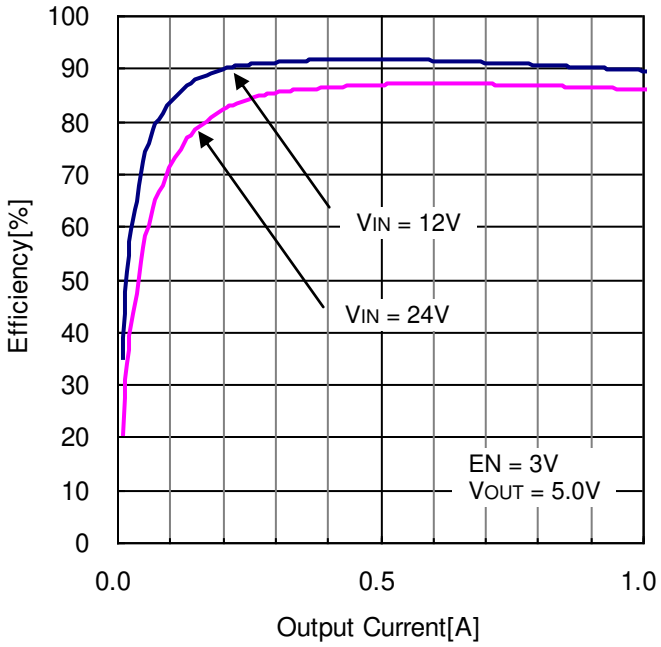


Figure 19. Efficiency vs Output Current
(VOUT = 3.3V, L=10µH)

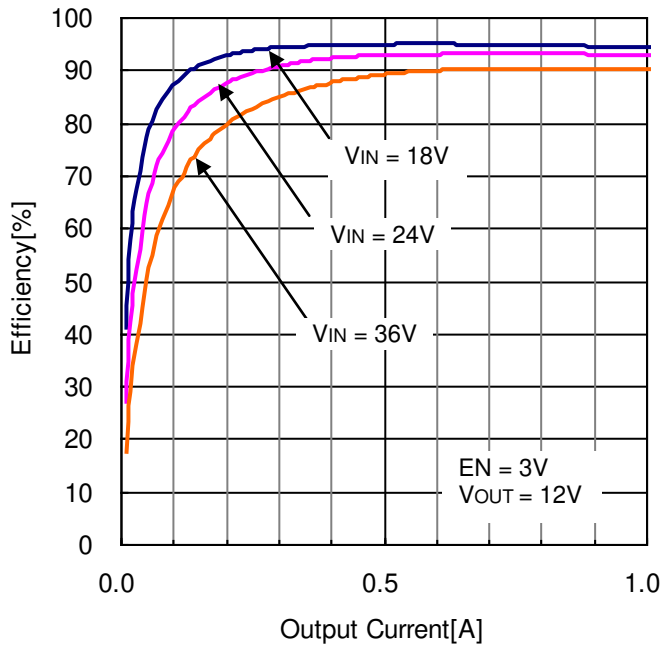


Figure 20. Efficiency vs Output Current
(VOUT = 12V, L=10µH)

Typical Performance Curves - continued

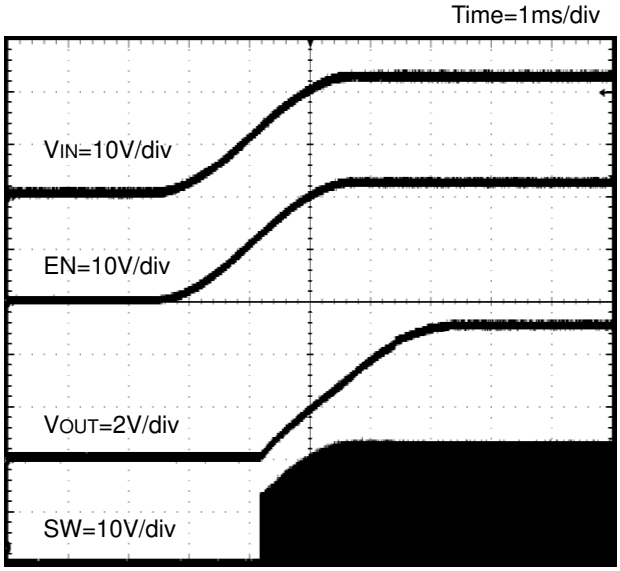


Figure 21. Power Up (VIN = EN)
(VOUT = 5.0V)

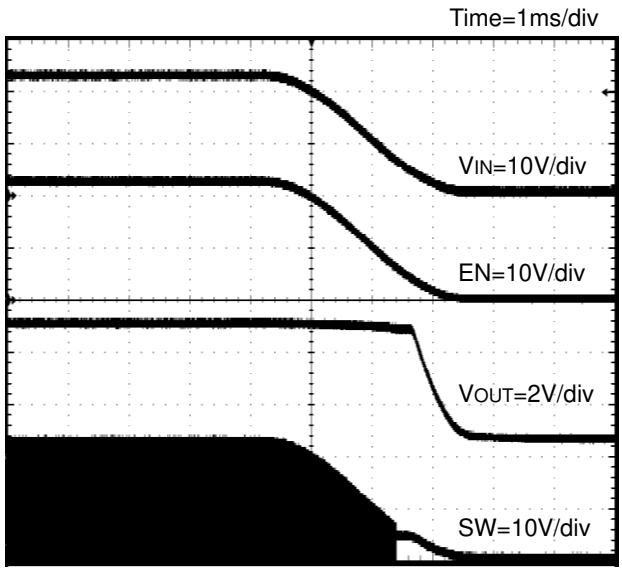


Figure 22. Power Down (VIN = EN)
(VOUT = 5.0V)

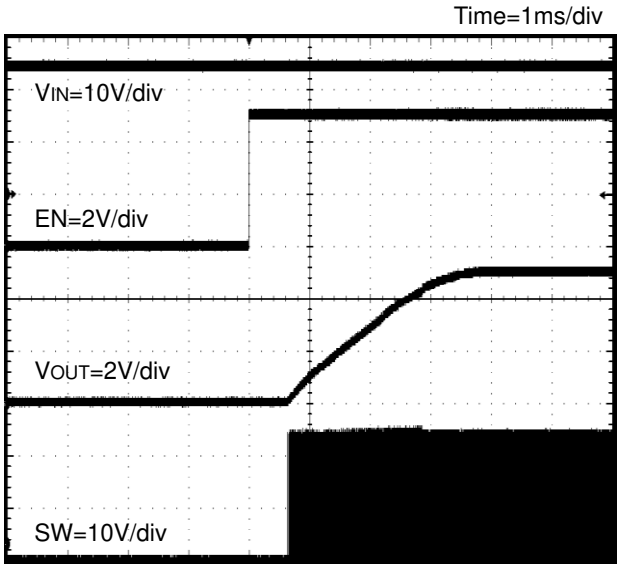


Figure 23. Power Up (EN = 0V→5V)
(VOUT = 5.0V)

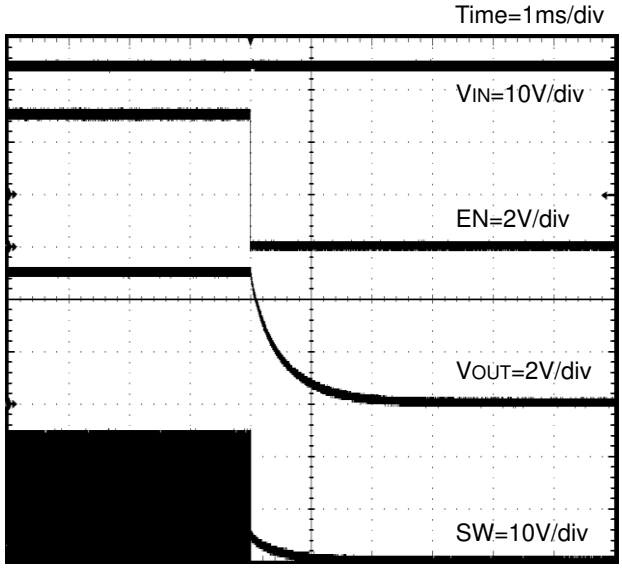


Figure 24. Power Down (EN = 5V→0V)
(VOUT = 5.0V)

Typical Performance Curves - continued

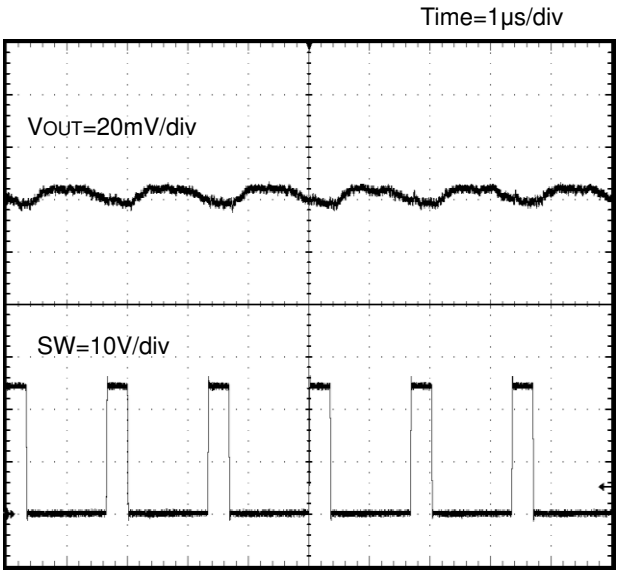


Figure 25. VOUT Ripple
(VIN = 24V, VOUT = 5V, IOUT = 0A)

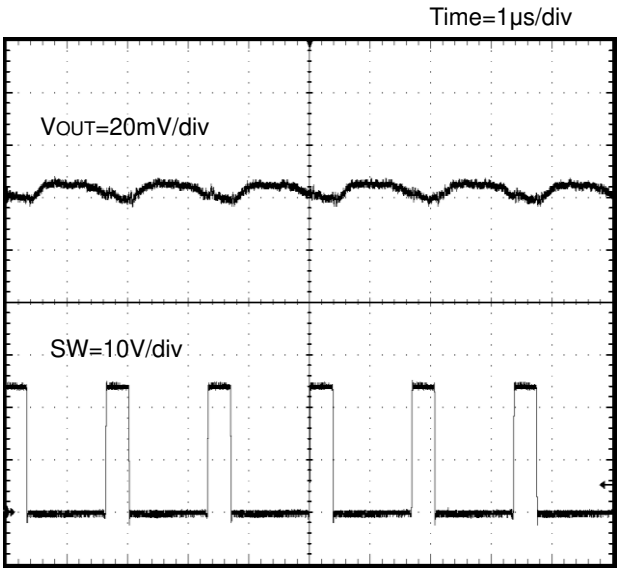


Figure 26. VOUT Ripple
(VIN = 24V, VOUT = 5V, IOUT = 1.0A)

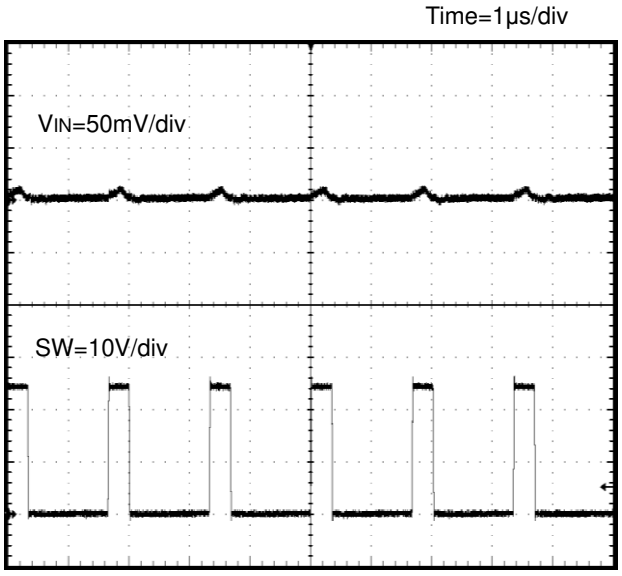


Figure 27. VIN Ripple
(VIN = 24V, VOUT = 5V, IOUT = 0A)

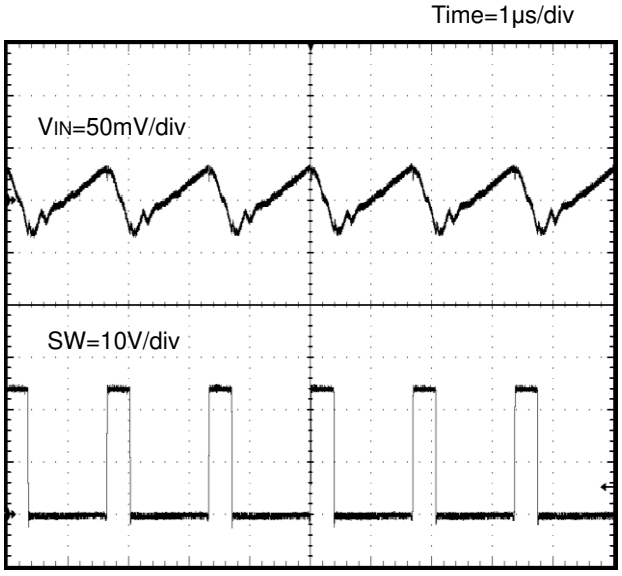


Figure 28. VIN Ripple
(VIN = 24V, VOUT = 5V, IOUT = 1.0A)

Typical Performance Curves - continued

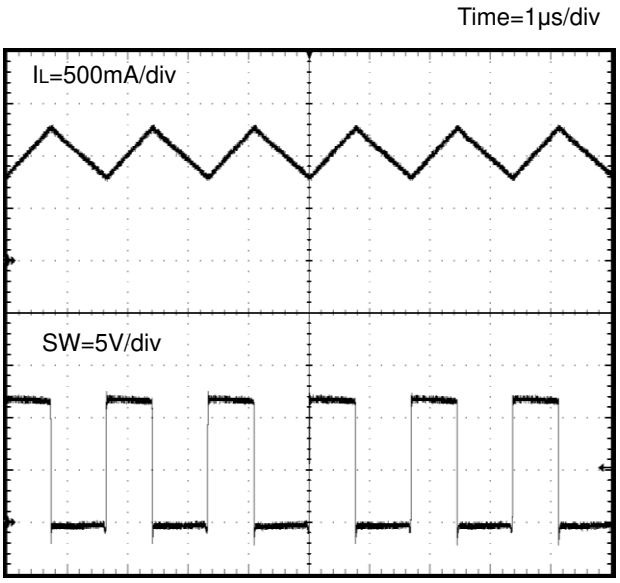


Figure 29. Switching Waveform
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.0A)

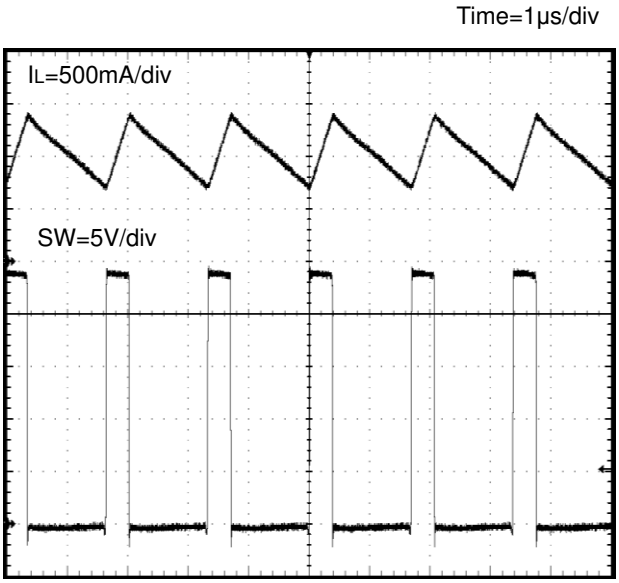


Figure 30. Switching Waveform
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1.0A)

Typical Performance Curves - continued

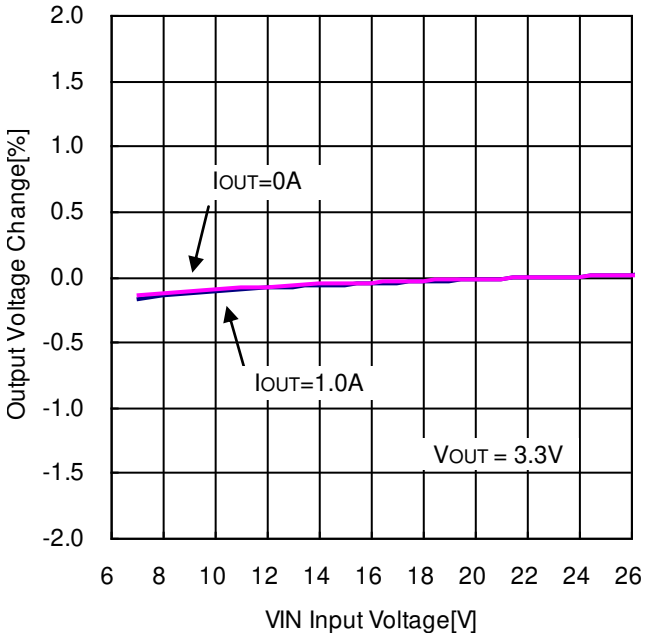


Figure 31. VOUT Line Regulation

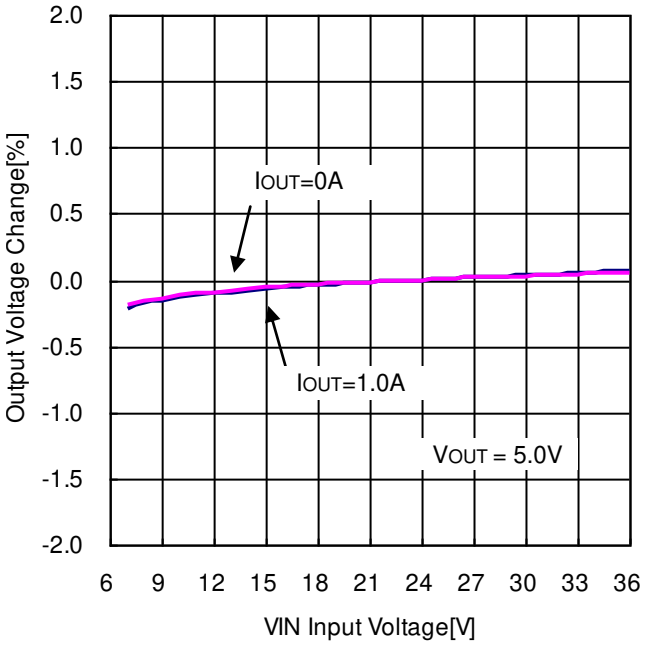


Figure 32. VOUT Line Regulation

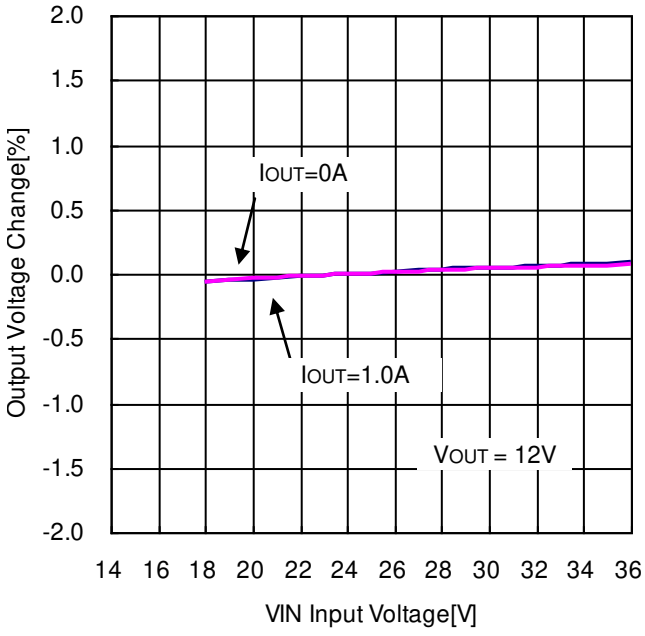


Figure 33. VOUT Line Regulation

Typical Performance Curves - continued

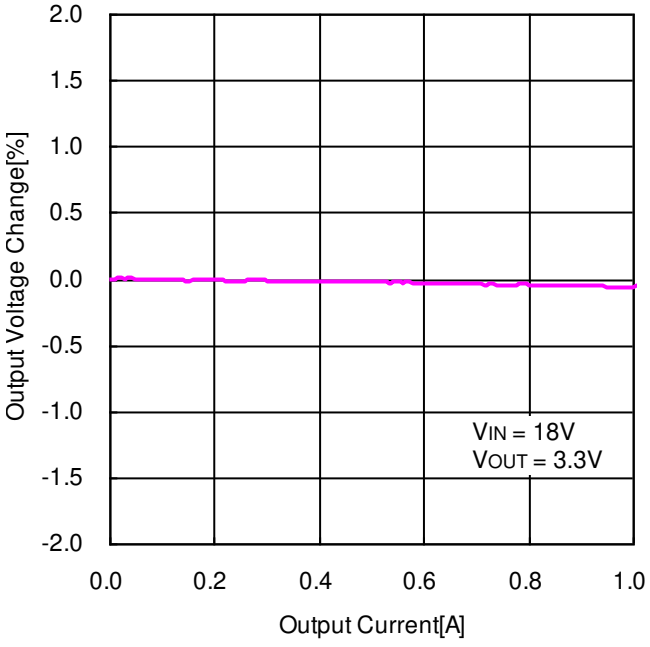


Figure 34. VOUT Load Regulation

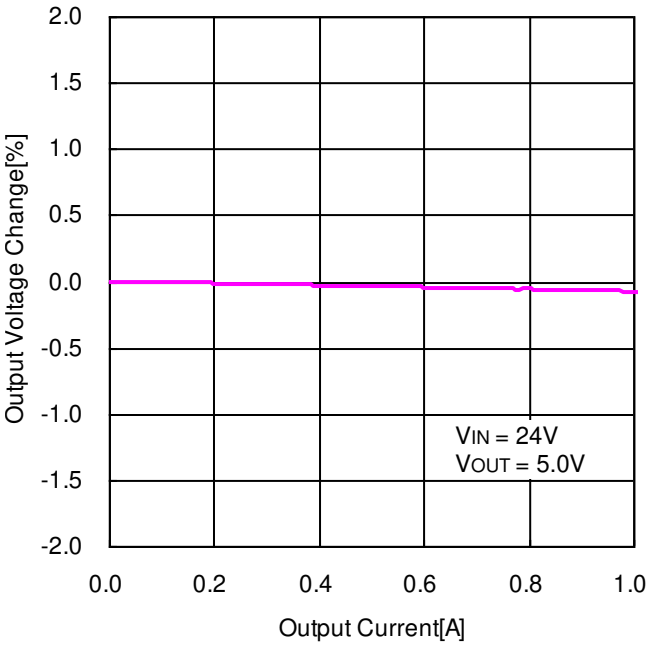


Figure 35. VOUT Load Regulation

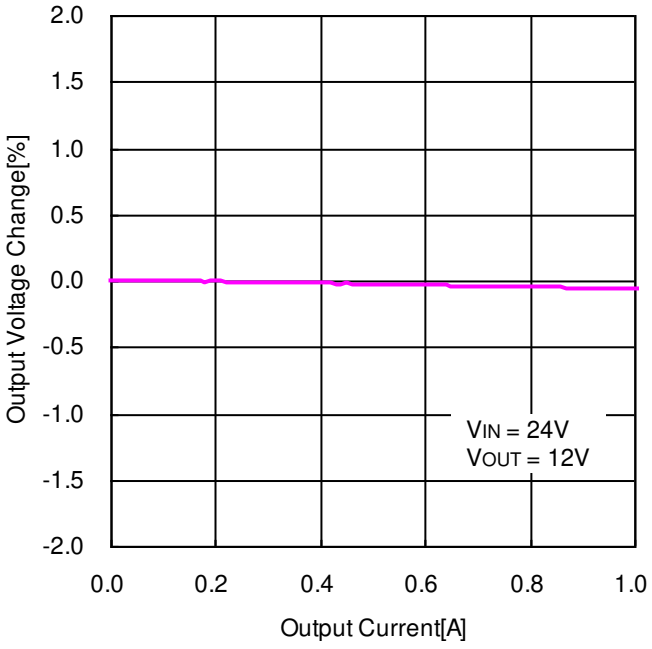


Figure 36. VOUT Load Regulation

Typical Performance Curves – continued

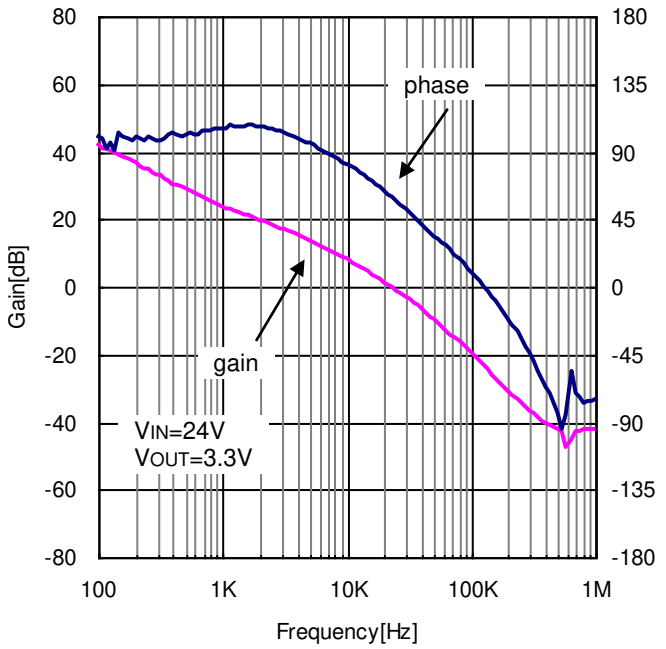


Figure 37. Loop Response
(VIN=12V, VOUT=3.3V, IOUT=1.0A, COUT=Ceramic22μF×2)

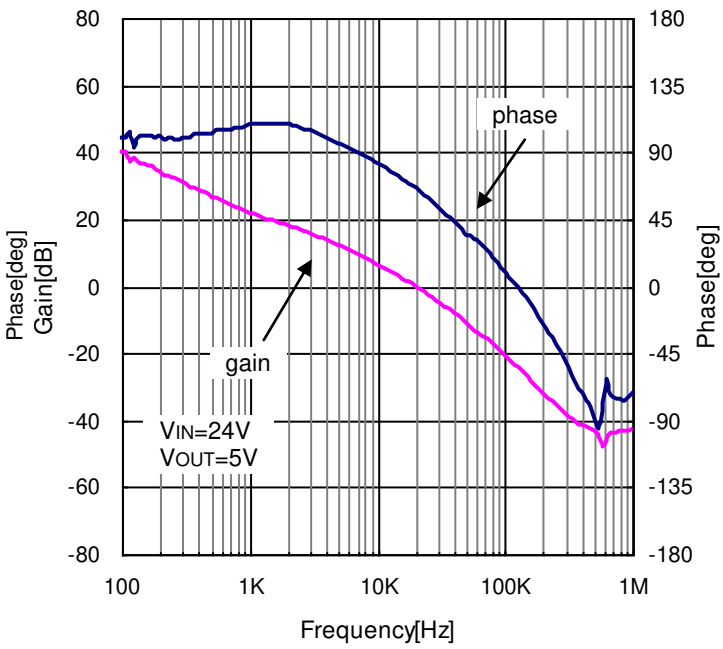


Figure 38. Loop Response
(VIN=24V, VOUT=5V, IOUT=1.0A, COUT=Ceramic22μF×2)

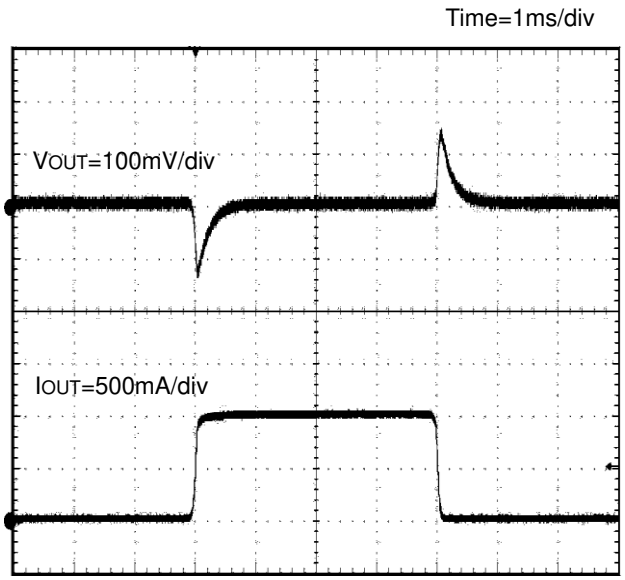


Figure 39. Load Transient Response IOUT=0A – 1.0A
(VIN=12V, VOUT=3.3V, COUT=Ceramic22μF×2)

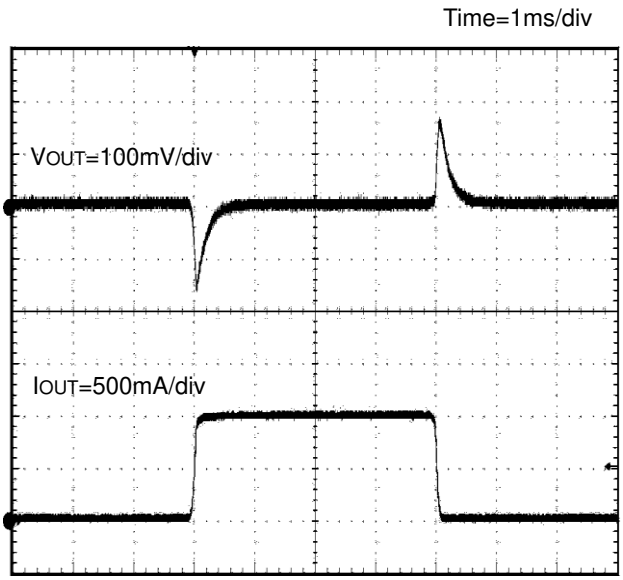


Figure 40. Load Transient Response IOUT=0A – 1.0A
(VIN=24V, VOUT=5.0V, COUT=Ceramic22μF×2)

Function Description

1. Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When EN voltage reaches 2.5V (Typ), the internal circuit is activated and the IC starts up. Setting the shutdown interval (Low Level interval) of EN to 100µs or longer will enable the shutdown control with the EN terminal.

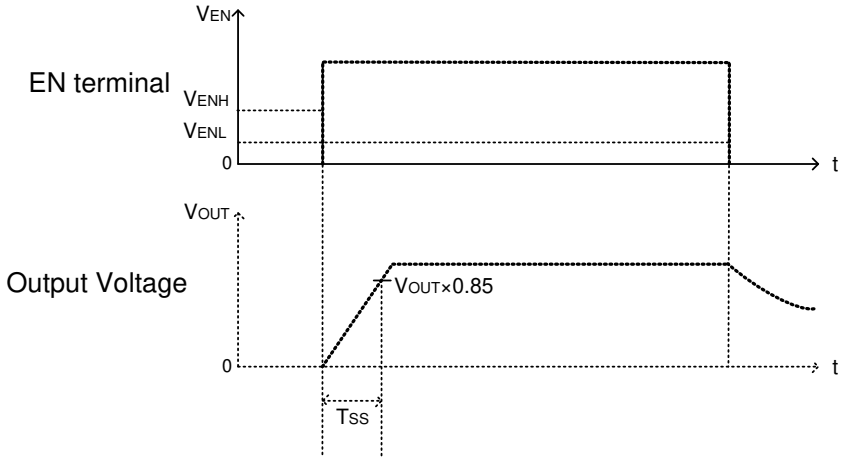


Figure 41. Timing Chart with Enable Control

2. Protective Functions

The protective circuits are intended for the prevention of damages caused by unexpected accidents. Do not use them for continuous protective operation.

(1) Short Circuit Protection (SCP)

The short circuit protection block compares the FB terminal voltage with the internal reference voltage VREF. When the FB terminal voltage has fallen below 0.85V (Typ) and remained in that state for 1.0msec (Typ), SCP activates and stops the operation for 16msec (Typ) and subsequently initiates a restart.

Table 1. Short Circuit Protection Function

EN pin	FB pin	Short circuit protection	Switching Frequency
2.5V or higher	0.30V (Typ)≧FB	Enabled	142.5kHz (Typ)
	0.30V (Typ)＞B≧0.85V (Typ)		285kHz (Typ)
	FB＞0.85V (Typ)		570kHz (Typ)
0.8V or lower	-	Disabled	OFF

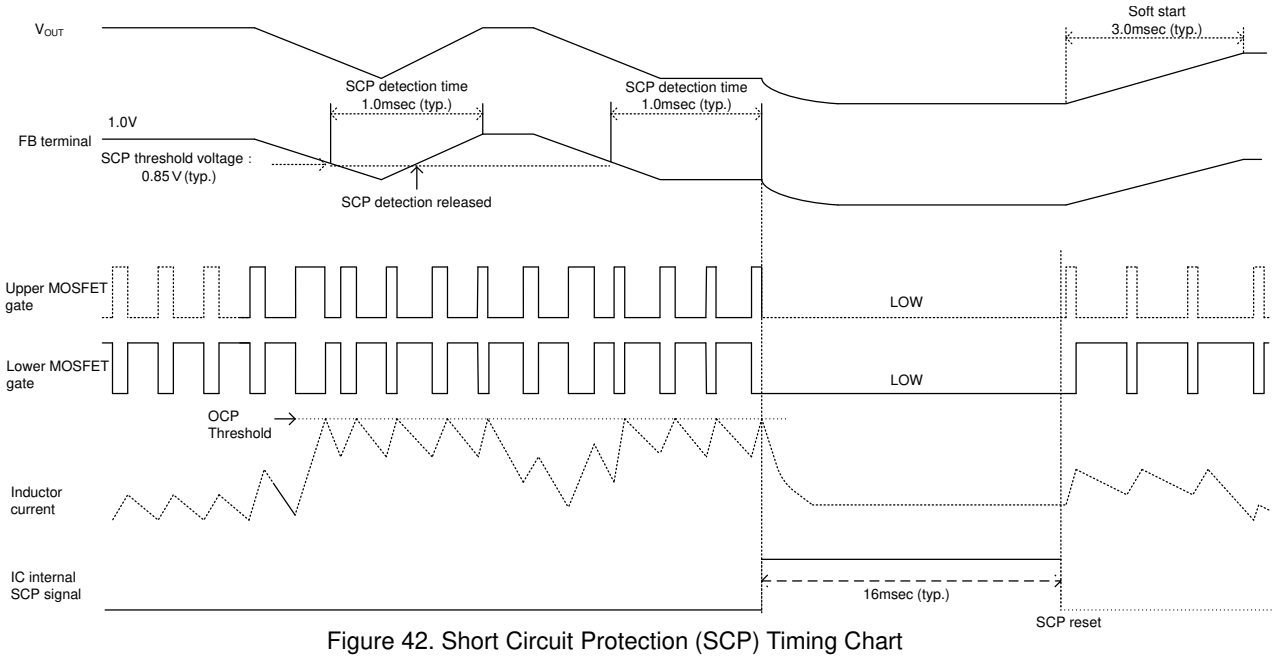


Figure 42. Short Circuit Protection (SCP) Timing Chart

(2) Under Voltage Lockout Protection (UVLO)

The under voltage lockout protection circuit monitors the VIN terminal voltage.
The operation enters standby when the VIN terminal voltage is 6.4V (Typ) or lower.
The operation starts when the VIN terminal voltage is 6.6V (Typ) or higher.

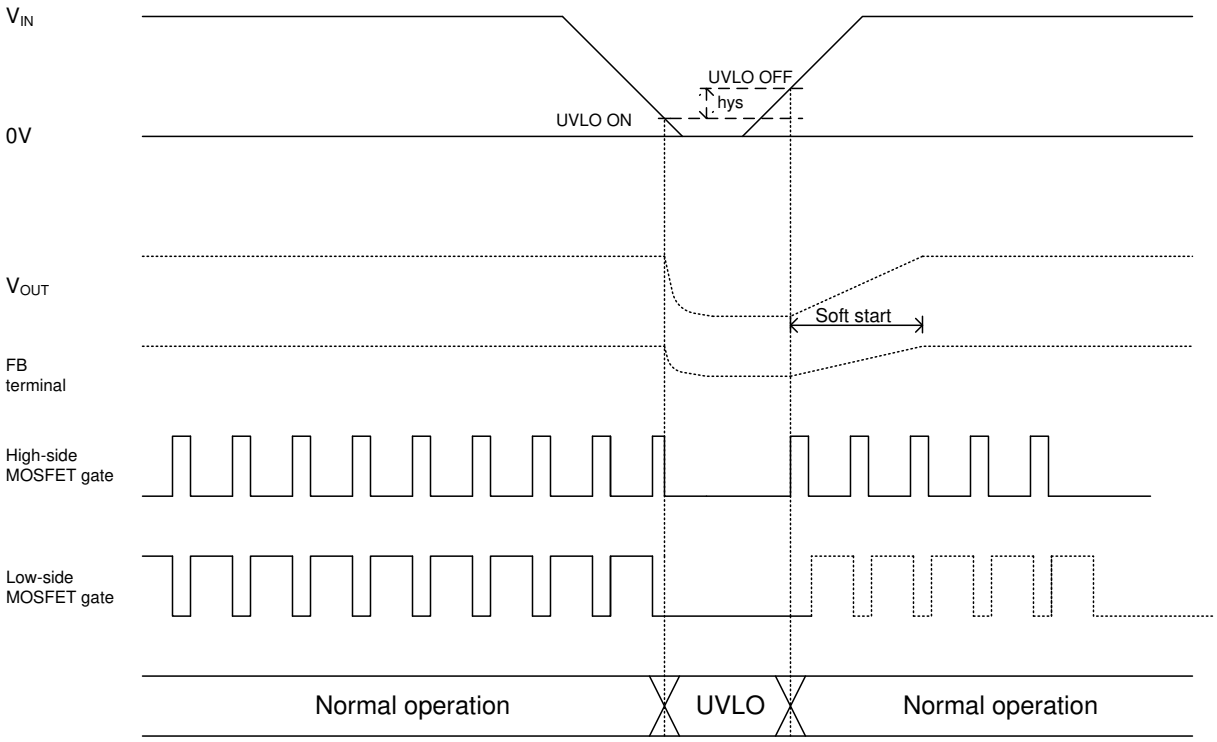


Figure 43. UVLO Timing Chart

(3) Thermal Shutdown (TSD)

When the chip temperature exceeds Tj = 175°C, the DC/DC converter output is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding Tjmax = 150°C. It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.

(4) Over Current Protection (OCP)

The over-current protection function is realized by using the current mode control to limit the current that flows through the high-side MOSFET at each cycle of the switching frequency.

(5) Reverse Current Protection (RCP)

The reverse current protection function is realized by using the current mode control to limit the current that flows through the low-side MOSFET at each cycle of the switching frequency.

(6) Over Voltage Protection (OVP)

Over voltage protection function (OVP) compares FB terminal voltage with internal standard voltage VREF. When the FB terminal voltage exceeds 1.30V (Typ), it turns output MOSFETs off. When output voltage drops until it reaches the hysteresis, it will return to normal operation.

Application Example

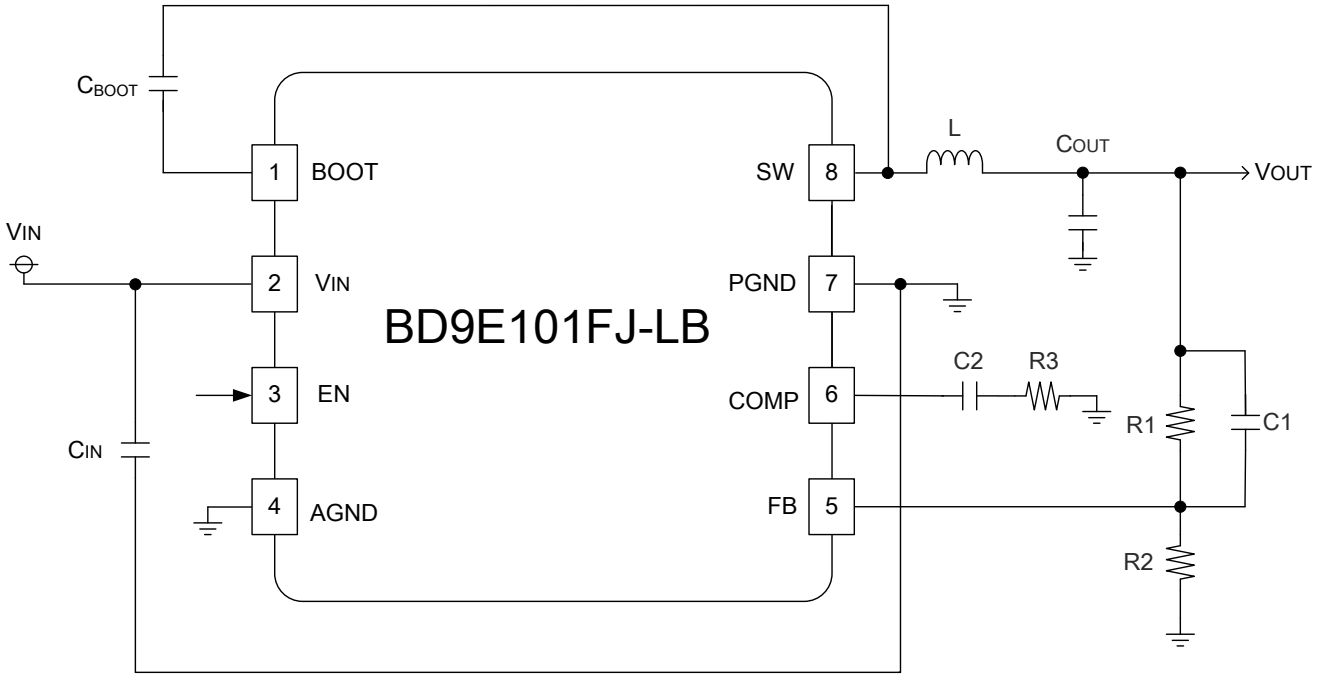


Figure 44. Application Circuit

Table 2. Recommendation Component Valves

VIN	12V			24V		
VOUT	3.3V			5V		
CIN	10µF	10µF	10µF	10µF	10µF	10µF
CBOOT	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF
L	6.8µH	6.8µH	6.8µH	10µH	10µH	10µH
R1	6.8kΩ	6.8kΩ	6.8kΩ	12kΩ	12kΩ	12kΩ
R2	3.0kΩ	3.0kΩ	3.0kΩ	3.0kΩ	3.0kΩ	3.0kΩ
R3	24kΩ	24kΩ	24kΩ	30kΩ	30kΩ	30kΩ
C1	-	-	-	-	-	-
C2	6800pF	6800pF	6800pF	4700pF	4700pF	4700pF
COUT	Ceramic 22µF×2	Ceramic 10µF×3	Ceramic 10µF and Aluminum 100µF	Ceramic 22µF×2	Ceramic 10µF×3	Ceramic 10µF and Aluminum 100µF

Selection of Components Externally Connected

1. Output LC Filter

The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. Selecting an inductor with a large inductance causes the ripple current ΔIL that flows into the inductor to be small, decreasing the ripple voltage generated in the output voltage, but it is not advantageous in terms of the load transient response characteristic. Selecting an inductor with a small inductance improves the transient response characteristic but causes the inductor ripple current to be large, which increases the ripple voltage in the output voltage, showing a trade-off relationship. Here, select an inductance so that the size of the ripple current component of the inductor will be 20% to 50% of the average output current (average inductor current).

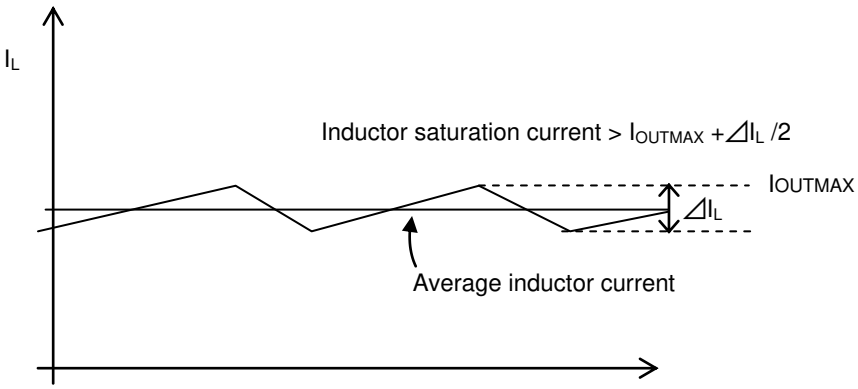


Figure 45. Waveform of current through inductor

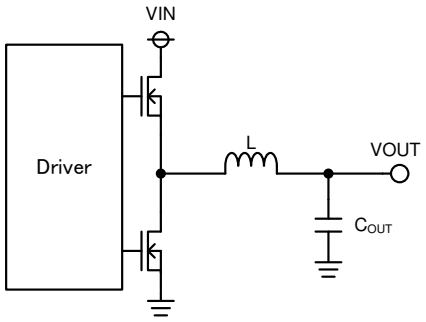


Figure 46. Output LC filter circuit

Computation with VIN = 24V, VOUT = 5V, L = 10μH, switching frequency FOSC = 570kHz, the method is as below.

Inductor ripple current

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times L} = 694 \text{ [mA]}$$

where :

ΔI_L is the inductor ripple current

F_{OSC} is the swithing frequency

L is the inductor

V_{IN} is the input voltage

V_{OUT} is the output voltage

Also for saturation current of inductor, select the one with larger current than maximum output current added by 1/2 of inductor ripple current ΔIL.

Output capacitor COUT affects output ripple voltage characteristics. Select output capacitor COUT so that necessary ripple voltage characteristics are satisfied.

Output ripple voltage can be expressed in the following method.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}}) \text{ [V]}$$

where :

ΔV_{RPL} is the output ripple voltage

R_{ESR} is the serial equivalent series resistance

C_{OUT} is the output capacitor

With COUT = 44μF, RESR = 10mΩ the output ripple voltage is calculated as

$$\Delta V_{RPL} = 0.69 \times (10m + \frac{1}{8 \times 44\mu \times 570k}) = 10.3 \text{ [mV]}$$

* When selecting the value of the output capacitor COUT, please note that the value of capacitor CLOAD will add up to the value of COUT to be connected to VOUT.
Charging current to flow through the CLOAD, COUT and the IC startup, must be completed within the soft-start time this charge. Over-current protection circuit operates when charging is continued beyond the soft-start time, the IC may not start. Please consider in the calculation the condition that the lower maximum value capacitor CLOAD that can be connected to VOUT (max) is other than COUT.

Inductor ripple current maximum value of start-up (ILSTART) < Over Current Protection Threshold 1.8 [A](min)

Inductor ripple current maximum value of start-up (ILSTART) can be expressed in the following method.

ILSTART = Output maximum load current(IOMAX) + Charging current to the output capacitor (ICAP) + $\frac{\Delta I_L}{2}$ [mV]

Charging current to the output capacitor (ICAP) can be expressed in the following method.

$$I_{CAP} = \frac{(C_{OUT} + C_{LOAD}) \times V_{OUT}}{T_{SS}} \text{ [A]}$$

where :

C_{OUT} is the output capacitance

C_{LOAD} is the output load capacitance

T_{SS} is the soft start time

From the above equation, VIN = 24V, VOUT = 5V, L = 10µH, IOMAX = 1.0A (max), switching frequency FOSC = 484kHz (min), the output capacitor COUT = 44µF, TSS = 1.5ms soft-start time (min), it becomes the following equation when calculating the maximum output load capacitance CLOAD (max) that can be connected to VOUT.

$$C_{LOAD}(max) < \frac{(1.8 - I_{OMAX} - \Delta I_L/2) \times T_{SS}}{V_{OUT}} - C_{OUT} = 73 \text{ [µF]}$$

2. Output Voltage Set Point

The output voltage value can be set by the feedback resistance ratio.

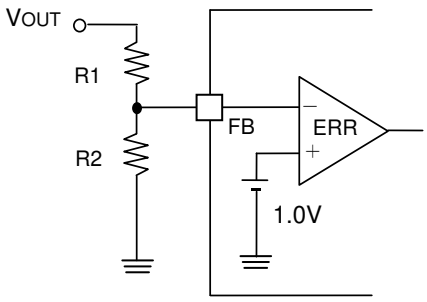


Figure 47. Feedback Resistor Circuit

$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times 1.0 \text{ [V]}$$

※ Minimum pulse range that can be produced at the output stably through all the load area is 150nsec for BD9E101FJ-LB.
Use input/output condition which satisfies the following method.

$$150(nsec) \leq \frac{V_{OUT}}{V_{IN} \times F_{OSC}}$$

3. Input voltage start-up

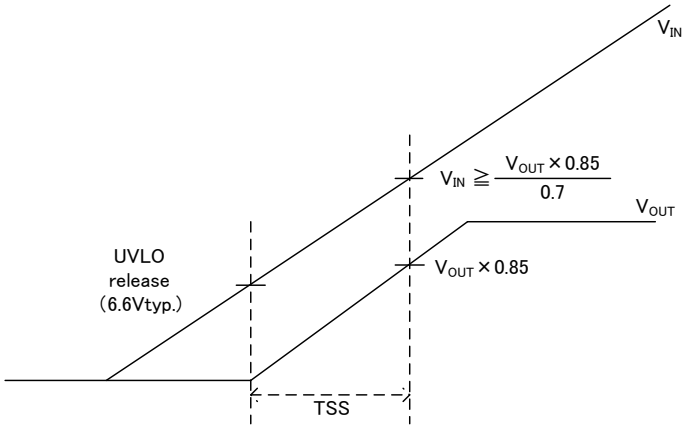


Figure 48. Input Voltage Start-up Time

Soft-start function is designed for the IC so that the output voltage will start according to the time it was decided internally. After UVLO release, the output voltage range will be less than 70% of the input voltage at soft-start operation. Please be sure that the input voltage of the soft-start after startup is as follows.

$$V_{IN} \geq \frac{V_{OUT} \times 0.85}{0.7} \text{ [V]}$$

4. Phase Compensation

A current mode control buck DC/DC converter is a two-pole, one-zero system. The two poles are formed by an error amplifier and load and the one zero point is added by the phase compensation. The phase compensation resistor R_{CMP} determines the crossover frequency F_{CRS} where the total loop gain of the DC/DC converter is 0 dB. The high value of this crossover frequency F_{CRS} provides a good load transient response characteristic but inferior stability. Conversely, specifying a low value for the crossover frequency F_{CRS} greatly stabilizes the characteristics but the load transient response characteristic is impaired.

(1) Selection of Phase Compensation Resistor R_{CMP}

The phase compensation resistance R_{CMP} can be determined by using the following equation.

$$R_{CMP} = \frac{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} [\Omega]$$

where :

V_{OUT} is the output voltage

F_{CRS} is the crossover frequency

C_{OUT} is the output capacitance

V_{FB} is the feedback reference voltage (1.0 V (Typ))

G_{MP} is the current sense gain (7 A/V (Typ))

G_{MA} is the error amplifier transconductance (150 µA/V (Typ))

(2) Selection of phase compensation capacitance C_{CMP}

For stable operation of the DC/DC converter, inserting a zero point under 1/6 of the zero crossover frequency cancels the phase delay due to the pole formed by the load often, thus, providing favorable characteristics.

The phase compensation capacitance C_{CMP} can be determined by using the following equation.

$$C_{CMP} = \frac{1}{2\pi \times R_{CMP} \times F_Z} [F]$$

where

F_Z is the Zero point inserted

(3) Loop stability

To ensure the stability of the DC/DC converter, make sure that a sufficient phase margin is provided. Phase margin of at least 45 degrees in the worst conditions is recommended. The feed forward capacitor C_{RUP} is used for the purpose of forming a zero point together with the resistor R_{UP} to increase the phase margin within the limited frequency range. Using a C_{RUP} is effective when the R_{UP} resistance is larger than the combined parallel resistance of R_{UP} and R_{DW}.

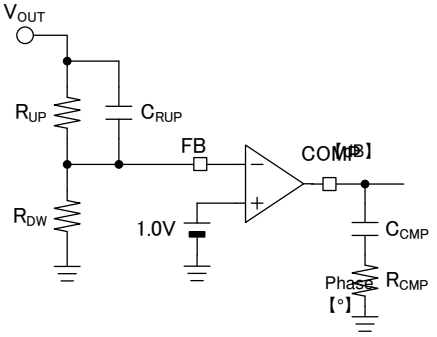


Figure 49. Phase compensation circuit

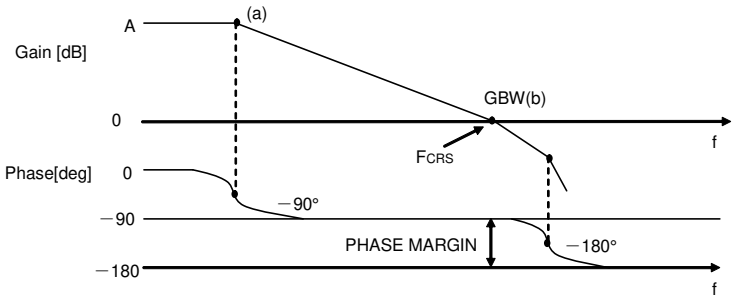


Figure 50. Bode plot

PCB Layout Design

In buck DC/DC converters, a large pulsed current flows in two loops. The first loop is the one into which the current flows when the High Side FET is turned on. The flow starts from the input capacitor CIN, runs through the FET, inductor L and output capacitor COUT and back to ground of CIN via ground of COUT. The second loop is the one into which the current flows when the Low Side FET is turned on. The flow starts from the Low Side FET, runs through the inductor L and output capacitor COUT and back to ground of the Low Side FET via ground of COUT. Tracing these two loops as thick and short as possible allows noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors, in particular, to the ground plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

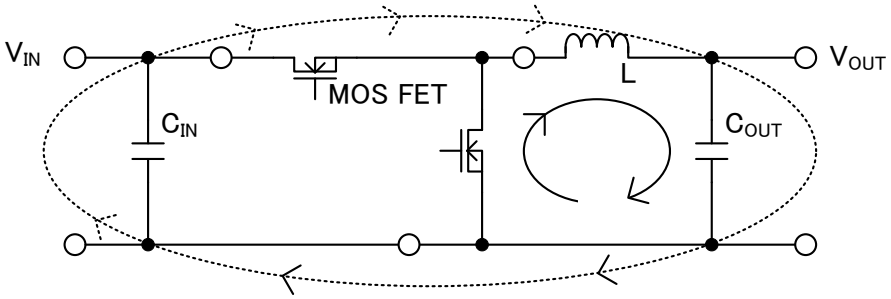
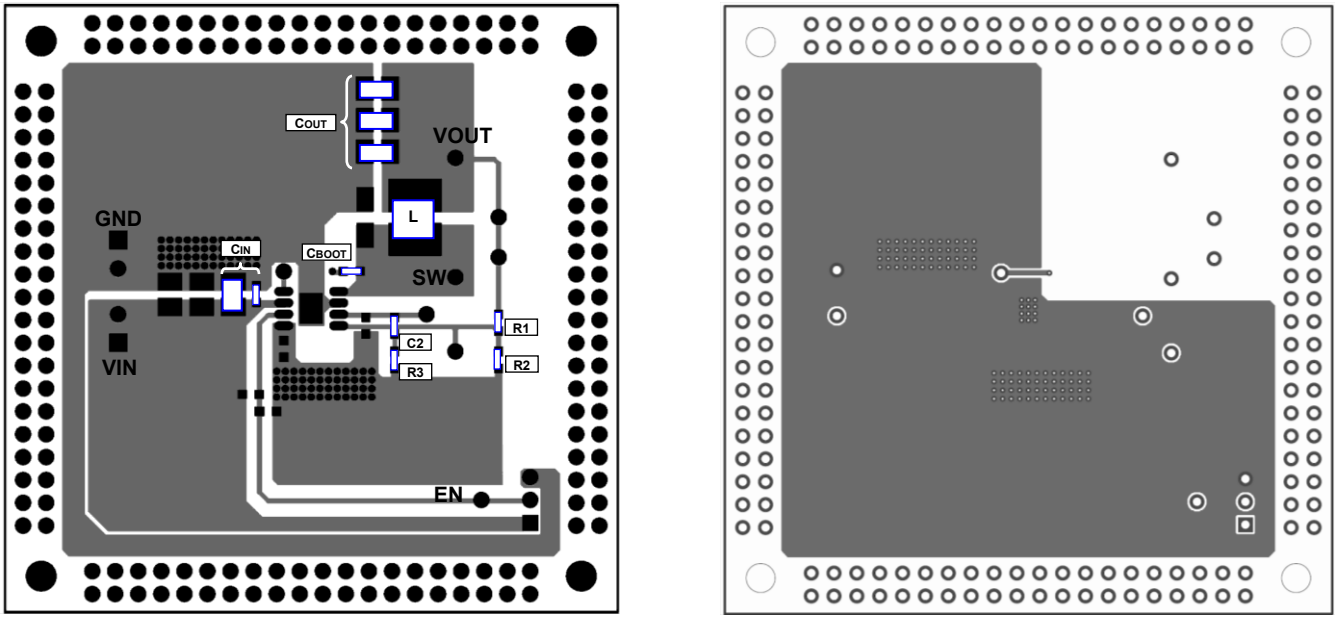


Figure 51. Current Loop of Buck Converter

Accordingly, design the PCB layout with particular attention paid to the following points.

- Provide the input capacitor as close to the VIN terminal as possible on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the ground node to assist in heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Trace to the inductor as thick and as short as possible.
- Provide lines connected to FB and COMP as far as possible from the SW node.
- Provide the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.

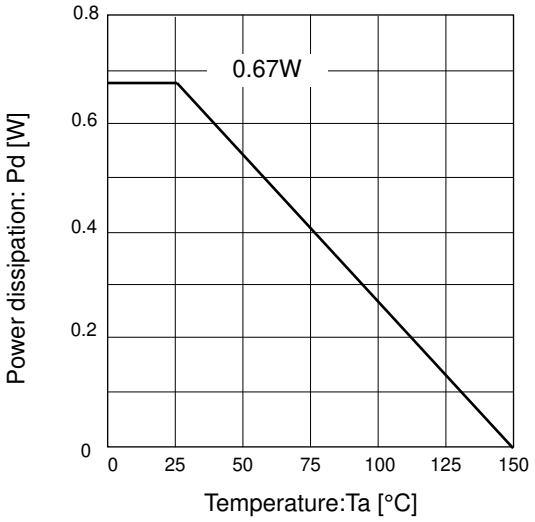


Top Layer Bottom Layer

Figure 52. Example of Sample Board Layout Pattern

Power Dissipation

When designing the PCB layout and peripheral circuitry, sufficient consideration must be given to ensure that the power dissipation is within the allowable dissipation curve.



θJA=185.2°C/W
1 layer board
(back side copper foil area:70mm × 70mm)

Figure 53. Power Dissipation (SOP-J8)

I/O equivalence circuit(s)

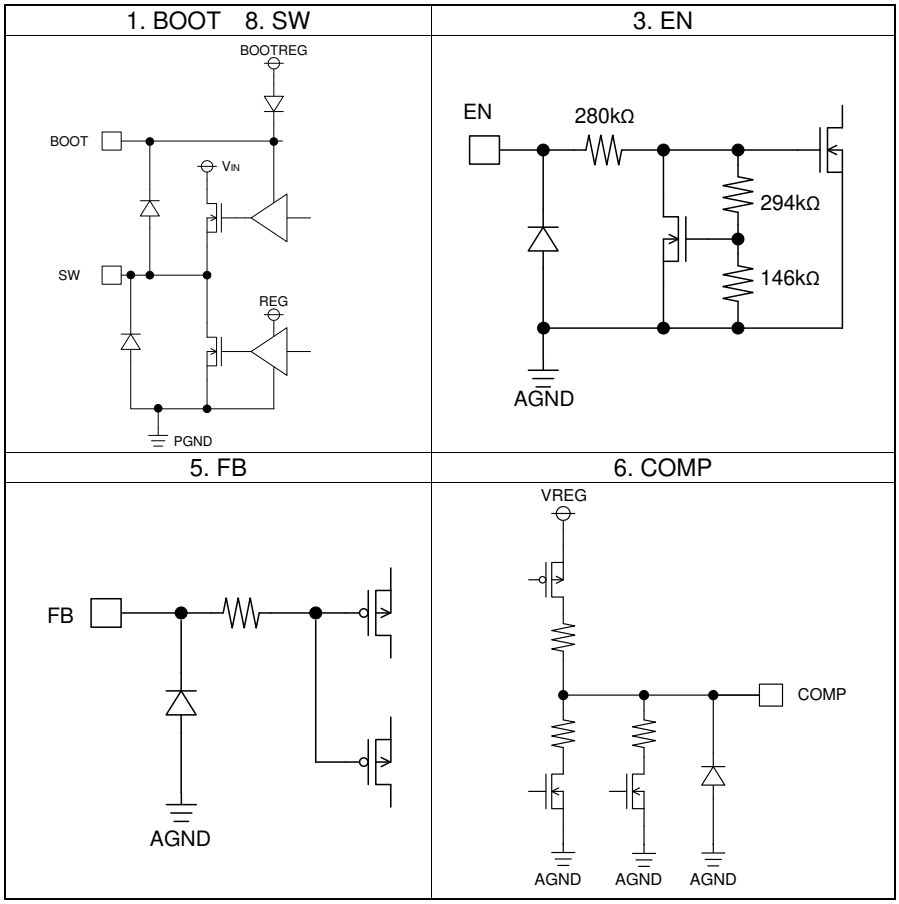


Figure 54. I/O Equivalent Circuit Chart