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7.0V to 36V Input, 3.0A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9E303EFJ-LB

General Description

This is the product guarantees long time support in Industrial market.BD9E303EFJ-LB is a synchronous buck switching regulator with built-in power MOSFETs. It is a current mode control DC/DC converter and features high-speed transient response. Phase compensation can also be set easily.

Features

- Long Time Support Product for Industrial Applications.
- Synchronous single DC/DC converter.
- Over-Current Protection.
- Short Circuit Protection.
- Thermal Shutdown Protection.
- Under voltage Lockout Protection.
- Soft Start.
- HTSOP-J8 package (Exposed Pad).

Applications

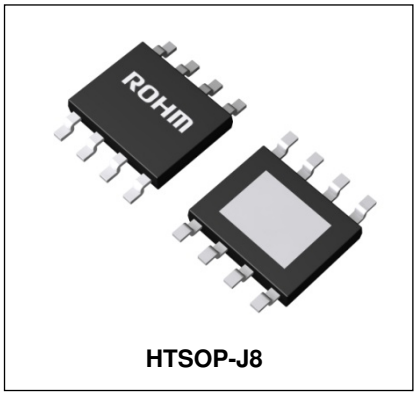
- Industrial Equipment.
- Power supply for FA's industrial device using 24V bass.
- Consumer applications such as home appliance. Distribution type power supply system for 12V, and 24V.

Key Specifications

- Input Voltage Range: 7.0V to 36V
- Output Voltage Range: 1.0V to V_{IN}×0.8V
- Output Current: 3.0A (Max)
- Switching Frequency: 300kHz (Typ)
- High-Side MOSFET ON-Resistance: 90mΩ (Typ)
- Low-Side MOSFET ON-Resistance: 80mΩ (Typ)
- Standby Current: 0μA (Typ)

Package

	W (Typ) x D (Typ) x H (Max)
HTSOP-J8	4.90mm x 6.00mm x 1.00mm



HTSOP-J8

Typical Application Circuit

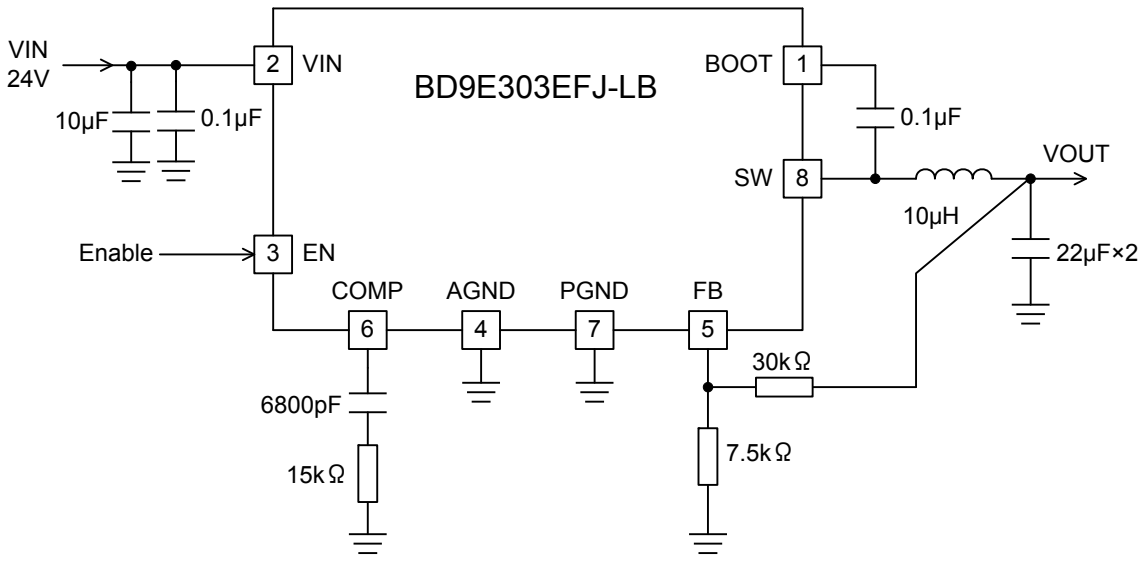


Figure 1. Application circuit

Pin Configuration

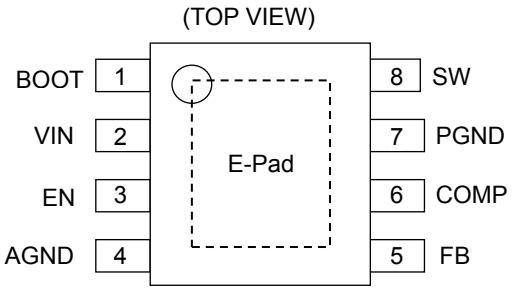


Figure 2. Pin assignment

Pin Description(s)

Pin No	Pin Name	Description
1	BOOT	Connect a bootstrap capacitor of 0.1μF between this terminal and SW terminal. The voltage of this capacitor is the gate drive voltage of the high-side MOSFET.
2	VIN	Power supply terminal for the switching regulator and control circuit. Connecting a 10μF and 0.1μF ceramic capacitor is recommended.
3	EN	Turning this terminal signal low-level (0.8V or lower) forces the device to enter the shut down mode. Turning this terminal signal high-level (2.5V or higher) enables the device. This terminal must be terminated.
4	AGND	Ground terminal for the control circuit.
5	FB	Inverting input node for the gm error amplifier. See page 18 on how to calculate the resistance of the output voltage setting.
6	COMP	Output of gm error amplifier, and input of PWM comparator. Connect phase compensation components to this pin. See page 20 on how to calculate the resistance and capacitance for phase compensation.
7	PGND	Ground terminal for the output stage of the switching regulator.
8	SW	Switch node. This terminal is connected to the source of the high-side MOSFET and drain of the low-side MOSFET. Connect a bootstrap capacitor of 0.1μF between this terminal and BOOT terminal. In addition, connect an inductor considering the direct current superimposition characteristic.
-	E-Pad	Exposed pad. Connecting this to the internal PCB ground plane using multiple vias provides excellent heat dissipation characteristics.

Block Diagram

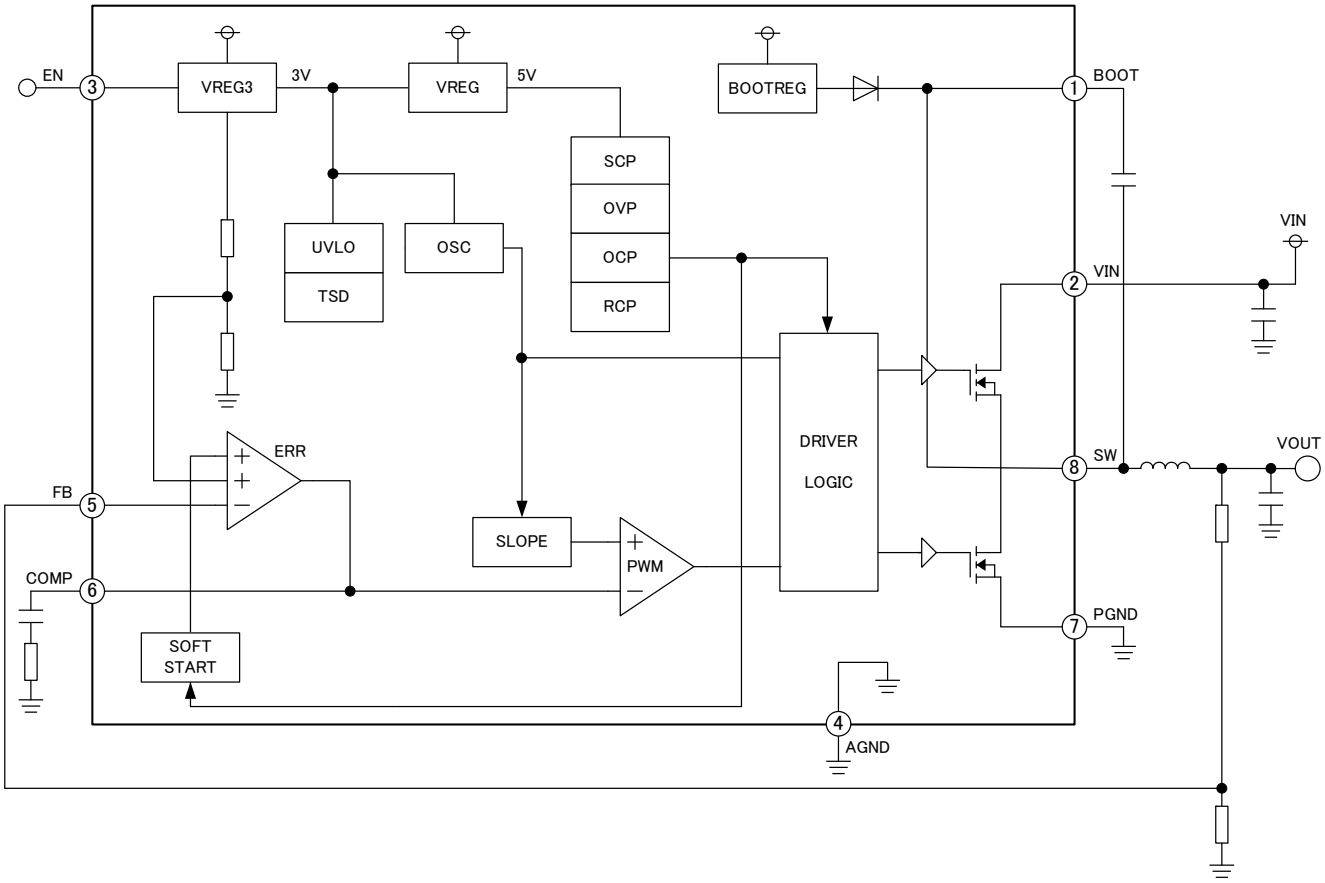


Figure 3. Block diagram

Description of Block

- VREG3
  Block creating internal reference voltage 3V (Typ).

- VREG
  Block creating internal reference voltage 5V (Typ).

- BOOTREG
  Block creating gate drive voltage.

- TSD
  This is the thermal shutdown block. Thermal shutdown circuit shuts down the whole system if temperature exceeds 175°C (Typ). When the temperature decreases, it returns to normal operation with hysteresis of 25°C (Typ).

- UVLO
  This is the under voltage lock-out block. IC shuts down when VIN is under 5V (Typ). The threshold voltage has a hysteresis of 1.4V (Typ).

- ERR
  This circuit compares the feedback voltage at the output to the reference voltage. The output of this circuit is the COMP terminal voltage and this determines the switching duty. Also, because of soft start during start-up, COMP terminal voltage is controlled by internal slope voltage.

- OSC
  Block generating oscillation frequency.

- SLOPE
  This circuit creates a triangular wave from generated clock in OSC. The voltage converted from current sense signal of high side MOSFET and the triangular wave is sent to PWM comparator.

- PWM
  This block determines the switching duty by comparing the output COMP terminal voltage of error amplifier and output of SLOPE block.

- DRIVER LOGIC
  This is the DC/DC driver block. Input to this block is signal from PWM and output drives the MOSFETs.

- SOFT START
  This circuit prevents the overshoot of output voltage and In-rush current by forcing the output voltage to rise slowly, thus, avoiding surges in current during start-up.

- OCP
  This block limits the current flowing in high side MOSFET for each cycle of switching frequency during over-current.

- RCP
  This block limits the current flowing in low side MOSFET for each cycle of switching frequency during over-current.

- SCP
  The short circuit protection block compares the FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage has fallen below 0.7V (Typ) and remained in that state for 1.0msec (Typ), SCP activates and stops the operation for 14msec (Typ) and subsequently initiates a restart.

- OVP
  Over voltage protection function (OVP) compares FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage exceeds 1.30V (Typ) it turns MOSFET of output part MOSFET off. After output voltage drop it returns with hysteresis.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	VIN	-0.3 to +40	V
EN Input Voltage	VEN	-0.3 to +40	V
Voltage from GND to BOOT	VBOOT	-0.3 to +45	V
Voltage from SW to BOOT	ΔVBOOT	-0.3 to +7	V
FB Input Voltage	VFB	-0.3 to +7	V
COMP Input Voltage	VCOMP	-0.3 to +7	V
SW Input Voltage	VSW	-0.5 to VIN + 0.3	V
Allowable Power Dissipation(Note 1)	Pd	2.76 (Note 1)	W
Operating Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) HTSOP-J8:Derating in done 22mW/°C for operating Ta ≥ 25°C
(PCB size: 114.3 mm × 76.2 mm × 1.6 mm, copper foil area (on 2nd & 3rd layer and reverse side): 74.2 mm × 74.2 mm when mounted on 4-layer PCB)
Copper foil thickness: Front side and reverse side 70μm be used, 2nd & 3rd 35μm be used.

Caution1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution2: Reliability is decreased at junction temperature greater than 125°C.

Recommended Operating Conditions (Ta= -40°C to +85°C)

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	VIN	7.0	-	36	V
Output Current	IOUT	0	-	3	A
Output Voltage Range	VRANGE	1.0 (Note 2)	-	VIN × 0.8	V

(Note 2) Please use it in output voltage setting of which output pulse width does not become 200nsec (Typ) or less. See the page 18 for how to calculate the resistance of the output voltage setting.

Electrical Characteristics (Unless otherwise specified V_{IN}=24V V_{EN}=3V Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply Current in Operating	IOPR	-	2.2	3.0	mA	VFB = 1.1V No switching
Supply Current in Standby	ISTBY	-	0	10	μA	VEN = 0V
Reference Voltage (TJ =25°C)	VFB	0.990	1.000	1.010	V	
Reference Voltage (TJ =-40 to +150°C)	VFB	0.965	1.000	1.035	V	
FB Input Current	IFB	-1	0	1	μA	VFB = 1.1V
Switching frequency	FOSC	255	300	345	kHz	
Maximum Duty ratio	Maxduty	90	95	99	%	
High-side FET on-resistance	RONH	-	90	-	mΩ	ISW = 100mA
Low-side FET on-resistance	RONL	-	80	-	mΩ	ISW = 100mA
Over Current limit	ILIMIT	-	5.2	-	A	
UVLO detection voltage	VUVLO	4.7	5.0	5.3	V	VIN falling
UVLO hysteresis voltage	VUVLOHYS	1.2	1.4	1.6	V	
EN high-level input voltage	VENH	2.5	-	VIN	V	
EN low-level input voltage	VENL	0	-	0.8	V	
EN Input current	IEN	2.1	4.2	8.4	μA	VEN = 3V
Soft Start time	TSS	1.25	2.50	5.00	msec	EN rising to FB=0.85V

- VFB : FB Input Voltage. VEN : EN Input Voltage.
- Pd should not be exceeded.

Typical Performance Curves

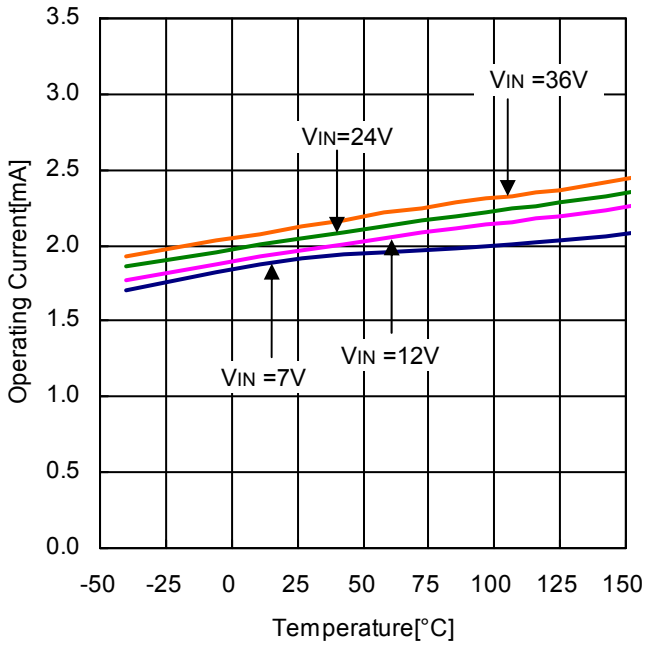


Figure 4. Operating Current vs Junction Temperature

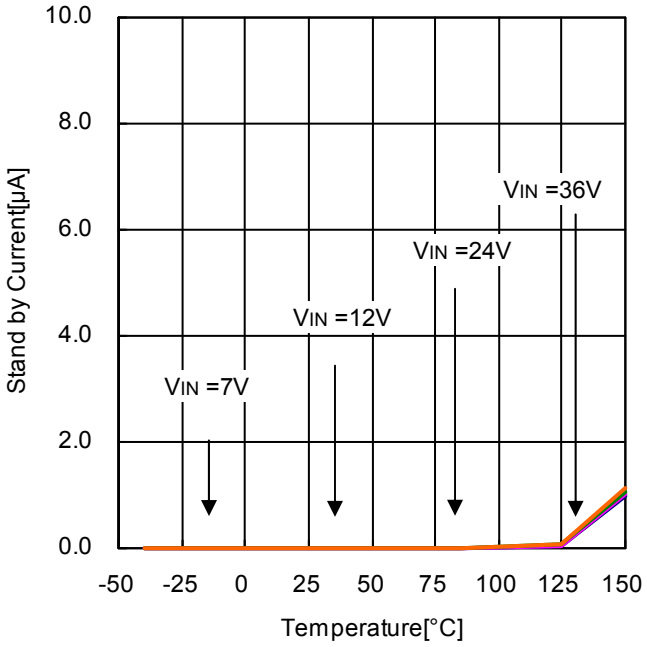


Figure 5. Stand-by Current vs Junction Temperature

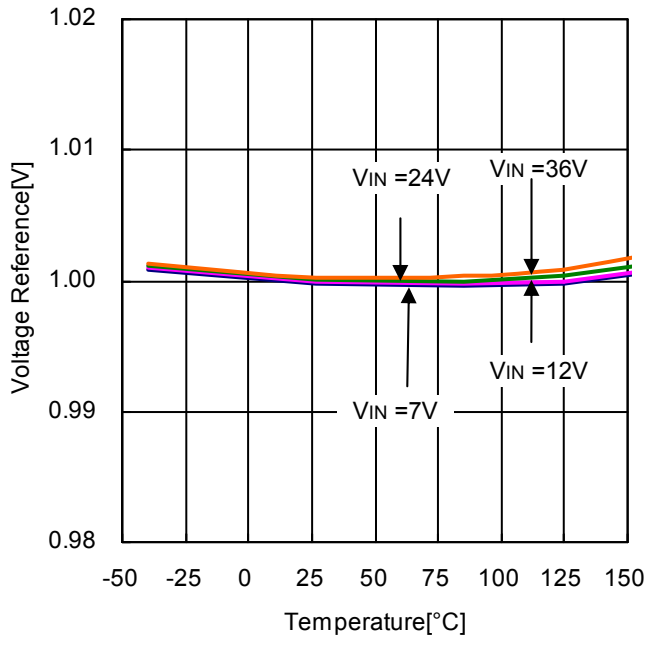


Figure 6. FB Voltage Reference vs Junction Temperature

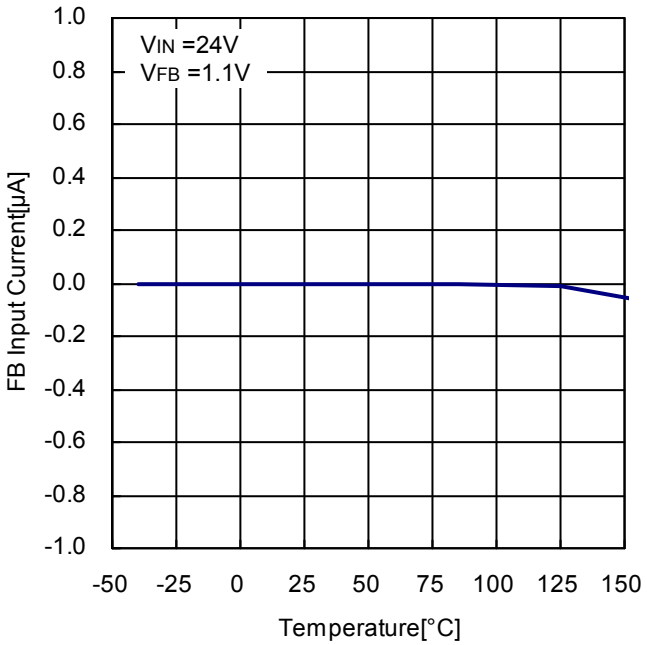


Figure 7. FB Input Current vs Junction Temperature

Typical Performance Curves - continued

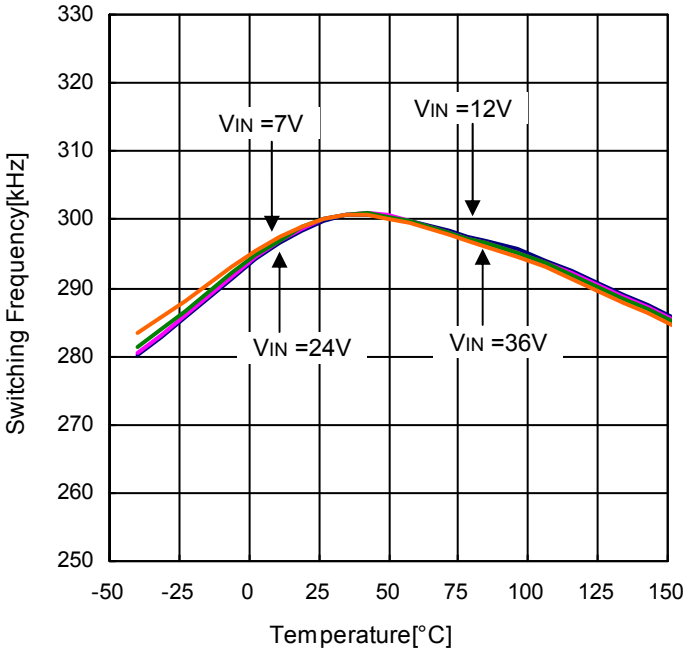


Figure 8. Switching Frequency vs Junction Temperature

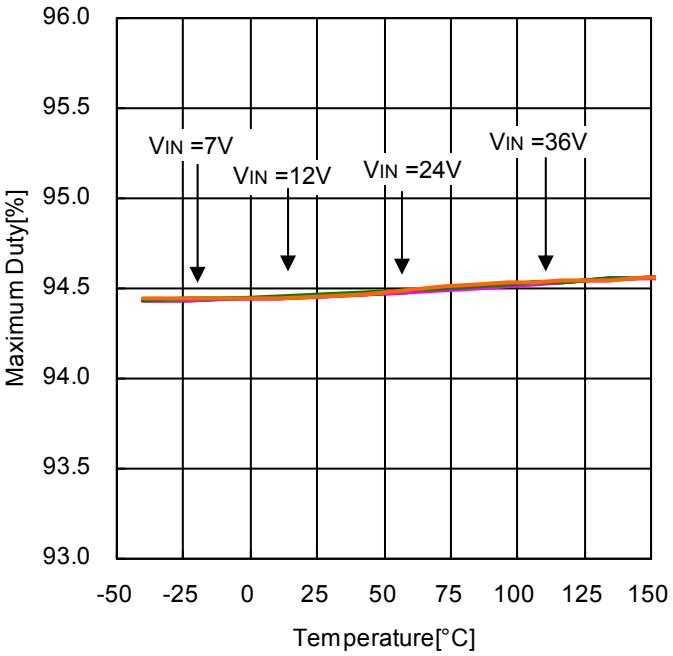


Figure 9. Maximum Duty vs Junction Temperature

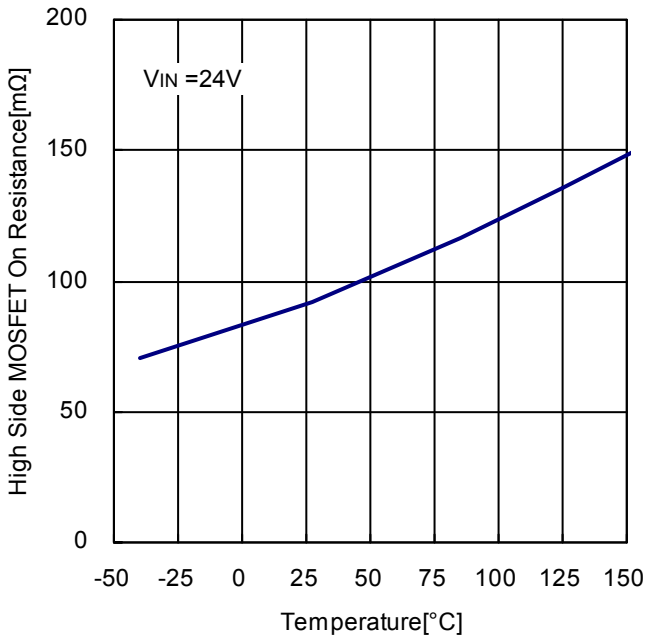


Figure 10. High Side MOSFET ON - Resistance vs Junction Temperature

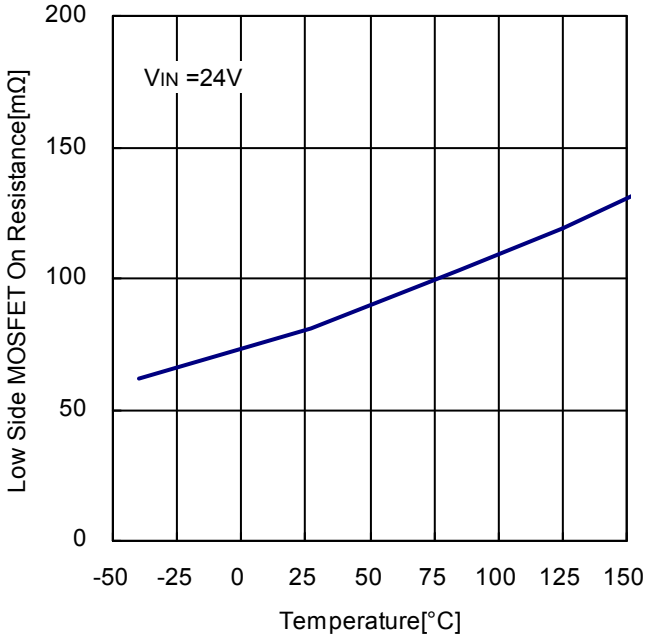


Figure 11. Low Side MOSFET ON -Resistance vs Junction Temperature

Typical Performance Curves - continued

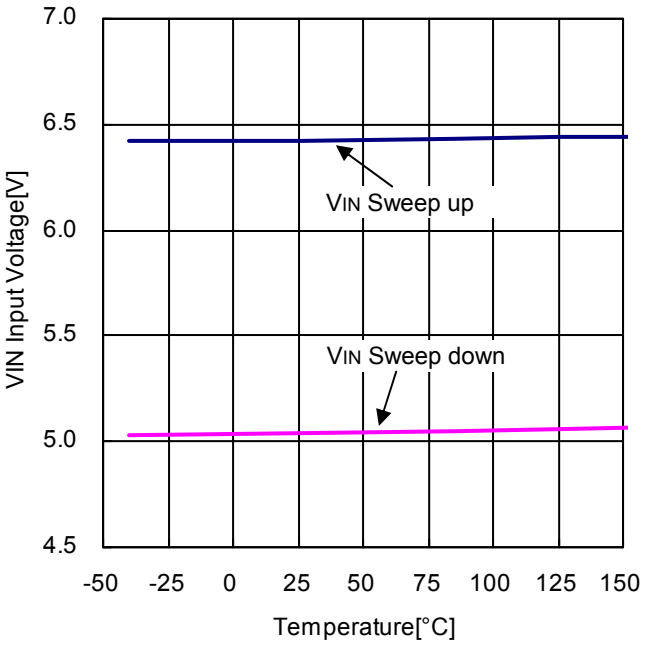


Figure 12. UVLO Threshold vs Junction Temperature

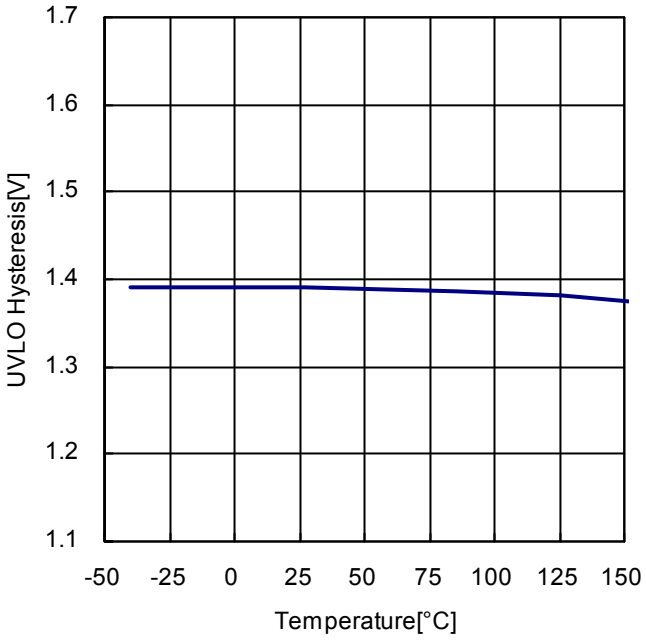


Figure 13. UVLO Hysteresis vs Junction Temperature

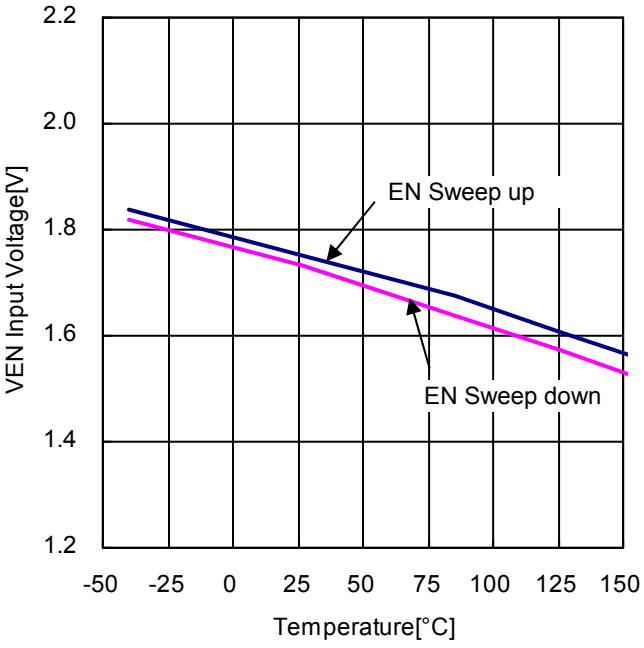


Figure 14. EN Threshold vs Junction Temperature

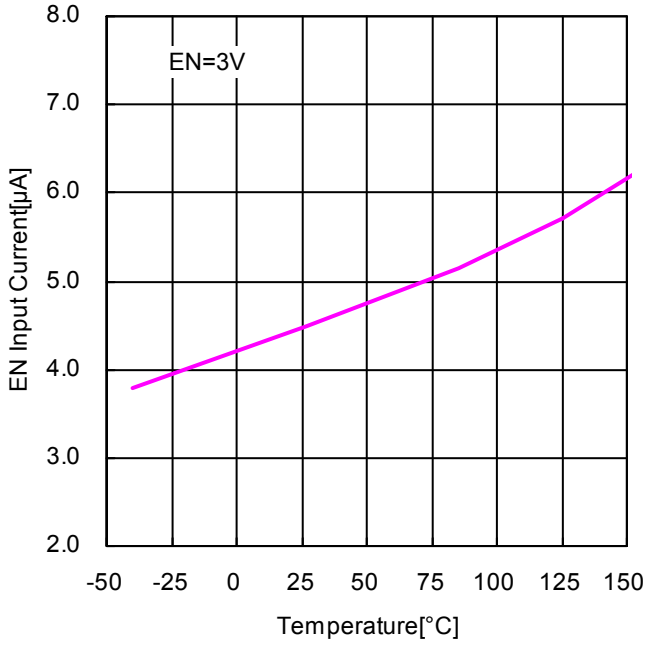


Figure 15. EN Input Current vs Junction Temperature

Typical Performance Curves - continued

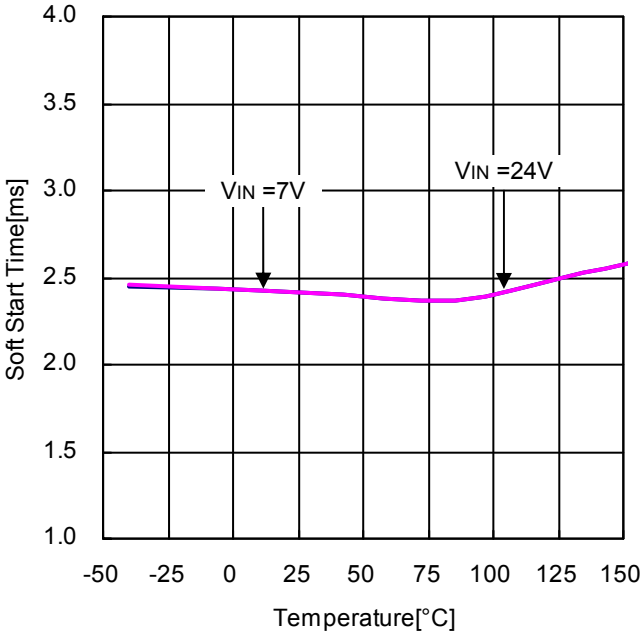


Figure 16. Soft Start Time vs Junction Temperature

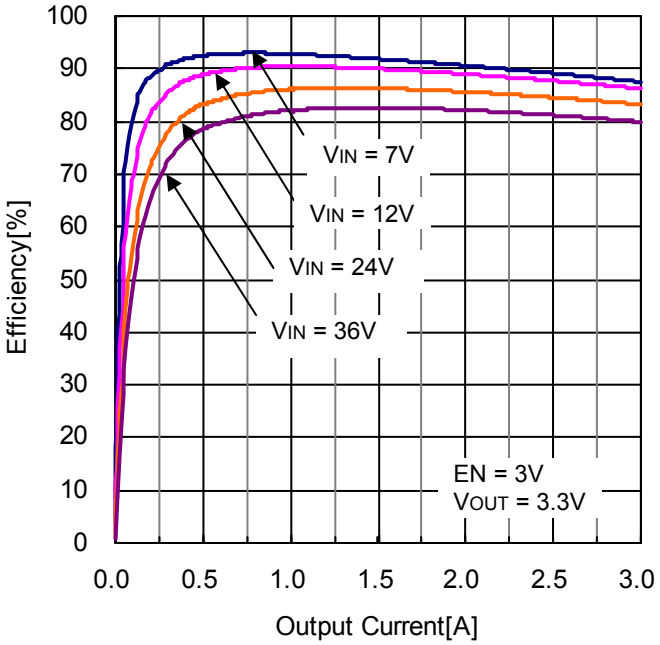


Figure 17. Efficiency vs Output Current
(VOUT = 3.3V, L = 10µH)

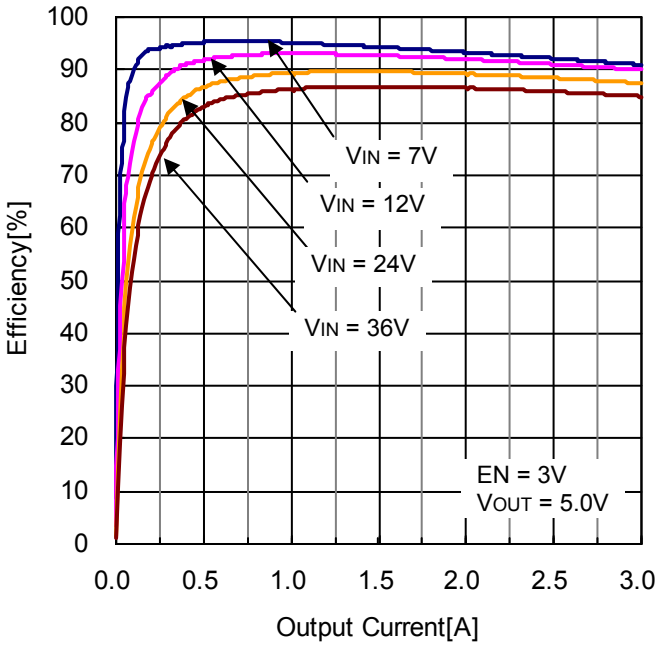


Figure 18. Efficiency vs Output Current
(VOUT = 5.0V, L = 10µH)

Typical Performance Curves - continued

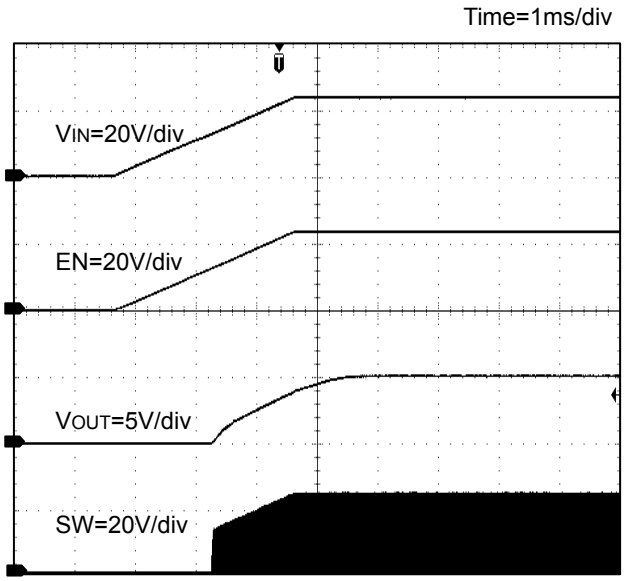


Figure 19. Power Up (VIN = EN)
(VOUT = 5.0V)

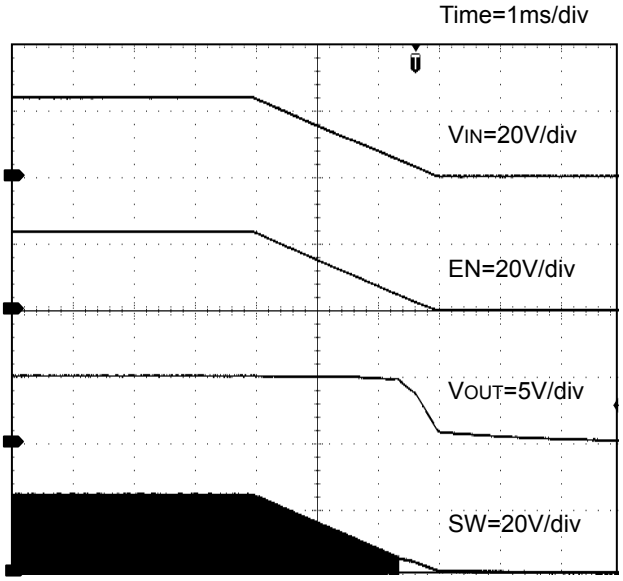


Figure 20. Power Down (VIN = EN)
(VOUT = 5.0V)

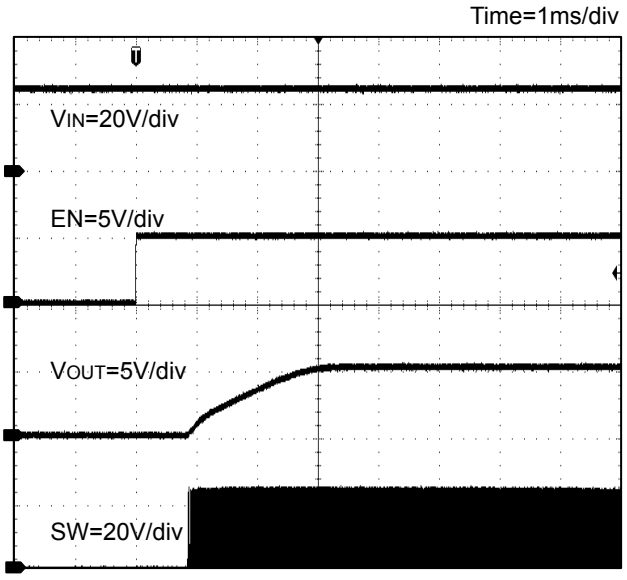


Figure 21. Power Up (EN = 0V→5V)
(VOUT = 5.0V)

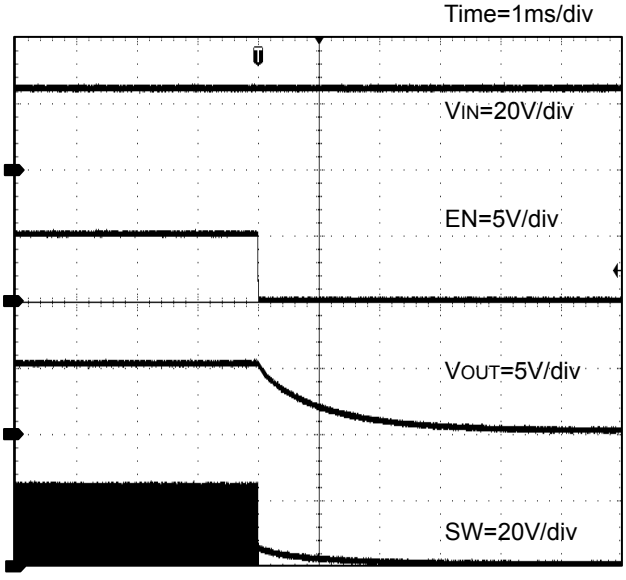


Figure 22. Power Down (EN = 5V→0V)
(VOUT = 5.0V)

Typical Performance Curves - continued

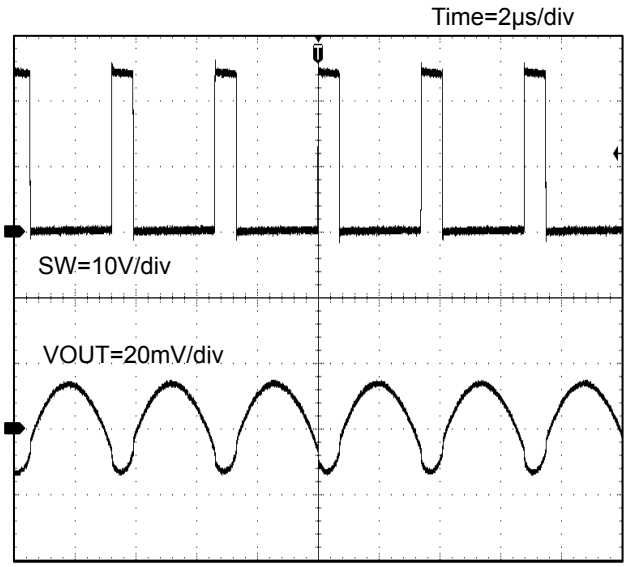


Figure 23. VOUT Ripple
(VIN = 24V, VOUT = 5V, IOUT = 0A)

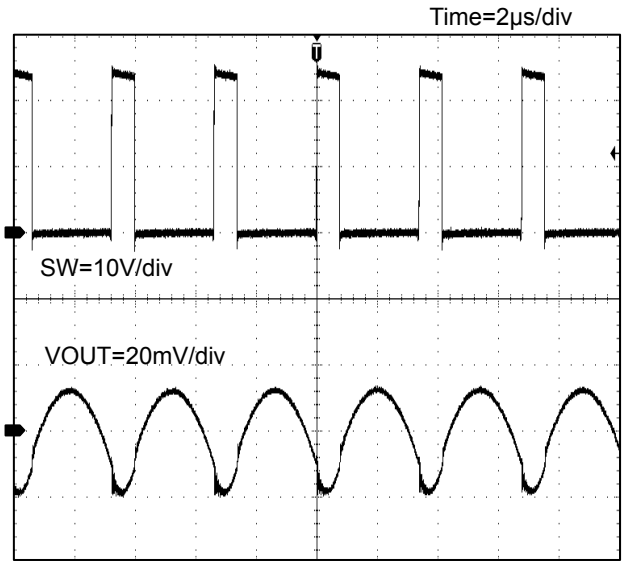


Figure 24. VOUT Ripple
(VIN = 24V, VOUT = 5V, IOUT = 3A)

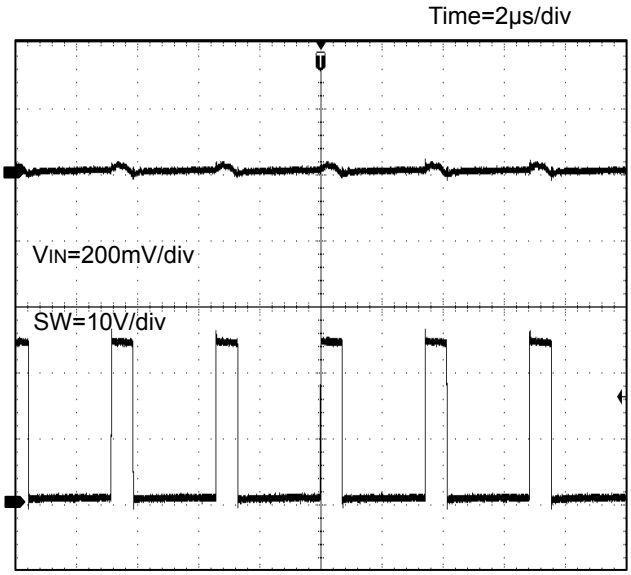


Figure 25. VIN Ripple
(VIN = 24V, VOUT = 5V, IOUT = 0A)

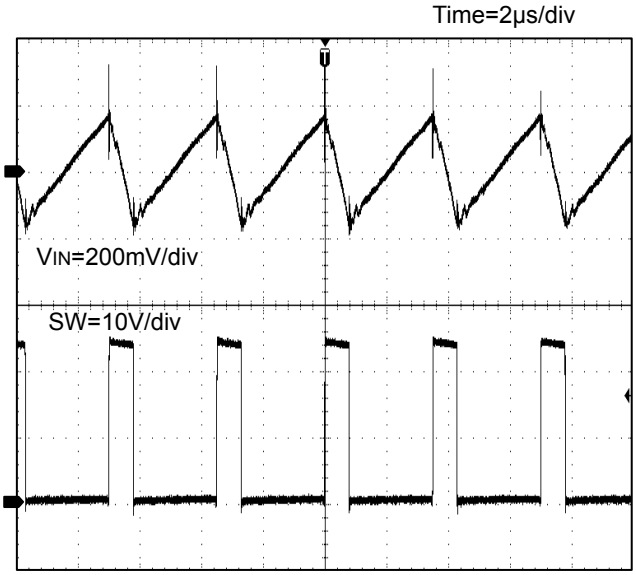


Figure 26. VIN Ripple
(VIN = 24V, VOUT = 5V, IOUT = 3A)

Typical Performance Curves - continued

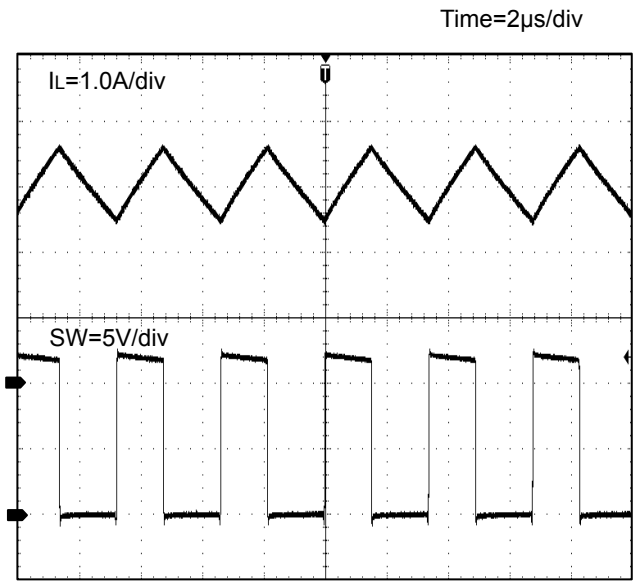


Figure 27. Switching Waveform
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A)

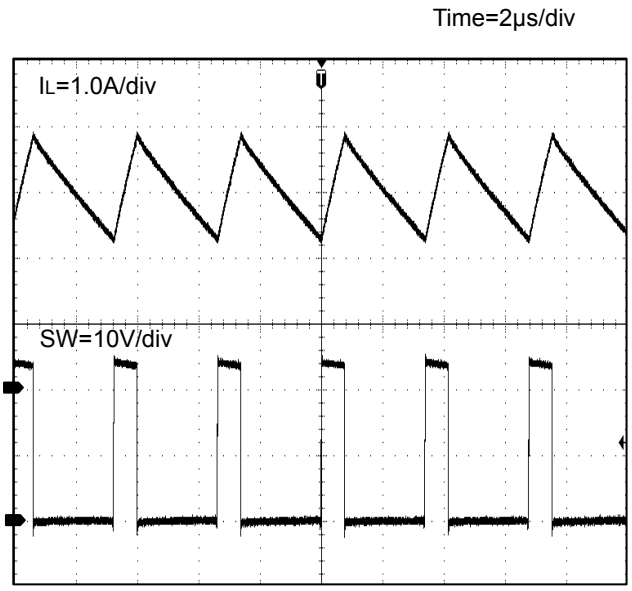


Figure 28. Switching Waveform
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 3A)

Typical Performance Curves - continued

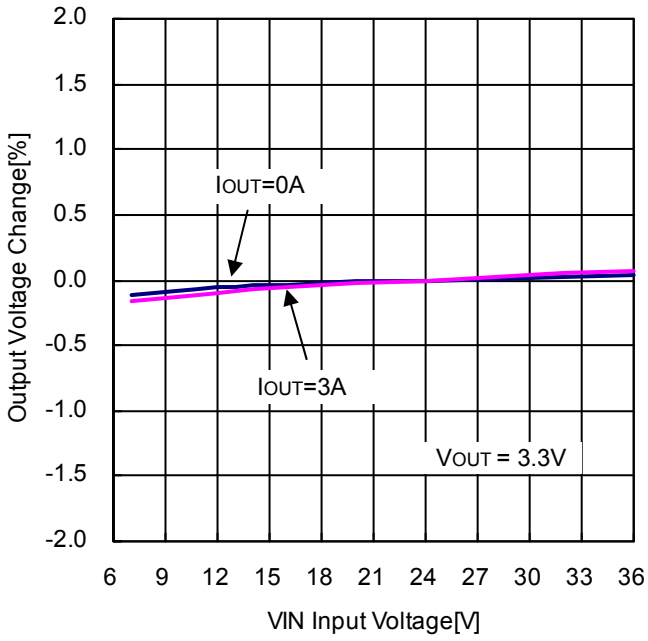


Figure 29. VOUT Line Regulation

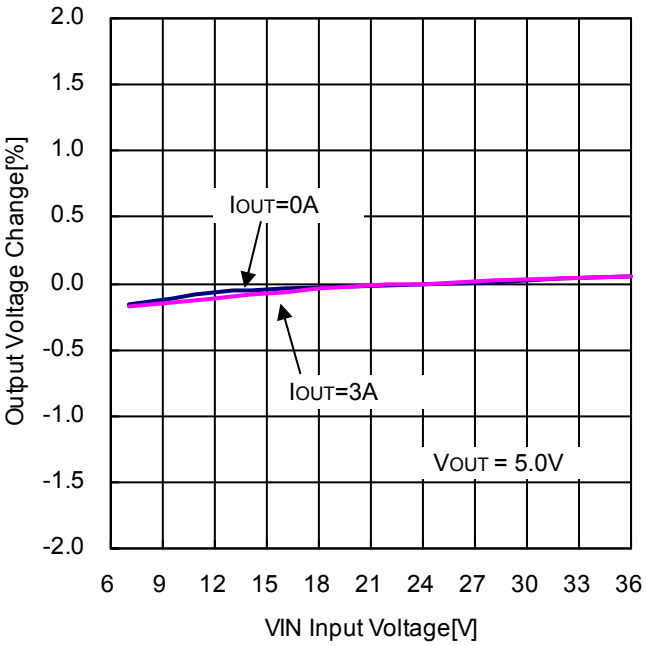


Figure 30. VOUT Line Regulation

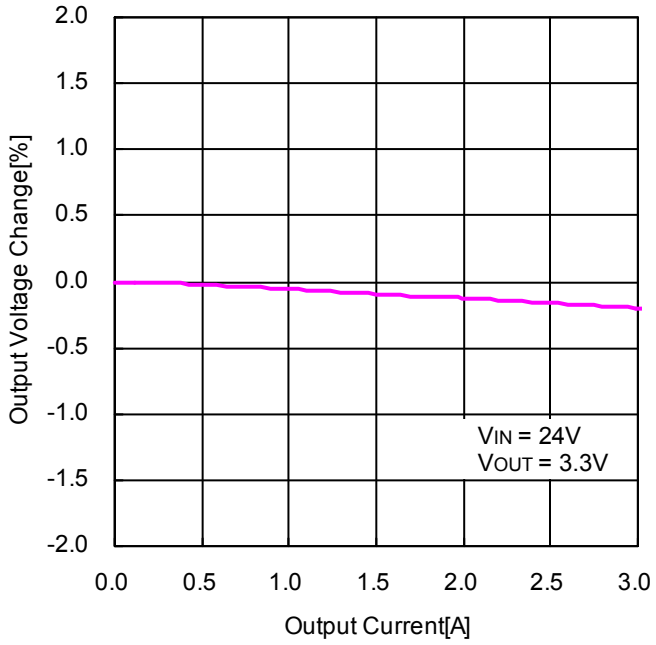


Figure 31. VOUT Load Regulation
(VOUT = 3.3V)

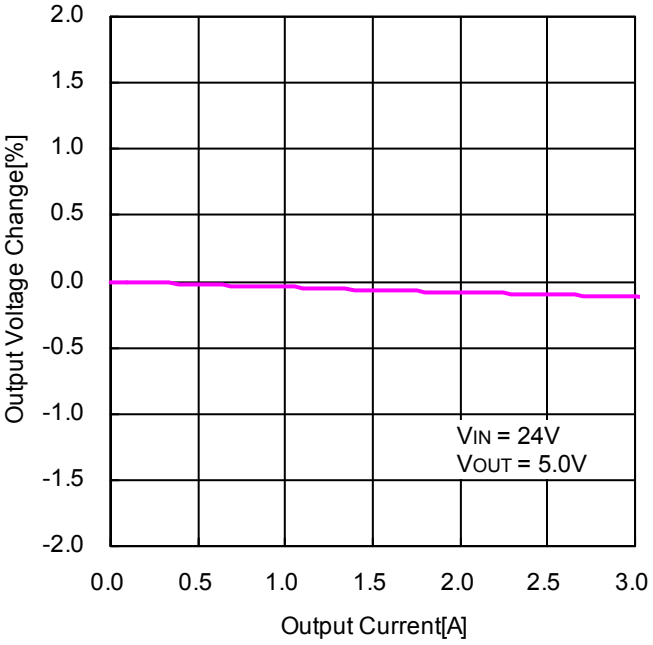


Figure 32. VOUT Load Regulation
(VOUT = 5.0V)

Typical Performance Curves – continued

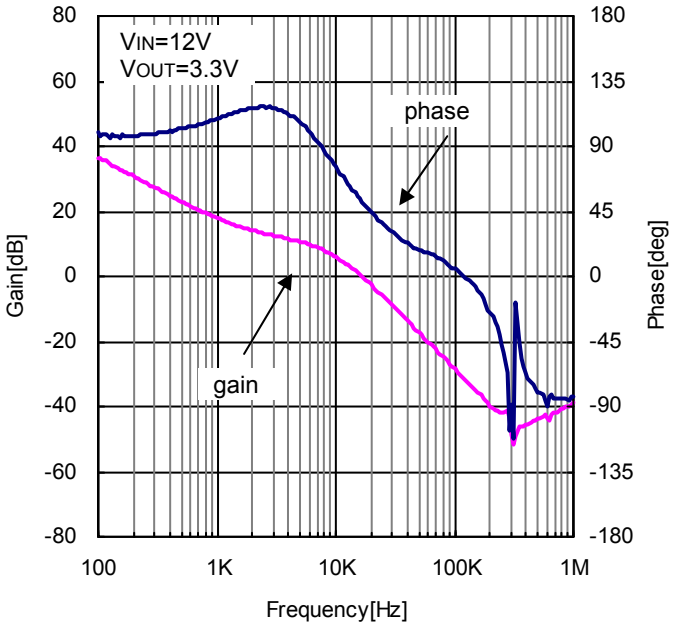


Figure 33.Closed Loop Response
(VIN=12V, VOUT=3.3V, IOUT=3A, COUT=Ceramic22μF×2)

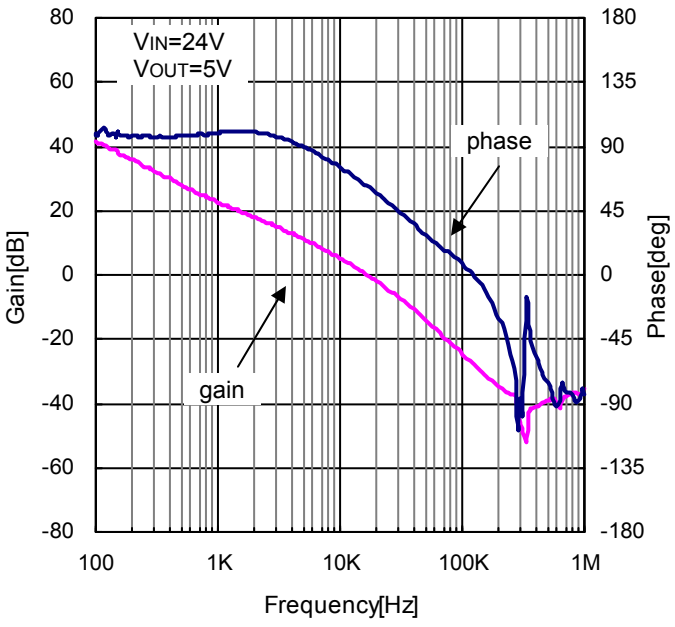


Figure 34. Closed Loop Response
(VIN=24V, VOUT=5V, IOUT=3A, COUT=Ceramic22μF×2)

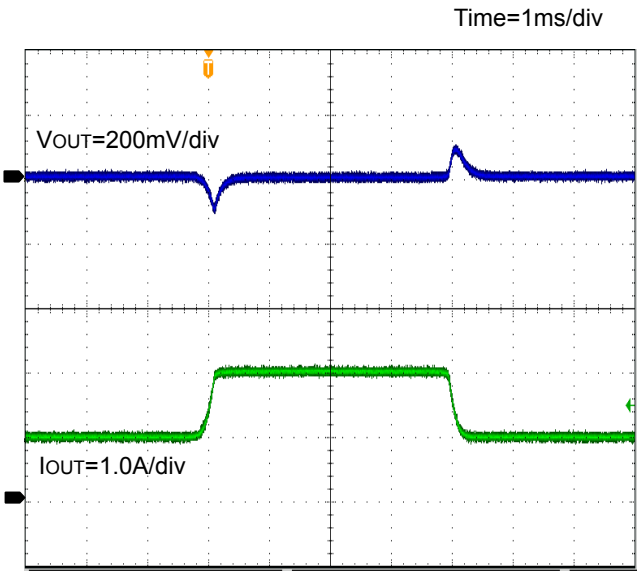


Figure 35. Load Transient Response IOUT=1A – 2A
(VIN=24V, VOUT=5V, COUT=Ceramic22μF×2)

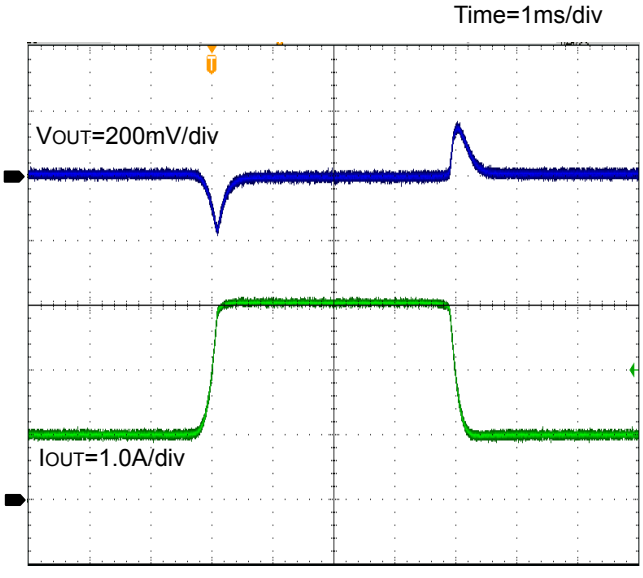


Figure 36. Load Transient Response IOUT=1A – 3A
(VIN=24V, VOUT=5.0V, COUT=Ceramic22μF×2)

Function Description

1. Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When EN voltage reaches 2.5V, the internal circuit is activated and the IC starts up. Setting the shutdown interval (Low Level interval) of EN to 100µs or longer will enable the shutdown control with the EN terminal.

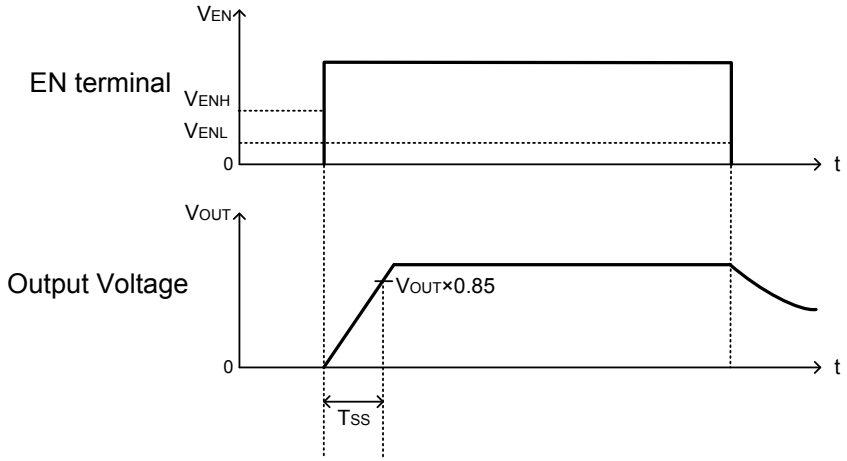


Figure 37. Timing Chart with Enable Control

2. Protective Functions

The protective circuits are intended for the prevention of damages caused by unexpected accidents. Do not use them for continuous protective operation.

(1) Short Circuit Protection (SCP)

The short circuit protection block compares the FB terminal voltage with the internal reference voltage VREF. When the FB terminal voltage has fallen below 0.7V (Typ) and remained in that state for 1.0msec (Typ), SCP activates and stops the operation for 14msec (Typ) and subsequently initiates a restart.

Table 1. Short Circuit Protection Function

EN pin	FB pin	Short circuit protection	Switching Frequency
2.5V or higher	0.30V (Typ) ≥FB	Enabled	75kHz (Typ)
	0.30V (Typ)<FB≤0.7V (Typ)		150kHz (Typ)
	FB>0.7V (Typ)		300kHz (Typ)
0.8V or lower	-	Disabled	OFF

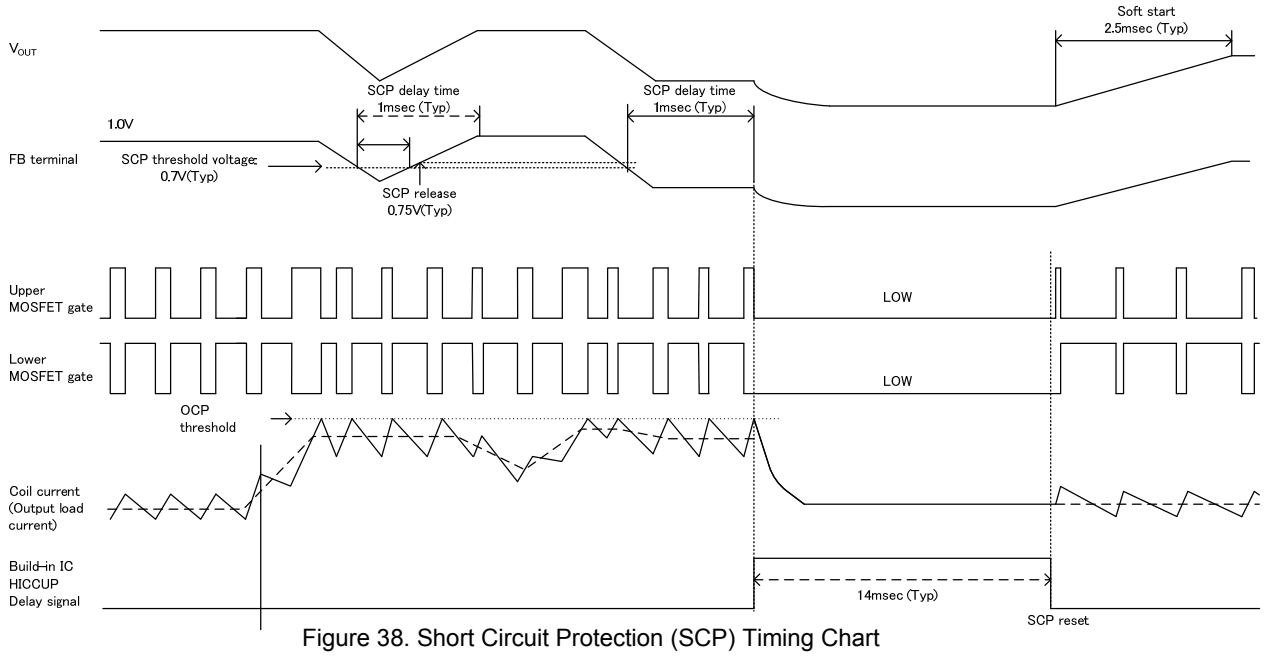


Figure 38. Short Circuit Protection (SCP) Timing Chart

(2) Under Voltage Lockout Protection (UVLO)

The under voltage lockout protection circuit monitors the VIN terminal voltage.
The operation enters standby when the VIN terminal voltage is 5.0V (Typ) or lower.
The operation starts when the VIN terminal voltage is 6.4V (Typ) or higher.

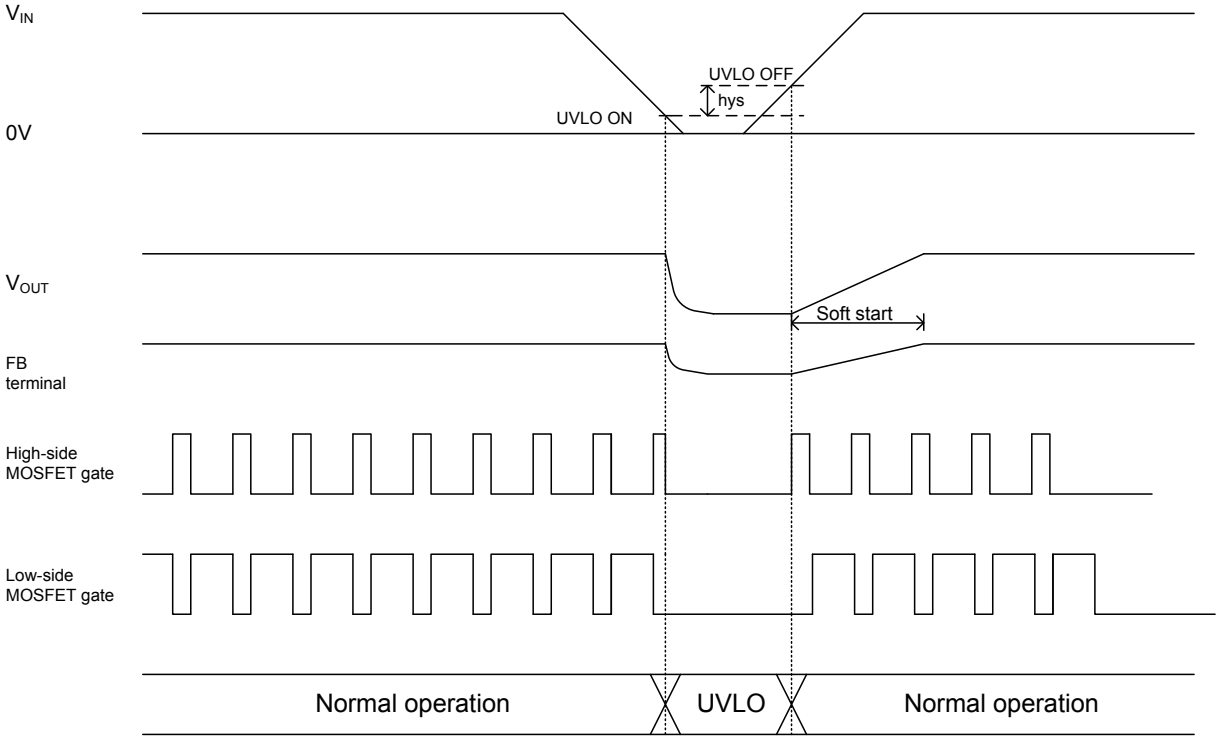


Figure 39. UVLO Timing Chart

(3) Thermal Shutdown (TSD)

When the chip temperature exceeds Tj = 175°C, the DC/DC converter output is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding Tjmax = 150°C. It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.

(4) Over Current Protection (OCP)

The over-current protection function observes the current flowing in upper-side MOSFET by switching cycle and when it detects over flow current, it limits ON duty and protects by dropping output voltage.

(5) Reverse Current Protection (RCP)

The reverse-current protection function observes the current flowing in low-side MOSFET and when it detects over flow current, it turns off the MOSFET.

(6) Over Voltage Protection (OVP)

Over voltage protection function (OVP) compares FB terminal voltage with internal standard voltage VREF. When the FB terminal voltage exceeds 1.30V (Typ), it turns output MOSFETs off. When output voltage drops until it reaches the hysteresis, it will return to normal operation.

Application Example

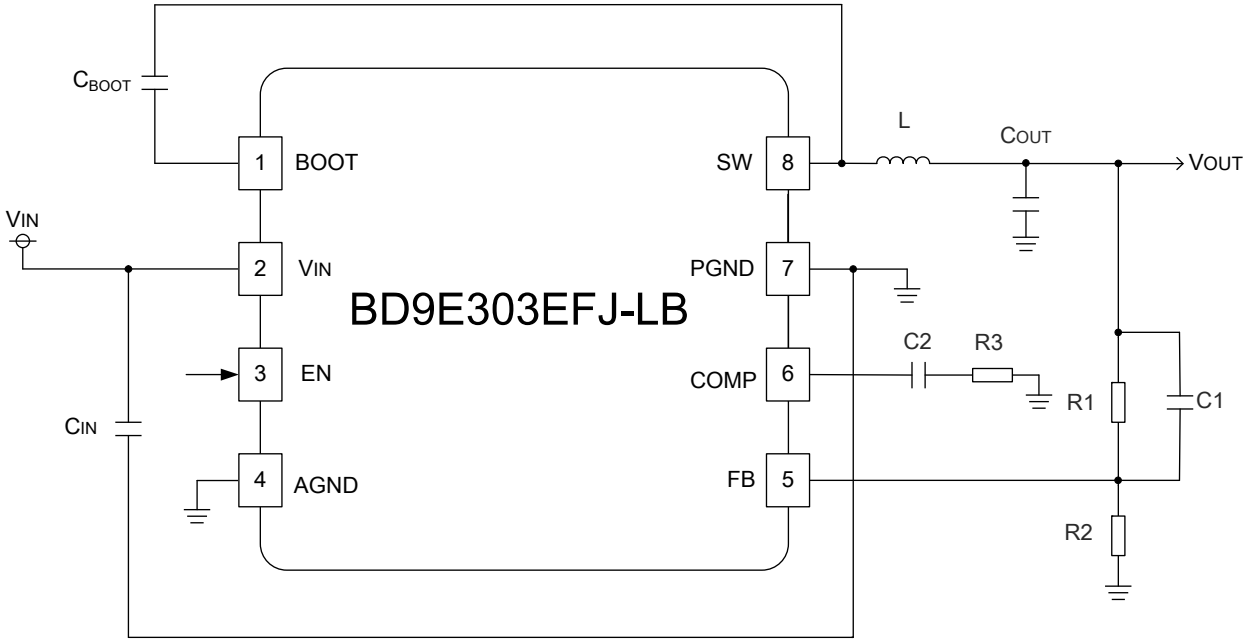


Figure 40. Application Circuit

Table 2. Recommendation Component Valves

VIN	12V			24V	
VOUT	1.8V	3.3V	5V	3.3V	5V
CIN (Note 3)	10μF	10μF	10μF	10μF	10μF
CIN1	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF
CBOOT	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF
L	4.7μH	10μH	10μH	10μH	10μH
R1	12kΩ	30kΩ	30kΩ	30kΩ	30kΩ
R2	15kΩ	13kΩ	7.5kΩ	13kΩ	7.5kΩ
R3	5.6kΩ	10kΩ	15kΩ	10kΩ	15kΩ
C1	-	-	-	-	-
C2	15000pF	10000pF	6800pF	10000pF	6800pF
COUT (Note 4)	Ceramic 22μF×2	Ceramic 22μF×2	Ceramic 22μF×2	Ceramic 22μF×2	Ceramic 22μF×2

(Note 3) For capacitance of input capacitor, take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 4.7μF.

(Note 4) In case capacitance value fluctuates due to temperature characteristics, DC bias characteristics, etc. of output capacitor, crossover frequency may fluctuate.
When selecting a capacitor, confirm the characteristics of the capacitor in its datasheet.
Also, in order to reduce output ripple voltage, low ESR capacitors such as ceramic type are recommended for output capacitor.

Selection of Components Externally Connected

Parameters required to design a power supply are as follows.

Parameter	Unit	Value Example
Input Voltage	V_{IN}	24 V
Output Voltage	V_{OUT}	5 V
Switching Frequency	F_{OSC}	300kHz(Typ)
Inductor ripple current	ΔI_L	1.3A
ESR of the output capacitor	R_{ESR}	10mΩ
Output capacitor	C_{OUT}	44μF
Soft-start time	T_{SS}	2.5ms(Typ)
Max output current	I_{OMAX}	3A

1. Switching Frequency

Switching frequency is fixed to F_{OSC} = 300kHz (Typ).

2. Output Voltage Set Point

The output voltage value can be set by the feedback resistance ratio.

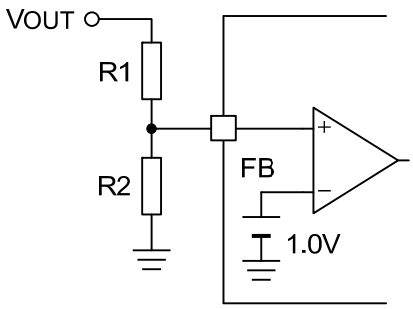


Figure 41. Feedback Resistor Circuit

$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times 1.0 \text{ [V]}$$

※ Minimum pulse range that can be produced at the output stably through all the load area is 200nsec for BD9E303EFJ-LB.
Use input/output condition which satisfies the following method.

$$200(nsec) \leq \frac{V_{OUT}}{V_{IN} \times F_{OSC}}$$

3. Input capacitor configuration

For input capacitor, use a ceramic capacitor. For normal setting, 10μF is recommended, but with larger value, input ripple voltage can be further reduced. Also, for capacitance of input capacitor, take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 4.7μF.

4. Output LC Filter

The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. Selecting an inductor with a large inductance causes the ripple current ΔIL that flows into the inductor to be small, decreasing the ripple voltage generated in the output voltage, but it is not advantageous in terms of the load transient response characteristic. Selecting an inductor with a small inductance improves the transient response characteristic but causes the inductor ripple current to be large, which increases the ripple voltage in the output voltage, showing a trade-off relationship. Here, select an inductance so that the size of the ripple current component of the inductor will be 20% to 50% of the Max output current (3A).

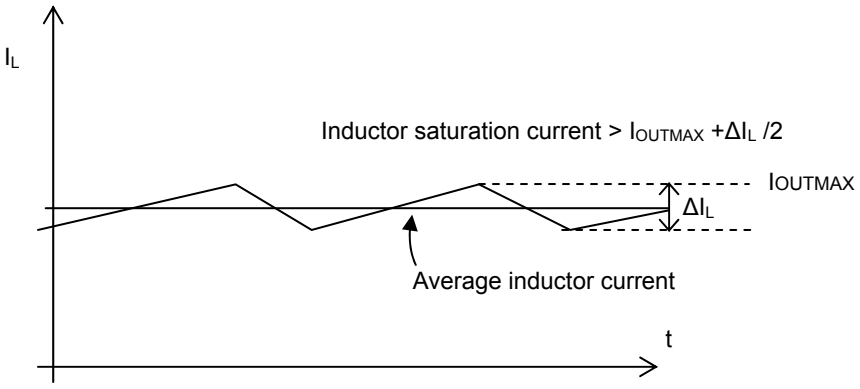


Figure 42. Waveform of current through inductor

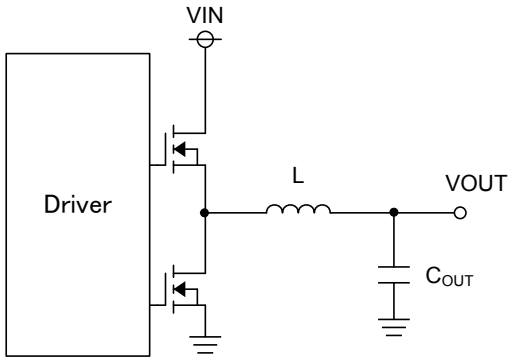


Figure 43. Output LC filter circuit

Now calculating with VIN = 24V, VOUT = 5V, switching frequency FOSC = 300kHz, ΔIL is1.3A, inductance value That can be used is calculated as follows:

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times \Delta I_L} = 10.15 \fallingdotseq 10 [\mu H]$$

* If the output voltage setting is larger than half of VIN please calculated as follows:

$$L = \frac{V_{IN}}{4 \times F_{OSC} \times \Delta I_L}$$

Also for saturation current of inductor, select the one with larger current than maximum output current added by 1/2 of inductor ripple current ΔIL.
Output capacitor COUT affects output ripple voltage characteristics. Select output capacitor COUT so that necessary ripple voltage characteristics are satisfied.

Output ripple voltage can be expressed in the following method.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}})$$

With COUT = 44μF, RESR = 10mΩ the output ripple voltage is calculated as

$$\Delta V_{RPL} = 1.3 \times (10m + \frac{1}{8 \times 44\mu \times 300k}) = 25.31 \text{ [mV]}$$

* When selecting the value of the output capacitor COUT, please note that the value of capacitor CLOAD will add up to the value of COUT to be connected to VOUT.
Charging current to flow through the CLOAD, COUT and the IC startup, must be completed within the soft-start time this charge. Over-current protection circuit operates when charging is continued beyond the soft-start time, the IC may not start. Please consider in the calculation the condition that the lower maximum value capacitor CLOAD that can be connected to VOUT (max) is other than COUT.

Inductor ripple current maximum value of start-up (ILSTART) < Over Current Protection Threshold 4.25 [A](min)

Inductor ripple current maximum value of start-up (ILSTART) can be expressed in the following method.

ILSTART = Output maximum load current(IOMAX) + Charging current to the output capacitor (ICAP) + $\frac{\Delta I_L}{2}$

Charging current to the output capacitor (ICAP) can be expressed in the following method.

$$I_{CAP} = \frac{(C_{OUT} + C_{LOAD}) \times V_{OUT}}{T_{SS}}$$

From the above equation, VIN = 24V, VOUT = 5V, L = 10μH, IOMAX = 3.0A (max), switching frequency FOSC = 255kHz (min), the output capacitor COUT = 44μF, TSS = 1.25ms soft-start time (min), it becomes the following equation when calculating the maximum output load capacitance CLOAD (max) that can be connected to VOUT.

$$C_{LOAD}(max) < \frac{(4.25 - I_{OMAX} - \Delta I_L/2) \times T_{SS}}{V_{OUT}} - C_{OUT} = 74.5 \text{ [μF]}$$

5. Phase Compensation

A current mode control buck DC/DC converter is a one-pole, one-zero system. The poles are formed by an error amplifier and the one load and the one zero point is added by the phase compensation. The phase compensation resistor R_{CMP} determines the crossover frequency F_{CRS}(15kHz (Typ)) where the total loop gain of the DC/DC converter is 0 dB. The high value of this crossover frequency F_{CRS} provides a good load transient response characteristic but inferior stability. Conversely, specifying a low value for the crossover frequency F_{CRS} greatly stabilizes the characteristics but the load transient response characteristic is impaired.

(1) Selection of Phase Compensation Resistor R_{CMP}

The phase compensation resistance R_{CMP} can be determined by using the following equation.

$$R_{CMP} = \frac{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} [\Omega]$$

where :

V_{OUT} is the output voltage

F_{CRS} is the crossover frequency

C_{OUT} is the output capacitance

V_{FB} is the feedback reference voltage (1.0 V (Typ))

G_{MP} is the current sense gain (9A/V (Typ))

G_{MA} is the error amplifier transconductance (150 µA/V (Typ))

(2) Selection of phase compensation capacitance C_{CMP}

For stable operation of the DC/DC converter, inserting a zero point under 1/9 of the zero crossover frequency cancels the phase delay due to the pole formed by the load often, thus, providing favorable characteristics.

The phase compensation capacitance C_{CMP} can be determined by using the following equation.

$$C_{CMP} = \frac{1}{2\pi \times R_{CMP} \times F_Z} \quad [F]$$

where

F_Z is the Zero point inserted

* In case C_{CMP} calculation result above exceeds 15000pF, set the value of compensation capacitance C_{CMP} for use to15000pF. Setting too large C_{CMP} value may cause startup failure, etc.

(3) Loop stability

In order to secure stability of DC/DC converter, confirm there is enough phase margin on actual equipment.
Under the worst condition, it is recommended to secure phase margin more than 45°.
In practice, the characteristics may vary depending on PCB layout, routing of wiring, types of parts to use and operating environments (temperature, etc.).
Use gain-phase analyzer or FRA to confirm frequency characteristics on actual equipment. Contact the manufacturer of each measuring equipment to check its measuring method, etc.
In case these measuring equipment are not available, there is a way to deduce phase margin degree from load response.
Monitor the fluctuation of output voltage when unloaded condition is changed to maximum loaded condition. It can be said that responsiveness is low when fluctuation is significant, and that phase margin degree is small when ringing is made many times after the condition change. Normally, ringing is made 2 times or more as standard.
However, this method cannot confirm a quantitative phase margin degree.

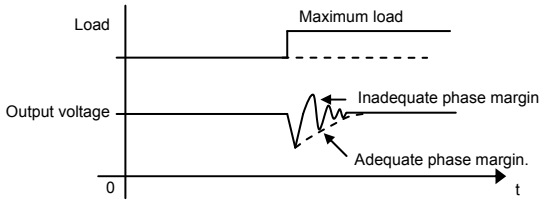


Figure 44. Load Response

6. Input voltage start-up

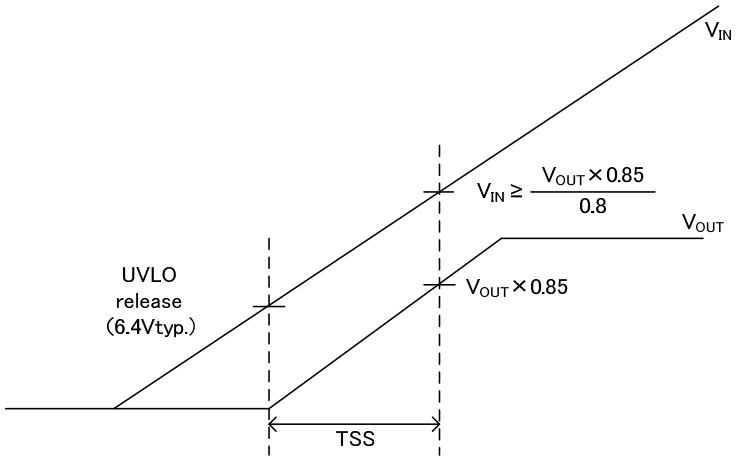


Figure 45. Input Voltage Start-up Time

Soft-start function is designed for the IC so that the output voltage will start according to the time it was decided internally. After UVLO release, the output voltage range will be less than 80% of the input voltage at soft-start operation. Please be sure that the input voltage of the soft-start after startup is as follows.

$$V_{IN} \geq \frac{V_{OUT} \times 0.85}{0.8} \text{ [V]}$$

7. Bootstrap capacitor

Bootstrap capacitor C_{BOOT} shall be 0.1μF. Connect a bootstrap capacitor between SW pin and BOOT pin.
For capacitance of Bootstrap capacitor, take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 0.047μF.

PCB Layout Design

In buck DC/DC converters, a large pulsed current flows in two loops. The first loop is the one into which the current flows when the High Side FET is turned on. The flow starts from the input capacitor CIN, runs through the FET, inductor L and output capacitor COUT and back to ground of CIN via ground of COUT. The second loop is the one into which the current flows when the Low Side FET is turned on. The flow starts from the Low Side FET, runs through the inductor L and output capacitor COUT and back to ground of the Low Side FET via ground of COUT. Tracing these two loops as thick and short as possible allows noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors, in particular, to the ground plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

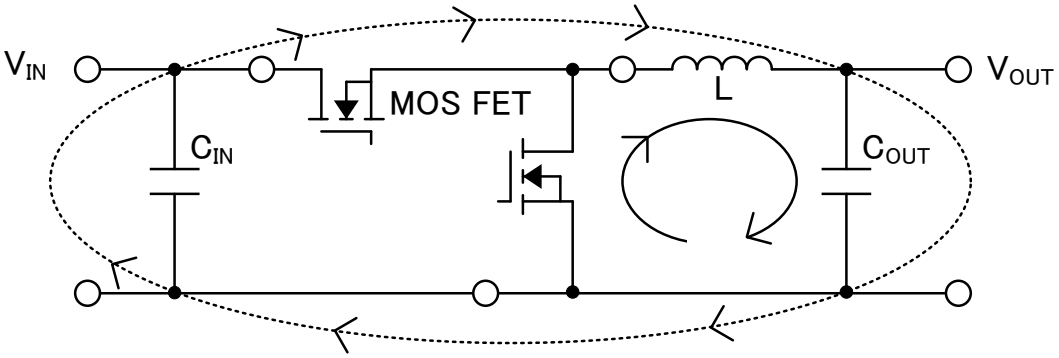
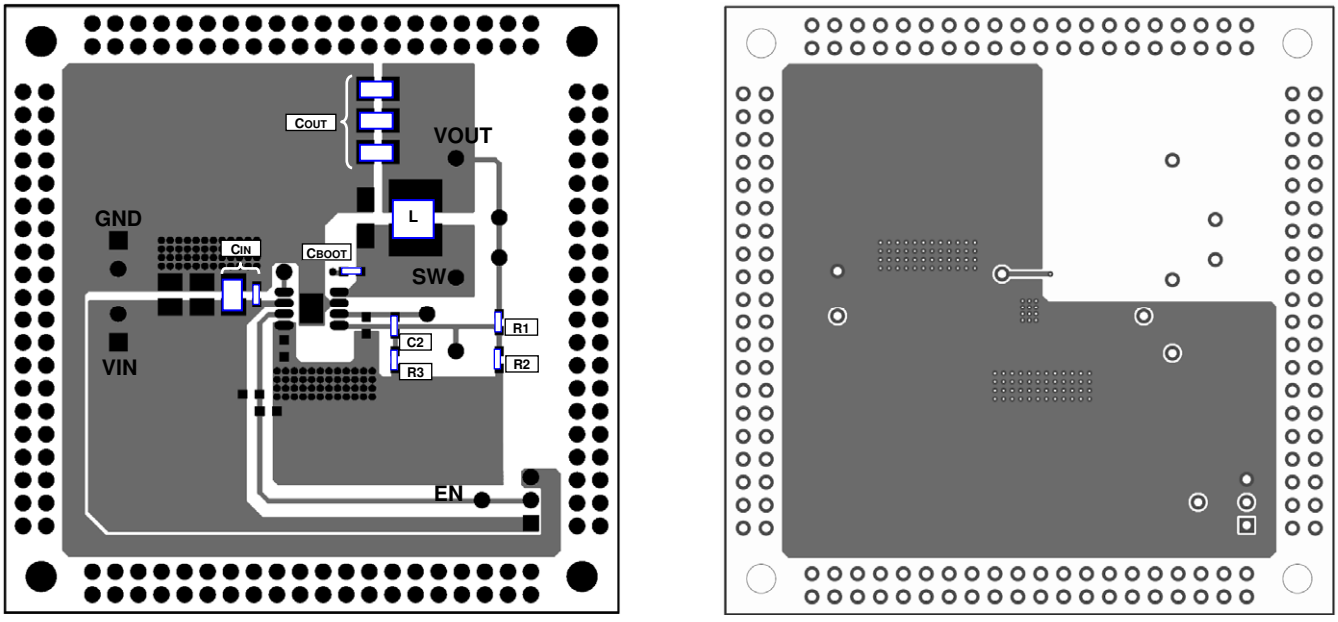


Figure 46. Current Loop of Buck Converter

Accordingly, design the PCB layout with particular attention paid to the following points.

- Provide the input capacitor as close to the VIN terminal as possible on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the ground node to assist in heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Trace to the inductor as thick and as short as possible.
- Provide lines connected to FB and COMP as far as possible from the SW node.
- Provide the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.



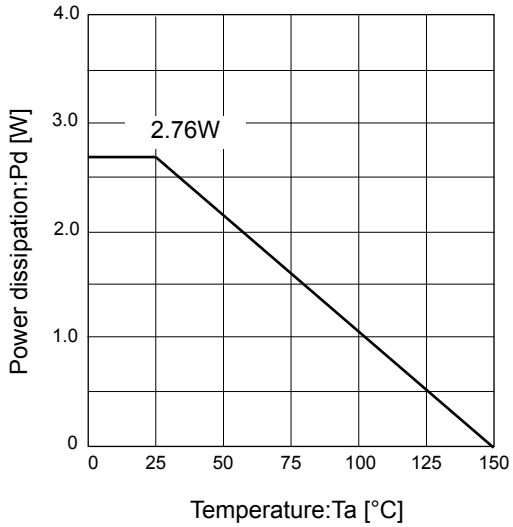
Top Layer Bottom Layer

Figure 47. Example of Sample Board Layout Pattern

Power Dissipation

Take into careful consideration that the power dissipation is within the allowable dissipation curve to design the PCB layout and peripheral circuits.

HTSOP-J8



Mounting on ROHM standard board based on JEDEC.
Board specification: FR4 (Glass-Epoxy), 114.3mm × 76.2 mm ×1.6 mm

Copper foil on the front side: ROHM recommended land pattern + wiring to measure.

PCB: 4-layer PCB
(copper foil area on 2nd & 3rd layer and reverse side,
74.2 mm × 74.2 mm)

Copper foil thickness: Front side and reverse side 70µm be used,
2nd & 3rd 35µm be used.

Condition: θ_{JA} = 45.2 °C / W

Figure 48. Power Dissipation (HTSOP-J8)

I/O equivalence circuit(s)

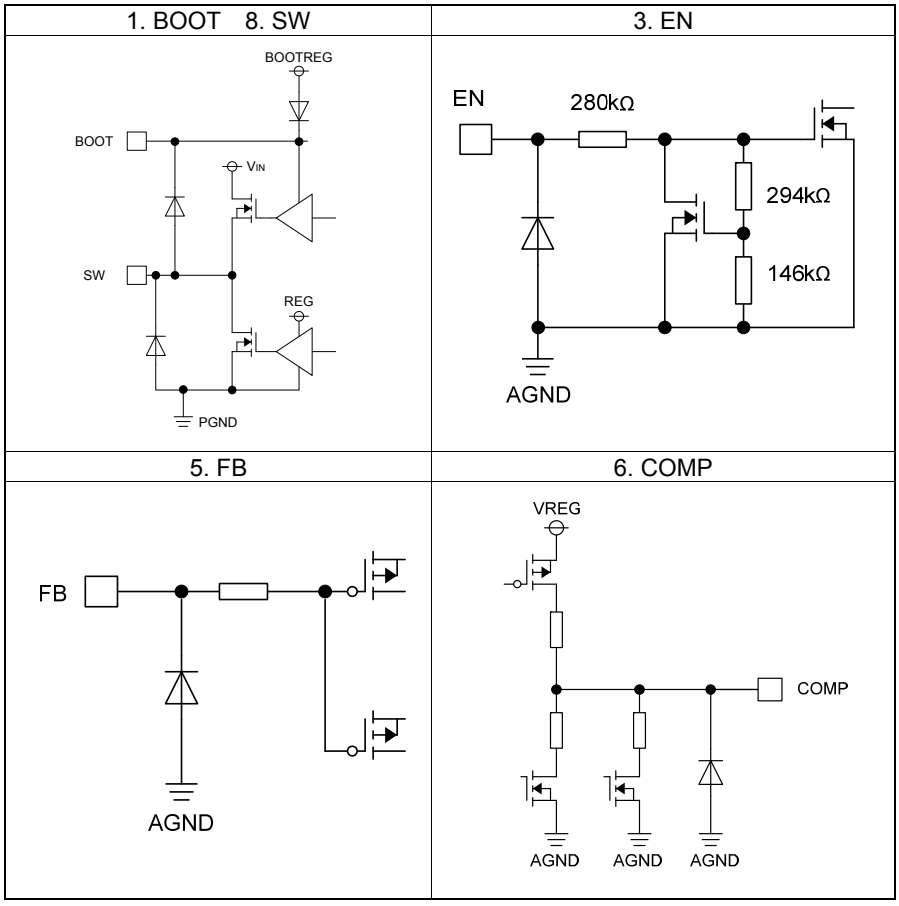


Figure 49. I/O Equivalent Circuit Chart

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

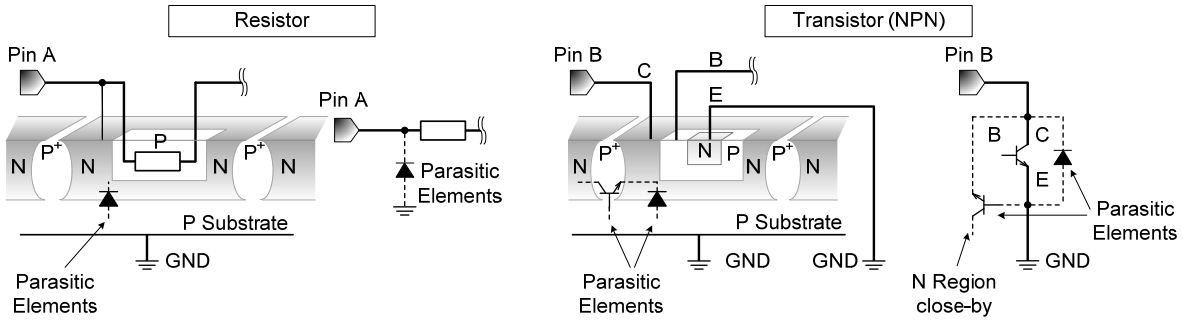


Figure 50. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.