Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

BF1100; BF1100R

Dual-gate MOS-FETs

Rev. 02 — 13 November 2007 Product data sheet

IMPORTANT NOTICE

Dear customer,

As from October 1st, 2006 Philips Semiconductors has a new trade name
- NXP Semiconductors, which will be used in future data sheets together with new contact details.
In data sheets where the previous Philips references remain, please use the new links as shown below.

http://www.philips.semiconductors.com use http://www.nxp.com

http://www.semiconductors.philips.com use http://www.nxp.com (Internet)

sales.addresses@www.semiconductors.philips.com use salesaddresses@nxp.com (email)

The copyright notice at the bottom of each page (or elsewhere in the document, depending on the version)
- © Koninklijke Philips Electronics N.V. (year). All rights reserved -
is replaced with:
- © NXP B.V. (year). All rights reserved. -

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or phone (details via salesaddresses@nxp.com). Thank you for your cooperation and understanding,

NXP Semiconductors

NXP founded by Philips

Dual-gate MOS-FETs BF1100; BF1100R

FEATURES

- Specially designed for use at 9 to 12 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications such as television tuners and professional communications equipment.

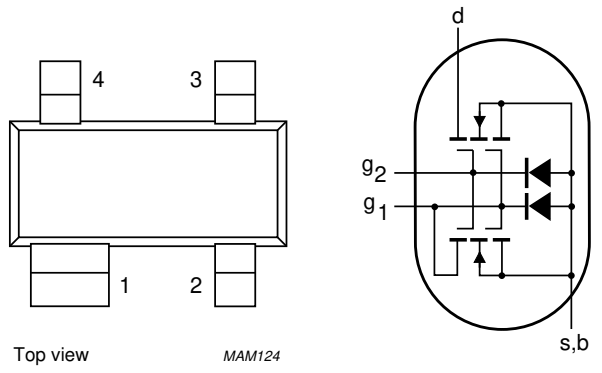
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143 or SOT143R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

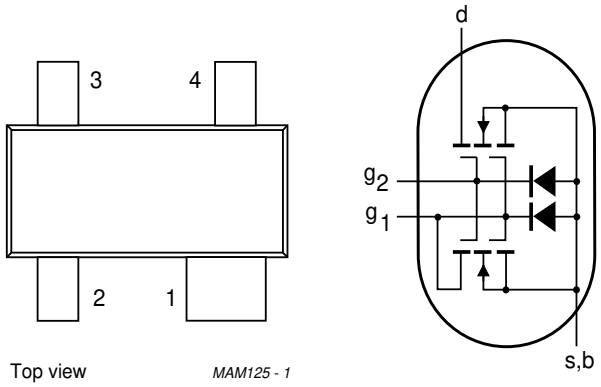
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



BF1100 marking code: %MY.

Fig.1 Simplified outline (SOT143) and symbol.



BF1100R marking code: %MZ.

Fig.2 Simplified outline (SOT143R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	14	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		24	28	33	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	14	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.3			
	BF1100	up to T_{amb} = 50 °C; note 1	–	200	mW
	BF1100R	up to T_{amb} = 40 °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

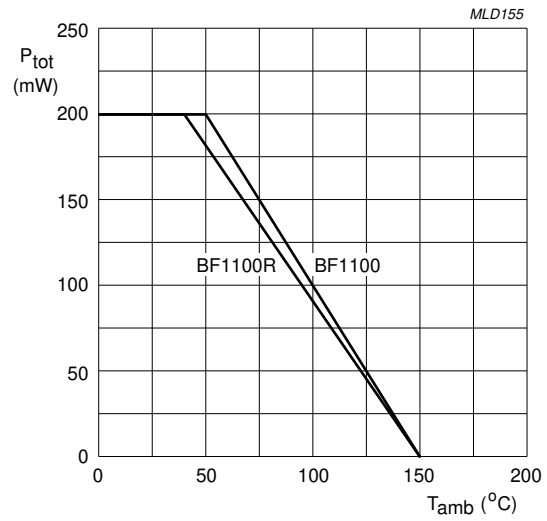


Fig.3 Power derating curves.

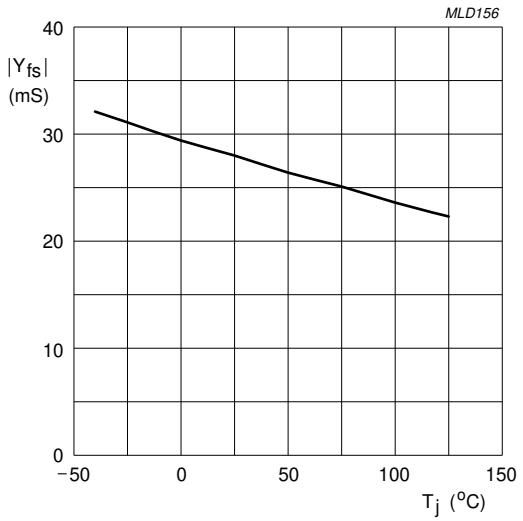


Fig.4 Forward transfer admittance as a function of junction temperature; typical values.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1		
	BF1100		500	K/W
	BF1100R		550	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2		
	BF1100	T_s = 92 °C	290	K/W
	BF1100R	T_s = 78 °C	360	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 1 mA	13.2	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 1 mA	13.2	20	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 μA	0.3	1	V
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 μA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 μA	0.3	1.2	V
		$V_{G1\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 μA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; R_{G1} = 180 kΩ; note 1	8	13	mA
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; R_{G1} = 250 kΩ; note 2	8	13	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 12 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 12 V	–	50	nA

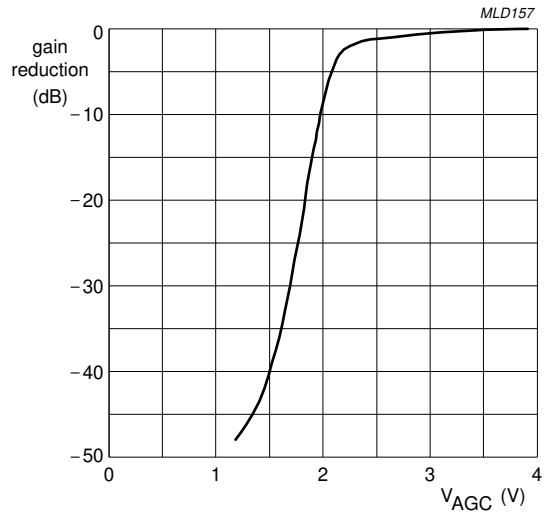
Notes

1. R_{G1} connects gate 1 to V_{GG} = 9 V; see Fig.27.
2. R_{G1} connects gate 1 to V_{GG} = 12 V; see Fig.27.

DYNAMIC CHARACTERISTICS

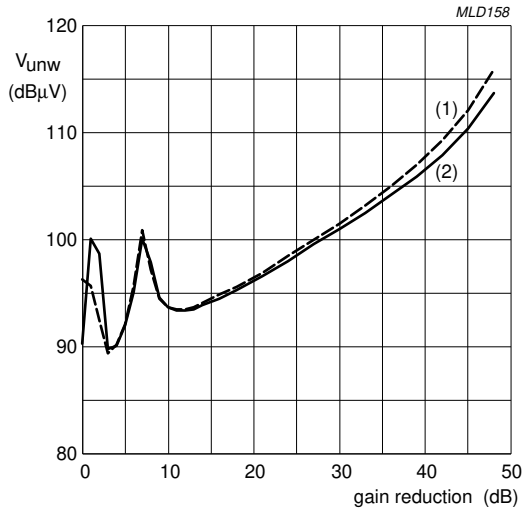
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|y_{fs}\|$	forward transfer admittance	pulsed; T_j = 25 °C				
		V_{DS} = 9 V	24	28	33	mS
		V_{DS} = 12 V	24	28	33	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz				
		V_{DS} = 9 V	–	2.2	2.6	pF
		V_{DS} = 12 V	–	2.2	2.6	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz				
		V_{DS} = 9 V	–	1.6	–	pF
		V_{DS} = 12 V	–	1.4	–	pF
C_{os}	drain-source capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	1.4	1.8	pF
		V_{DS} = 12 V	–	1.1	1.5	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	25	35	fF
		V_{DS} = 12 V	–	25	35	fF
F	noise figure	f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$				
		V_{DS} = 9 V	–	2	2.8	dB
		V_{DS} = 12 V	–	2	2.8	dB



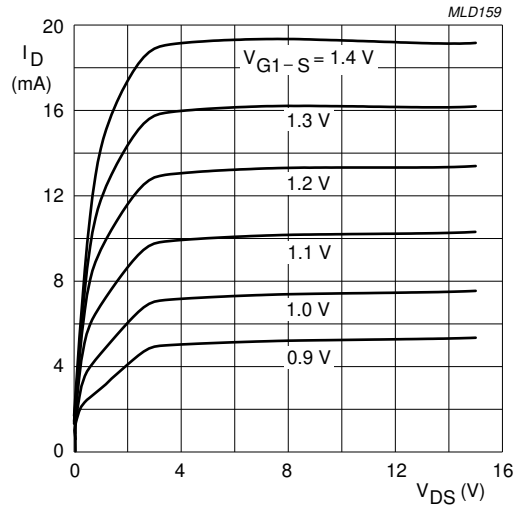
f = 50 MHz.
T_j = 25 °C.

Fig.5 Gain reduction as a function of the AGC voltage; typical values.



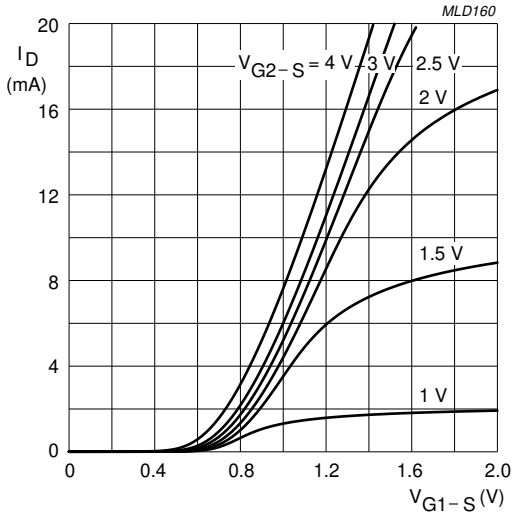
(1) R_G = 250 kΩ to V_{GG} = 12 V
(2) R_G = 180 kΩ to V_{GG} = 9 V
f_w = 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.6 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.27.



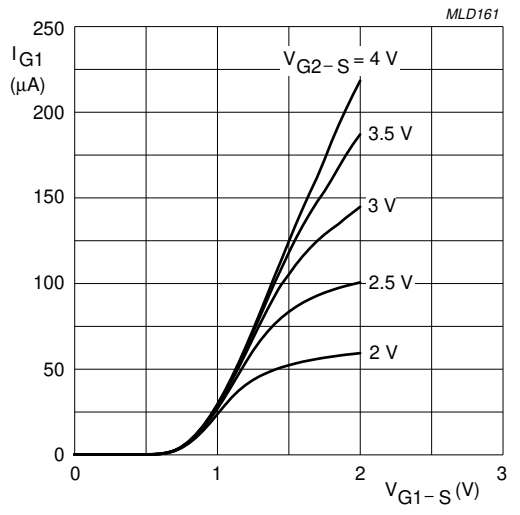
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.7 Output characteristics; typical values.



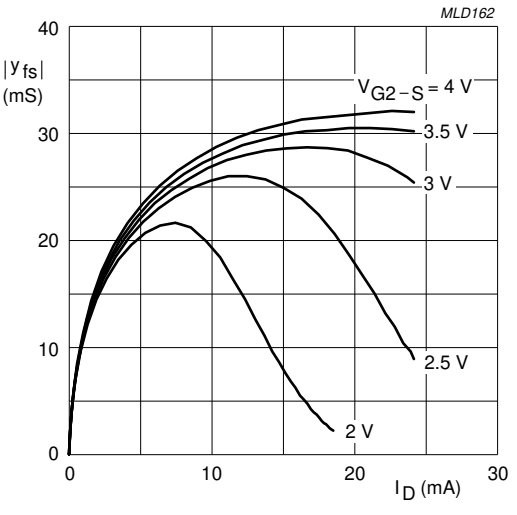
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.8 Transfer characteristics; typical values.



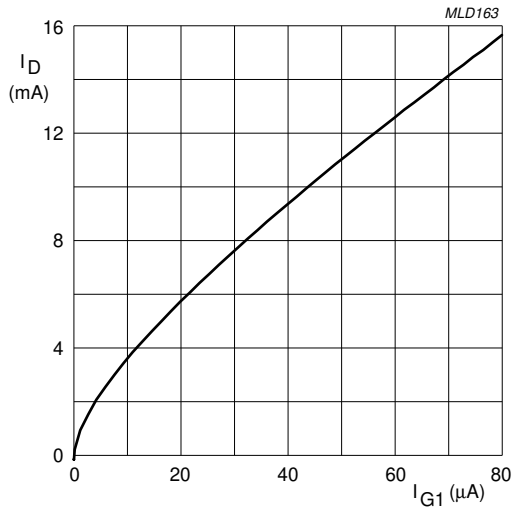
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.9 Gate 1 current as a function of gate 1 voltage; typical values.



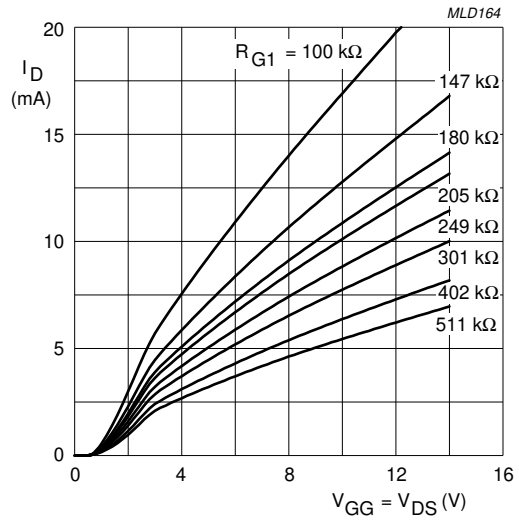
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.10 Forward transfer admittance as a function of drain current; typical values.



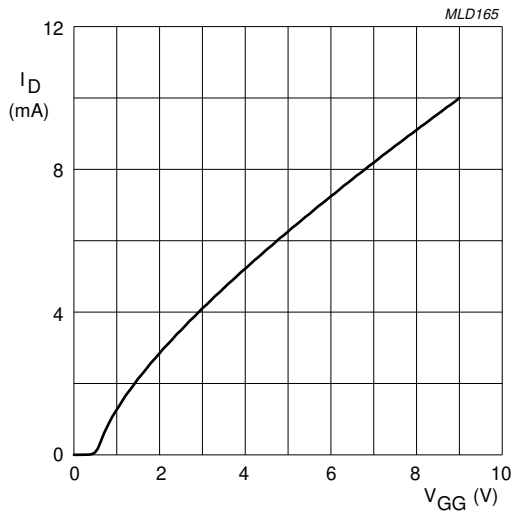
V_{DS} = 9 to 12 V.
$V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 current; typical values.



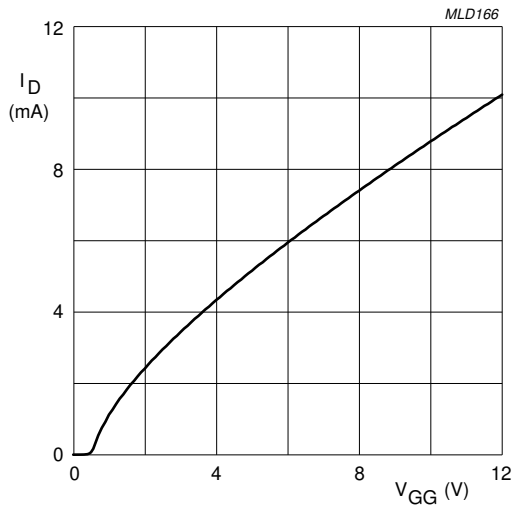
$V_{G2\text{-}S}$ = 4 V.
R_{G1} connected to V_{GG}.
T_j = 25 °C.

Fig.12 Drain current as a function of gate 1 supply voltage (= V_{GG}) and drain supply voltage; typical values; see Fig.27.



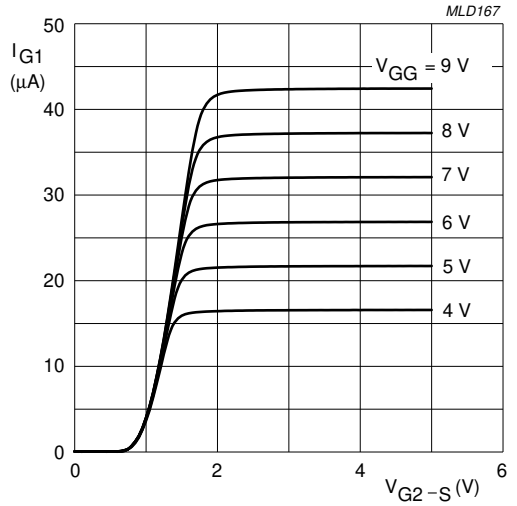
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.13 Drain current as a function of gate 1 voltage (= V_{GG}); typical values; see Fig.27.



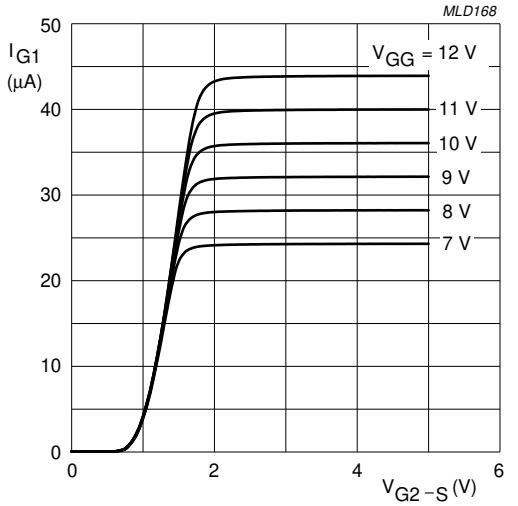
V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.14 Drain current as a function of gate 1 voltage; (= V_{GG}); typical values; see Fig.27.



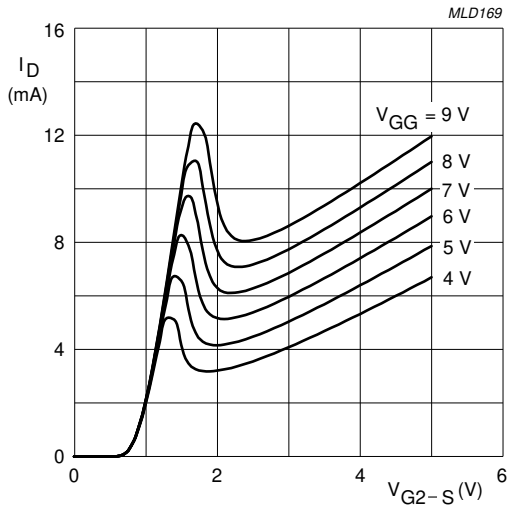
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.15 Gate 1 current as a function of gate 2 voltage; typical values.



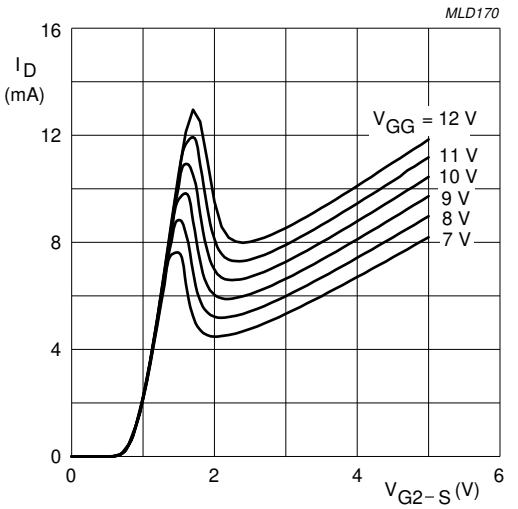
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.16 Gate 1 current as a function of gate 2 voltage; typical values.



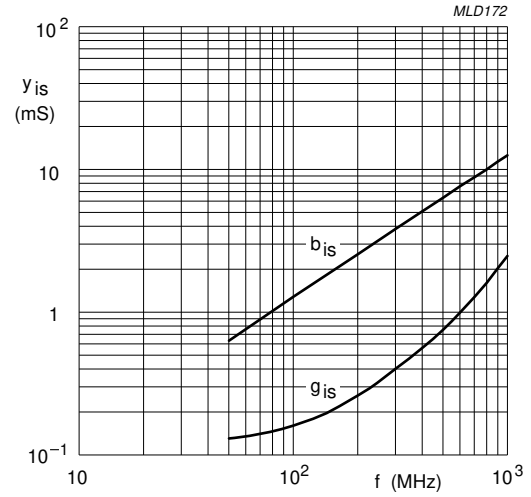
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.17 Drain current as a function of the gate 2 voltage; typical values; see Fig.27.



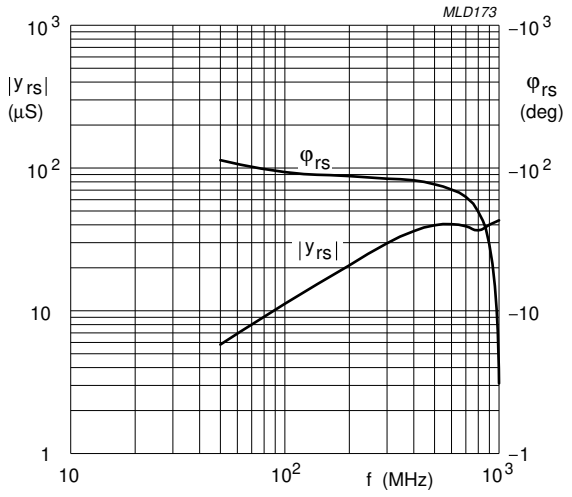
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.18 Drain current as a function of the gate 2 voltage; typical values; see Fig.27.



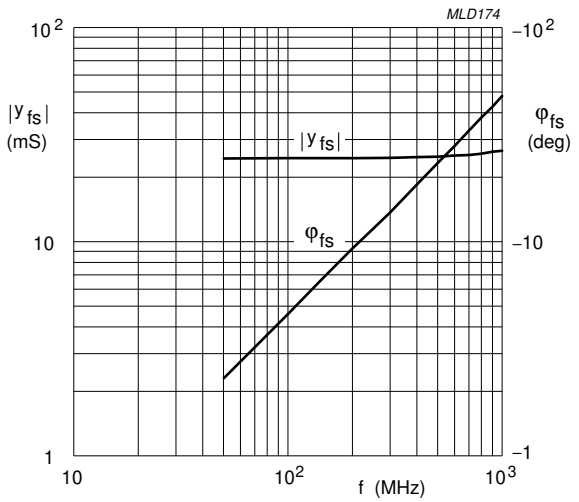
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.19 Input admittance as a function of frequency; typical values.



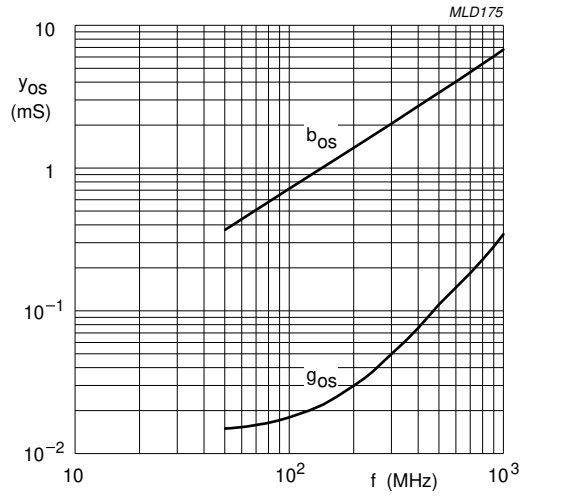
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse transfer admittance and phase as a function of frequency; typical values.



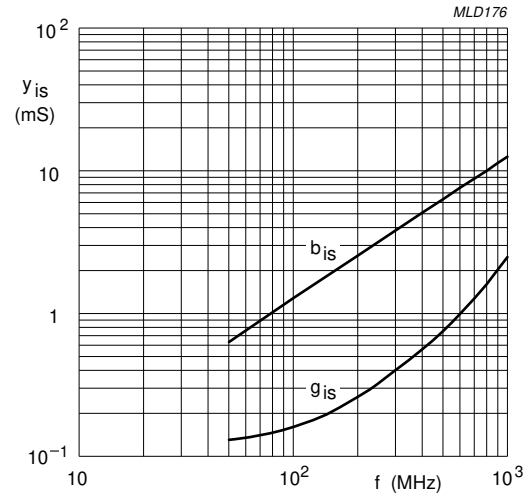
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Forward transfer admittance and phase as a function of frequency; typical values.



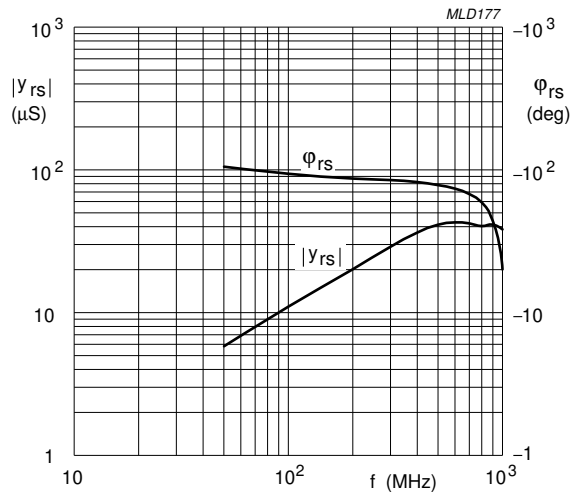
V_{DS} = 9 V; V_{G2} = 4 V.
I_D =10 mA; T_{amb} = 25 °C.

Fig.22 Output admittance as a function of frequency; typical values.



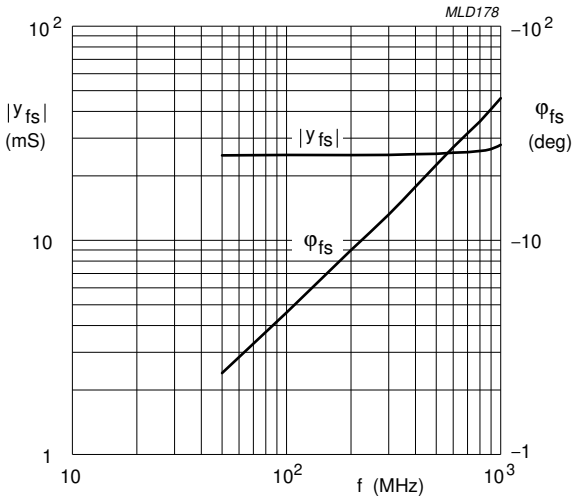
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.23 Input admittance as a function of frequency; typical values.



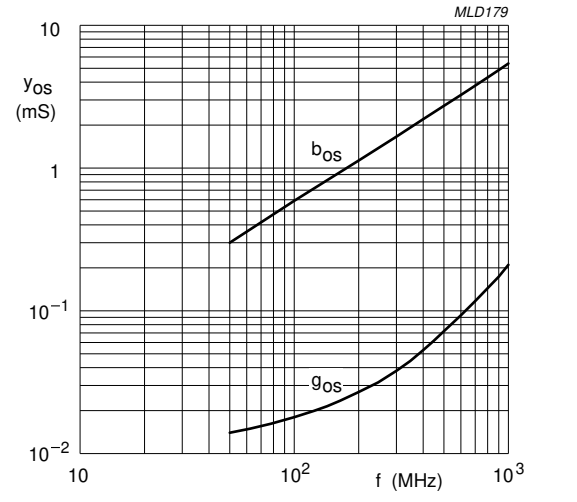
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.24 Reverse transfer admittance and phase as a function of frequency; typical values.



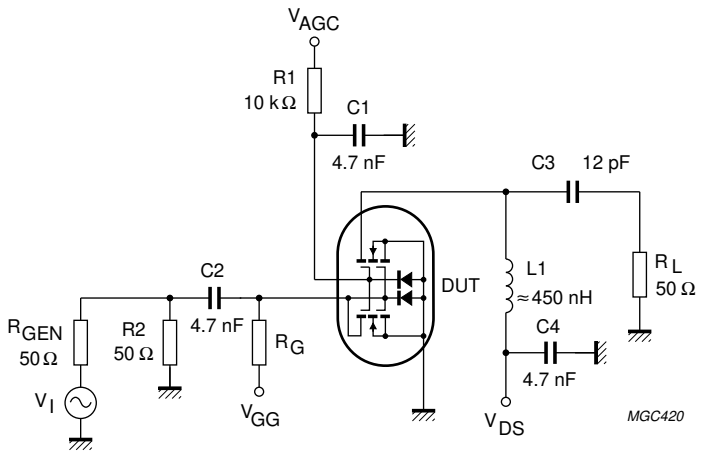
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.25 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.26 Output admittance as a function of frequency; typical values.



For $V_{GG} = V_{DS} = 9$ V, $R_G = 180$ kΩ.
For $V_{GG} = V_{DS} = 12$ V, $R_G = 250$ kΩ.

Fig.27 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.986	−3.6	2.528	174.4	0.001	63.7	1.000	−2.0
100	0.983	−7.4	2.531	169.8	0.001	80.7	1.000	−4.2
200	0.974	−14.7	2.490	159.5	0.002	81.0	0.996	−8.1
300	0.960	−21.8	2.446	149.8	0.002	80.3	0.994	−11.9
400	0.953	−28.7	2.412	139.8	0.003	76.3	0.992	−15.7
500	0.933	−35.4	2.341	130.1	0.003	76.5	0.987	−19.4
600	0.915	−42.0	2.283	120.4	0.004	79.0	0.984	−23.0
700	0.895	−47.9	2.205	111.6	0.003	81.5	0.981	−26.7
800	0.880	−53.5	2.146	102.9	0.003	90.8	0.978	−30.3
900	0.864	−59.6	2.087	93.4	0.003	106.6	0.974	−33.9
1000	0.839	−65.0	1.998	84.4	0.003	135.4	0.971	−37.6

Table 2 Noise data: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.67	43.9	0.89

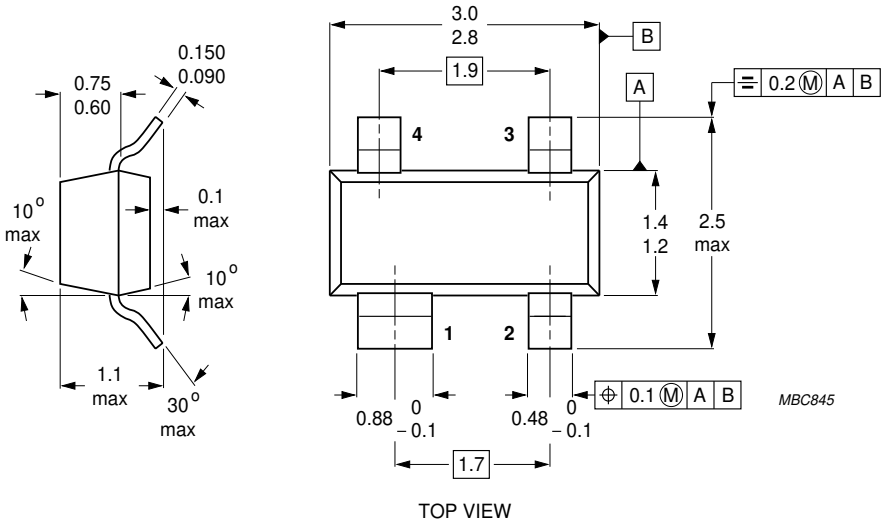
Table 3 Scattering parameters: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.986	−3.7	2.478	174.7	0.001	72.2	1.000	−1.6
100	0.984	−7.4	2.480	170.3	0.001	80.9	1.000	−3.5
200	0.974	−14.6	2.440	160.6	0.002	82.7	0.997	−6.6
300	0.960	−21.8	2.400	151.4	0.002	79.9	0.996	−9.7
400	0.953	−28.7	2.371	141.9	0.003	77.7	0.994	−12.8
500	0.933	−35.3	2.306	132.7	0.003	77.1	0.991	−15.8
600	0.915	−41.9	2.255	123.6	0.004	77.1	0.989	−18.7
700	0.894	−47.8	2.183	115.3	0.004	79.3	0.986	−21.7
800	0.879	−53.5	2.131	107.2	0.003	83.9	0.984	−24.6
900	0.863	−59.5	2.080	98.2	0.003	95.1	0.982	−27.5
1000	0.838	−65.0	1.999	89.7	0.003	115.8	0.980	−30.4

Table 4 Noise data: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.66	43.3	0.97

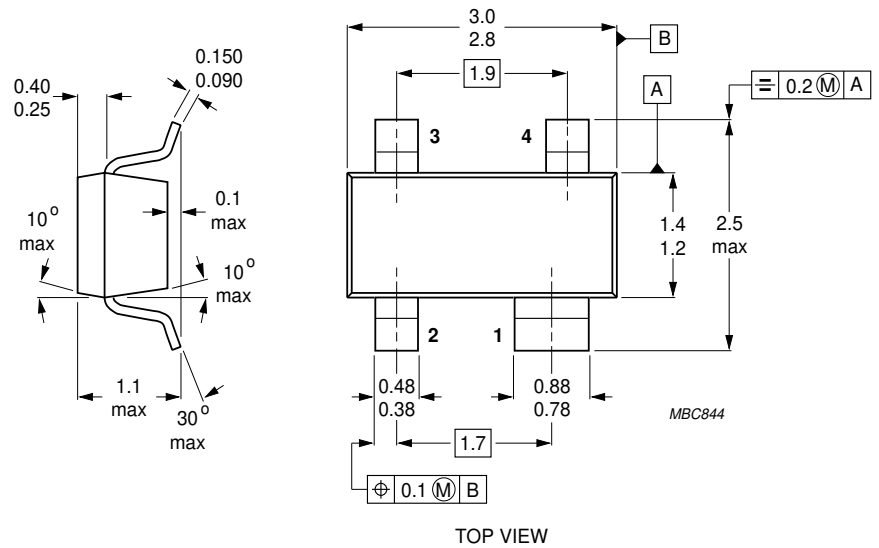
PACKAGE OUTLINES



TOP VIEW

Dimensions in mm.

Fig.28 SOT143.



TOP VIEW

Dimensions in mm.

Fig.29 SOT143R.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

Revision history

Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BF1100_N_2	20071113	Product data sheet	-	BF1100_1
Modifications:	• Fig. 1 and 2 on page 2; Figure note changed			
BF1100_1	19950425	Product specification	-	-

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2007. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 November 2007

Document identifier: BF1100_N_2

founded by

PHILIPS