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BF1217WR

N-channel dual gate MOSFET

Rev. 2 — 20 June 2011 Product data sheet

1. Product profile

1.1 General description

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1217WR is encapsulated in the SOT343R plastic package.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

- Excellent low frequency noise performance
- Superior cross modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio

1.3 Applications

- Gain controlled low noise amplifiers for VHF and UHF applications with 5 V supply voltage
  - digital and analog television tuners
  - professional communication equipment

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	DC		-	-	6	V
I_D	drain current	DC		-	-	30	mA
P_{tot}	total power dissipation	$T_{sp} \leq 107$ °C	[1]	-	-	180	mW
$\|y_{fs}\|$	forward transfer admittance	f = 100 MHz; T_j = 25 °C; I_D = 18 mA		23	27	38	mS
$C_{iss(G1)}$	input capacitance at gate1	f = 100 MHz	[2]	-	2.5	-	pF
C_{rss}	reverse transfer capacitance	f = 100 MHz	[2]	-	20	-	fF
NF	noise figure	f = 400 MHz; $Y_S = Y_{S(opt)}$		-	1.0	-	dB
		f = 800 MHz; $Y_S = Y_{S(opt)}$		-	1.5	-	dB
Xmod	cross modulation	input level for k = 1 % at 40 dB AGC; f_w = 50 MHz; f_{unw} = 60 MHz	[3]	105	107	-	dBμV
T_j	junction temperature			-	-	150	°C

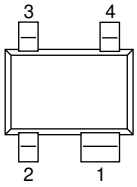
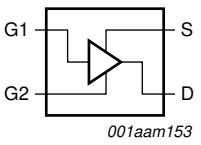
[1] T_{sp} is the temperature at the soldering point of the source lead.

[2] Calculated from S-parameters.

[3] Measured in Figure 17 test circuit.

2. Pinning information

Table 2. Discrete pinning

Pin	Description	Simplified outline	Graphic symbol
1	source		
2	drain		
3	gate 2		
4	gate 1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BF1217WR	-	plastic surface-mounted package; reverse pinning; 4 leads	SOT343R

4. Marking

Table 4. Marking

Type number	Marking	Description
BF1217WR	VA%	% = p : made in Hong Kong
		% = t : made in Malaysia
		% = w : made in China

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per MOSFET						
V_{DS}	drain-source voltage	DC		-	6	V
I_D	drain current	DC		-	30	mA
I_{G1}	gate1 current			-	±10	mA
I_{G2}	gate2 current			-	±10	mA
P_{tot}	total power dissipation	$T_{sp} \leq 107$ °C	[1]	-	180	mW
T_{stg}	storage temperature			−65	+150	°C
T_j	junction temperature			-	150	°C

[1] T_{sp} is the temperature at the soldering point of the source lead.

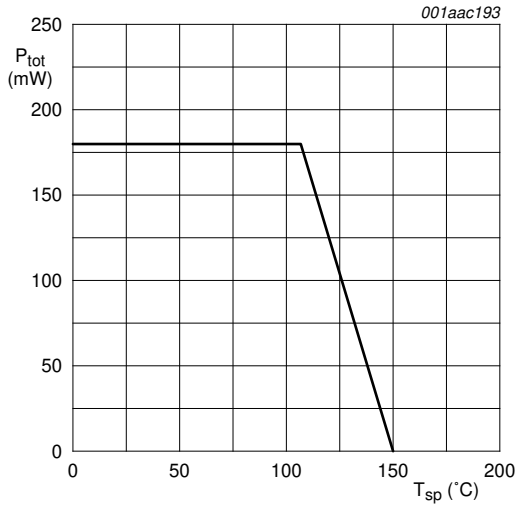


Fig 1. Power derating curve

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		240	K/W

7. Static characteristics

Table 7. Static characteristics

T_j = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per MOSFET; unless otherwise specified							
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{G1-S} = V_{G2-S} = 0 V; I_D = 10 μA		6	-	-	V
$V_{(BR)G1-SS}$	gate1-source breakdown voltage	V_{G2-S} = V_{DS} = 0 V; I_{G1-S} = 10 mA		6	-	10	V
$V_{(BR)G2-SS}$	gate2-source breakdown voltage	V_{G1-S} = V_{DS} = 0 V; I_{G2-S} = 10 mA		6	-	10	V
$V_{F(S-G1)}$	forward source-gate1 voltage	V_{G2-S} = V_{DS} = 0 V; I_{S-G1} = 10 mA		0.5	-	1.5	V
$V_{F(S-G2)}$	forward source-gate2 voltage	V_{G1-S} = V_{DS} = 0 V; I_{S-G2} = 10 mA		0.5	-	1.5	V
$V_{G1-S(th)}$	gate1-source threshold voltage	V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 100 μA		0.3	-	1.0	V
$V_{G2-S(th)}$	gate2-source threshold voltage	V_{DS} = 5 V; V_{G1-S} = 5 V; I_D = 100 μA		0.4	-	1.0	V
I_{DS}	drain-source current	V_{G2-S} = 4 V; V_{DS} = 5 V; R_{G1} = 82 kΩ	[1]	-	-	24	mA
I_{G1-S}	gate1 cut-off current	V_{G2-S} = 0 V; V_{DS} = 0 V; V_{G1-S} = 5 V		-	-	50	nA
I_{G2-S}	gate2 cut-off current	V_{G2-S} = 4 V; V_{DS} = 0 V; V_{G1-S} = 0 V		-	-	20	nA

[1] R_{G1} connects gate1 to V_{GG} = 5 V. See Figure 17.

8. Dynamic characteristics

Table 8. Dynamic characteristics

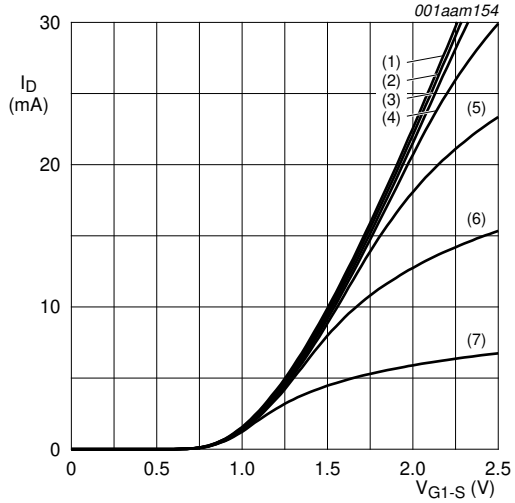
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 18 mA.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\|y_{fs}\|$	forward transfer admittance	f = 100 MHz; T_j = 25 °C		23	27	38	mS
$C_{iss(G1)}$	input capacitance at gate1	f = 100 MHz	[1]	-	2.5	-	pF
$C_{iss(G2)}$	input capacitance at gate2	f = 100 MHz	[1]	-	1.0	-	pF
C_{oss}	output capacitance	f = 100 MHz	[1]	-	0.8	-	pF
C_{rss}	reverse transfer capacitance	f = 100 MHz	[1]	-	20	-	fF
G_{tr}	transducer power gain	$B_S = B_{S(opt)}$; $B_L = B_{L(opt)}$	[1]				
		f = 200 MHz; G_S = 2 mS; G_L = 0.5 mS		-	34	-	dB
		f = 400 MHz; G_S = 2 mS; G_L = 1 mS		-	30	-	dB
		f = 800 MHz; G_S = 3.3 mS; G_L = 1 mS		-	26	-	dB
NF	noise figure	f = 400 MHz; $Y_S = Y_{S(opt)}$		-	1.0	-	dB
		f = 800 MHz; $Y_S = Y_{S(opt)}$		-	1.5	-	dB
Xmod	cross modulation	input level for k = 1 %; f_w = 50 MHz; f_{unw} = 60 MHz	[2]				
		at 0 dB AGC		90	104	-	dBμV
		at 10 dB AGC		-	100	-	dBμV
		at 20 dB AGC		-	104	-	dBμV
		at 40 dB AGC		105	107	-	dBμV

[1] Calculated from S-parameters.

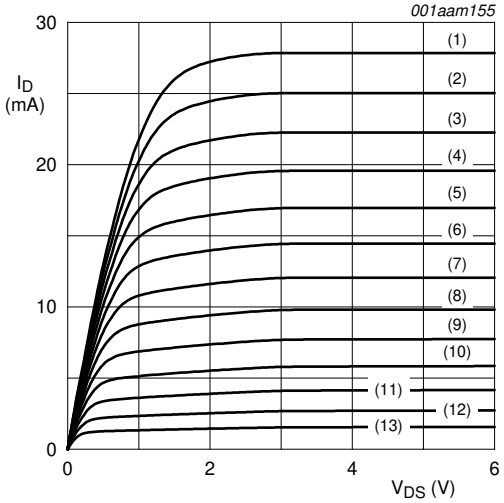
[2] Measured in Figure 17 test circuit.

8.1 Graphs



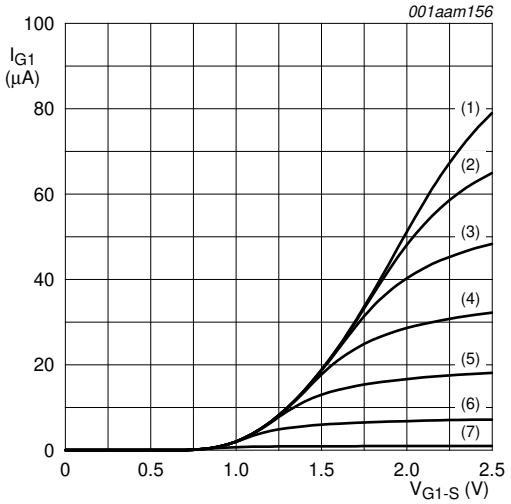
(1) V_{G2-S} = 4.0 V
(2) V_{G2-S} = 3.5 V
(3) V_{G2-S} = 3.0 V
(4) V_{G2-S} = 2.5 V
(5) V_{G2-S} = 2.0 V
(6) V_{G2-S} = 1.5 V
(7) V_{G2-S} = 1.0 V
V_{DS} = 5 V; T_j = 25 °C.

Fig 2. Transfer characteristics; typical values



(1) V_{G1-S} = 2.2 V
(2) V_{G1-S} = 2.1 V
(3) V_{G1-S} = 2.0 V
(4) V_{G1-S} = 1.9 V
(5) V_{G1-S} = 1.8 V
(6) V_{G1-S} = 1.7 V
(7) V_{G1-S} = 1.6 V
(8) V_{G1-S} = 1.5 V
(9) V_{G1-S} = 1.4 V
(10) V_{G1-S} = 1.3 V
(11) V_{G1-S} = 1.2 V
(12) V_{G1-S} = 1.1 V
(13) V_{G1-S} = 1.0 V
V_{G2-S} = 4 V; T_j = 25 °C.

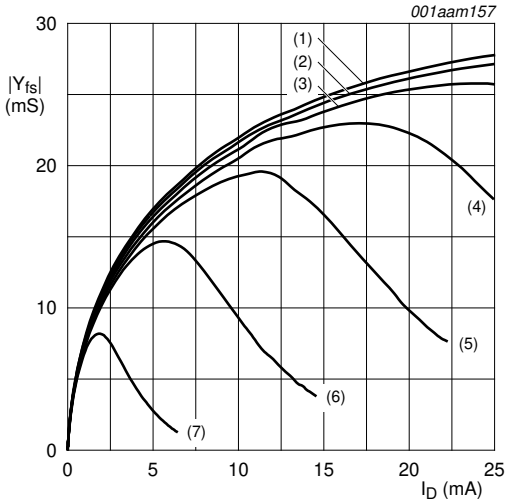
Fig 3. Output characteristics; typical values



(1) V_{G2-S} = 4.0 V
(2) V_{G2-S} = 3.5 V
(3) V_{G2-S} = 3.0 V
(4) V_{G2-S} = 2.5 V
(5) V_{G2-S} = 2.0 V
(6) V_{G2-S} = 1.5 V
(7) V_{G2-S} = 1.0 V

V_{DS} = 5 V; T_j = 25 °C.

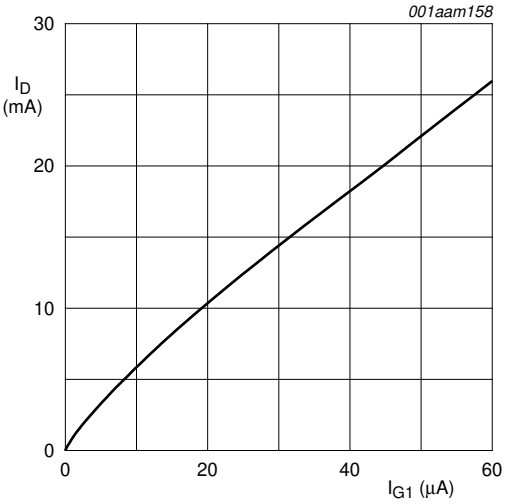
Fig 4. Gate1 current as a function of gate1 voltage; typical values



(1) V_{G2-S} = 4.0 V
(2) V_{G2-S} = 3.5 V
(3) V_{G2-S} = 3.0 V
(4) V_{G2-S} = 2.5 V
(5) V_{G2-S} = 2.0 V
(6) V_{G2-S} = 1.5 V
(7) V_{G2-S} = 1.0 V

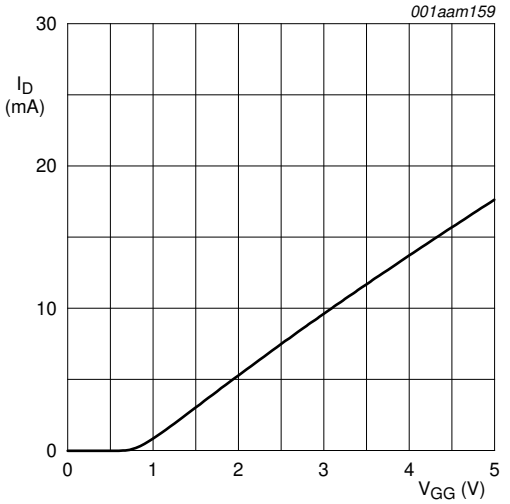
V_{DS} = 5 V; T_j = 25 °C.

Fig 5. Forward transfer admittance as a function of drain current; typical values



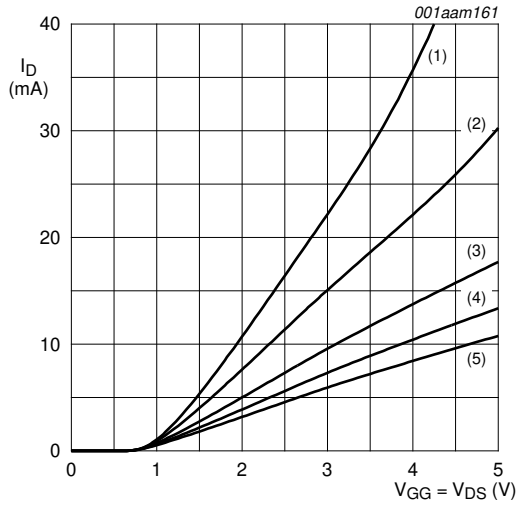
V_{DS} = 5 V; V_{G2-S} = 4 V; T_j = 25 °C.

Fig 6. Drain current as a function of gate1 current; typical values



V_{DS} = 5 V; V_{G2-S} = 4 V; R_{G1} = 82 kΩ; T_j = 25 °C.

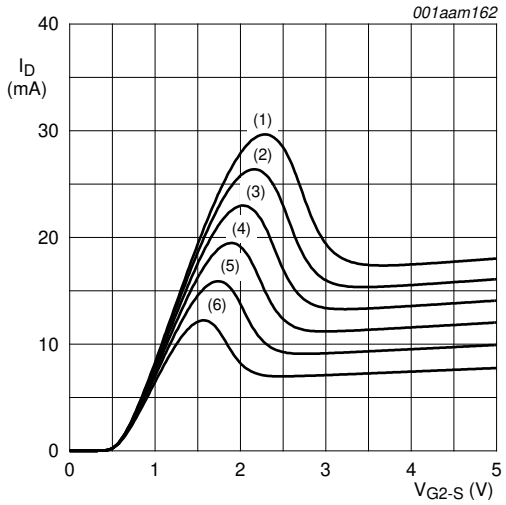
Fig 7. Drain current as a function of gate1 supply voltage (V_{GG}); typical values



(1) R_{G1} = 20 kΩ
(2) R_{G1} = 40 kΩ
(3) R_{G1} = 80 kΩ
(4) R_{G1} = 120 kΩ
(5) R_{G1} = 160 kΩ

V_{G2-S} = 4 V; T_j = 25 °C.

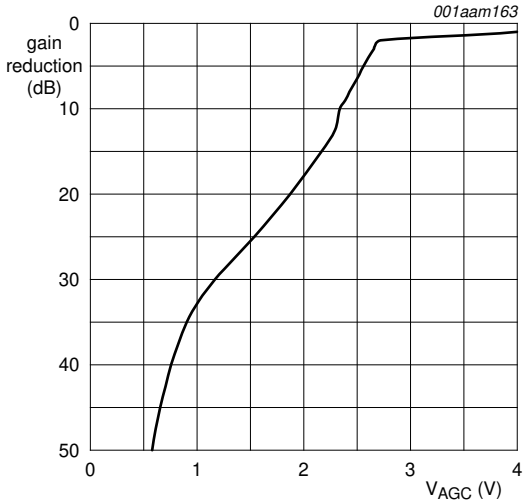
Fig 8. Drain current as a function of V_{DS} and V_{GG}; typical values



(1) V_{GG} = 5.0 V
(2) V_{GG} = 4.5 V
(3) V_{GG} = 4.0 V
(4) V_{GG} = 3.5 V
(5) V_{GG} = 3.0 V
(6) V_{GG} = 2.5 V

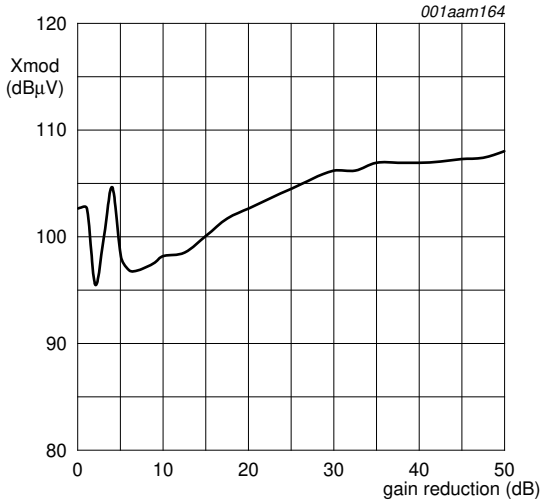
T_j = 25 °C; R_{G1} = 82 kΩ (connected to V_{GG}).

Fig 9. Drain current as a function of gate2 voltage; typical values



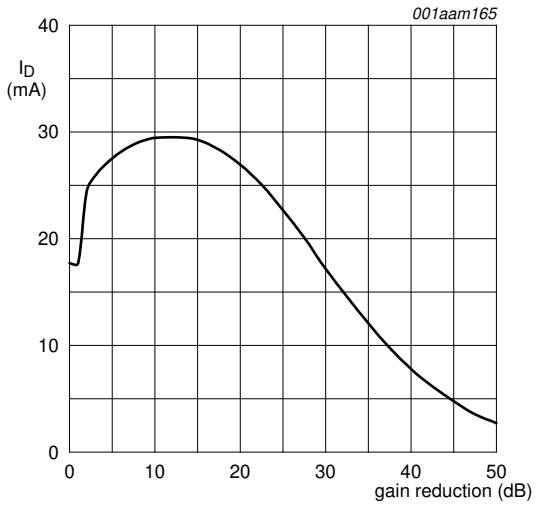
V_{DS} = 5 V; V_{GG} = 5 V; $I_{D(nom)}$ = 19 mA; R_{G1} = 82 kΩ; f = 50 MHz; T_j = 25 °C; see Figure 17.

Fig 10. Typical gain reduction as a function of the AGC voltage; typical values



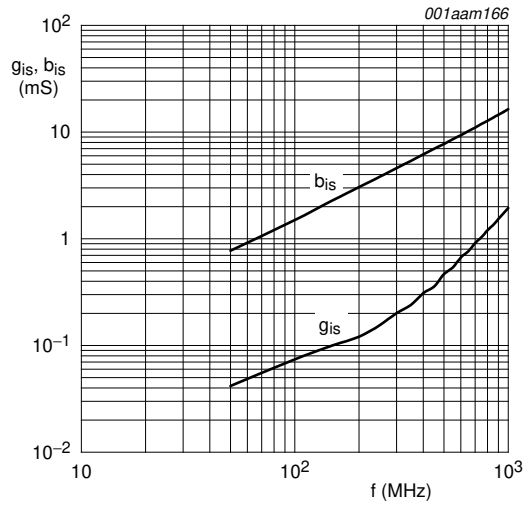
V_{DS} = 5 V; V_{GG} = 5 V; $V_{G2\text{-}S(nom)}$ = 4 V; R_{G1} = 82 kΩ; f_w = 50 MHz; f_{unw} = 60 MHz; $I_{D(nom)}$ = 19 mA; T_j = 25 °C; see Figure 17.

Fig 11. Unwanted voltage for 1 % cross modulation as a function of gain reduction; typical values



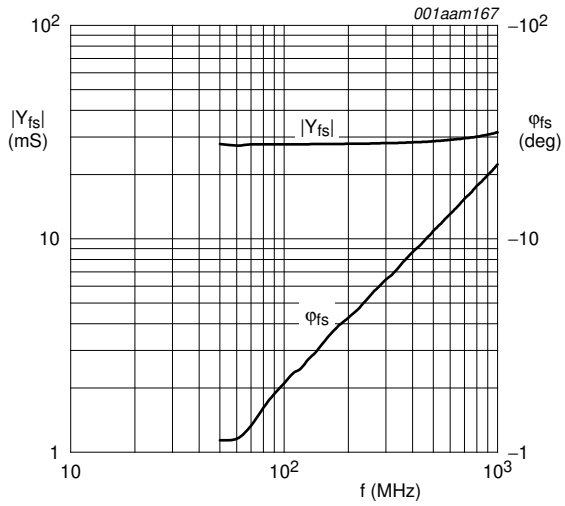
V_{DS} = 5 V; V_{GG} = 5 V; $V_{G2\text{-}S(nom)}$ = 4 V; R_{G1} = 82 kΩ; f_w = 50 MHz; $I_{D(nom)}$ = 19 mA; T_j = 25 °C; see Figure 17.

Fig 12. Typical drain current as a function of gain reduction; typical values



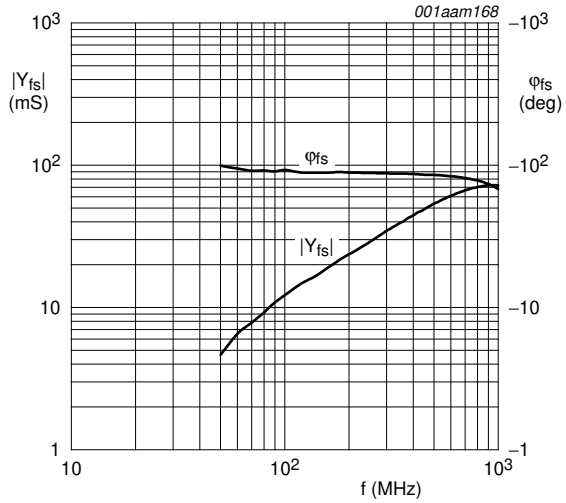
V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 19 mA.

Fig 13. Input admittance as a function of frequency; typical values



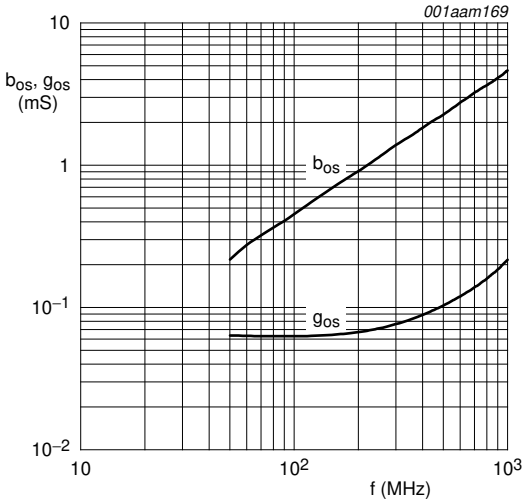
V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 19 mA.

Fig 14. Forward transfer admittance and phase as a function of frequency; typical values



V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 19 mA.

Fig 15. Reverse transfer admittance and phase as a function of frequency; typical values



V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 19 mA.

Fig 16. Output admittance as a function of frequency; typical values

8.2 Scattering parameters

Table 9. Scattering parameters

V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 19 mA; T_{amb} = 25 °C; Z_0 = 50 Ω; typical values.

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)
40	0.9960	−3.50	2.77	177.20	0.00034	82.80	0.9945	−1.00
50	0.9957	−4.46	2.76	176.02	0.00046	82.50	0.9944	−1.28
100	0.9935	−8.66	2.74	172.19	0.00121	81.86	0.9938	−2.69
200	0.9880	−17.55	2.73	164.42	0.00231	80.28	0.9927	−5.39
300	0.9805	−26.17	2.69	156.64	0.00331	75.66	0.9909	−8.17
400	0.9712	−34.58	2.64	149.07	0.00414	71.21	0.9896	−10.79
500	0.9589	−42.78	2.58	141.74	0.00482	67.42	0.9872	−13.30
600	0.9451	−50.61	2.52	134.58	0.00526	64.33	0.9850	−16.08
700	0.9309	−58.23	2.45	127.49	0.00549	61.90	0.9836	−18.74
800	0.9166	−65.68	2.37	120.79	0.00551	60.77	0.9818	−21.05
900	0.9034	−72.70	2.29	114.37	0.00536	60.73	0.9796	−23.59
1000	0.8894	−79.30	2.22	107.90	0.00505	62.45	0.9781	−26.44

8.3 Noise data

Table 10. Noise data

V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 19 mA, T_{amb} = 25 °C; typical values.

f (MHz)	NF_{min} (dB)	Γ_{opt}		r_n (ratio)
		(ratio)	(deg)	
400	1.0	0.798	29.5	0.907
800	1.5	0.703	57.7	0.749

9. Test information

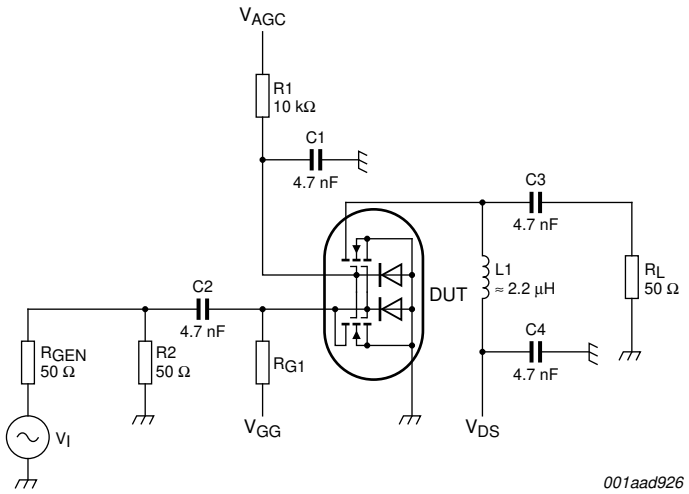
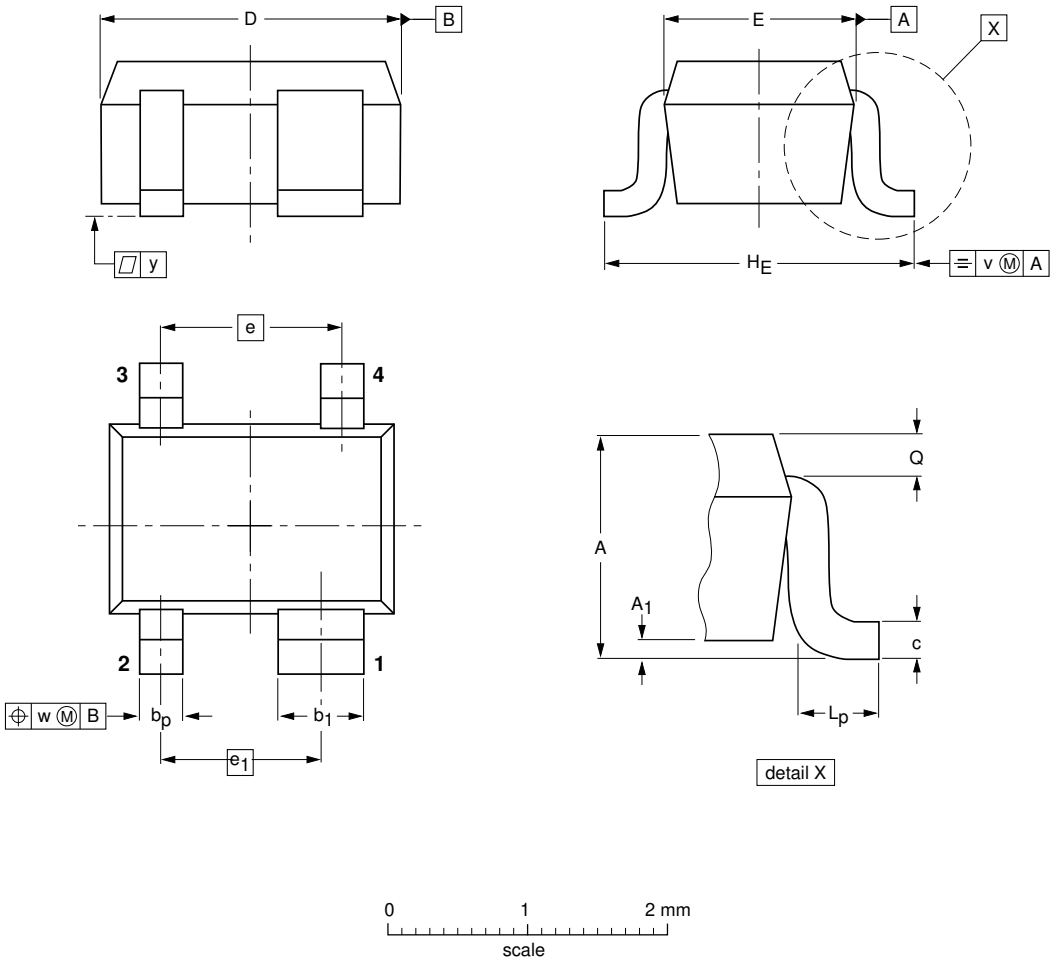


Fig 17. Cross modulation test setup

10. Package outline

Plastic surface-mounted package; reverse pinning; 4 leads **SOT343R**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						~~97-05-21~~ 06-03-16

Fig 18. Package outline SOT343

11. Abbreviations

Table 11. Abbreviations

Acronym	Description
AGC	Automatic Gain Control
DC	Direct Current
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
UHF	Ultra High Frequency
VHF	Very High Frequency

12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BF1217WR v.2	20110620	Product data sheet	-	BF1217WR v.1
Modifications:	• Package outline corrected.			
BF1217WR v.1	20100803	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

13.2 Definitions

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14. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

15. Contents

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