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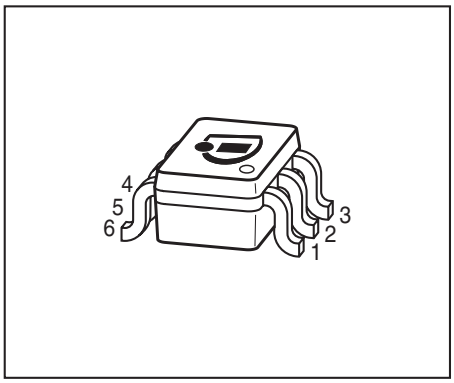
DUAL N-Channel MOSFET Tetrode

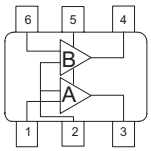


- Designed for input stages of 2 band tuners
- Two AGC amplifiers in one single package with on-chip internal switch
- Only one switching line to control both FETs
- Integrated gate protection diodes
- High gain, low noise figure, high AGC-range
- Good cross modulation at gain reduction
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101

Detailed functional diagram on page 4

AEC Qualified RoHS

BG3430R



ESD (**E**lectro**s**tatic **d**ischarge) sensitive device, observe handling precaution!

Type	Package	Pin Configuration						Marking
BG3430R	SOT363	1=G1*	2=S	3=D*	4=D**	5=G2	6=G1**	KNs

* For amp. A; ** for amp. B

180° rotated tape loading orientation available

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	8	V
Continuous drain current	I_D	25	mA
Gate 1/ gate 2-source current	$\pm I_{G1/2SM}$	1	
Gate 1/ gate 2-source voltage	$\pm V_{G1/G2S}$	6	V
Total power dissipation	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel - soldering point[1)]	R_{thchs}	≤ 280	K/W

[1]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at T_A = 25°C, unless otherwise specified

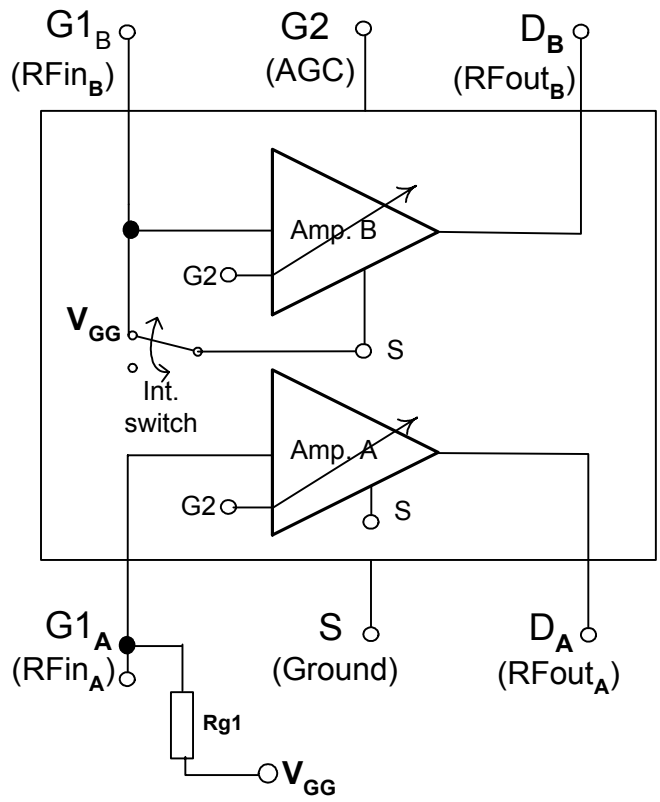
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage I_D = 100 µA, V_{G1S} = 0 V, V_{G2S} = 0 V	$V_{(BR)DS}$	12	-	-	V
Gate1-source breakdown voltage +I_{G1S} = 10 mA, V_{G2S} = 0 V, V_{DS} = 0 V	+$V_{(BR)G1SS}$	6	-	15	
Gate2-source breakdown voltage +I_{G2S} = 10 mA, V_{G1S} = 0 V, V_{DS} = 0 V	+$V_{(BR)G2SS}$	6	-	15	
Gate1-source leakage current V_{G1S} = 6 V, V_{G2S} = 0 V	+I_{G1SS}	-	-	5	µA
Gate2-source leakage current V_{G2S} = 6 V, V_{G1S} = 0 V, V_{DS} = 0 V	+I_{G2SS}	-	-	50	nA
Drain current V_{DS} = 5 V, V_{G1S} = 0 V, V_{G2S} = 4 V	I_{DSS}	-	-	100	µA
Operating current (selfbiased) V_{DS} = 5 V, V_{G2S} = 4 V, amp.B	I_{DSO}	-	13	-	mA
Drain-source current V_{DS} = 5 V, V_{G2S} = 4 V, R_{G1} = 100 kΩ, amp. A	I_{DSX}	-	13	-	
Gate1-source pinch-off voltage V_{DS} = 5 V, V_{G2S} = 4 V, I_D = 100 µA	$V_{G1S(p)}$	-	0.5	-	V
Gate2-source pinch-off voltage V_{DS} = 5 V, I_D = 100 µA	$V_{G2S(p)}$	-	0.6	-	

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics V_{DS} = 5V, V_{G2S} = 4V, (I_D = 14 mA) (verified by random sampling)					
Forward transconductance	g_{fs}	-	33	-	mS
Gate1 input capacitance f = 10 MHz	C_{g1ss}	-	1.9	-	pF
Output capacitance f = 10 MHz	C_{dss}	-	1.3	-	
Power gain	G_p				dB
f = 800 MHz		-	25	-	
f = 45 MHz		-	33	-	
Noise figure	F				dB
f = 800 MHz		-	1.3	-	
f = 45 MHz		-	1	-	
Gain control range V_{G2S} = 4 ... 0 V , f = 800 MHz	ΔG_p	45	-	-	
Cross-modulation k=1%, f_w=50MHz, f_{unw}=60MHz	X_{mod}				-
AGC = 0 dB		90	-	-	
AGC = 10 dB		-	93	-	
AGC = 40 dB		-	105	-	

Functional diagram

a) shows pinning of BG3430R.



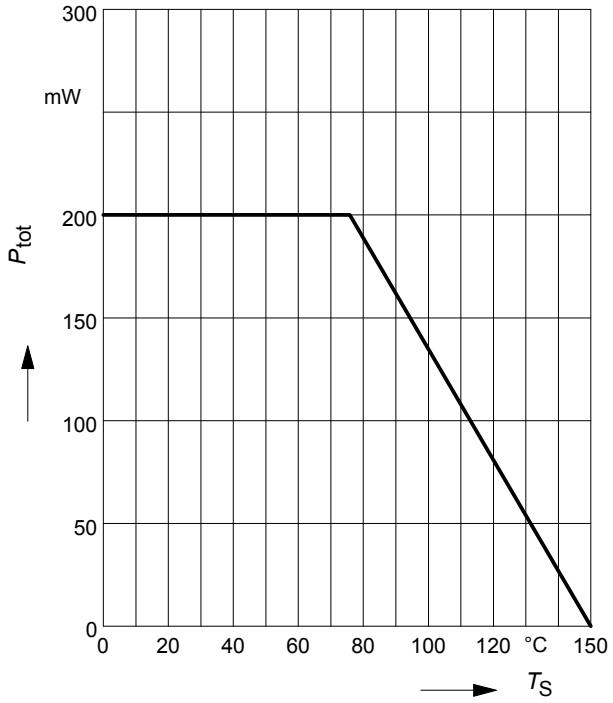
Amp. A bias network partially integrated
Amp. B bias network fully integrated

V_{gg} = 5 V : Amp. A is ON ; Amp. B is OFF
V_{gg} = 0 V : Amp. A is OFF ; Amp. B is ON

Amp. A and Amp. B share
G2 and S pins

Total power dissipation $P_{tot} = f(T_S)$

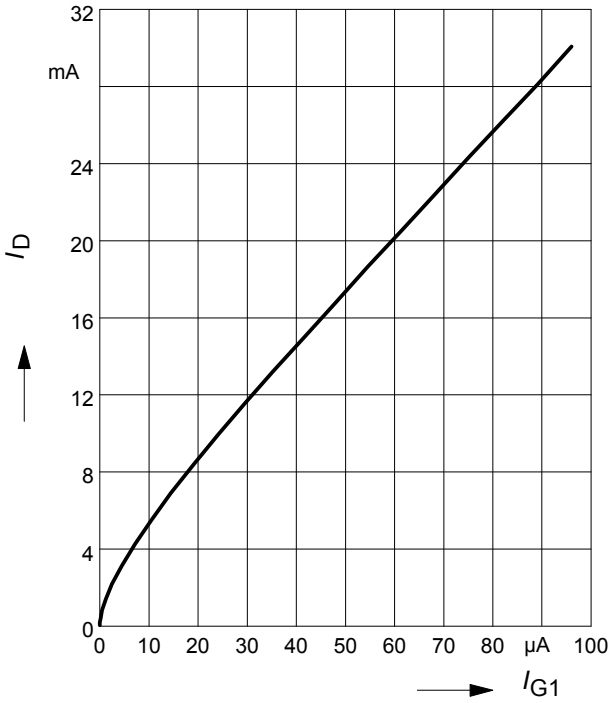
amp. A = amp. B



Drain current $I_D = f(I_{G1})$

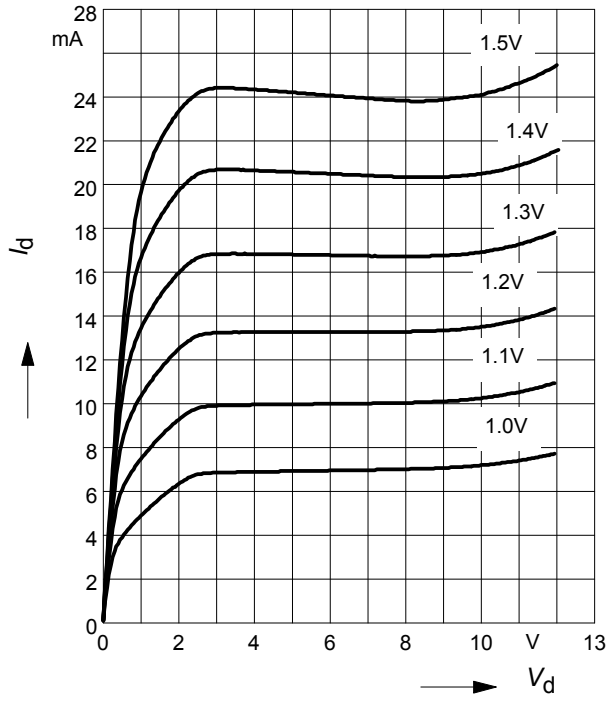
V_{G2S} = 4V

amp. A



Output characteristics $I_D = f(V_{DS})$

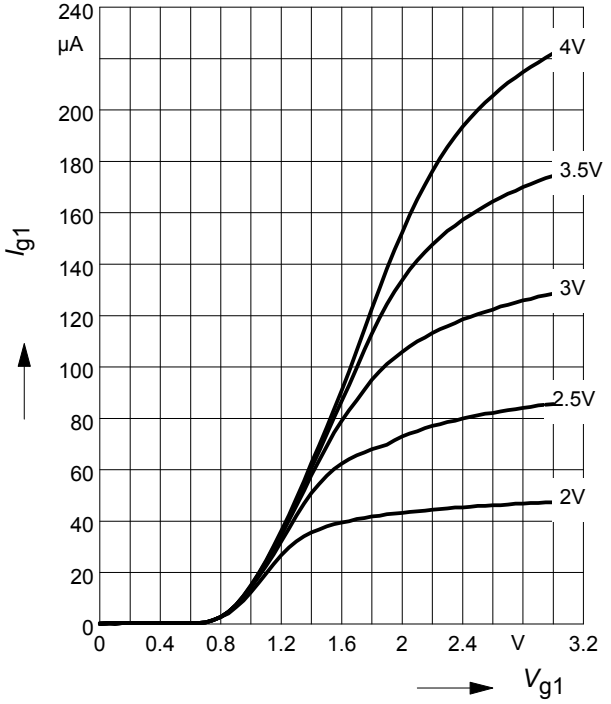
amp. A = amp. B



Gate 1 current $I_{G1} = f(V_{G1S})$

V_{DS} = 5V, V_{G2S} = Parameter

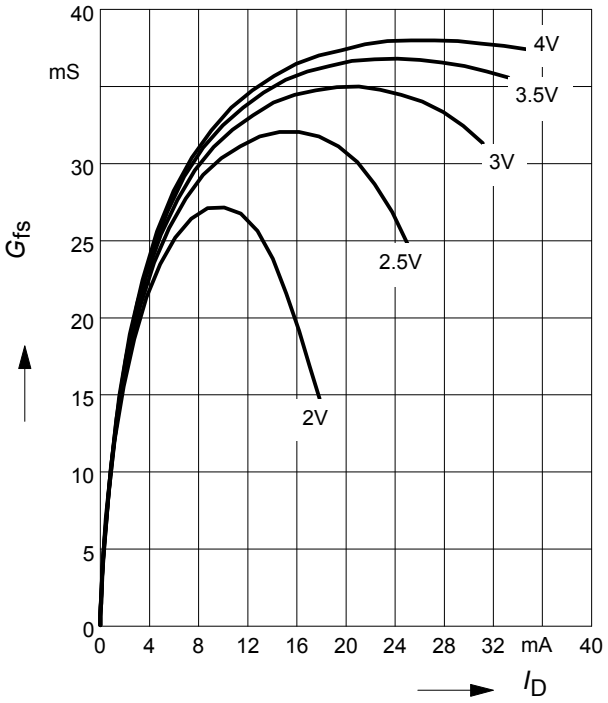
amp. A



Gate 1 forward transconductance

$g_{fs} = f(I_D)$, V_{DS} = 5V, V_{G2S} = Parameter

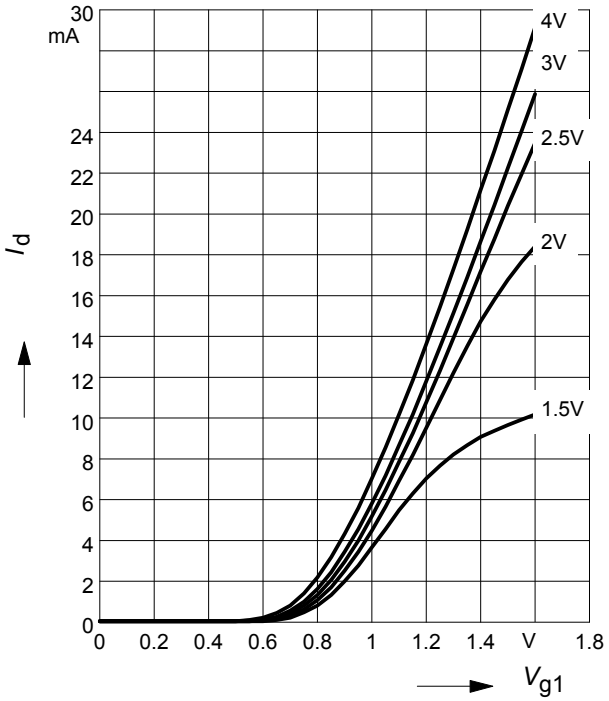
amp. A = amp. B



Drain current $I_D = f(V_{G1S})$

V_{DS} = 5V, V_{G2S} = Parameter

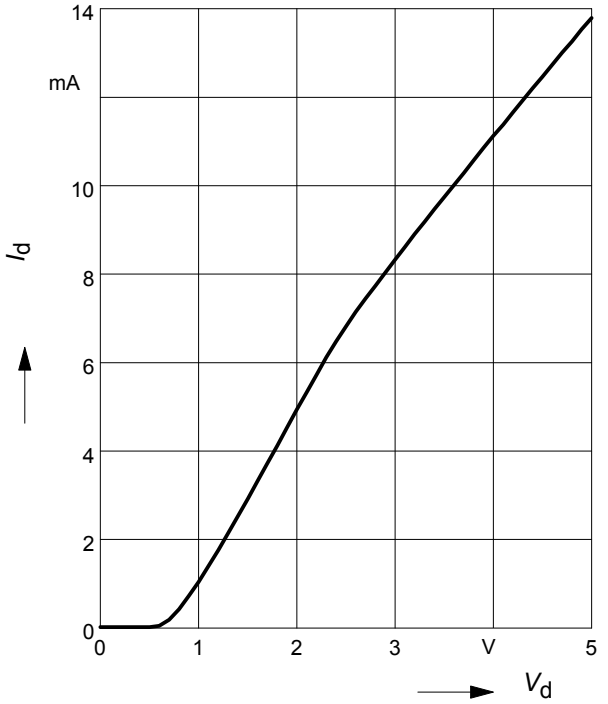
amp. A = amp. B



Drain current $I_D = f(V_{GG})$ amp.A

V_{DS} = 5V, V_{G2S} = 4V, R_{G1} = 100kΩ

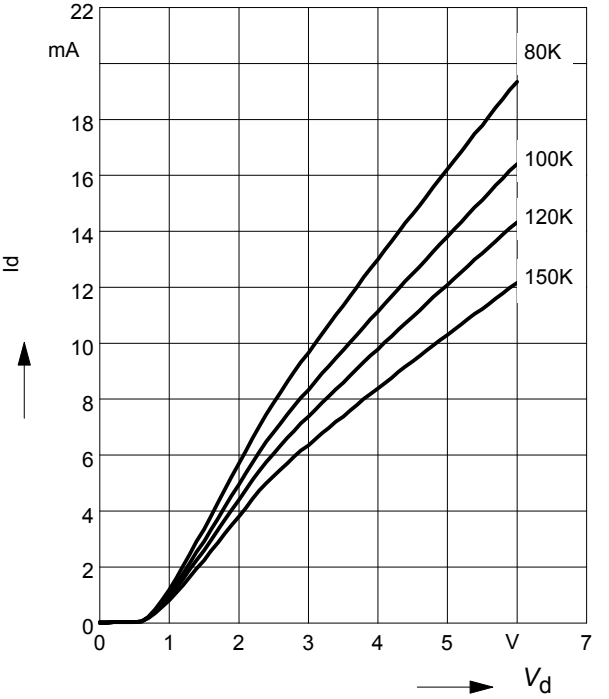
(connected to V_{GG}, V_{GG}=gate1 supply voltage)



Drain current $I_D = f(V_{GG})$

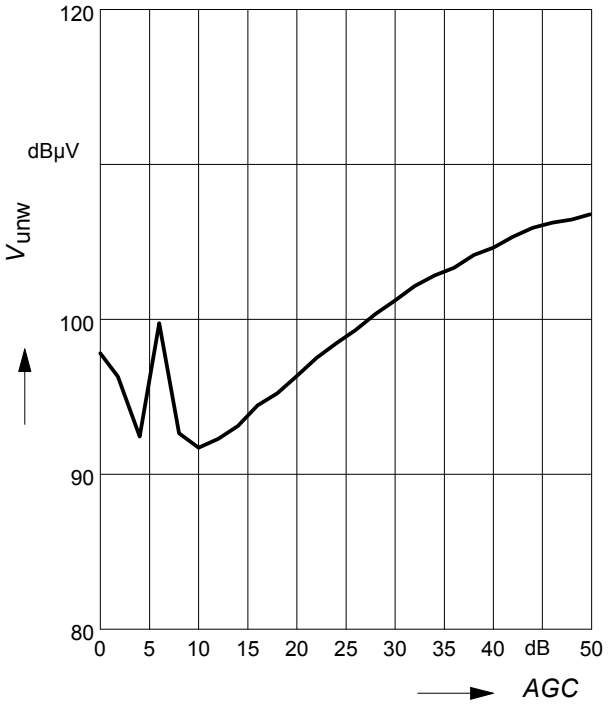
V_{G2S} = 4V, R_{G1} = Parameter in kΩ

amp. A

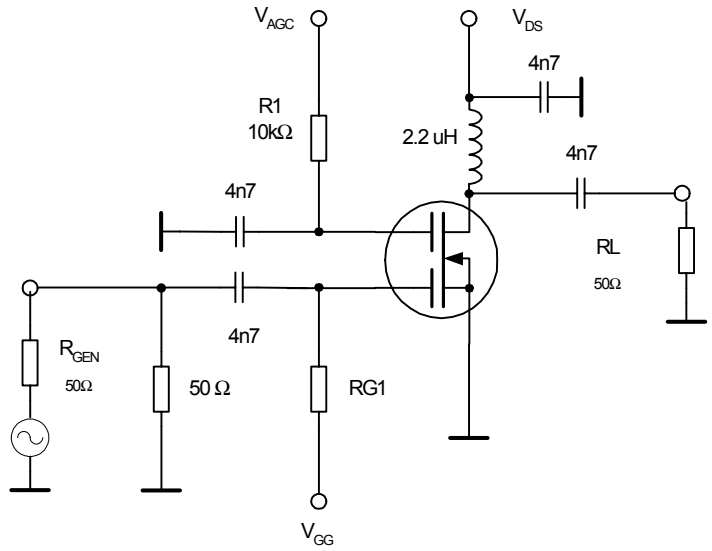


Crossmodulation V_{unw} = (*AGC*)

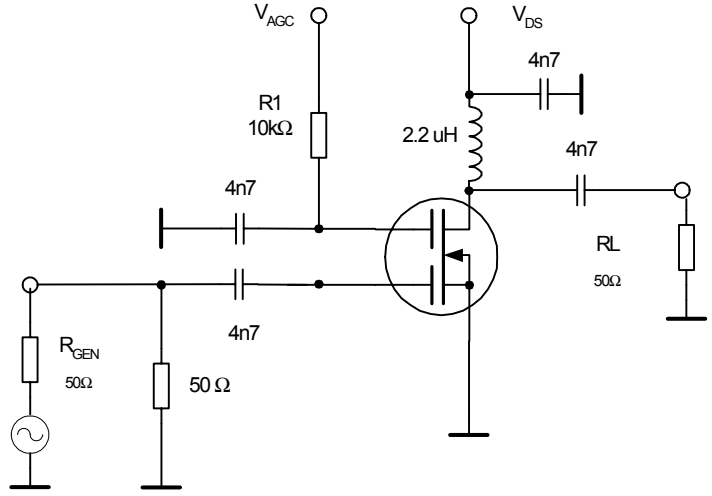
V_{DS} = 5 V, amp. A = amp. B



Crossmodulation test circuit

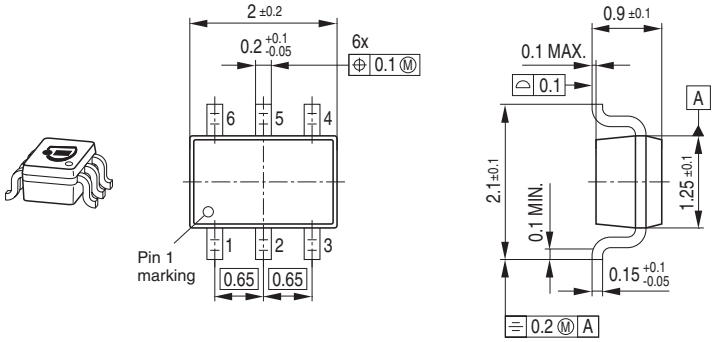


Semibiased

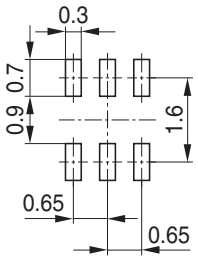


fullbiased

Package Outline

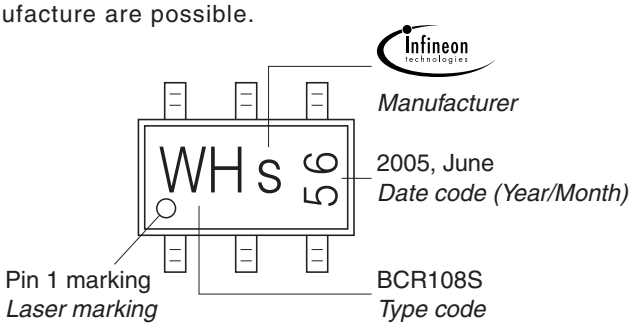


Foot Print



Marking Layout (Example)

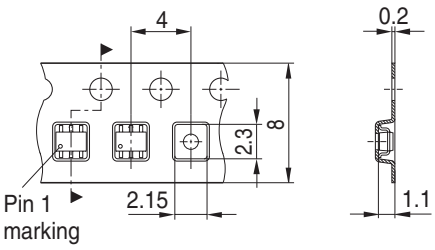
Small variations in positioning of
Date code, Type code and Manufacture are possible.



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel

For symmetric types no defined Pin 1 orientation in reel.



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