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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# BGM113 Blue Gecko *Bluetooth*® Module Data Sheet



The Blue Gecko BGM113 is a Bluetooth® Module targeted for Bluetooth low energy applications where small size, reliable RF, low-power consumption, and easy application development are key requirements. At +3 dBm TX power, BGM113 is ideal for applications requiring short and medium range Bluetooth connectivity.

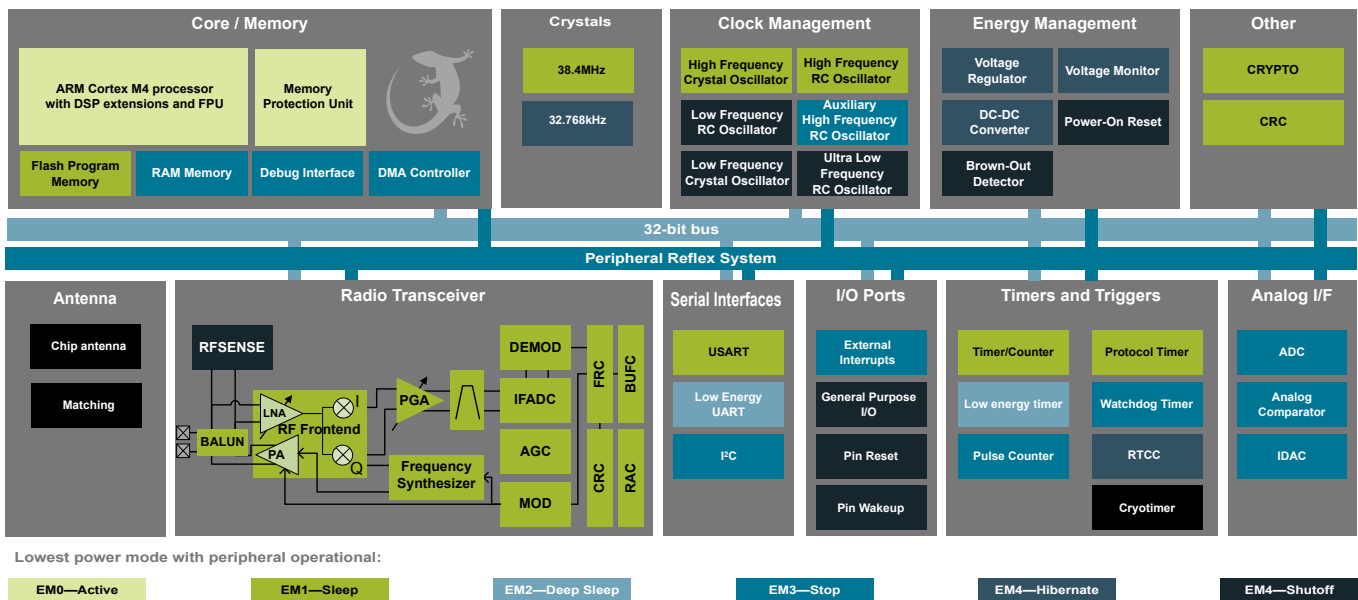
The BGM113 integrates all of the necessary elements required for a Bluetooth application: Bluetooth radio, a software stack, and GATT-based profiles, and it can also host end user applications, which means no external microcontroller is required in size, price or power constrained devices. The BGM113 Bluetooth Module also has highly flexible hardware interfaces to connect to different peripherals or sensors.

BGM113 can be used in a wide variety of applications:

- IoT Sensors and End Devices
- Commercial and Retail
- Health and Wellness
- Industrial, Home and Building Automation
- Smart Phone, Tablet and PC Accessories

## KEY FEATURES

- Bluetooth 4.2 compliant
- Integrated antenna
- TX power: up to +3 dBm
- RX sensitivity: down to -92 dBm
- Range: up to 50 meters
- 32-bit ARM® Cortex®-M4 core at 38.4 MHz
- Flash memory: 256kB
- RAM: 32 kB
- Autonomous hardware crypto accelerator and random number generator
- Integrated DC-DC Converter
- Onboard Bluetooth stack



## 1. Feature List

The BGM113 highlighted features are listed below.

- **Low Power Wireless System-on-Chip.**
  - High Performance 32-bit 38.4 MHz ARM Cortex<sup>®</sup>-M4 with DSP instruction and floating-point unit for efficient signal processing
  - 256 kB flash program memory
  - 32 kB RAM data memory
  - 2.4 GHz radio operation
  - TX power up to +3 dBm
- **Low Energy Consumption**
  - 8.7 mA RX current at 2.4 GHz
  - 8.2 mA TX current @ 0 dBm output power at 2.4 GHz
  - 63  $\mu$ A/MHz in Active Mode (EM0)
  - 2.5  $\mu$ A EM2 DeepSleep current (full RAM retention and RTCC running from LFXO)
  - 2.1  $\mu$ A EM3 Stop current (State/RAM retention)
  - Wake on Radio with signal strength detection, preamble pattern detection, frame detection and timeout
- **High Receiver Performance**
  - -92 dBm sensitivity @ 1 Mbit/s GFSK (2.4 GHz)
- **Supported Protocols**
  - Bluetooth<sup>®</sup>
- **Support for Internet Security**
  - General Purpose CRC
  - Random Number Generator
  - Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **Wide Selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2  $\times$  Analog Comparator (ACMP)
  - Digital to Analog Current Converter (IDAC)
  - 14 pins connected to analog channels (APORT) shared between Analog Comparators, ADC, and IDAC
  - 14 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2 $\times$ 16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter with asynchronous operation
  - Watchdog Timer with dedicated RC oscillator @ 50nA
  - 2 $\times$ Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I<sup>2</sup>S)
  - Low Energy UART (LEUART<sup>™</sup>)
  - I<sup>2</sup>C interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.85 V to 3.8 V single power supply
  - 2.4 V to 3.8 V when using DC-DC
  - Integrated DC-DC
  - -40 °C to +85 °C
- **Dimensions**
  - 9.15 x 15.73 x 1.9 mm

## 2. Ordering Information

| Ordering Code           | Protocol Stack  | Frequency Band | Max TX Power (dBm) | Encryption | Flash (KB) | RAM (KB) | GPIO | Package                |
|-------------------------|-----------------|----------------|--------------------|------------|------------|----------|------|------------------------|
| BGM113A256V2            | Bluetooth Smart | 2.4 GHz        | 3                  | Full       | 256        | 32       | 14   | 100 pcs cut reel       |
| BGM113A256V2R           | Bluetooth Smart | 2.4 GHz        | 3                  | Full       | 256        | 32       | 14   | 1000 pcs tape and reel |
| SLWRB4301A <sup>1</sup> |                 |                |                    |            |            |          |      |                        |

**Note:**

1. BGM113 Bluetooth module radio board. Requires also SLWSTK6101C (or SLWSTK6101A or SLWSTK6101B).



### 3. System Overview

#### 3.1 Introduction

The BGM113 product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application, as well as other system requiring high performance and low-energy consumption. This section gives a short introduction to the full radio and MCU system. A detailed functional description can be found in the *EFR32BG1 Blue Gecko Bluetooth® Smart SoC Family Data Sheet* (see general sections and QFN48 2.4 GHz SoC related sections).

A detailed block diagram of the EFR32BG SoC is shown in the figure below which is used in the BGM113 Bluetooth Smart module.

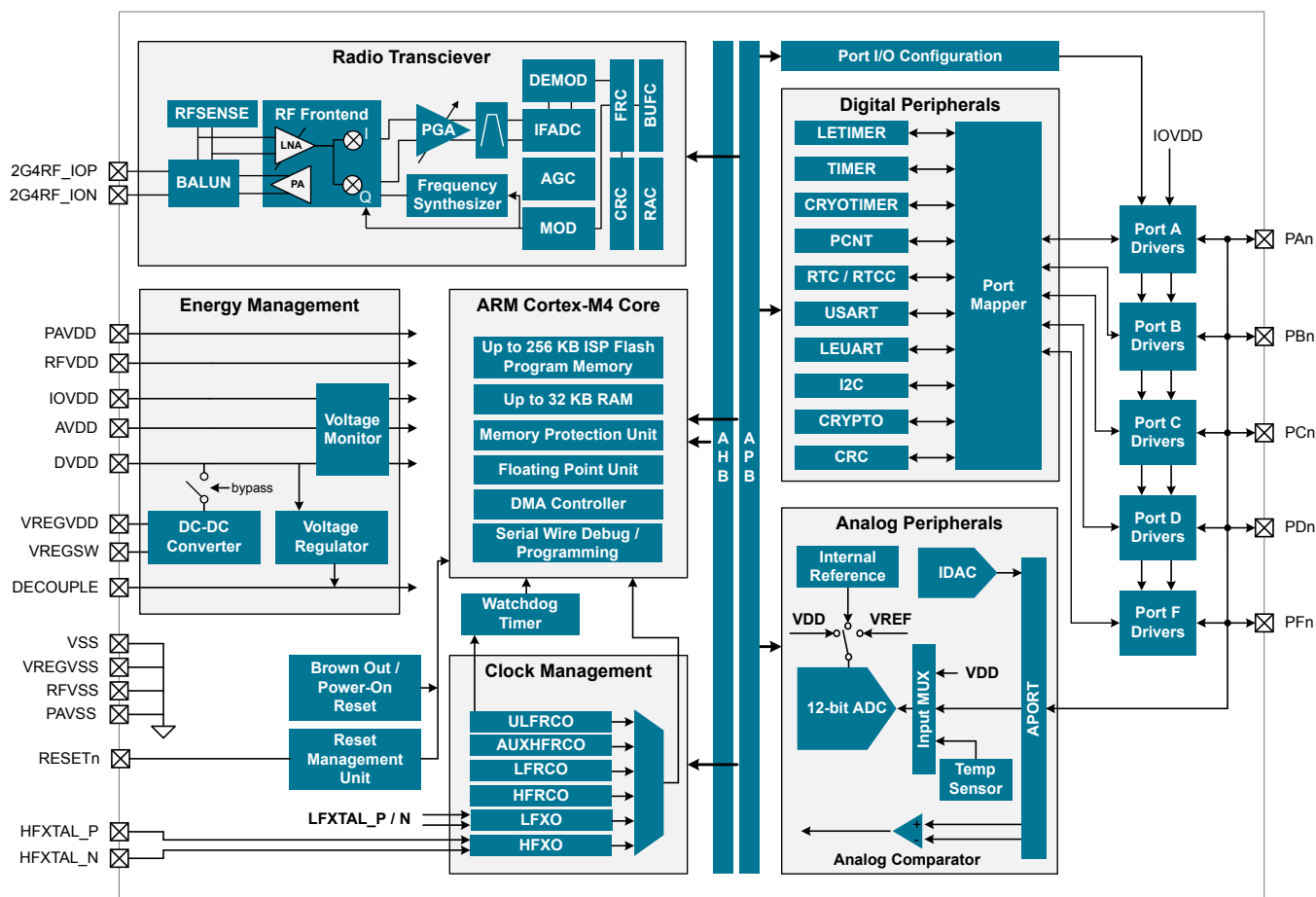


Figure 3.1. Detailed EFR32BG1 Block Diagram

#### 3.2 Radio

The BGM113 features a radio transceiver supporting Bluetooth® low energy protocol.

##### 3.2.1 Antenna Interface

The BGM113 module includes an integrated chip-antenna. The table below includes performance specifications for the integrated chip-antenna.

**Table 3.1. Antenna Efficiency and Peak Gain**

| Parameter  | With optimal layout | Note  |
|------------|---------------------|---|
| Efficiency | -3 to -4 dB         | Efficiency and peak gain depend on the application PCB layout and mechanical design |
| Peak gain  | 0.5 dBi             |   |

### 3.2.2 Wake on Radio

The Wake on Radio feature allows flexible, autonomous RF sensing, qualification, and demodulation without required MCU activity, using a subsystem of the BGM113 including the Radio Controller (RAC), Peripheral Reflex System (PRS), and Low Energy peripherals.

### 3.2.3 RFSENSE

The RFSENSE module generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

### 3.2.4 Packet and State Trace

The BGM113 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

### 3.2.5 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

### 3.3 Power

The BGM113 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator is utilized to further reduce the current consumption.

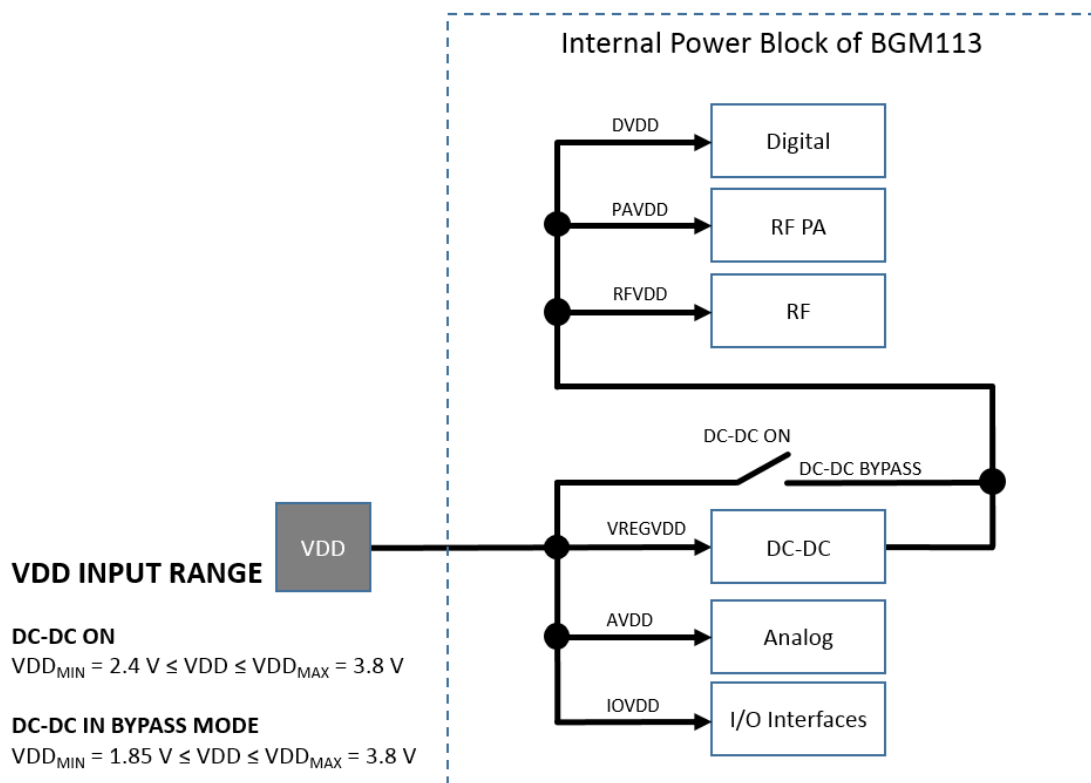


Figure 3.2. Power Supply Configuration

#### 3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

#### 3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

### 3.4 General Purpose Input/Output (GPIO)

BGM113 has up to 14 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

## 3.5 Clocking

### 3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the BGM113. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

### 3.5.2 Internal Oscillators

The BGM113 fully integrates two crystal oscillators and four RC oscillators, listed below.

- A 38.4MHz high frequency crystal oscillator (HF XO) provides a precise timing reference for the MCU and radio.
- A 32.768 kHz crystal oscillator (LF XO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

## 3.6 Counters/Timers and PWM

### 3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER\_0 only.

### 3.6.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

### 3.6.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

### 3.6.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LF XO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.



### 3.6.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn\_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

### 3.6.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

## 3.7 Communications and Other Digital Peripherals

### 3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I<sup>2</sup>S

### 3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

### 3.7.3 Inter-Integrated Circuit Interface (I<sup>2</sup>C)

The I<sup>2</sup>C module provides an interface between the MCU and a serial I<sup>2</sup>C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I<sup>2</sup>C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

### 3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

## 3.8 Security Features

### 3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

### 3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. It supports AES encryption and decryption with 128- or 256-bit keys and ECC over both GF(P) and GF(2<sup>m</sup>), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

## 3.9 Analog

### 3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to analog modules ADC, ACMP, and IDAC on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

### 3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

### 3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 MSamples/s. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

### 3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The current is programmable between 0.05  $\mu$ A and 64  $\mu$ A with several ranges with various step sizes.

## 3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the BGM113. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset and watchdog reset.

## 3.11 Core and Memory

### 3.11.1 Processor Core

The ARM Cortex-M4F processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4F RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- 256 KB flash program memory
- 32 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

### 3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

### 3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

### 3.12 Memory Map

The BGM113 memory map is shown in the figures below.

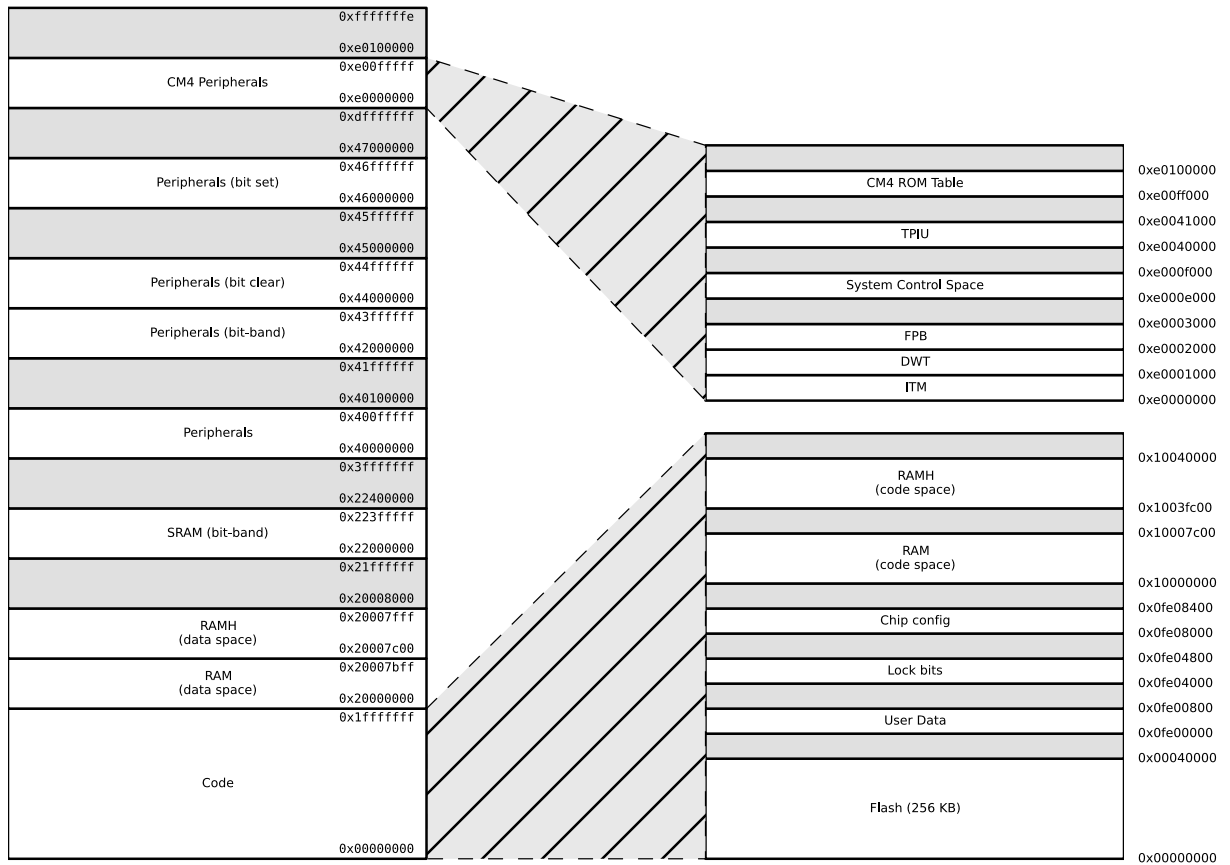


Figure 3.3. BGM113 Memory Map — Core Peripherals and Code Space

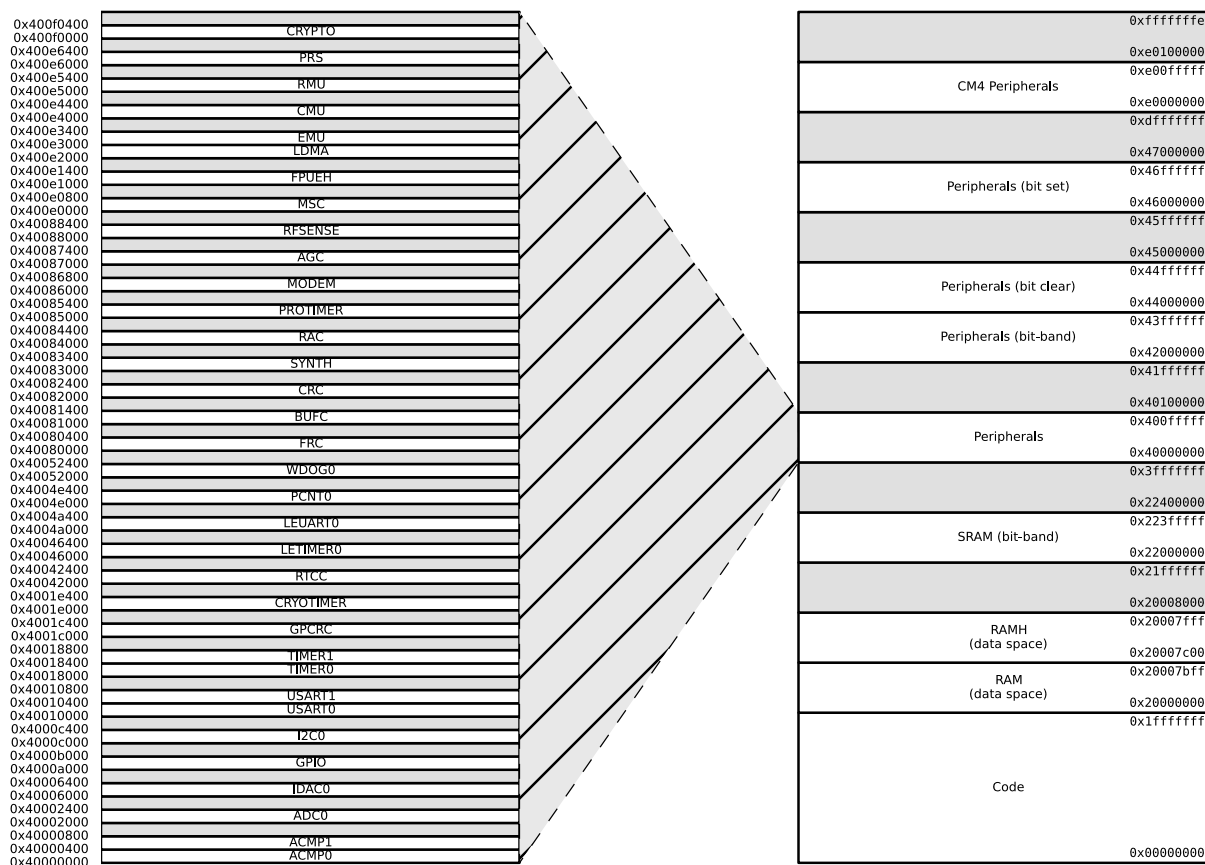


Figure 3.4. BGM113 Memory Map — Peripherals

### 3.13 Configuration Summary

The features of the BGM113 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

| Module | Configuration                   | Pin Connections                 |
|--------|---------------------------------|---------------------------------|
| USART0 | IrDA SmartCard                  | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | IrDA I <sup>2</sup> S SmartCard | US1_TX, US1_RX, US1_CLK, US1_CS |
| TIMER0 | with DTI                        | TIM0_CC[2:0], TIM0_CDTI[2:0]    |
| TIMER1 |                                 | TIM1_CC[3:0]                    |



## 4. Electrical Specifications

### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on  $T_{AMB}=25\text{ }^{\circ}\text{C}$  and  $V_{DD}=3.3\text{ V}$ , by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a  $50\ \Omega$  antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to [Table 4.2 General Operating Conditions on page 13](#) for more details about operational supply and temperature limits.

#### 4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 4.1. Absolute Maximum Ratings**

| Parameter  | Symbol          | Test Condition | Min  | Typ | Max                      | Unit               |
|--|-----------------|----------------|------|-----|--------------------------|--------------------|
| Storage temperature range                              | $T_{STG}$       |                | -40  | —   | +85                      | $^{\circ}\text{C}$ |
| External main supply voltage                           | $V_{DDMAX}$     |                | 0    | —   | 3.8                      | V                  |
| External main supply voltage ramp rate                 | $V_{DDRAMPMAX}$ |                | —    | —   | 1                        | V / $\mu\text{s}$  |
| External main supply voltage with DC-DC in bypass mode |                 |                | 1.85 |     | 3.8                      | V                  |
| Voltage on any 5V tolerant GPIO pin <sup>1</sup>       | $V_{DIGPIN}$    |                | -0.3 | —   | Min of 5.25 and IOVDD +2 | V                  |
| Voltage on non-5V tolerant GPIO pins                   |                 |                | -0.3 | —   | IOVDD+0.3                | V                  |
| Max RF level at input                                  | $P_{RFMAX2G4}$  |                | —    | —   | 10                       | dBm                |
| Total current into VDD power lines (source)            | $I_{VDDMAX}$    |                | —    | —   | 200                      | mA                 |
| Total current into VSS ground lines (sink)             | $I_{VSSMAX}$    |                | —    | —   | 200                      | mA                 |
| Current per I/O pin (sink)                             | $I_{IOMAX}$     |                | —    | —   | 50                       | mA                 |
| Current per I/O pin (source)                           |                 |                | —    | —   | 50                       | mA                 |
| Current for all I/O pins (sink)                        | $I_{IOALLMAX}$  |                | —    | —   | 200                      | mA                 |
| Current for all I/O pins (source)                      |                 |                | —    | —   | 200                      | mA                 |
| Voltage difference between AVDD and VREGVDD            | $\Delta V_{DD}$ |                | —    | —   | 0.3                      | V                  |

**Note:**

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

## 4.1.2 Operating Conditions

The following subsections define the operating conditions for the module.

### 4.1.2.1 General Operating Conditions

**Table 4.2. General Operating Conditions**

| Parameter  | Symbol            | Test Condition                          | Min  | Typ  | Max | Unit |
|--|-------------------|---|------|------|-----|------|
| Operating temperature range  | T <sub>OP</sub>   | Ambient temperature range               | -40  | 25   | 85  | °C   |
| VDD Operating supply voltage <sup>1</sup>  | V <sub>VDD</sub>  | DCDC in regulation                      | 2.4  | 3.3  | 3.8 | V    |
|  |                   | DCDC in bypass, 50mA load               | 1.85 | 3.3  | 3.8 | V    |
| VDD Current  | I <sub>VDD</sub>  | DCDC in bypass                          | —    | —    | 200 | mA   |
| HFCLK frequency  | f <sub>CORE</sub> | 0 wait-states (MODE = WS0) <sup>2</sup> | —    | —    | 26  | MHz  |
|  |                   | 1 wait-states (MODE = WS1) <sup>2</sup> | —    | 38.4 | 40  | MHz  |
| <b>Note:</b>   |                   |   |      |      |     |      |
| 1. The minimum voltage required in bypass mode is calculated using R <sub>BYP</sub> from the DC-DC specification table. Requirements for other loads can be calculated as $V_{VDD\_min} + I_{LOAD} * R_{BYP\_max}$ |                   |   |      |      |     |      |
| 2. In MSC_READCTRL register  |                   |   |      |      |     |      |

### 4.1.3 DC-DC Converter

Test conditions:  $V_{DCDC\_I}=3.3$  V,  $V_{DCDC\_O}=1.8$  V,  $I_{DCDC\_LOAD}=50$  mA, Heavy Drive configuration,  $F_{DCDC\_LN}=7$  MHz, unless otherwise indicated.

**Table 4.3. DC-DC Converter**

| Parameter                                      | Symbol        | Test Condition   | Min  | Typ | Max                | Unit |
|--|---------------|--|------|-----|--------------------|------|
| Input voltage range                            | $V_{DCDC\_I}$ | Bypass mode, $I_{DCDC\_LOAD} = 50$ mA  | 1.85 | —   | $V_{VREGVDD\_MAX}$ | V    |
|  |               | Low noise (LN) mode, 1.8 V output, $I_{DCDC\_LOAD} = 100$ mA, or Low power (LP) mode, 1.8 V output, $I_{DCDC\_LOAD} = 10$ mA | 2.4  | —   | $V_{VREGVDD\_MAX}$ | V    |
|  |               | Low noise (LN) mode, 1.8 V output, $I_{DCDC\_LOAD} = 200$ mA   | 2.6  | —   | $V_{VREGVDD\_MAX}$ | V    |
| Output voltage programmable range <sup>1</sup> | $V_{DCDC\_O}$ |  | 1.8  | —   | $V_{VREGVDD}$      | V    |
| Regulation DC Accuracy                         | $ACC_{DC}$    | Low noise (LN) mode, 1.8 V target output   | 1.7  | —   | 1.9                | V    |
| Regulation Window <sup>2</sup>                 | $WIN_{REG}$   | Low power (LP) mode, $LPCMPBIAS^3 = 0$ , 1.8 V target output, $I_{DCDC\_LOAD} \leq 75$ $\mu$ A                               | 1.63 | —   | 2.2                | V    |
|  |               | Low power (LP) mode, $LPCMPBIAS^3 = 3$ , 1.8 V target output, $I_{DCDC\_LOAD} \leq 10$ mA                                    | 1.63 | —   | 2.1                | V    |
| Steady-state output ripple                     | $V_R$         | Radio disabled.  | —    | 3   | —                  | mVpp |
| Output voltage under/overshoot                 | $V_{OV}$      | CCM Mode ( $LNFORCECCM^3 = 1$ ), Load changes between 0 mA and 100 mA  | —    | —   | 150                | mV   |
|  |               | DCM Mode ( $LNFORCECCM^3 = 0$ ), Load changes between 0 mA and 10 mA   | —    | —   | 150                | mV   |
|  |               | Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode   | —    | 200 | —                  | mV   |
|  |               | Undershoot during BYP/LP to LN CCM ( $LNFORCECCM^3 = 1$ ) mode transitions compared to DC level in LN mode                   | —    | 50  | —                  | mV   |
|  |               | Undershoot during BYP/LP to LN DCM ( $LNFORCECCM^3 = 0$ ) mode transitions compared to DC level in LN mode                   | —    | 125 | —                  | mV   |
| DC line regulation                             | $V_{REG}$     | Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V   | —    | 0.1 | —                  | %    |
| DC load regulation                             | $I_{REG}$     | Load changes between 0 mA and 100 mA in CCM mode   | —    | 0.1 | —                  | %    |

| Parameter   | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|-----|-----|-----|------|
| <b>Note:</b> <ol style="list-style-type: none"><li>1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, <math>V_{VREGVDD}</math></li><li>2. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits</li><li>3. In EMU_DCDCMISCCTRL register</li><li>4. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.</li></ol> |        |                |     |     |     |      |

#### 4.1.4 Current Consumption

##### 4.1.4.1 Current Consumption 3.3 V (DC-DC in Bypass Mode)

Unless otherwise indicated, typical conditions are: VDD = 3.3 V. T<sub>OP</sub> = 25 °C. EMU\_PWRCFG\_PWRCG=NODCDC. EMU\_DCDCCTRL\_DCDCMODE=BYPASS. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T<sub>OP</sub> = 25 °C.

**Table 4.4. Current Consumption 3.3V without DC/DC**

| Parameter  | Symbol              | Test Condition   | Min | Typ  | Max  | Unit   |
|--|---------------------|--|-----|------|------|--------|
| Current consumption in EM0 Active mode with all peripherals disabled | I <sub>ACTIVE</sub> | 38.4 MHz crystal, CPU running while loop from flash <sup>1</sup> | —   | 130  | —    | µA/MHz |
|  |                     | 38 MHz HFRCO, CPU running Prime from flash                       | —   | 88   | —    | µA/MHz |
|  |                     | 38 MHz HFRCO, CPU running while loop from flash                  | —   | 100  | 105  | µA/MHz |
|  |                     | 38 MHz HFRCO, CPU running CoreMark from flash                    | —   | 112  | —    | µA/MHz |
|  |                     | 26 MHz HFRCO, CPU running while loop from flash                  | —   | 102  | 106  | µA/MHz |
|  |                     | 1 MHz HFRCO, CPU running while loop from flash                   | —   | 222  | 350  | µA/MHz |
| Current consumption in EM1 Sleep mode with all peripherals disabled  | I <sub>EM1</sub>    | 38.4 MHz crystal <sup>1</sup>                                    | —   | 65   | —    | µA/MHz |
|  |                     | 38 MHz HFRCO   | —   | 35   | 38   | µA/MHz |
|  |                     | 26 MHz HFRCO   | —   | 37   | 41   | µA/MHz |
|  |                     | 1 MHz HFRCO  | —   | 157  | 275  | µA/MHz |
| Current consumption in EM2 Deep Sleep mode.                          | I <sub>EM2</sub>    | Full RAM retention and RTCC running from LFXO                    | —   | 3.3  | —    | µA     |
|  |                     | 4 kB RAM retention and RTCC running from LFRCO                   | —   | 3    | 6.3  | µA     |
| Current consumption in EM3 Stop mode                                 | I <sub>EM3</sub>    | Full RAM retention and CRYO-TIMER running from ULFRCO            | —   | 2.8  | 6    | µA     |
| Current consumption in EM4H Hibernate mode                           | I <sub>EM4</sub>    | 128 byte RAM retention, RTCC running from LFXO                   | —   | 1.1  | —    | µA     |
|  |                     | 128 byte RAM retention, CRYO-TIMER running from ULFRCO           | —   | 0.65 | —    | µA     |
|  |                     | 128 byte RAM retention, no RTCC                                  | —   | 0.65 | 1.3  | µA     |
| Current consumption in EM4S Shutoff mode                             | I <sub>EM4S</sub>   | no RAM retention, no RTCC  | —   | 0.04 | 0.11 | µA     |
| <b>Note:</b>   |                     |  |     |      |      |        |
| 1. CMU_HFXOCTRL_LOWPOWER=0   |                     |  |     |      |      |        |



#### 4.1.4.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VDD = 3.3V. T<sub>OP</sub> = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T<sub>OP</sub> = 25 °C.

**Table 4.5. Current Consumption 3.3V with DC-DC**

| Parameter   | Symbol              | Test Condition   | Min | Typ  | Max | Unit   |
|---|---------------------|--|-----|------|-----|--------|
| Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise DCM mode <sup>1</sup> . | I <sub>ACTIVE</sub> | 38.4 MHz crystal, CPU running while loop from flash <sup>2</sup> | —   | 88   | —   | µA/MHz |
|   |                     | 38 MHz HFRCO, CPU running Prime from flash                       | —   | 63   | —   | µA/MHz |
|   |                     | 38 MHz HFRCO, CPU running while loop from flash                  | —   | 71   | —   | µA/MHz |
|   |                     | 38 MHz HFRCO, CPU running CoreMark from flash                    | —   | 78   | —   | µA/MHz |
|   |                     | 26 MHz HFRCO, CPU running while loop from flash                  | —   | 76   | —   | µA/MHz |
| Current consumption in EM0 Active mode with all peripherals disabled, DCDC in Low Noise CCM mode <sup>3</sup> . | I <sub>ACTIVE</sub> | 38.4 MHz crystal, CPU running while loop from flash <sup>2</sup> | —   | 98   | —   | µA/MHz |
|   |                     | 38 MHz HFRCO, CPU running Prime from flash                       | —   | 75   | —   | µA/MHz |
|   |                     | 38 MHz HFRCO, CPU running while loop from flash                  | —   | 81   | —   | µA/MHz |
|   |                     | 38 MHz HFRCO, CPU running CoreMark from flash                    | —   | 88   | —   | µA/MHz |
|   |                     | 26 MHz HFRCO, CPU running while loop from flash                  | —   | 94   | —   | µA/MHz |
| Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise DCM mode <sup>1</sup> .  | I <sub>EM1</sub>    | 38.4 MHz crystal <sup>2</sup>                                    | —   | 49   | —   | µA/MHz |
|   |                     | 38 MHz HFRCO   | —   | 32   | —   | µA/MHz |
|   |                     | 26 MHz HFRCO   | —   | 38   | —   | µA/MHz |
| Current consumption in EM1 Sleep mode with all peripherals disabled, DCDC in Low Noise CCM mode <sup>3</sup> .  | I <sub>EM1</sub>    | 38.4 MHz crystal <sup>2</sup>                                    | —   | 61   | —   | µA/MHz |
|   |                     | 38 MHz HFRCO   | —   | 45   | —   | µA/MHz |
|   |                     | 26 MHz HFRCO   | —   | 58   | —   | µA/MHz |
| Current consumption in EM2 Deep Sleep mode. DCDC in Low Power mode <sup>4</sup> .                               | I <sub>EM2</sub>    | Full RAM retention and RTCC running from LFXO                    | —   | 2.5  | —   | µA     |
|   |                     | 4 kB RAM retention and RTCC running from LFRCO                   | —   | 2.2  | —   | µA     |
| Current consumption in EM3 Stop mode  | I <sub>EM3</sub>    | Full RAM retention and CRYO-TIMER running from ULFRCO            | —   | 2.1  | —   | µA     |
| Current consumption in EM4H Hibernate mode  | I <sub>EM4</sub>    | 128 byte RAM retention, RTCC running from LFXO                   | —   | 0.86 | —   | µA     |
|   |                     | 128 byte RAM retention, CRYO-TIMER running from ULFRCO           | —   | 0.58 | —   | µA     |
|   |                     | 128 byte RAM retention, no RTCC                                  | —   | 0.58 | —   | µA     |
| Current consumption in EM4S Shutoff mode  | I <sub>EM4S</sub>   | no RAM retention, no RTCC  | —   | 0.04 | —   | µA     |

| Parameter   | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------|----------------|-----|-----|-----|------|
| <b>Note:</b>  |        |                |     |     |     |      |
| 1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD           |        |                |     |     |     |      |
| 2. CMU_HFXOCTRL_LOWPOWER=0  |        |                |     |     |     |      |
| 3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD           |        |                |     |     |     |      |
| 4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPBIAS=3, LPCILIMSEL=1, ANASW=DVDD |        |                |     |     |     |      |

#### 4.1.4.3 Current Consumption 1.85 V (DC-DC in Bypass Mode)

Unless otherwise indicated, typical conditions are: VDD = 1.85 V. T<sub>OP</sub> = 25 °C. DC-DC in bypass mode. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T<sub>OP</sub> = 25 °C.

**Table 4.6. Current Consumption 1.85V without DC/DC**

| Parameter  | Symbol              | Test Condition   | Min | Typ  | Max | Unit   |
|--|---------------------|--|-----|------|-----|--------|
| Current consumption in EM0 Active mode with all peripherals disabled | I <sub>ACTIVE</sub> | 38.4 MHz crystal, CPU running while loop from flash <sup>1</sup> | —   | 131  | —   | µA/MHz |
|  |                     | 38 MHz HFRCO, CPU running Prime from flash                       | —   | 88   | —   | µA/MHz |
|  |                     | 38 MHz HFRCO, CPU running while loop from flash                  | —   | 100  | —   | µA/MHz |
|  |                     | 38 MHz HFRCO, CPU running CoreMark from flash                    | —   | 112  | —   | µA/MHz |
|  |                     | 26 MHz HFRCO, CPU running while loop from flash                  | —   | 102  | —   | µA/MHz |
|  |                     | 1 MHz HFRCO, CPU running while loop from flash                   | —   | 220  | —   | µA/MHz |
| Current consumption in EM1 Sleep mode with all peripherals disabled  | I <sub>EM1</sub>    | 38.4 MHz crystal <sup>1</sup>                                    | —   | 65   | —   | µA/MHz |
|  |                     | 38 MHz HFRCO   | —   | 35   | —   | µA/MHz |
|  |                     | 26 MHz HFRCO   | —   | 37   | —   | µA/MHz |
|  |                     | 1 MHz HFRCO  | —   | 154  | —   | µA/MHz |
| Current consumption in EM2 Deep Sleep mode                           | I <sub>EM2</sub>    | Full RAM retention and RTCC running from LFXO                    | —   | 3.2  | —   | µA     |
|  |                     | 4 kB RAM retention and RTCC running from LFRCO                   | —   | 2.8  | —   | µA     |
| Current consumption in EM3 Stop mode                                 | I <sub>EM3</sub>    | Full RAM retention and CRYO-TIMER running from ULFRCO            | —   | 2.7  | —   | µA     |
| Current consumption in EM4H Hibernate mode                           | I <sub>EM4</sub>    | 128 byte RAM retention, RTCC running from LFXO                   | —   | 1    | —   | µA     |
|  |                     | 128 byte RAM retention, CRYO-TIMER running from ULFRCO           | —   | 0.62 | —   | µA     |
|  |                     | 128 byte RAM retention, no RTCC                                  | —   | 0.62 | —   | µA     |
| Current consumption in EM4S Shutoff mode                             | I <sub>EM4S</sub>   | No RAM retention, no RTCC  | —   | 0.02 | —   | µA     |
| <b>Note:</b>   |                     |  |     |      |     |        |
| 1. CMU_HFXOCTRL_LOWPOWER=0   |                     |  |     |      |     |        |

#### 4.1.4.4 Current Consumption Using Radio

Unless otherwise indicated, typical conditions are: VDD = 3.3 V. T<sub>OP</sub> = 25 °C. DC-DC on. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T<sub>OP</sub> = 25 °C.

**Table 4.7. Current Consumption Using Radio 3.3 V with DC-DC**

| Parameter  | Symbol               | Test Condition  | Min | Typ  | Max | Unit |
|--|----------------------|---|-----|------|-----|------|
| Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled) | I <sub>RX</sub>      | 1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4        | —   | 8.7  | —   | mA   |
| Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)                         | I <sub>TX</sub>      | F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 3 | —   | 8.2  | —   | mA   |
|  |                      | F = 2.4 GHz, CW, 3 dBm output power                             | —   | 16.5 | —   | mA   |
| RFSENSE current consumption  | I <sub>RFSENSE</sub> |   | —   | 51   | —   | nA   |

#### 4.1.5 Wake up times

**Table 4.8. Wake up times**

| Parameter  | Symbol               | Test Condition            | Min | Typ  | Max | Unit       |
|--|----------------------|---------------------------|-----|------|-----|------------|
| Wake up from EM2 Deep Sleep  | t <sub>EM2_WU</sub>  | Code execution from flash | —   | 10.7 | —   | µs         |
|  |                      | Code execution from RAM   | —   | 3    | —   | µs         |
| Wakeup time from EM1 Sleep   | t <sub>EM1_WU</sub>  | Executing from flash      | —   | 3    | —   | AHB Clocks |
|  |                      | Executing from RAM        | —   | 3    | —   | AHB Clocks |
| Wake up from EM3 Stop  | t <sub>EM3_WU</sub>  | Executing from flash      | —   | 10.7 | —   | µs         |
|  |                      | Executing from RAM        | —   | 3    | —   | µs         |
| Wake up from EM4H Hibernate <sup>1</sup>   | t <sub>EM4H_WU</sub> | Executing from flash      | —   | 60   | —   | µs         |
| Wake up from EM4S Shut-off <sup>1</sup>  | t <sub>EM4S_WU</sub> |                           | —   | 290  | —   | µs         |
| <b>Note:</b>   |                      |                           |     |      |     |            |
| 1. Time from wakeup request until first instruction is executed. Wakeup results in device reset. |                      |                           |     |      |     |            |

#### 4.1.6 Brown Out Detector

For the table below, see [Figure 3.2 Power Supply Configuration on page 5](#) on page 5 to see the relation between the modules external VDD pin and internal voltage supplies. The module itself has only one external power supply input (VDD).

**Table 4.9. Brown Out Detector**

| Parameter           | Symbol                     | Test Condition               | Min  | Typ | Max  | Unit |
|---------------------|----------------------------|------------------------------|------|-----|------|------|
| AVDD BOD threshold  | V <sub>AVDDBOD</sub>       | AVDD rising                  | —    | —   | 1.85 | V    |
|                     |                            | AVDD falling                 | 1.62 | —   | —    | V    |
| AVDD BOD hysteresis | V <sub>AVDDBOD_HYST</sub>  |                              | —    | 21  | —    | mV   |
| AVDD response time  | t <sub>AVDDBOD_DELAY</sub> | Supply drops at 0.1V/μs rate | —    | 2.4 | —    | μs   |
| EM4 BOD threshold   | V <sub>EM4BOD</sub>        | AVDD rising                  | —    | —   | 1.7  | V    |
|                     |                            | AVDD falling                 | 1.45 | —   | —    | V    |
| EM4 BOD hysteresis  | V <sub>EM4BOD_HYST</sub>   |                              | —    | 46  | —    | mV   |
| EM4 response time   | t <sub>EM4BOD_DELAY</sub>  | Supply drops at 0.1V/μs rate | —    | 300 | —    | μs   |

#### 4.1.7 Frequency Synthesizer Characteristics

**Table 4.10. Frequency Synthesizer Characteristics**

| Parameter  | Symbol                  | Test Condition          | Min  | Typ | Max    | Unit |
|--|-------------------------|-------------------------|------|-----|--------|------|
| RF Synthesizer Frequency range                       | F <sub>RANGE_2400</sub> | 2.4 GHz frequency range | 2400 | —   | 2483.5 | MHz  |
| LO tuning frequency resolution with 38.4 MHz crystal | F <sub>RES_2400</sub>   | 2400 - 2483.5 MHz       | —    | —   | 73     | Hz   |
| Maximum frequency deviation with 38.4 MHz crystal    | ΔF <sub>MAX_2400</sub>  |                         | —    | —   | 1677   | kHz  |

## 4.1.8 2.4 GHz RF Transceiver Characteristics

### 4.1.8.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are:  $T_{OP} = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ , DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

**Table 4.11. RF Transmitter General Characteristics for 2.4 GHz Band**

| Parameter  | Symbol          | Test Condition   | Min  | Typ | Max    | Unit |
|--|-----------------|--|------|-----|--------|------|
| Maximum TX power                                       | $POUT_{MAX}$    |  | —    | +3  | —      | dBm  |
| Minimum active TX Power                                | $POUT_{MIN}$    | CW   |      | -26 | —      | dBm  |
| Output power step size                                 | $POUT_{STEP}$   | -5 dBm < Output power < 0 dBm  | —    | 1   | —      | dB   |
|  |                 | 0 dBm < output power < $POUT_{MAX}$  | —    | 0.5 | —      | dB   |
| Output power variation vs supply at $POUT_{MAX}$       | $POUT_{VAR\_V}$ | 1.85 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected directly to external supply, for output power = 8 dBm. | —    | 3.8 | —      | dB   |
|  |                 | 1.85 V < $V_{VREGVDD}$ < 3.3 V using DC-DC converter   | —    | 2.2 | —      | dB   |
| Output power variation vs temperature at $POUT_{MAX}$  | $POUT_{VAR\_T}$ | From -40 to +85 °C, PAVDD connected to DC-DC output  | —    | 1.5 | —      | dB   |
| Output power variation vs RF frequency at $POUT_{MAX}$ | $POUT_{VAR\_F}$ | Over RF tuning frequency range   | —    | 0.4 | —      | dB   |
| RF tuning frequency range                              | $F_{RANGE}$     |  | 2400 | —   | 2483.5 | MHz  |



**4.1.8.2 RF Receiver General Characteristics for the 2.4 GHz Band**

Unless otherwise indicated, typical conditions are:  $T_{OP} = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ , DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.440 GHz. Conducted measurement from the antenna feedpoint.

**Table 4.12. RF Receiver General Characteristics for 2.4 GHz Band**

| Parameter   | Symbol            | Test Condition                            | Min  | Typ   | Max    | Unit |
|---|-------------------|---|------|-------|--------|------|
| RF tuning frequency range   | $F_{RANGE}$       |   | 2400 | —     | 2483.5 | MHz  |
| Receive mode maximum spurious emission                                    | $SPUR_{RX}$       | 30 MHz to 1 GHz                           | —    | -57   | —      | dBm  |
|   |                   | 1 GHz to 12 GHz                           | —    | -47   | —      | dBm  |
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX\_FCC}$  | 216 MHz to 960 MHz, Conducted Measurement | —    | -55.2 | —      | dBm  |
|   |                   | Above 960 MHz, Conducted Measurement      | —    | -47.2 | —      | dBm  |
| Level above which RFSENSE will trigger <sup>1</sup>                       | $RFSENSE_{TRIG}$  | CW at 2.45 GHz                            | —    | -24   | —      | dBm  |
| Level below which RFSENSE will not trigger <sup>1</sup>                   | $RFSENSE_{THRES}$ |   | —    | -50   | —      | dBm  |

**Note:**

1. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

### 4.1.8.3 RF Receiver Characteristics for Bluetooth Smart in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are:  $T_{OP} = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ . Crystal frequency = 38.4 MHz. RF center frequency 2.440 GHz. DC-DC on. Conducted measurement from the antenna feedpoint.

**Table 4.13. RF Receiver Characteristics for Bluetooth Smart in the 2.4GHz Band**

| Parameter  | Symbol               | Test Condition  | Min | Typ   | Max  | Unit |
|--|----------------------|---|-----|-------|------|------|
| Max usable receiver input level, 0.1% BER  | SAT                  | Signal is reference signal <sup>1</sup> . Packet length is 20 bytes.  | —   | 10    | —    | dBm  |
| 30.8% Packet Error Rate <sup>2</sup>   | SENS                 | With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1 | —   | -92   | —    | dBm  |
| Signal to co-channel interferer, 0.1% BER  | $C/I_{CC}$           | Desired signal 3 dB above reference sensitivity                       | —   | 8.3   | —    | dB   |
| Blocking, 0.1% BER, Desired is reference signal at -67 dBm. Interferer is CW in OOB range. | BLOCK <sub>OOB</sub> | Interferer frequency $30\text{ MHz} \leq f \leq 2000\text{ MHz}$      | —   | -27   | —    | dBm  |
|  |                      | Interferer frequency $2003\text{ MHz} \leq f \leq 2399\text{ MHz}$    | —   | -32   | —    | dBm  |
|  |                      | Interferer frequency $2484\text{ MHz} \leq f \leq 2997\text{ MHz}$    | —   | -32   | —    | dBm  |
|  |                      | Interferer frequency $3\text{ GHz} \leq f \leq 12.75\text{ GHz}$      | —   | -27   | —    | dBm  |
| Intermodulation performance  | IM                   | Per Core_4.1, Vol 6, Part A, Section 4.4 with $n = 3$                 | —   | -25.8 | —    | dBm  |
| Upper limit of input power range over which RSSI resolution is maintained                  | RSSI <sub>MAX</sub>  |   | 4   | —     | —    | dBm  |
| Lower limit of input power range over which RSSI resolution is maintained                  | RSSI <sub>MIN</sub>  |   | —   | —     | -101 | dBm  |
| RSSI resolution  | RSSI <sub>RES</sub>  | Over RSSI <sub>MIN</sub> to RSSI <sub>MAX</sub>                       | —   | —     | 0.5  | dB   |

**Note:**

- Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm
- Receive sensitivity on Bluetooth Smart channel 26 is -86 dBm

## 4.1.9 Oscillators

### 4.1.9.1 LFXO

**Table 4.14. LFXO**

| Parameter  | Symbol     | Test Condition | Min  | Typ    | Max | Unit |
|--|------------|----------------|------|--------|-----|------|
| Crystal frequency  | $f_{LFXO}$ |                | —    | 32.768 | —   | kHz  |
| Overall frequency tolerance in all conditions <sup>1</sup>       |            |                | -100 |        | 100 | ppm  |
| <b>Note:</b><br>1. XTAL nominal frequency tolerance = +/- 20 ppm |            |                |      |        |     |      |

### 4.1.9.2 HFXO

**Table 4.15. HFXO**

| Parameter                   | Symbol     | Test Condition | Min | Typ  | Max | Unit |
|-----------------------------|------------|----------------|-----|------|-----|------|
| Crystal frequency           | $f_{HFXO}$ |                | -   | 38.4 | -   | MHz  |
| Crystal frequency tolerance |            |                | -40 |      | 40  | ppm  |

### 4.1.9.3 LFRCO

**Table 4.16. LFRCO**

| Parameter   | Symbol      | Test Condition              | Min    | Typ    | Max    | Unit |
|---|-------------|-----------------------------|--------|--------|--------|------|
| Oscillation frequency   | $f_{LFRCO}$ | ENVREF = 1 in CMU_LFRCOCTRL | 30.474 | 32.768 | 34.243 | kHz  |
|   |             | ENVREF = 0 in CMU_LFRCOCTRL | 30.474 | 32.768 | 33.915 | kHz  |
| Startup time  | $t_{LFRCO}$ |                             | —      | 500    | —      | μs   |
| Current consumption <sup>1</sup>  | $I_{LFRCO}$ | ENVREF = 1 in CMU_LFRCOCTRL | —      | 342    | —      | nA   |
|   |             | ENVREF = 0 in CMU_LFRCOCTRL | —      | 494    | —      | nA   |
| <b>Note:</b><br>1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register |             |                             |        |        |        |      |