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BGSX212MA18

DP12T Diversity Cross Switch for Carrier Aggregation

Data Sheet

Revision 3.1 - 2016-11-03

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| Page | Subjects (major changes since last revision) |
|------|--|
| 9 | RF performance updated in Table 5 |
| 13 | Application information updated in Table 12 |
| | |

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Contents

| | | |
|----------|--------------------------------|-----------|
| 1 | Features | 5 |
| 2 | Product Description | 5 |
| 3 | Maximum Ratings | 6 |
| 4 | Operation Ranges | 8 |
| 5 | RF Characteristics | 9 |
| 6 | MIPI RFFE Specification | 10 |
| 7 | Application Information | 13 |
| 8 | Package Information | 14 |

List of Figures

| | | |
|---|---|----|
| 1 | BGSX212MA18 Block diagram | 6 |
| 2 | BGSX212MA18 Application Schematic | 13 |
| 3 | BGSX212MA18 Pin Configuration (top view) | 14 |
| 4 | ATSLP-18 Package Outline (top, side and bottom views) | 15 |
| 5 | Land Pattern and Stencil Mask | 15 |
| 6 | Laser Marking (top view) | 16 |
| 7 | Carrier Tape | 16 |

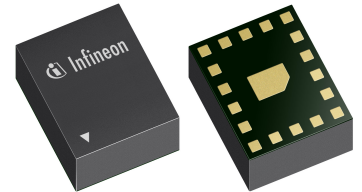
List of Tables

| | | |
|----|---|----|
| 1 | Maximum Ratings, Table I | 6 |
| 2 | Maximum Ratings, Table II | 7 |
| 3 | Operation Ranges | 8 |
| 4 | RF Input Power | 8 |
| 5 | RF Characteristics | 9 |
| 6 | MIPI Features | 10 |
| 7 | Startup Behavior | 10 |
| 8 | Register Mapping | 10 |
| 9 | Truth Table, Switch A | 12 |
| 10 | Truth Table, Switch B | 12 |
| 11 | Truth Table, Cross Ports | 12 |
| 12 | Bill of Materials for frequency range 2500 to 2700MHz | 13 |
| 13 | Bill of Materials for frequency range 3400 to 3800MHz | 13 |
| 14 | Pin Definition and Function | 14 |

BGSX212MA18 DP12T Diversity Cross Switch for Carrier Aggregation

1 Features

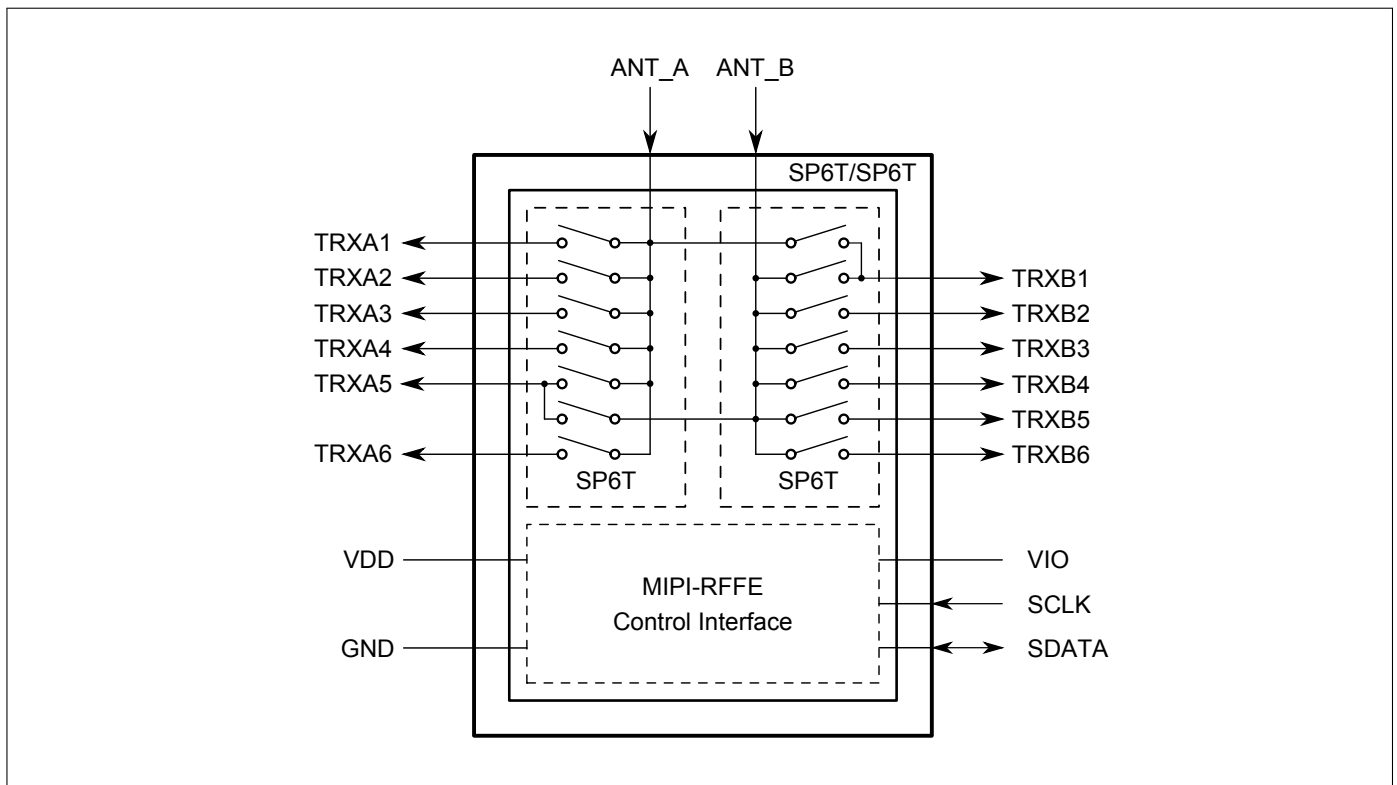
- RF CMOS DP12T diversity switch with power handling capability of up to 27 dBm
- Industry's first flexible carrier aggregation switch via cross switch functionality of two ports
- Device configurations SP6T/SP6T, SP5T/SP7T, and SP7T/SP5T featured via cross switch functionality
- Suitable for LTE carrier aggregation applications
- Ultra-low insertion loss and harmonics generation
- 0.1 to 3.8 GHz coverage
- High port-to-port-isolation
- No decoupling capacitors required if no DC applied on RF lines
- Integrated MIPI RFFE interface operating in 1.1 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- Leadless and halogen free package ATSLP-18 with lateral size of 2.0 mm x 2.4 mm and thickness of 0.6 mm
- No power supply blocking required
- High EMI robustness
- RoHS and WEEE compliant package



2 Product Description

The BGSX212MA18 RF CMOS switch is specifically designed for LTE carrier aggregation applications. This DP12T offers low insertion loss and low harmonic generation. In addition, two ports feature cross functionality enabling higher flexibility for carrier aggregation applications.

The switch is controlled via a MIPI RFFE controller. The on-chip controller allows power-supply voltages from 1.1 to 1.95 V. The switch features direct-connect-to-battery functionality and DC-free RF ports. Unlike GaAs technology, external DC blocking capacitors at the RF Ports are only required if DC voltage is applied externally. The BGSX212MA18 RF Switch is manufactured in Infineon's patented MOS technology, offering the performance of GaAs with the economy and integration of conventional CMOS including the inherent higher ESD robustness. The device has a very small size of only 2.0 x 2.4 mm² and a maximum thickness of 0.6 mm.


Figure 1: BGSX212MA18 Block diagram

3 Maximum Ratings

Table 1: Maximum Ratings, Table I at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------------------|--|
| | | Min. | Typ. | Max. | | |
| Frequency Range | f | 0.1 | – | 3.8 | GHz | 1) |
| Supply voltage | V_{DD} | -0.5 | – | 3.6 | V | – |
| Storage temperature range | T_{STG} | -55 | – | 150 | $^\circ\text{C}$ | – |
| Junction temperature | T_j | – | – | 125 | $^\circ\text{C}$ | – |
| RF input power at all TRX ports | P_{RF} | – | – | 32 | dBm | CW |
| ESD capability, HBM ²⁾ | V_{ESDHBM} | -1 | – | +1 | kV | |
| ESD capability, system level ³⁾ | V_{ESDANT} | -8 | – | +8 | kV | ANT versus system GND, with 27 nH shunt inductor |

¹⁾Switch has no highpass response. There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0V.

²⁾ANSI/ESDA/JEDEC JS-001-2012 (R=1.5 k Ω , C=100 pF).

³⁾IEC 61000-4-2 (R=330 Ω , C=150 pF), contact discharge.

Table 2: Maximum Ratings, Table II at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------------------------|--------|------|-------------------------------|------|------------------------------------|
| | | Min. | Typ. | Max. | | |
| Maximum DC-voltage on RF-Ports and RF-Ground | V_{RFDC} | 0 | – | 0 | V | No DC voltages allowed on RF-Ports |
| RFFE Supply Voltage | V_{IO} | -0.5 | – | 3.6 | V | – |
| RFFE Control Voltage Levels | V_{SCLK} , V_{SDATA} | -0.7 | – | $V_{IO}+0.7$ (max. 3.6) | V | – |

4 Operation Ranges

Table 3: Operation Ranges

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------------------|------|--------------------|--------------------|--|
| | | Min. | Typ. | Max. | | |
| Supply voltage | V_{DD} | 2.5 | – | 3.4 | V | – |
| Supply current ²⁾ | I_{DD} | – | 90 | 200 | μA | – |
| Supply current in standby mode ²⁾ | I_{DD} | – | 0.5 | 1 | μA | $V_{IO}=\text{low}$ or MIPI low-power mode |
| RFFE supply voltage | V_{IO} | 1.1 | 1.8 | 1.95 | V | – |
| RFFE input high voltage ¹⁾ | V_{IH} | $0.7 \cdot V_{IO}$ | – | V_{IO} | V | – |
| RFFE input low voltage ¹⁾ | V_{IL} | 0 | – | $0.3 \cdot V_{IO}$ | V | – |
| RFFE output high voltage ¹⁾ | V_{OH} | $0.8 \cdot V_{IO}$ | – | V_{IO} | V | – |
| RFFE output low voltage ¹⁾ | V_{OL} | 0 | – | $0.2 \cdot V_{IO}$ | V | – |
| RFFE control input capacitance | C_{Ctrl} | – | – | 2 | pF | – |
| RFFE supply current | I_{VIO} | – | 15 | – | μA | Idle State |
| Ambient temperature | T_A | -30 | 25 | 85 | $^{\circ}\text{C}$ | – |

¹⁾SCLK and SDATA

²⁾ $T_A = -30^{\circ}\text{C} \dots 85^{\circ}\text{C}$, $V_{DD} = 2.5 \dots 3.4\text{V}$
Table 4: RF Input Power

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------|----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| TRX ports ($50\ \Omega$) | P_{RF} | – | – | 27 | dBm | – |

5 RF Characteristics

Table 5: RF Characteristics at $T_A = -30\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$, $P_{IN} = 0\text{ dBm}$, Supply Voltage $V_{DD} = 2.5\text{ V} \dots 3.4\text{ V}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------|--------|------|------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Insertion Loss¹⁾ | | | | | | |
| All TRX ports | IL | – | 0.30 | 0.45 | dB | 100 to 960MHz |
| | | – | 0.45 | 0.75 | dB | 960 to 2170MHz |
| | | – | 0.65 | 0.90 | dB | 2170 to 2700MHz ²⁾ |
| | | – | 0.90 | 1.35 | dB | 3400 to 3800MHz ³⁾ |
| Insertion Loss | | | | | | |
| All TRX ports | IL | – | 0.30 | 0.50 | dB | 100 to 960MHz |
| | | – | 0.45 | 0.85 | dB | 960 to 2170MHz |
| | | – | 0.65 | 1.00 | dB | 2170 to 2700MHz ²⁾ |
| | | – | 0.90 | 1.45 | dB | 3400 to 3800MHz ³⁾ |
| Return Loss | | | | | | |
| All TRX ports | RL | 17 | 24 | – | dB | 100 to 960MHz |
| | | 14 | 21 | – | dB | 960 to 2170MHz |
| | | 12 | 16 | – | dB | 2170 to 2700MHz ²⁾ |
| | | 10 | 15 | – | dB | 3400 to 3800MHz ³⁾ |
| Isolation | | | | | | |
| Adjacent TRX ports A-A/B-B | ISO | 26 | 36 | – | dB | 100 to 960MHz |
| | | 19 | 26 | – | dB | 960 to 2170MHz |
| | | 16 | 21 | – | dB | 2170 to 2700MHz |
| Opposite TRX ports A-B/B-A | ISO | 38 | 48 | – | dB | 100 to 960MHz |
| | | 31 | 41 | – | dB | 960 to 2170MHz |
| | | 29 | 39 | – | dB | 2170 to 2700MHz |
| Harmonic Generation⁴⁾ | | | | | | |
| All TRX ports, H2 | P_{Harm} | 80 | 90 | – | dBc | 25 dBm, 50 Ω , CW mode |
| All TRX ports, H3 | P_{Harm} | 80 | 90 | – | dBc | 25 dBm, 50 Ω , CW mode |
| Intermodulation Distortion in Rx Band^{1) 4)} ($T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V}$) | | | | | | |
| IMD2, low | $IMD2_{low}$ | – | -105 | -100 | dBm | Tx = 20 dBm, Interferer = -15 dBm, 50 Ω |
| IMD3 | IMD3 | – | -115 | -110 | dBm | |
| IMD2, high | $IMD2_{high}$ | – | -105 | -100 | dBm | |
| Switching Time | | | | | | |
| MIPI to RF time ¹⁾ | t_{INT} | – | 1.5 | 3 | μs | 50 % last SCLK falling edge to 90 % ON |
| Power up settling time ¹⁾ | t_{PUP} | – | 10 | 25 | μs | After power down mode |

¹⁾ Measured at 25°C.

²⁾ On application board with application circuit according to Fig. 2 and Tab. 12.

³⁾ On application board with application circuit according to Fig. 2 and Tab. 13.

⁴⁾ Measured at Band 5.

6 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011.

Table 6: MIPI Features

| Feature | Supported | Comment |
|--|-----------|--|
| Register write command sequence | Yes | |
| Register read command sequence | Yes | |
| Extended register write command sequence | No | Up to 4 Bytes |
| Extended register read command sequence | No | Up to 4 Bytes |
| Register 0 write command sequence | Yes | |
| Trigger function | Yes | Trigger assignment to each control register is supported |
| Programmable USID | Yes | 3 register command sequence |
| Status Register | Yes | Register for debugging |
| Reset | Yes | By VIO, Power Mode and RFFE_STATUS |
| Group SID | Yes | |
| USID_Sel pin | No | External pin for changing USID is not implemented |
| Full speed write | Yes | |
| Half speed read | Yes | |
| Full speed read | Yes | |

Table 7: Startup Behavior

| Feature | State | Comment |
|------------------|-----------|---|
| Power status | LOW POWER | The chip is in low power mode after startup |
| Trigger function | ENABLED | Trigger function is enabled after startup. Trigger function can be disabled via PM_TRIG register. |

Table 8: Register Mapping

| Register Address | Register Name | Data Bits | Function | Description | Default | Broadcast_ID Support | Trigger Support | R/W |
|------------------|-----------------|-----------|-----------------------|---|----------|----------------------|-----------------|-----|
| 0x0000 | REGISTER_0 | 7:0 | MODE_CTRL | Switch control | 00000000 | No | Yes | R/W |
| 0x0001 | REGISTER_1 | 7:0 | MODE_CTRL | Switch control | 00000000 | No | Yes | R/W |
| 0x001D | PRODUCT_ID | 7:0 | PRODUCT_ID | This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value. | 11011111 | No | No | R |
| 0x001E | MANUFACTURER_ID | 7:0 | MANUFACTURER_ID [7:0] | This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. | 00011010 | No | No | R |

Continued on next page

Table 8: Register Mapping – Continued from previous page

| Register Address | Register Name | Data Bits | Function | Description | Default | Broadcast_ID Support | Trigger Support | R/W |
|------------------|---------------|-----------|--------------------------|---|---------|----------------------|-----------------|-----|
| 0x001C | PM_TRIG | 7:6 | PWR_MODE | 00: Normal operation 01: Default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved | 10 | Yes | No | R/W |
| | | 5 | TRIGGER_MASK_2 | If this bit is set, trigger 2 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 2, the data goes directly to the destination register. | 0 | No | No | |
| | | 4 | TRIGGER_MASK_1 | If this bit is set, trigger 1 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 1, the data goes directly to the destination register. | 0 | No | No | |
| | | 3 | TRIGGER_MASK_0 | If this bit is set, trigger 0 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 0, the data goes directly to the destination register. | 0 | No | No | |
| | | 2 | TRIGGER_2 | A write of a one to this bit loads trigger 2's registers. | 0 | Yes | No | |
| | | 1 | TRIGGER_1 | A write of a one to this bit loads trigger 1's registers. | 0 | Yes | No | R/W |
| | | 0 | TRIGGER_0 | A write of a one to this bit loads trigger 0's registers. | 0 | Yes | No | |
| 0x001F | MAN_USID | 7:6 | SPARE | These are read-only bits that are reserved and yield a value of 0b00 at readback. | 00 | No | No | R/W |
| | | 5:4 | MANUFACTURER_ID [9:8] | These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value. | 01 | | | |
| | | 3:0 | USID | Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device. | 1010 | | | |
| 0x001A | RFFE_STATUS | 7 | SOFTWARE RESET | 0: Normal operation 1: Software reset | 0 | No | No | R/W |
| | | 6 | COMMAND_FRAME_PARITY_ERR | Command sequence received with parity error - discard command. | 0 | No | No | R |
| | | 5 | COMMAND_LENGTH_ERR | Command length error | 0 | | | |
| | | 4 | ADDRESS_FRAME_PARITY_ERR | Address frame parity error = 1 | 0 | | | |
| | | 3 | DATA_FRAME_PARITY_ERR | Data frame with parity error | 0 | | | |
| | | 2 | READ_UNUSED_REG | Read command to an invalid address | 0 | | | |
| | | 1 | WRITE_UNUSED_REG | Write command to an invalid address | 0 | | | |
| | | 0 | BID_GID_ERR | Read command with a BROADCAST_ID or GROUP_SID | 0 | | | |
| 0x001B | GROUP_SID | 7:4 | RESERVED | | 0 | No | No | R/W |
| | | 3:0 | GROUP_SID | Group slave ID | 0 | | | |

Table 9: Modes of Operation (Truth Table, Switch A)

| State | Mode | REGISTER_1 Bits | | | | | | | |
|-------|---------------|-----------------|----|----|----|----|----|----|----|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | All Isolation | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | TRXA1 | x | x | x | 0 | 0 | 0 | 0 | 1 |
| 3 | TRXA2 | x | x | x | 0 | 0 | 0 | 1 | 0 |
| 4 | TRXA3 | x | x | x | 0 | 0 | 0 | 1 | 1 |
| 5 | TRXA4 | x | x | x | 0 | 0 | 1 | 0 | 0 |
| 6 | TRXA5 | x | x | x | 0 | 0 | 1 | 0 | 1 |
| 7 | TRXA6 | x | x | x | 0 | 0 | 1 | 1 | 0 |
| 8 | TRXA6+TRXA5 | x | x | x | 0 | 0 | 1 | 1 | 1 |
| 9 | TRXA6+TRXA4 | x | x | x | 0 | 1 | 0 | 0 | 0 |
| 10 | TRXA6+TRXA3 | x | x | x | 0 | 1 | 0 | 0 | 1 |
| 11 | TRXA6+TRXA2 | x | x | x | 0 | 1 | 0 | 1 | 0 |
| 12 | TRXA6+TRXA1 | x | x | x | 0 | 1 | 0 | 1 | 1 |
| 13 | TRXA5+TRXA4 | x | x | x | 0 | 1 | 1 | 0 | 0 |
| 14 | TRXA5+TRXA3 | x | x | x | 0 | 1 | 1 | 0 | 1 |
| 15 | TRXA5+TRXA2 | x | x | x | 0 | 1 | 1 | 1 | 0 |
| 16 | TRXA5+TRXA1 | x | x | x | 0 | 1 | 1 | 1 | 1 |
| 17 | TRXA4+TRXA3 | x | x | x | 1 | 0 | 0 | 0 | 0 |
| 18 | TRXA4+TRXA2 | x | x | x | 1 | 0 | 0 | 0 | 1 |
| 19 | TRXA4+TRXA1 | x | x | x | 1 | 0 | 0 | 1 | 0 |
| 20 | TRXA3+TRXA2 | x | x | x | 1 | 0 | 0 | 1 | 1 |
| 21 | TRXA3+TRXA1 | x | x | x | 1 | 0 | 1 | 0 | 0 |
| 22 | TRXA2+TRXA1 | x | x | x | 1 | 0 | 1 | 0 | 1 |
| 23-32 | All Isolation | 0x16 - 0x1F | | | | | | | |

Table 10: Modes of Operation (Truth Table, Switch B)

| State | Mode | REGISTER_0 Bits | | | | | | | |
|-------|---------------|-----------------|----|----|----|----|----|----|----|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 33 | All Isolation | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 34 | TRXB1 | x | x | x | 0 | 0 | 0 | 0 | 1 |
| 35 | TRXB2 | x | x | x | 0 | 0 | 0 | 1 | 0 |
| 36 | TRXB3 | x | x | x | 0 | 0 | 0 | 1 | 1 |
| 37 | TRXB4 | x | x | x | 0 | 0 | 1 | 0 | 0 |
| 38 | TRXB5 | x | x | x | 0 | 0 | 1 | 0 | 1 |
| 39 | TRXB6 | x | x | x | 0 | 0 | 1 | 1 | 0 |
| 40 | TRXB6+TRXB5 | x | x | x | 0 | 0 | 1 | 1 | 1 |
| 41 | TRXB6+TRXB4 | x | x | x | 0 | 1 | 0 | 0 | 0 |
| 42 | TRXB6+TRXB3 | x | x | x | 0 | 1 | 0 | 0 | 1 |
| 43 | TRXB6+TRXB2 | x | x | x | 0 | 1 | 0 | 1 | 0 |
| 44 | TRXB6+TRXB1 | x | x | x | 0 | 1 | 0 | 1 | 1 |
| 45 | TRXB5+TRXB4 | x | x | x | 0 | 1 | 1 | 0 | 0 |
| 46 | TRXB5+TRXB3 | x | x | x | 0 | 1 | 1 | 0 | 1 |
| 47 | TRXB5+TRXB2 | x | x | x | 0 | 1 | 1 | 1 | 0 |
| 48 | TRXB5+TRXB1 | x | x | x | 0 | 1 | 1 | 1 | 1 |
| 49 | TRXB4+TRXB3 | x | x | x | 1 | 0 | 0 | 0 | 0 |
| 50 | TRXB4+TRXB2 | x | x | x | 1 | 0 | 0 | 0 | 1 |
| 51 | TRXB4+TRXB1 | x | x | x | 1 | 0 | 0 | 1 | 0 |
| 52 | TRXB3+TRXB2 | x | x | x | 1 | 0 | 0 | 1 | 1 |
| 53 | TRXB3+TRXB1 | x | x | x | 1 | 0 | 1 | 0 | 0 |
| 54 | TRXB2+TRXB1 | x | x | x | 1 | 0 | 1 | 0 | 1 |
| 55-64 | All Isolation | 0x16 - 0x1F | | | | | | | |

Table 11: Modes of Operation (Truth Table, Cross Ports)

| State | Mode | REGISTER_2 Bits | | | | | | | |
|-------|-------------|-----------------|----|----|----|----|----|----|----|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 65 | ANT_A-TRXB1 | x | x | x | x | x | x | x | 1 |
| 66 | ANT_B-TRXA5 | x | x | x | x | x | x | 1 | x |

7 Application Information

Application Board Configuration

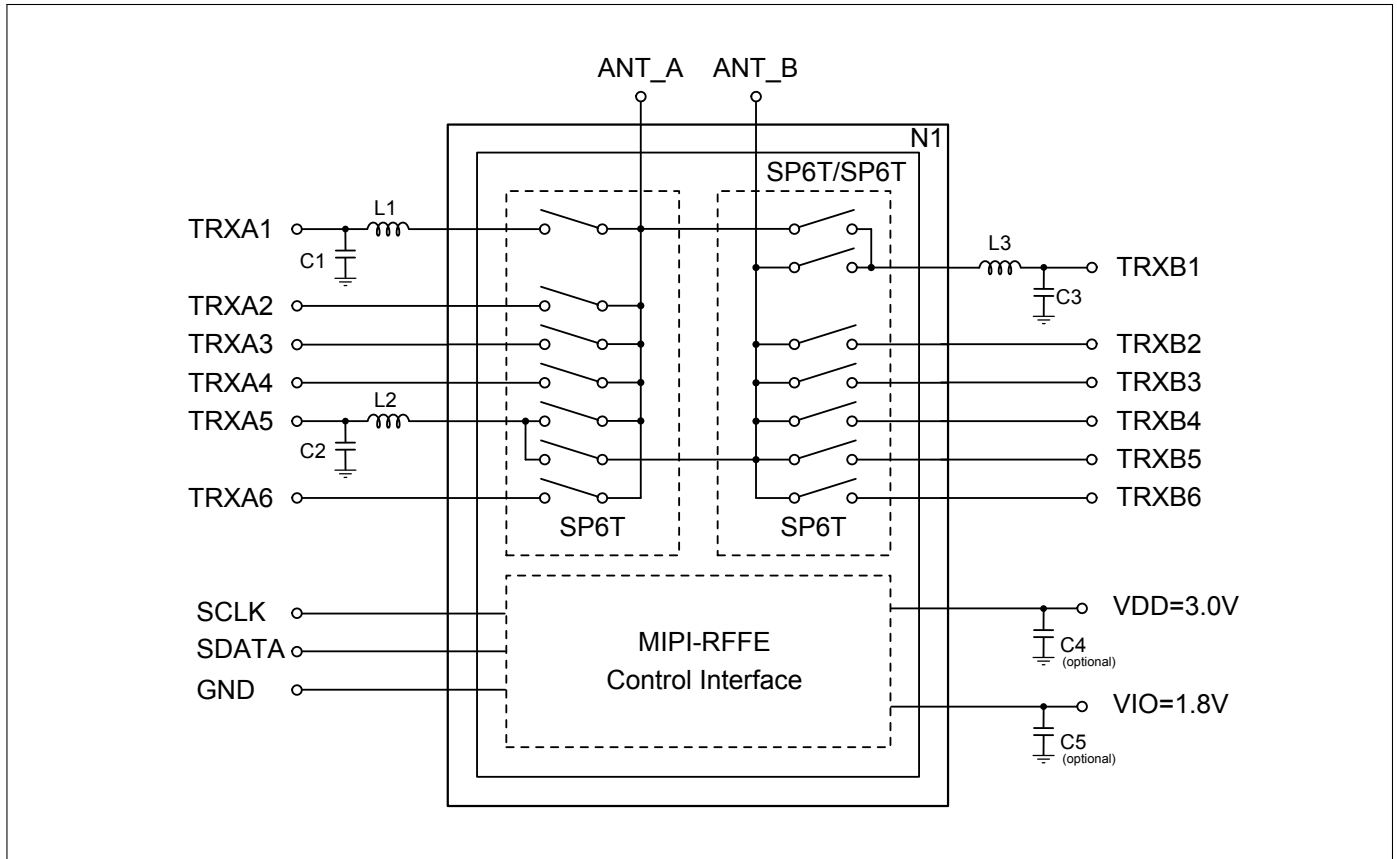


Figure 2: BGSX212MA18 Application Schematic

Table 12: Bill of Materials Table for frequency range 2500 to 2700MHz

| Name | Value | Package | Manufacturer | Function |
|------------------|-------------|----------|--------------|--------------------|
| C1=C2=C3 | 0.8 pF | 0402 | Various | Impedance Matching |
| C4=C5 (optional) | 1 nF | 0402 | Various | Impedance Matching |
| L1=L2=L3 | 2.1 nH | 0402 | Various | Impedance Matching |
| N1 | BGSX212MA18 | ATSLP-18 | Infineon | RF CMOS Switch |

Table 13: Bill of Materials Table for frequency range 3400 to 3800MHz

| Name | Value | Package | Manufacturer | Function |
|------------------|-------------|----------|--------------|--------------------|
| C1=C2=C3 | 0.8 pF | 0402 | Various | Impedance Matching |
| C4=C5 (optional) | 1 nF | 0402 | Various | Impedance Matching |
| L1=L2=L3 | 1 nH | 0402 | Various | Impedance Matching |
| N1 | BGSX212MA18 | ATSLP-18 | Infineon | RF CMOS Switch |

8 Package Information

Pin Configuration and Function

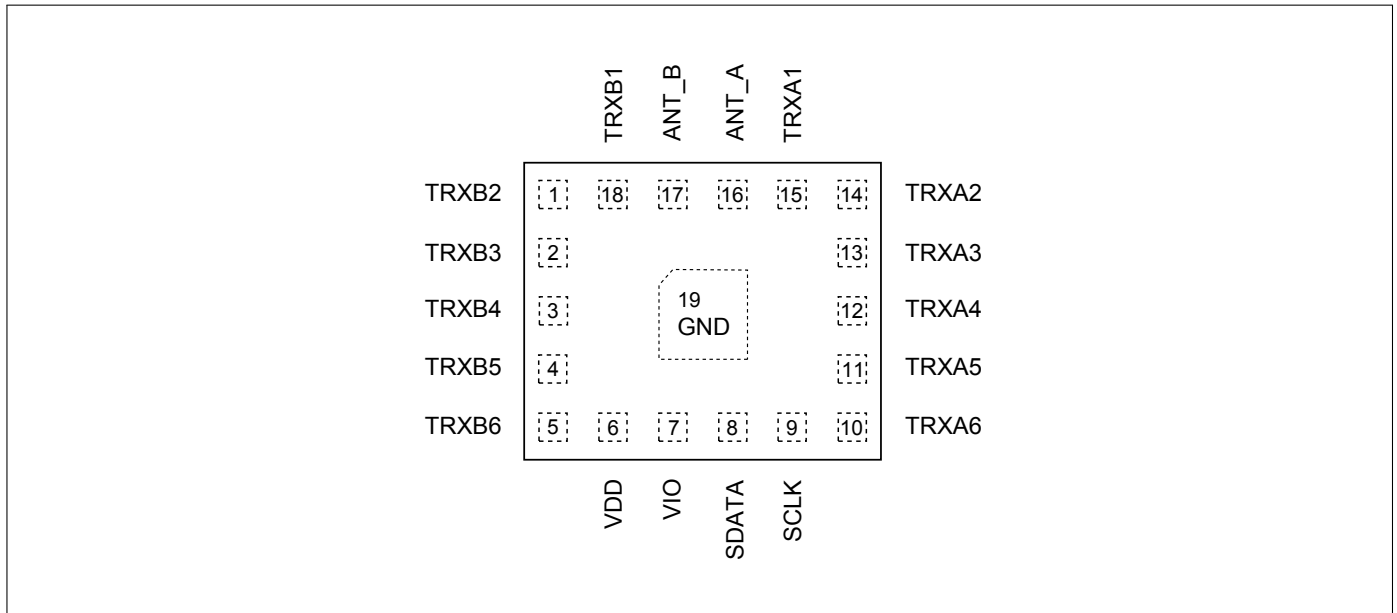


Figure 3: BGSX212MA18 Pin Configuration (top view)

Table 14: Pin Definition and Function

| Pin No. | Name | Function |
|---------|-------|------------------------|
| 1 | TRXB2 | TRX port B2 |
| 2 | TRXB3 | TRX port B3 |
| 3 | TRXB4 | TRX port B4 |
| 4 | TRXB5 | TRX port B5 |
| 5 | TRXB6 | TRX port B6 |
| 6 | VDD | Power supply |
| 7 | VIO | MIPI RFFE power supply |
| 8 | SDATA | MIPI RFFE data |
| 9 | SCLK | MIPI RFFE clock |
| 10 | TRXA6 | TRX port A6 |
| 11 | TRXA5 | TRX port A5 |
| 12 | TRXA4 | TRX port A4 |
| 13 | TRXA3 | TRX port A3 |
| 14 | TRXA2 | TRX port A2 |
| 15 | TRXA1 | TRX port A1 |
| 16 | ANT_A | Antenna port A |
| 17 | ANT_B | Antenna port B |
| 18 | TRXB1 | TRX port B1 |
| 19 | GND | RF ground |

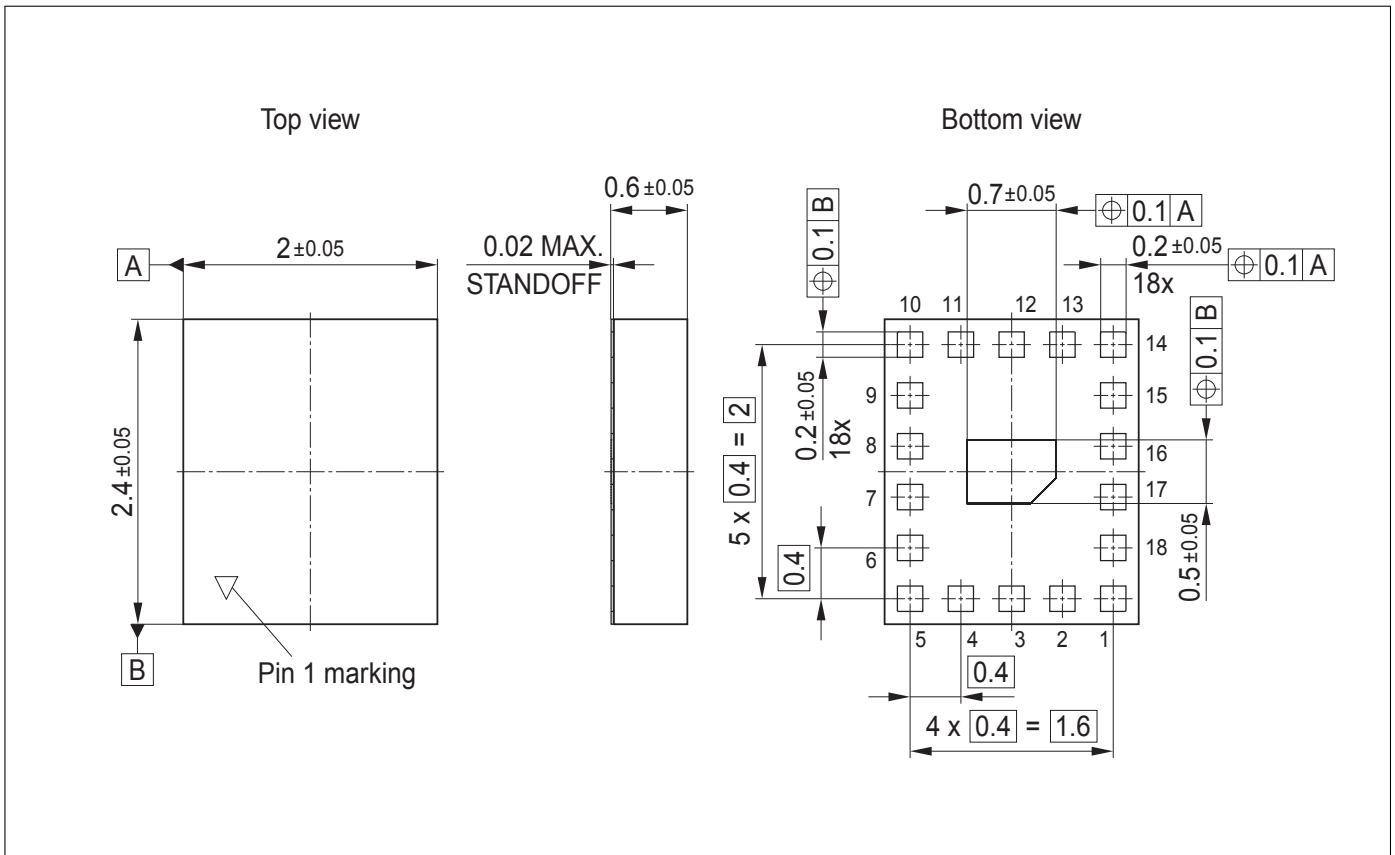


Figure 4: ATSLP-18 Package Outline (top, side and bottom views)

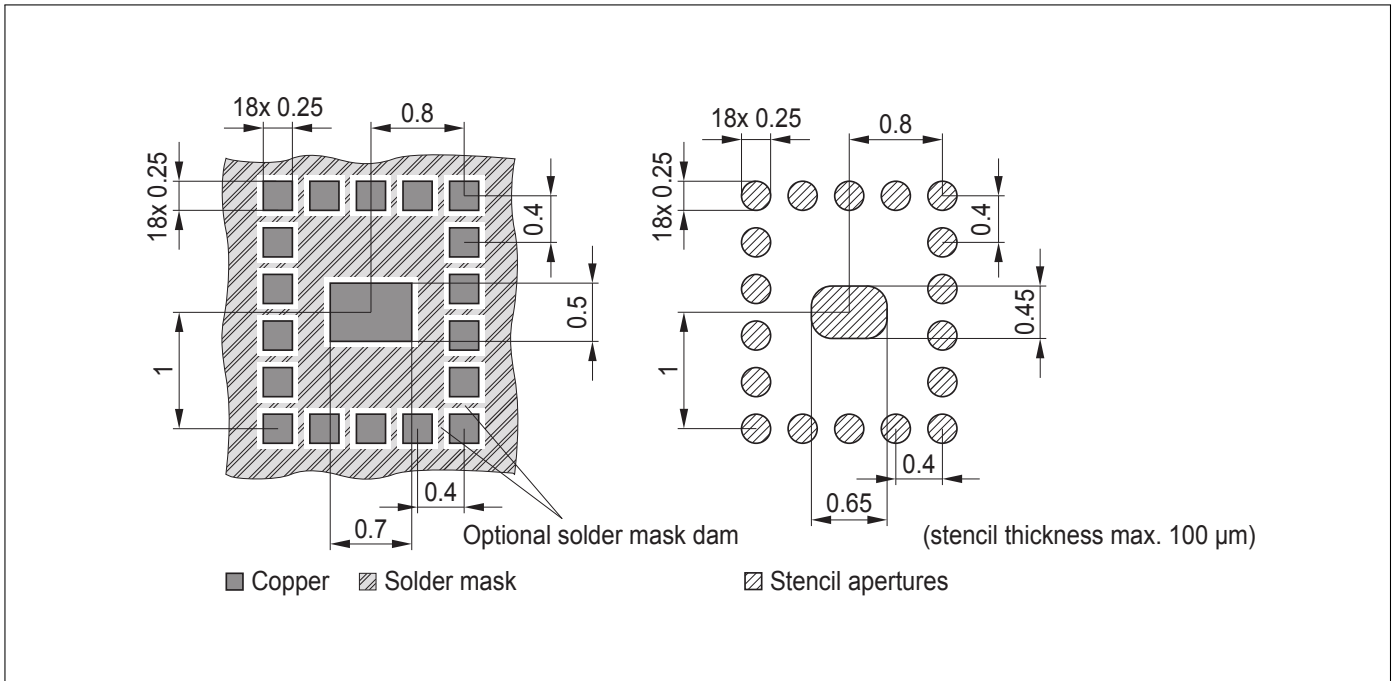


Figure 5: Land Pattern and Stencil Mask

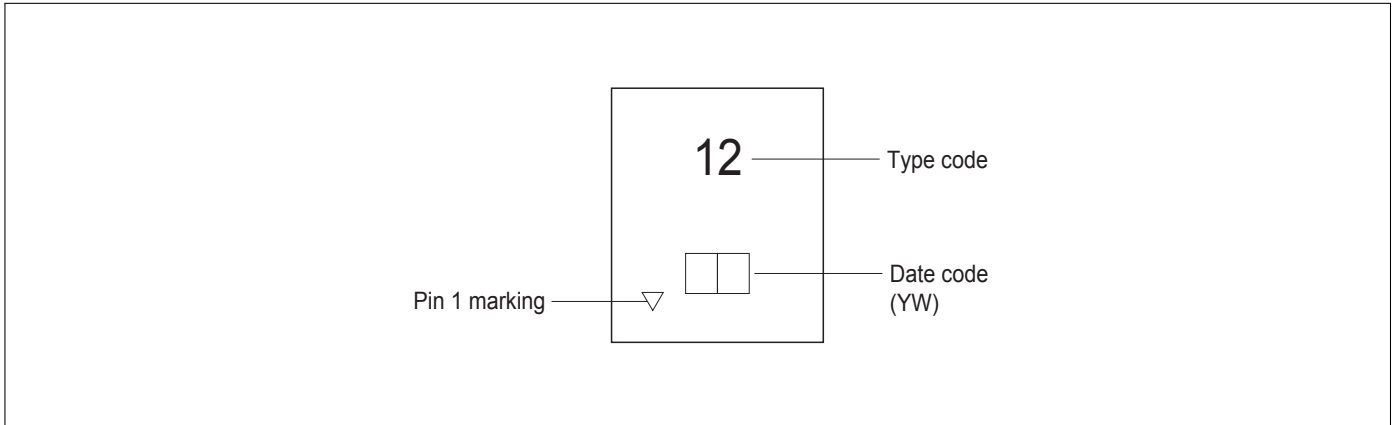


Figure 6: Laser Marking (top view)

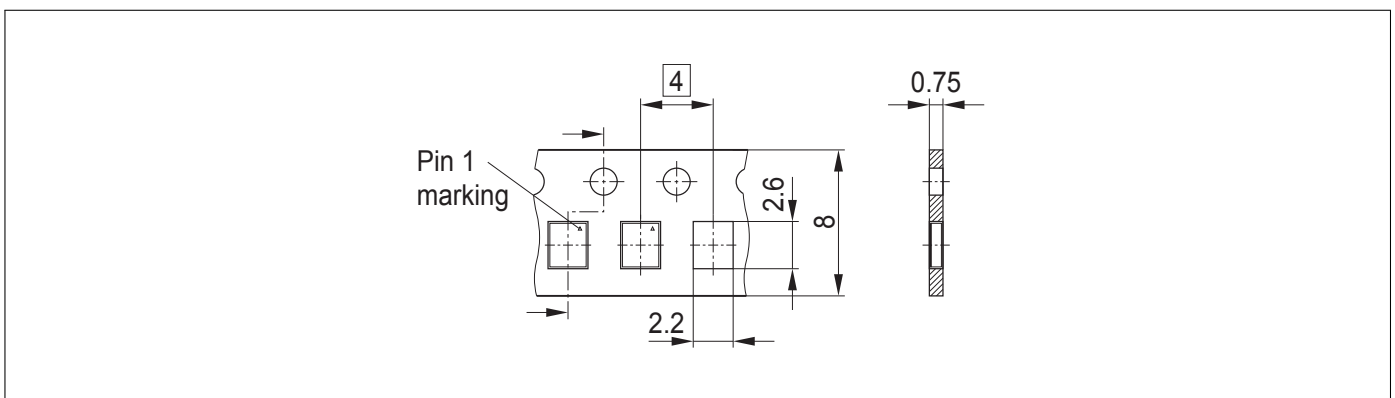


Figure 7: Carrier Tape

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