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# BGW200EG

## IEEE 802.11b System-in-Package

Rev. 01 — 18 July 2007 Product data sheet

## 1. General description

The BGW200EG is a plug-and-play System-in-Package (SiP) for IEEE Std 802.11b - 1999 Wireless Local Area Network (WLAN) intended for embedded and mobile applications.

The BGW200EG comprises an ARM7TDMI microcontroller with SRAM and ROM, an 802.11b Medium Access Controller (MAC) and compliant modem, a highly integrated RF transceiver, a linear power amplifier and an RF front-end with integrated baluns, filters and switches.

The power management and supply decoupling are fully incorporated in the BGW200EG resulting in a low height, small form factor implementation of the complete 802.11b function from the host interface to the antenna(s).

## 2. Features

### 2.1 General

- Plug-and-play IEEE Std 802.11b - 1999 WLAN System-in-Package (SiP)
- Includes all the baseband and radio functions, from host interface up to antenna, needs only external antenna and reference clock
- Support for IEEE 802.11e and Wi-Fi Multi Media (WMM) quality of service enhancements (see Section 2.6)
- Support for IEEE 802.11i and Wi-Fi Protected Access (WPA) security enhancements
- Zero host load; all WLAN functionality is implemented by the BGW200EG
- Small dimensions (10 mm × 15 mm × 1.3 mm) HLLGA68 package
- Lead-free package, RoHS 2006 compliant
- Moisture sensitivity level 4
- Ambient temperature: −30 °C to +85 °C

### 2.2 Power management

- Supply voltage range:
  - Radio transceiver: 2.7 V to 3.0 V (can be extended to $V_{DD(PA)}$ + 0.6 V)
  - Power amplifier: 2.7 V to 3.0 V
  - Baseband digital parts: 1.65 V to 1.95 V
  - Baseband analog parts: 2.7 V to 3.0 V (can be extended to $V_{DD(PA)}$ + 0.6 V)
  - Baseband peripherals: 2.7 V to 3.0 V (can be extended to $V_{DD(PA)}$ + 0.6 V)
- Low power:
  - Internal or external low-frequency sleep clock
  - Sleep power consumption: 200 μW (typical)

- Receive power consumption: 480 mW (typical)
- Transmit power consumption (17 dBm output): 750 mW (typical)

## 2.3 Radio transceiver

- Receiver sensitivity (Packet Error Rate: PER = 8 %) at 11 Mbit/s data rate: –83 dBm
- Receiver maximum input power: 0 dBm
- RX blocking filter for suppression of Global System for Mobile communication (GSM) and Data Communication System (DCS) interference signals
- Receiver RF antenna diversity fully supported
- Transmitter maximum output power: 17 dBm (with 15 dB adjustable gain)
- Transmitter Error Vector Magnitude (EVM) for 11 Msymbol/s QPSK modulation: 17 % (RMS)
- Transmitter FCC compliant spurious emission spectrum:
  - Optional output power software back-off to guarantee FCC compliance in application for low data rates in channel 1 and channel 11
  - External filter required for 2nd harmonic suppression
- Internal shielding for better ElectroMagnetic Interference (EMI) immunity

## 2.4 Baseband hardware

- IEEE 802.11b PHY and MAC:
  - Decision feedback equalizer with > 200 ns multipath delay spread tolerance
  - Antenna diversity fully supported
  - Data rates up to 11 Mbit/s
  - WEP, TKIP, CCM and AES encryption and decryption engines
- Bluetooth coexistence interface:
  - Interfaces to a range of NXP Semiconductors Bluetooth modules
  - Hardware functionality to facilitate connection to 3rd-party Bluetooth solutions
  - Hardware support for IEEE 802.15.2 packet traffic arbitration recommendations
- Embedded 32-bit microcontroller:
  - ARM7TDMI-S RISC controller featuring low mW/MHz
  - Up to 66 MHz core clock speed at 1.8 V supply voltage
  - Instruction pre-fetch unit for improved performance
  - Embedded nonvolatile memory: 256-kbit ROM
  - Embedded volatile memory: 5 × 256-kbit SRAM
  - JTAG compliant in-circuit emulation interface
- Microcontroller peripherals:
  - SPI master/slave interface
  - SPI high-speed slave interface with DMA controller
  - SDIO interface with support for SPI, SD1 and SD4 modes
  - 11 general-purpose I/O pins
  - UART
  - Five 32-bit system timers
  - Watchdog timer

### 2.5 Software

- Microcontroller firmware
- IEEE 802.11b/e/i protocol firmware (see Section 2.6)
- WPA and WMM1 protocol firmware (see Section 2.6)
- Host drivers for the following operating systems:
  - WinCE 4.2/5.0
  - Embedded Linux
- Configuration utility

### 2.6 Reference

- The MAC implemented in the SA2443A is fully compliant with the relevant parts of the published IEEE 802.11 standard and further enhanced with changes detailed in the IEEE 802.11b published amendment. The MAC has also been designed to support the soon to be published IEEE 802.11e amendment as well as the proposed WMM1 standard. The flexible architecture should allow incorporation of any further changes to these amendments and proposed standards before ratification and publication.

## 3. Applications

- IEEE 802.11b WLAN
- Smart phone or feature phone with embedded WLAN
- Personal Digital Assistant (PDA) with embedded WLAN
- Voice over IP (VoIP) cordless phone
- Mobile gaming

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BGW200EG/01 | HLLGA68 | plastic thermal enhanced low profile land grid array package; 68 lands; body 10 × 15 × 1.3 mm | SOT858-1 |

## 5. Block diagram

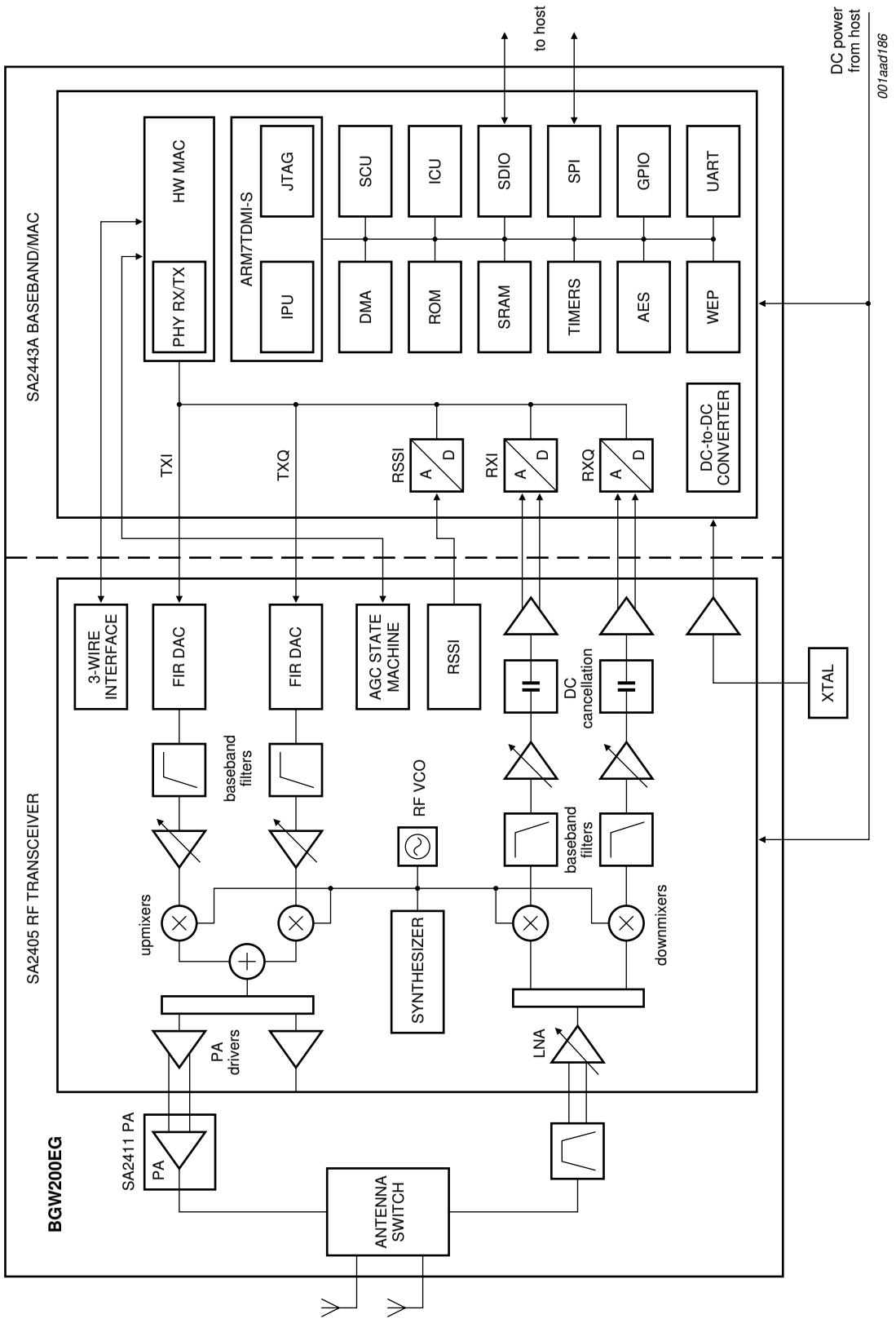
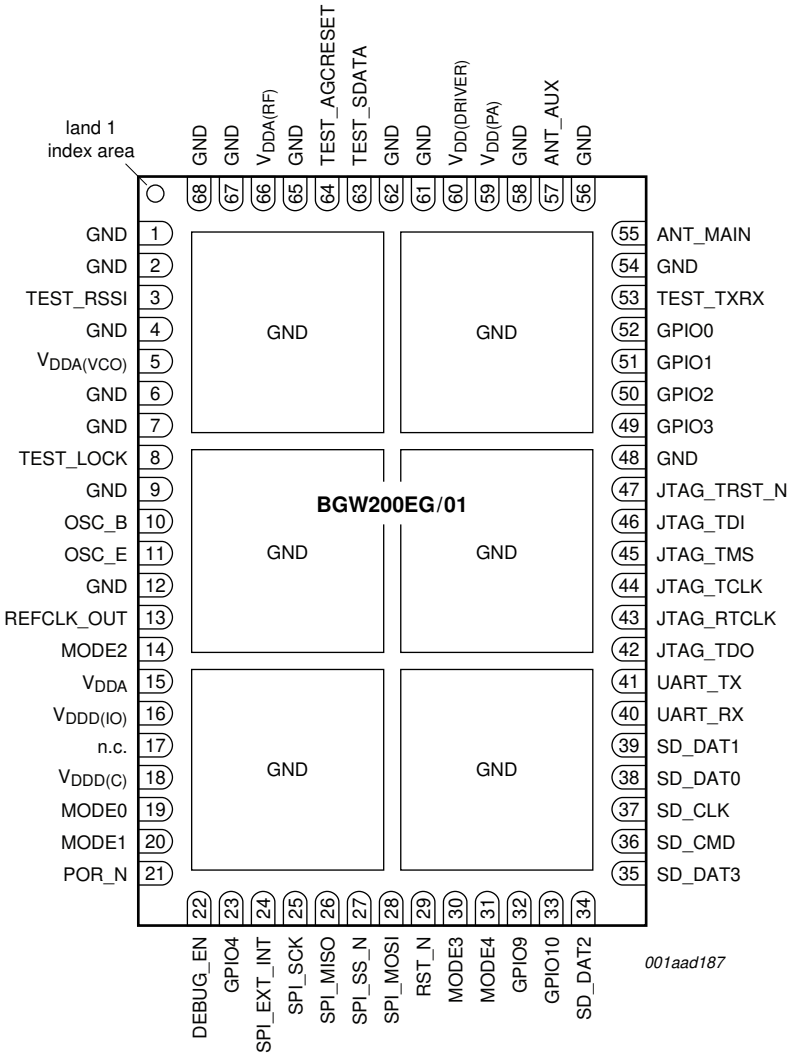



Fig 1. Block diagram

# 6. Pinning information

## 6.1 Pinning




Transparent top view

**Fig 2. Pin configuration**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Type | Circuit | Reset[1] | Supply | Description |
|---|---|---|---|---|---|---|
| **SPI interface** | | | | | | |
| SPI_SCK | 25 | I/O; I | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | SPI clock; bidirectional; 32 kHz sleep clock input |
| SPI_SS_N | 27 | I; I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | SPI slave select input; general-purpose I/O bit 6; bidirectional |
| SPI_EXT_INT | 24 | O; I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | SPI external interrupt output; general-purpose I/O bit 5; bidirectional |
| SPI_MISO | 26 | I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | SPI data (master in / slave out); bidirectional |
| SPI_MOSI | 28 | I/O | 3-state; 1 ns slew rate; 4 mA; CMOS | I, pull-down | $V_{DDD(IO)}$ | SPI data (master out / slave in); bidirectional |
| **SDIO Interface** | | | | | | |
| SD_CLK | 37 | I; I | CMOS; hysteresis | - | $V_{DDD(IO)}$ | SD clock input; 32 kHz clock input |
| SD_CMD | 36 | I/O | 3-state; 1 ns slew rate; 4 mA; CMOS | I | $V_{DDD(IO)}$ | SD command; bidirectional |
| SD_DAT0 | 38 | I/O | 3-state; 1 ns slew rate; 4 mA; CMOS | I | $V_{DDD(IO)}$ | SD data bit 0; bidirectional |
| SD_DAT1 | 39 | I/O | 3-state; 1 ns slew rate; 4 mA; CMOS | I | $V_{DDD(IO)}$ | SD data bit 1; bidirectional |
| SD_DAT2 | 34 | I/O | 3-state; 1 ns slew rate; 4 mA; CMOS | I | $V_{DDD(IO)}$ | SD data bit 2; bidirectional |
| SD_DAT3 | 35 | I/O | 3-state; 1 ns slew rate; 4 mA; CMOS | I, pull-up | $V_{DDD(IO)}$ | SD data bit 3; bidirectional |
| **UART interface** | | | | | | |
| UART_RX | 40 | I; I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | UART receive input; general-purpose I/O bit 7; bidirectional |
| UART_TX | 41 | O; I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | UART transmit output; general-purpose I/O bit 8; bidirectional |
| **Antenna RF ports** | | | | | | |
| ANT_MAIN | 55 | I/O | analog | - | - | RF main antenna port; 50 Ω |
| ANT_AUX | 57 | I | analog | - | - | RF auxiliary antenna port; 50 Ω |
| **Test pins** | | | | | | |
| TEST_RSSI | 3 | O | analog; $C_L$ = 100 pF | LOW | $V_{DDA(RF)}$ | test pin for RF RSSI signal output |
| TEST_LOCK | 8 | O | CMOS; 4.5 mA | LOW | $V_{DDA}$ | test pin for synthesizer lock indicator |
| TEST_TXRX | 53 | O | push-pull; 3 ns slew rate; 4 mA | LOW | $V_{DDD(IO)}$ | test pin for RF transmit/receive select signal |
| TEST_SDATA | 63 | I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ or $V_{DDA}$ | test pin for 3-wire bus data; bidirectional |

**Table 2. Pin description** *...continued*

| Symbol | Pin | Type | Circuit | Reset[1] | Supply | Description |
|---|---|---|---|---|---|---|
| TEST_AGCRESET | 64 | O | push-pull; 3 ns slew rate; 4 mA | LOW | $V_{DDD(IO)}$ | test pin for RF AGC reset; output |
| REFCLK_OUT | 13 | O | CMOS | - | $V_{DDA}$ | test pin for 44 MHz clock output |
| **Bluetooth coexistence interface** | | | | | | |
| GPIO0 | 52 | O; O; I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | WLAN arbitration signal output; HW MAC CCA output; general-purpose I/O bit 0; bidirectional |
| GPIO1 | 51 | I; I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | BT arbitration signal input; general-purpose I/O bit 1; bidirectional |
| GPIO2 | 50 | I; I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | BT high priority traffic indicator input; general-purpose I/O bit 2; bidirectional |
| GPIO3 | 49 | O; I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | WLAN receive indicator output; general-purpose I/O bit 3; bidirectional |
| **GPIO interface** | | | | | | |
| GPIO9 | 32 | I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | general-purpose I/O bit 9; bidirectional |
| GPIO10 | 33 | I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | general-purpose I/O bit 10; bidirectional |
| **JTAG and debug interface** | | | | | | |
| JTAG_TCLK | 44 | I | CMOS; hysteresis; pull-up | - | $V_{DDD(IO)}$ | JTAG clock input |
| JTAG_RTCLK | 43 | O | push-pull; 3 ns slew rate; 4 mA | LOW | $V_{DDD(IO)}$ | synchronized JTAG clock output |
| JTAG_TMS | 45 | I | CMOS; hysteresis; pull-up | - | $V_{DDD(IO)}$ | JTAG test mode select input |
| JTAG_TRST_N | 47 | I | CMOS; hysteresis; pull-up | - | $V_{DDD(IO)}$ | JTAG reset input; active LOW |
| JTAG_TDI | 46 | I | CMOS; hysteresis; pull-up | - | $V_{DDD(IO)}$ | JTAG test data input |
| JTAG_TDO | 42 | O | 3-state; 3 ns slew rate; 4 mA | high-Z | $V_{DDD(IO)}$ | JTAG test data output |
| DEBUG_EN | 22 | I | CMOS; hysteresis; pull-down | - | $V_{DDD(IO)}$ | debug enable input |
| **Miscellaneous** | | | | | | |
| OSC_B | 10 | I | analog | - | $V_{DDA}$ | crystal oscillator / buffer input |
| OSC_E | 11 | O | analog | - | $V_{DDA}$ | crystal oscillator output |
| GPIO4 | 23 | I; I/O | 3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis | I, pull-down | $V_{DDD(IO)}$ | 32 kHz sleep clock input; general-purpose I/O bit 4; bidirectional |
| RST_N[2] | 29 | I | CMOS; hysteresis | - | $V_{DDD(IO)}$ | system reset input; active LOW |
| POR_N | 21 | O | push-pull; 3 ns slew rate; 4 mA | LOW | $V_{DDD(IO)}$ | power-on reset output; active LOW |
| MODE0 | 19 | I | CMOS; hysteresis | - | $V_{DDD(IO)}$ | load source 0 input |
| MODE1 | 20 | I | CMOS; hysteresis | - | $V_{DDD(IO)}$ | load source 1 input |
| MODE2 | 14 | - | connected to ground | - | - | reserved for pin-compatibility with BGW211 |

**Table 2. Pin description** *...continued*

| Symbol | Pin | Type | Circuit | Reset[1] | Supply | Description |
|---|---|---|---|---|---|---|
| MODE3 | 30 | - | not connected | - | - | reserved for pin-compatibility with BGW211 |
| MODE4 | 31 | - | not connected | - | - | reserved for pin-compatibility with BGW211 |
| n.c. | 17 | - | not connected | - | - | reserved for pin-compatibility with BGW211 |
| **Power supplies** | | | | | | |
| $V_{DDA(VCO)}$ | 5 | - | - | - | - | VCO analog supply voltage |
| $V_{DDA}$ | 15 | - | - | - | - | analog supply voltage |
| $V_{DDD(IO)}$ | 16 | - | - | - | - | I/O digital supply voltage |
| $V_{DDD(C)}$ | 18 | - | - | - | - | core digital supply voltage |
| $V_{DD(PA)}$ | 59 | - | - | - | - | power amplifier supply voltage |
| $V_{DD(DRIVER)}$ | 60 | - | - | - | - | driver supply voltage |
| $V_{DDA(RF)}$ | 66 | - | - | - | - | RF analog supply voltage |
| GND | 1 | - | - | - | - | ground |
| GND | 2 | - | - | - | - | ground |
| GND | 4 | - | - | - | - | ground |
| GND | 6 | - | - | - | - | ground |
| GND | 7 | - | - | - | - | ground |
| GND | 9 | - | - | - | - | ground |
| GND | 12 | - | - | - | - | ground |
| GND | 48 | - | - | - | - | ground |
| GND | 54 | - | - | - | - | ground |
| GND | 56 | - | - | - | - | ground |
| GND | 58 | - | - | - | - | ground |
| GND | 61 | - | - | - | - | ground |
| GND | 62 | - | - | - | - | ground |
| GND | 65 | - | - | - | - | ground |
| GND | 67 | - | - | - | - | ground |
| GND | 68 | - | - | - | - | ground |

[1] I = input mode.

[2] The RST_N pin should be linked to the POR_N pin; use of an external reset signal is not supported.

# 7. Functional description

## 7.1 General

The BGW200EG contains the following parts in one SiP (with embedded software):

- IEEE 802.11b RF transceiver
- IEEE 802.11b compliant modem
- IEEE 802.11b MAC
- ARM7TDMI-S microcontroller
- Static RAM (SRAM)
- Interface circuits
- Power management circuit

Together with a reference clock and antenna with harmonic filter, this device forms a complete WLAN solution. The system architecture is ideal for mobile products and requires no load on the host processor. The host sleeps while the WLAN listens for the beacon and is woken by the WLAN when appropriate.

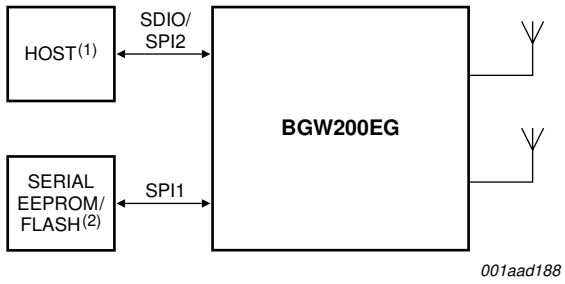
The BGW200EG is designed to be used for wireless links operating in the globally available ISM band, between 2402 MHz and 2497 MHz. The radio part is composed of a fully integrated, state-of-the-art, direct conversion transceiver chip, a linear power amplifier chip, an RX antenna filter for out-of-band blocking, TX/RX and antenna diversity switches, TX and RX baluns and a basic amount of supply decoupling. The SiP radio circuit is integrated on an organic substrate. The total WLAN system is integrated in a 10 mm $\times$ 15 mm HLLGA68 package and can be handled as a standard pick-and-place component. The device is a 'plug-and-play' SiP. Robust design requires no manufacturing trimming, resulting in a cost-optimized solution. The RF antenna ports have a normalized 50 $\Omega$ impedance and each can be connected directly to an external antenna with a 50 $\Omega$ transmission line.

The BGW200EG supports two host interfaces. The high-speed SPI slave (SPI2) interface is ideal for embedded applications since only 5 signal lines are required to connect to the host controller, and the protocol for this interface has a low processing overhead. The SDIO interface can operate in SPI, SD1 and SD4 modes, and can be used in an embedded application or in a secure digital NIC card. The ARM7TDMI-S RISC core, today considered as the standard RISC processor in the telecommunications industry, is integrated in the SA2443A. The processor is characterized by its extremely low mW/MIPS ratio. The BGW200EG has 1 Mbit of on-chip SRAM, thereby eliminating the need for external SRAM. This reduces the total footprint of the WLAN solution as well as the power consumption of the system. The functionality of the IEEE 802.11 MAC is split between hardware and software running on the ARM microcontroller. The IEEE 802.11b modem is implemented in hardware with control and configuration handled by software.

The BGW200EG is designed to be used as a low-cost, low-power wireless LAN link. Existing WLAN solutions, aimed at the computing market, have made use of the host processor to implement such functions as fragmentation and defragmentation. The BGW200EG implements all WLAN functions internally (implemented in either hardware or firmware) with the result that there is no processing load on the host controller. This link

will be the basis for smart phones and PDAs to communicate with a LAN network through a WLAN access point both for voice (VoIP) and data access. It is designed to handle the IEEE 802.11b specification.

The BGW200EG combines the IEEE 802.11b PHY and MAC with the embedded HCI firmware for selected host operating systems through either the SPI or SDIO interfaces. A typical example of the BGW200EG in its environment is illustrated in Figure 3. Together with an antenna, reference clock and filtering as required by the application, this device forms a complete WLAN solution. The system architecture is ideal for mobile products and requires no load on the host processor. The host sleeps while the WLAN listens for the beacon and is woken by the WLAN when appropriate.




(1) Host is typically a mobile device such as a cell phone or PDA.

(2) Serial EEPROM/flash is optional.

**Fig 3. Typical application of the BGW200EG**

## 7.2 Subblock overview

Table 3 gives an overview of some subblocks shown in Figure 1 and provides a reference to the section of the data sheet that describes these blocks.

**Table 3. Subblock overview**

| Block name | Description | Reference |
|---|---|---|
| **SA2405 RF transceiver** | | |
| FIRDAC | finite impulse response digital-to-analog converter | Section 8 |
| AGC state machine | automatic gain control state machine | |
| RSSI | receive signal strength indicator | |
| **SA2411 RF power amplifier** | | |
| PA | power amplifier | Section 9 |
| **SA2443A Baseband/MAC** | | |
| SCU | system configuration unit | Section 10.1 |
| Processor: | | |
| ARM7TDMI-S | fast RISC processor controlling other blocks via AHB and VPB buses | Section 10.2 |
| IPU | instruction pre-fetch unit | |
| JTAG | joint test action group interface for ARM7 emulation | |
| SRAM | system RAM for use by firmware | |
| ROM | read only program memory | |

**Table 3. Subblock overview** *…continued*

| Block name | Description | Reference |
|---|---|---|
| MAC: | | |
| HW MAC | hardware medium access control layer | Section 10.3 |
| PHYTX | physical layer transmitter | Section 10.7 |
| PHYRX | physical layer receiver | Section 10.8 |
| WEP | WEP encryption and decryption engine | Section 10.4 |
| AES (CCM) | CCM encryption and decryption engine | Section 10.5 |
| DMA | general-purpose DMA engine | Section 10.6 |
| RFIF | RF interface | Section 10.9 |
| TIMERS | system timers | Section 10.10 |
| ICU | interrupt control unit | Section 10.11 |
| UART | universal asynchronous receiver/transmitter interface | Section 10.12 |
| SPI: | | |
| SPI1 | master/slave serial peripheral interface | Section 10.13 |
| SPI2 | high-speed slave serial peripheral interface | Section 10.14 |
| SDIO | secure digital input/output interface | Section 10.15 |
| GPIO | general-purpose input/output pin(s) | Section 10.16 |

# 8. SA2405 RF transceiver

The SA2405 RF transceiver is targeted for operation in the 2.45 GHz band, specifically for IEEE 802.11b 1 Mbit/s and 2 Mbit/s DSSS, and 5.5 Mbit/s and 11 Mbit/s CCK high rate standards.

The RF VCO is common to both the transmitter and the receiver. The RF VCO is a differential 4.8 GHz Local Oscillator (LO) with the frequency determining components internal to the IC. The VCO is connected internally to a frequency divider and a quadrature generator circuit which produces the local oscillator frequencies for the I and Q up mixers and down mixers. The divider output is also internally connected to the synthesizer which can be programmed in order to produce the desired LO frequency. The frequency step size of the synthesizer is 0.5 MHz.

The RF LNA has two stepped gains controlled internally by the on-chip AGC control loop. The RF signal is downconverted to baseband by the quadrature mixers. The I and Q low-pass filters are fully integrated active Type I Chebychev filters. The I/Q pass band extends from DC to a −3 dB corner at 7 MHz. Three stepped gains are incorporated in the channel filters. Additional adjustable gain is provided in baseband amplifiers to achieve a totally adjustable gain range of 90 dB. The RX output to the baseband are differential I and Q signals.

The RX chain also integrates a high-pass filter (DC notch) for cancellation of the DC offset inherent to zero-IF architecture. The high-pass filter has a programmable lower 3 dB cut-off frequency of 10 MHz, 1 MHz, 100 kHz or 10 kHz. The DC offset cancellation occurs simultaneously with the on-chip AGC loop settling process. During the AGC settling phase, the high-pass cut-off frequency is dynamically selected between 10 MHz and 1 MHz to quickly reduce DC offset values from +50 dBc to below −20 dBc relative to a −76 dBm input signal at the antenna.

After the AGC settling (may be more than one AGC cycle with antenna diversity), the high-pass is configured to 100 kHz for 5 μs before switching to a final 10 kHz cut-off frequency. The low value of 10 kHz is required for minimizing the signal distortion created by a high-pass function at zero frequency. The high-pass will then remain set to the 10 kHz cut-off frequency until a new AGC cycle for the next receive data burst is started. Whenever there is a frequency change in the high-pass filter lower cut-off, the DC offset can change from a very low value to approximately 50 % (1 MHz ≥ 100 kHz step) or 10 % (100 kHz ≥ 10 kHz step) of the signal level. This DC offset then decays according to the high-pass response of the filter.

The receiver contains a fully integrated automatic gain control loop. It works by adjusting the internal gain such that the RX output amplitude meets a predefined target value. A measured RSSI is used to realize the gain adjustment. By default, the AGC is always set to a default maximum gain (adjustable by register value GMAX) whenever the BGW200EG enters the receive mode of operation from another operational mode. The receiver takes 5 μs to settle after entering the receive mode, which includes the time for DC offsets to be removed with a 1 MHz lower cut-off frequency of the high-pass filtering. This lower cut-off frequency of 1 MHz remains unchanged as long as the AGC remains in the default maximum gain state. By successively reducing the gain from its initial maximum value, the AGC loop searches for the correct gain value to provide a nominal RX output amplitude to the baseband. This is achieved after a maximum of 8 μs with the default wait periods. This settling time is determined by wait periods necessary to settle the receiver after gain switching actions. The individual wait periods can be adjusted by means of register settings.

The Receive Signal Strength Indicator (RSSI) is implemented as an error signal derived from comparing the signal level at the RX output to a nominal value. The RSSI acts on the modulated RF signal envelope that is extracted from the baseband I and Q signals, and reflects on a logarithmic scale the amplitude of the instantaneous modulated RF signal envelope. The RSSI signal is filtered by a 3rd-order Bessel low-pass filter with 0.5 MHz cut-off frequency. The RSSI signal will include DC offsets and will, therefore, show transient decaying errors when the DC cancellation corner frequency is changed.

The receiver is designed to exceed the 802.11 specifications for the blocking and intermodulation. It can accept continuous or randomly pulsed interference single signals or multitone signals that are more than 35 dB stronger than the required signal and up to −10 dBm of interference level. The spurious I and Q outputs are maintained to less than −20 dBc of the required signal level.

The transmitter input binary data streams are sampled with a 44 MHz reference clock and integrated FIRDACs provide additional pulse shaping filtering. The wideband I/Q up converter includes reconstruction filters (4th order low-pass Butterworth with 9.75 MHz 3 dB upper cut-off frequency). At 18 dBm maximum transmitter output level, the out-of-band (FCC forbidden band) spurious signal power is less than −77 dBc (integrated over 1 MHz with a 100 kHz resolution bandwidth) for the 11 Msymbol/s CCK modulation.

By using the on-chip calibration loop the transmitter carrier leakage can be reduced to levels far less than required by the standard. An RF power meter detects the LO level, converts it into a digital signal and a state machine determines the compensation values which are fed through an on-chip DAC directly to the I/Q inputs. The I/Q gain and phase imbalance, the InterSymbol Interference (ISI) of the reconstruction filter and in-channel noise produce a typical modulation EVM of less than 8 % (RMS) for 11 Msymbol/s CCK modulation.

Upon entering the TX mode, the ramping-up of the RF TX signal is delayed by an internal power ramping circuit. The ramping-up time is fixed while the delay prior to ramping-up can be programmed by register settings. There is 15 dB of gain control with 1 dB resolution. A gain adjustment range of 0 dB to 7 dB in 1 dB steps is provided in the TX reconstruction filter. An additional 8 dB of gain control is provided in the upconverters via a single 8 dB gain step.

# 9. SA2411 RF power amplifier

The power stage of the transmit amplifier is a fixed gain, class AB amplifier designed to give typically 18 dBm output power at the antenna pin for an 11 Msymbol/s CCK modulation. The device has differential inputs and an integrated balun and harmonic filter at the output. The integrated power detector detects the power level and transforms it into a low-frequency voltage input for the baseband.

# 10. SA2443A IEEE 802.11b medium access controller and modem

## 10.1 System configuration unit

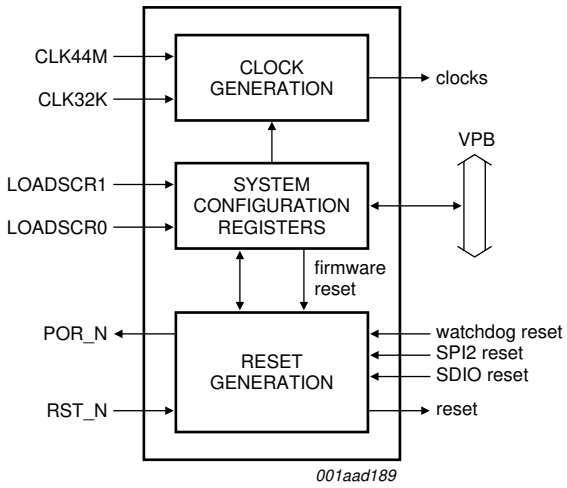



**Fig 4. Block diagram of the system configuration unit**

The 44 MHz reference clock for the SA2443A is supplied by the SA2405.

Power consumption is substantially reduced in doze mode using a low-frequency sleep clock. The sleep clock can be derived from an internal 1 MHz oscillator, located in the clock generation block, or supplied externally (typically 32 kHz).

The clock generation block generates all clocks required by the SA2443A from the 44 MHz, 1 MHz and 32 kHz clocks. The microcontroller and bus clock frequency can be configured between 32 kHz and 66 MHz to allow power consumption to be optimized.

The SA2443A has five reset sources:

- External reset (pin RST_N)
- Watchdog timer reset
- Firmware reset
- SPI2 reset
- SDIO reset

A power-on reset signal is generated when the core supply voltage is applied. The reset signal remains active for 4 ms after the 1.8 V supply is stable. The signal is available on pin POR_N. The RST_N pin should be linked to the POR_N pin; use of an external reset signal is not supported.

The MODE0 and MODE1 pins are used to control the boot mode of the SA2443A as shown in Table 4.

**Table 4. SA2443A boot modes**

| MODE0 | MODE1 | Boot mode | Description | Boot clock |
|---|---|---|---|---|
| L | L | SPI embedded | firmware download from the host via SPI2 | 44 MHz |
| H | L | SPI flash | firmware read from a serial flash via SPI1 | |
| L | H | SDIO embedded | firmware download from the host via SDIO | |
| H | H | reserved | - | - |

The SPI embedded boot mode is used when the WLAN solution is embedded in an application, such as a cellular phone or PDA. In this case, the SA2443A firmware will be downloaded from the host processor via the high-speed SPI slave interface (SPI2).

The SPI flash mode is used primarily for firmware development and debugging. In this mode, firmware is read from a serial flash memory connected to the master/slave SPI interface (SPI1).

The SDIO embedded mode operates in the same way as the SPI embedded mode, except that code is downloaded from the SDIO interface.

## 10.2 Microcontroller subsystem

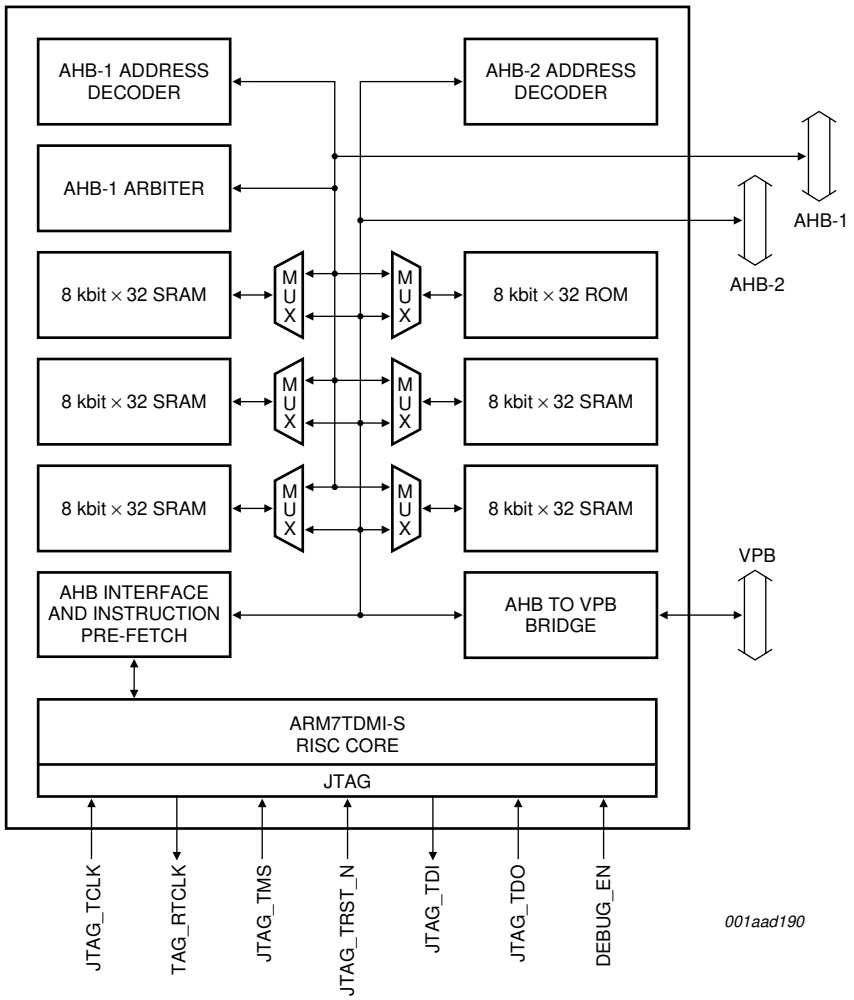



**Fig 5. Block diagram of the microcontroller subsystem**

The microcontroller subsystem is based around an ARM7TDMI-S RISC controller and has the following features:

- Embedded nonvolatile memory: 256-kbit ROM
- Embedded volatile memory: 5 × 256-kbit SRAM
- Instruction pre-fetch unit for enhanced microcontroller performance
- Two high-performance AHB buses for optimized throughput:
  - AHB1 is a multimaster bus used for DMA transfers
  - AHB2 is a single-master bus used by the microcontroller
- VPB bus for lower-speed peripherals
- JTAG-compliant interface for ARM7 in-circuit emulation (enabled by pulling the DEBUG_EN pin HIGH)

## 10.3 Hardware medium access control layer

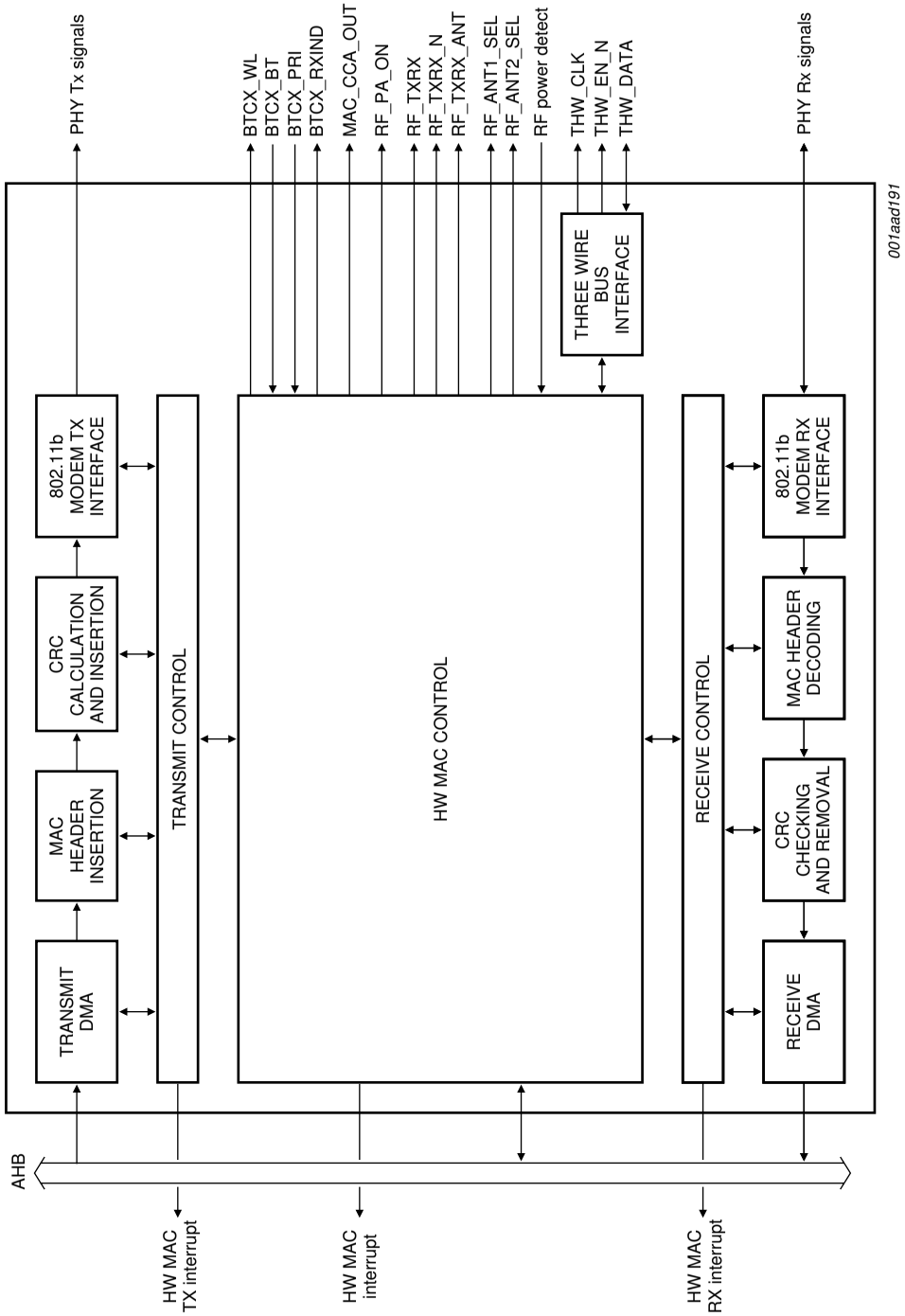



Fig 6. HW MAC block diagram

The IEEE 802.11b compliant HW MAC supports the following features:

- Data rates up to 11 Mbit/s
- SIFS timer
- Cyclic Redundancy Check (CRC) calculation and checking
- Back-off mechanism support
- Automated transmit timing control
- Automated TBTT/TXOP boundary checking
- Automated NAV timer update
- Automated IBSS mode beacon handling
- Automated TSF update from the beacon packet
- Automated insertion of TSF into the beacon packet
- Automatic wake-up for beacon reception
- Automated header field insertion (e.g. transmit address)
- QoS support:
  - 4 EDCF channels
  - 2 streams for HCF
- ATIM handler
- SW programmable automated response mechanism (e.g. ACK, RTS, CTS and QoS Null)
- Programmable unicast, multicast and beacon filtering
- Receive and transmit DMA engines for efficient data transfer
- Configurable TX/RX status interrupts
- Bluetooth coexistence Packet Traffic Arbitration (PTA) support
- Configurable antenna TX/RX and diversity switch control signals

The HW MAC block has the following external interfaces:

- SA2405 2.45 GHz transceiver control interface
- Antenna, TX/RX and diversity switch control signals
- Bluetooth coexistence interface

The HW MAC block has interfaces to the following subblocks:

- Physical layer transmitter (PHYTX); see Section 10.7
- Physical layer receiver (PHYRX); see Section 10.8
- RF interface (RFIF); see Section 10.9

## 10.4 WEP encryption and decryption coprocessor

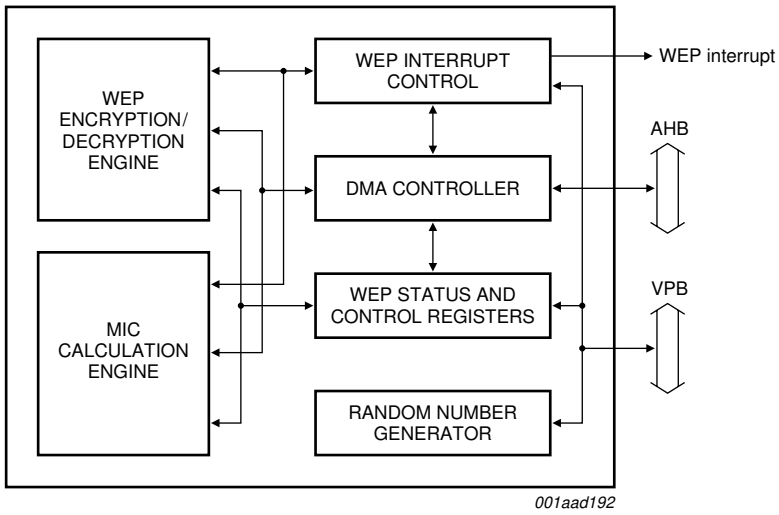



**Fig 7. Block diagram of the WEP encryption and decryption coprocessor**

The WEP encryption and decryption coprocessor has the following features:

- WEP 64-bit and 128-bit encryption and decryption
- WEP2 support in conjunction with firmware running on the microcontroller
- MIC calculation to facilitate TKIP support in conjunction with firmware running on the microcontroller
- DMA controller for high data throughput with minimum processing load on the microcontroller
- Random number generator to assist in the generation of encryption keys

## 10.5 CCM encryption and decryption coprocessor

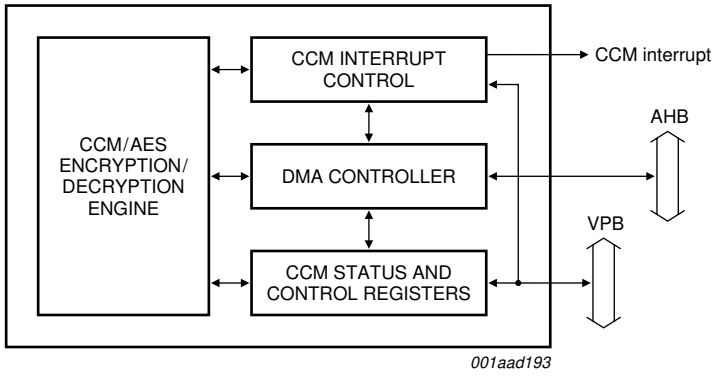



**Fig 8. Block diagram of the CCM encryption and decryption coprocessor**

The CCM encryption and decryption coprocessor supports both the CCM (counter mode with CBC-MAC) and the AES security algorithms. A DMA engine is incorporated to allow high data throughput with minimum loading on the microcontroller.

## 10.6 General-purpose DMA engine

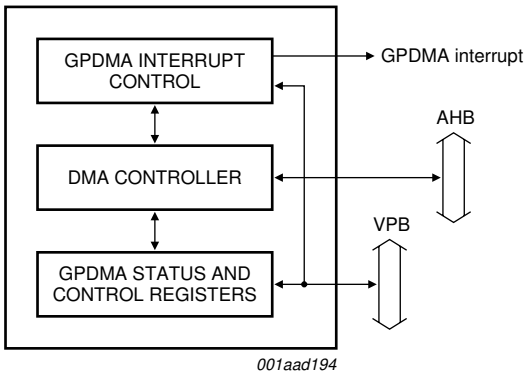



**Fig 9. Block diagram of the general-purpose DMA engine**

The general-purpose DMA engine can be used to move data from one memory location to another with minimum firmware involvement. Uses of the block include fragmentation and defragmentation assistance.

## 10.7 Physical layer transmitter

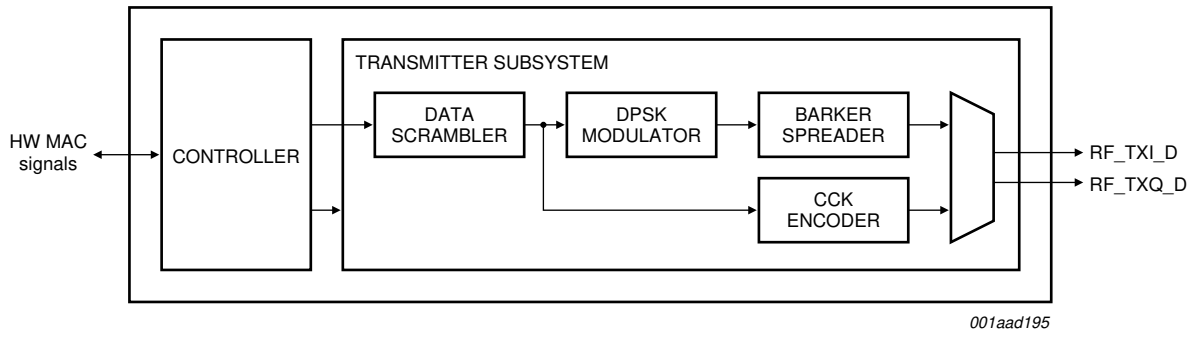



**Fig 10. Block diagram of the physical layer transmitter**

The PHYTX block is IEEE 802.11b compliant and supports the following features:

- 1 Mbit/s, 2 Mbit/s, 5.5 Mbit/s and 11 Mbit/s data rates
- Short and long preambles

The PHYTX block is tightly coupled to the SA2443A HW MAC block; see Section 10.3. Control and configuration of the PHYTX block are performed by the HW MAC block and firmware.

The PHYTX block comprises the controller and the transmitter subsystem.

The controller is responsible for interfacing with the HW MAC unit, generation of the PLCP header and control of the transmitter subsystem. The controller passes a serial bit stream into the transmitter subsystem. The transmitter subsystem generates modulated I and Q signals compatible with the serial digital transmit interface on the SA2405 transceiver.

The test modes available with the PHYTX block and their uses are given in Table 5.

**Table 5. PHYTX test modes**

| Test mode | Description | Measurement uses |
|---|---|---|
| RANDOM | continuous modulated random data | EVM, spectral mask |
| 0101 | continuous 0101 sequence | carrier suppression |
| CW | unmodulated I/Q data | transmit frequency offset |

## 10.8 Physical layer receiver

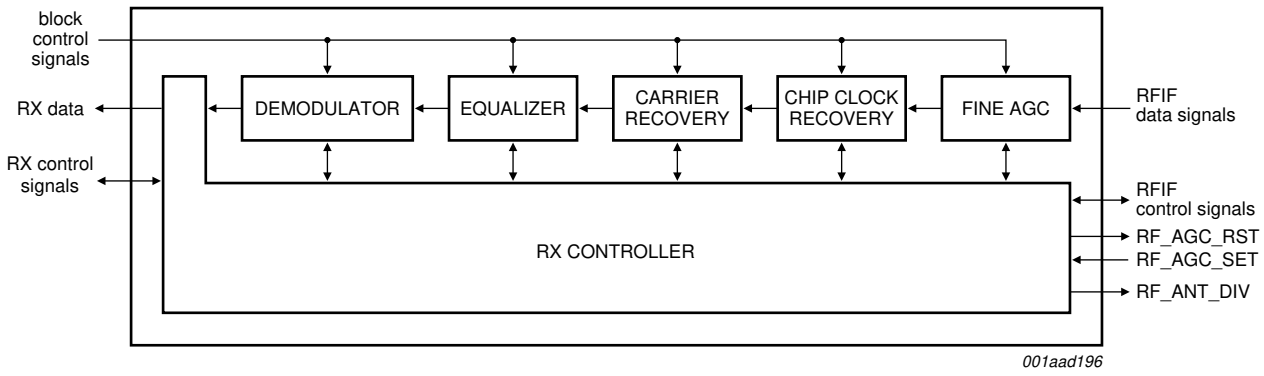



**Fig 11. Block diagram of the physical layer receiver**

The PHYRX block is IEEE 802.11b compliant and supports the following features:

- 1 Mbit/s, 2 Mbit/s, 5.5 Mbit/s and 11 Mbit/s data rates
- Short and long preambles
- Decision feedback equalizer with > 200 ns RMS multipath delay spread tolerance
- Antenna diversity

The PHYRX block is tightly coupled to the SA2443A HW MAC block; see Section 10.3. Control and configuration of the PHYRX block is performed by the HW MAC block and firmware. The PHYRX also interfaces to the RF interface block; see Section 10.9.

The RX controller contains the state machine that switches the modes of the RX blocks and performs the following functions:

- Clear Channel Assessment (CCA)
- Bit synchronization
- Antenna diversity

The fine AGC block adjusts the received signal level for optimum receiver performance. Sampling clock correction and carrier frequency correction are handled by the chip clock recovery and carrier recovery blocks respectively. Correction for multipath distortion is performed by a fractionally spaced decision feedback equalizer.

The operation performed by the demodulator is dependent on the data rate. For 1 Mbit/s or 2 Mbit/s rates the demodulator will differentially decode the output of a Barker de-spreader. For 5.5 Mbit/s or 11 Mbit/s data rates a CCK decoder is used to translate the output of the equalizer into data bits. In both cases, a descrambler removes the pseudorandom sequence from the data.

## 10.9 RF interface

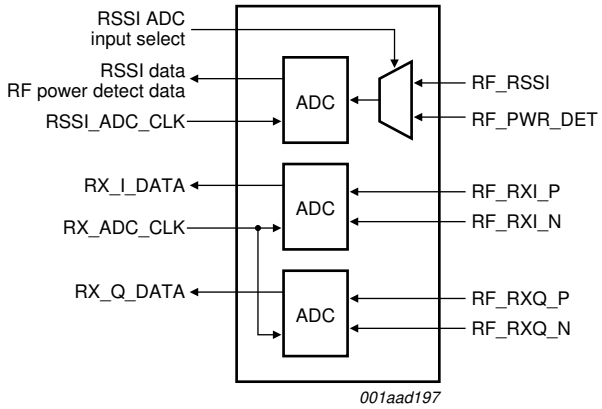



**Fig 12. Block diagram of the RF interface**

The RF interface has the following features:

- RSSI and power detect input:
  - 8-bit ADC
  - Multiplexed ADC input
- Analog receive inputs:
  - Differential inputs
  - 8-bit ADC

Digitized received I/Q signals are routed, together with RSSI values, to the physical layer receiver; see Section 10.8. Power detector samples are routed to the HW MAC; see Section 10.3.

## 10.10 System timers

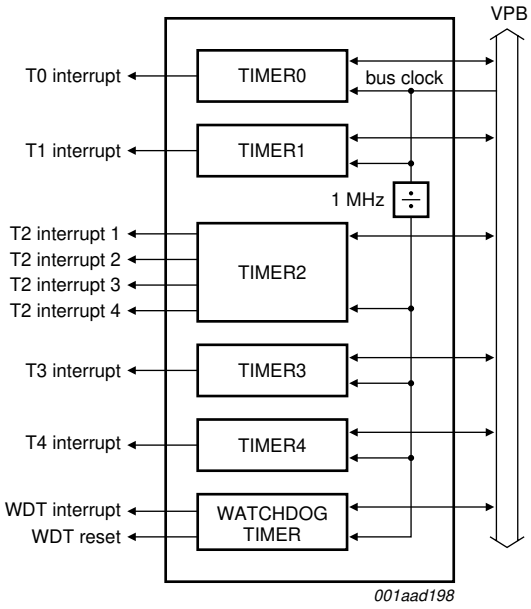



**Fig 13. Block diagram of system timers**

The SA2443A contains five general-purpose timers and a WatchDog Timer (WDT). Table 6 provides an overview of the timer functionality.

**Table 6. Timer overview**

| Timer name | Type | Count frequency | Interrupt conditions |
|---|---|---|---|
| TIMER0 | down count | bus clock | on zero |
| TIMER1 | down count | bus clock | on zero |
| TIMER2 | up count | 1 MHz | when count matches any of four programmed values |
| TIMER3 | down count | 1 MHz | on zero |
| TIMER4 | down count | 1 MHz | on zero |
| WDT | down count | 1 MHz | interrupt when count matches programmed value; reset generated when count reaches zero |

Timers 0, 1, 3 and 4 can be programmed with a start value. Operation can be either single shot or continuous. An interrupt is generated when a timer counts down to zero.

Timer 2 is programmed with up to four interrupt compare values. An interrupt is generated when the counter value matches one of the interrupt compare values. Operation can be either one shot or continuous.

The watchdog timer provides a mechanism to reset the SA2443A if for some reason the firmware becomes locked. A start value is programmed from which the counter counts down to zero. For correct operation of the SA2443A the firmware must reset the start value before the counter reaches zero. If the counter reaches zero the SA2443A is reset. An interrupt compare value can be programmed, allowing a warning to be generated prior to the full reset.

## 10.11 Interrupt control unit

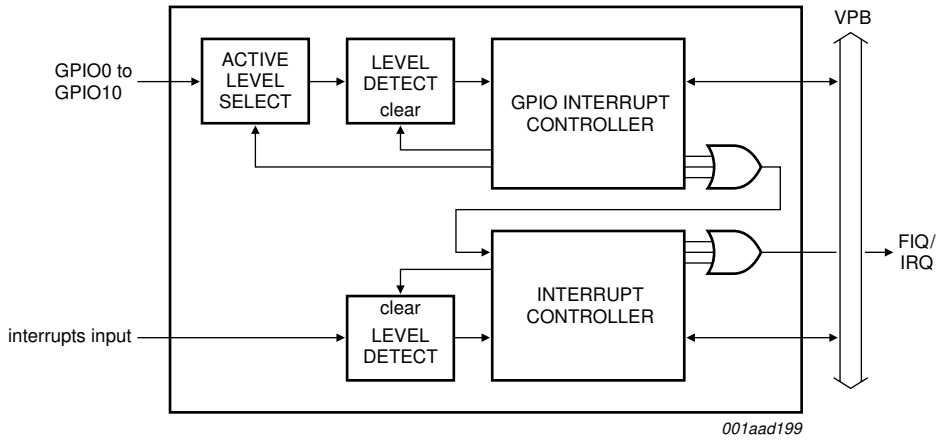



**Fig 14. Block diagram of the IRQ/FIQ interrupt controller**

Two primary interrupt controllers are implemented:

- Fast Interrupt reQuest (FIQ) interrupt controller
- Interrupt ReQuest (IRQ) interrupt controller

For each of the primary interrupt controllers there is a secondary GPIO interrupt controller.

The FIQ interrupt controller provides fast, low-latency interrupt handling, whereas the IRQ interrupt controller is used for general interrupts.

For each interrupt controller it is possible to enable or disable individual interrupts, read the status of the interrupts and observe the interrupt input status.

The FIQ and IRQ interrupt controllers also provide a vector register that contains an instruction address that the firmware interrupt handler can jump to. A different address will be reported for each interrupt. In the case of simultaneous interrupts, the vector address will be for the highest priority interrupt. Interrupt 0 is the highest priority and interrupt 31 is the lowest priority.

All interrupts are level sensitive and for GPIO interrupts the active level can be configured by firmware.

## 10.12 Universal asynchronous receiver transmitter

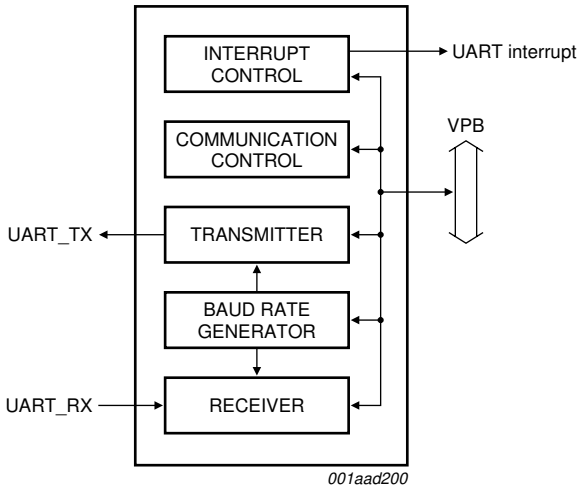



**Fig 15. Block diagram of the UART interface**

The Universal Asynchronous Receiver Transmitter (UART) supports the following features:

- Parity generation and detection: even, odd, fixed logic 1 or logic 0 or no parity
- Stop bit generation: 1, 1.5 (5-bit character size only) or 2 stop bits
- Character sizes: 5-bit, 6-bit, 7-bit or 8-bit
- Programmable standard baud rates up to 4.125 Mbit/s
- Automatic line error checking: stop bit failure (framing), RX overrun, parity error
- Compatible with the industry standard 16450 UART

The UART provides an asynchronous interface that includes interrupt handling and a baud rate generator allowing 16 times oversampling. The interface supports character formats from 5-bit to 8-bit length with an optional parity bit and 1, 1.5 or 2 stop bits. All standard bit rates are supported.

## 10.13 Master/slave serial peripheral interface

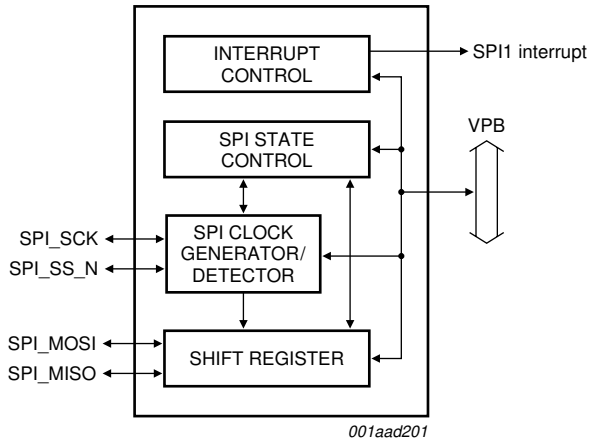



**Fig 16. Block diagram of the master/slave SPI interface (SPI1)**

The master/slave SPI interface (SPI1) has the following features:

- Master or slave mode operation
- SPI mode 0 and mode 3 supported in both master and slave modes
- Programmable clock frequency up to 8.25 MHz
- Automatic error checking: write collision, read overrun, mode fault and slave abort

The SPI1 interface block can be configured to work with most SPI master or slave devices. Clock frequency, polarity (bit CPOL) and phase (bit CPHA) are configurable by firmware, as is the data bit order (LSB first or MSB first).

The primary use of the interface is as an SPI master connected to a serial EEPROM or flash memory. In this case, one of the GPIO pins (see Section 10.16) must be controlled by firmware to generate the EEPROM slave select signal. When used in master mode pin SPI_SS_N must be held HIGH to prevent a mode fault occurring.

The SPI clock is oversampled by a factor of 8. The maximum SPI1 clock frequency is therefore limited to 1/8 of the bus clock.

The I/O pins for this interface are multiplexed with the I/O pins for the SPI2 block; see Section 10.14.