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BLA0912-250

Avionics LDMOS transistor

Rev. 4 — 1 September

AMPLEON

Product data sheet

1. Product profile

1.1 General description

Silicon N-channel enhancement mode LDMOS transistor encapsulated in a 2-lead SOT502A flange package with a ceramic cap. The common source is connected to the mounting flange.

Table 1. Test information

Typical RF performance measured in common source class-AB test circuit at P_L = 250 W and 960 MHz to 1215 MHz frequency band. T_h = 25 °C; $Z_{th(j-h)}$ = 0.15 K/W; unless otherwise specified.

Mode of operation	f (MHz)	t_p (µs)	δ %	V_{DS} (V)	P_L (W)	G_p (dB)	ΔG_p (dB)	η_D (%)	$P_{droop(pulse)}$ (dB)	t_r (ns)	t_f (ns)	$Z_{th(j-h)}$ (K/W)	$\varphi_{ins(rel)}$ (deg)
all modes	960 to 1215	100	10	36	250	13.5	0.8	50	0.1	25	6	0.18	±5
TCAS	1030 to 1090	32	0.1	36	250	14.0	0.8	50	0	25	6	0.07	±5
Mode-S	1030 to 1090	128	2	36	250	13.5	0.8	50	0.1	25	6	0.15	±5
	1030 to 1090	340	1	36	250	13.5	0.8	50	0.2	25	6	0.20	±5
JTIDS	960 to 1215	3300	22	36	200	13.0	1.2	45	0.2	25	6	0.45	±5

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

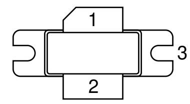
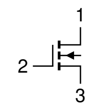
- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

1.3 Applications

- Avionics transmitter applications in the 960 MHz to 1215 MHz frequency range such as Mode-S, TCAS and JTIDS, DME or TACAN.

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
1	drain			
2	gate			
3	source	[1]		sym039

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA0912-250	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	75	V
V_{GS}	gate-source voltage		-	±22	V
P_{tot}	total power dissipation	$T_h \leq 25$ °C; $t_p = 50$ μs; $\delta = 2$ %	-	700	W
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$Z_{th(j-h)}$	transient thermal impedance from junction to heatsink	$T_h = 25$ °C	[1]	0.18	K/W

[1] Thermal resistance is determined under RF operating conditions; $t_p = 100$ μs, $\delta = 10$ %.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3 mA	75	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	4	-	5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 36 V	-	-	1	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	45	-	-	A
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V	-	-	1	μA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10 A	-	9	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = 9 V; I_D = 10 A	-	60	-	mΩ

Table 7. RF characteristics

RF performance in common source class-AB circuit; T_h = 25 °C; Z_{th} = 0.15 K/W; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage		-	-	36	V
f	frequency		960	-	1215	MHz
P_L	output power	t_p = 100 μs; δ = 10 %	250	-		W
G_p	power gain	P_L = 250 W	12	13		dB
η_D	drain efficiency	t_p = 100 μs; δ = 10 %	40	50		%
$Z_{th(j-h)}$	transient thermal impedance from junction to heatsink	t_p = 100 μs; δ = 10 %	-	-	0.2	K/W
T_h	heatsink temperature		–55	-	+70	°C
$P_{droop(pulse)}$	pulse droop power	t_p = 100 μs; δ = 10 %	-	0.1	0.5	dB
$\alpha_{resp(sp)}$	spurious response	$VSWR_{load}$ = 2 : 1	-	-	–60	dBc
t_r	rise time		-	25	50	ns
t_f	fall time		-	6	25	ns

6.1 Ruggedness in class-AB operation

The BLA0912-250 is capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: V_{DS} = 36 V; f = 960 MHz to 1215 MHz at rated load power.

7. Application information

7.1 Impedance information

Table 8. Typical impedance

Typical values per section unless otherwise specified.

f MHz	Z_S Ω	Z_L Ω
960	0.89 – j1.70	1.53 – j1.13
1030	1.37 – j1.23	1.47 – j0.99
1090	2.09 – j1.27	1.38 – j0.85
1140	2.40 – j1.97	1.30 – j0.71
1215	1.51 – j2.61	1.17 – j0.47

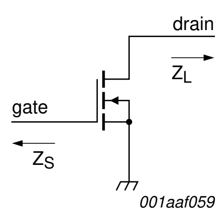
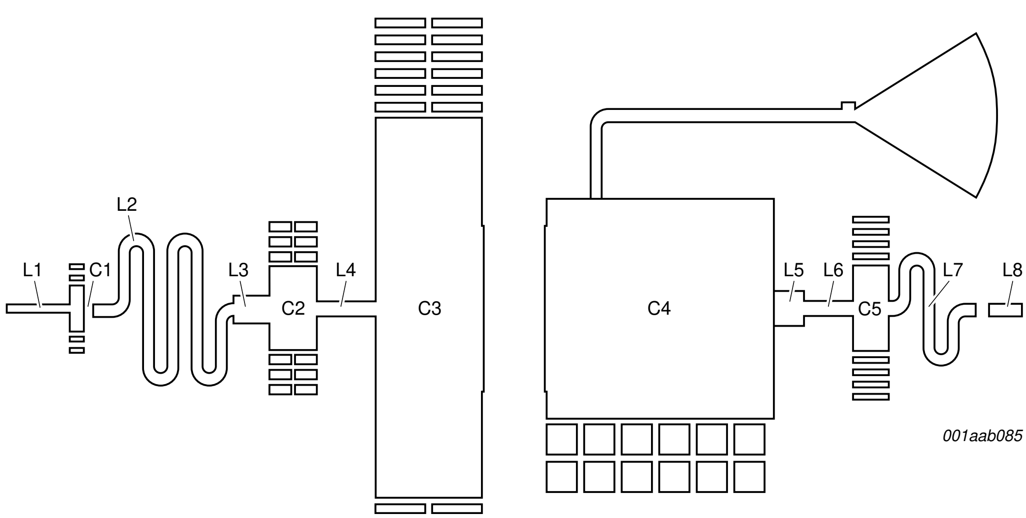


Fig 1. Definition of transistor impedance

7.2 Application circuit



See Table 9 for details of striplines.

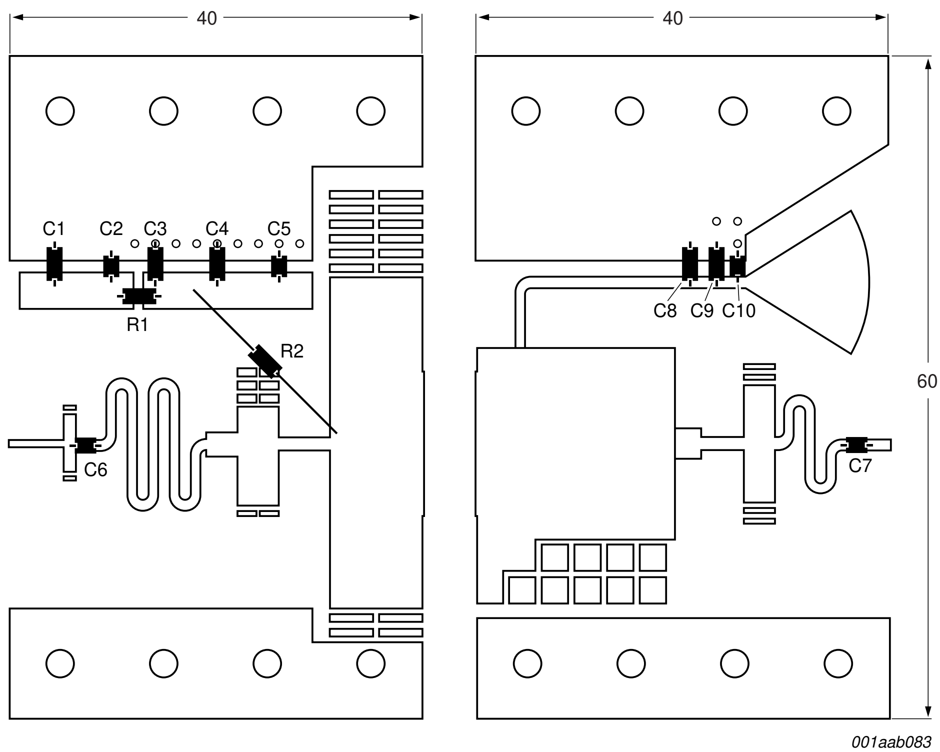
Fig 2. Layout of class-AB application circuit

Table 9. Layout details

See Figure 2.

Striplines are on a Rodgers Duroid 6010 Printed-Circuit Board (PCB); ε_r = 10.2 F/m; thickness = 0.64 mm

Component	Description	Dimensions
Input circuit		
L1	stripline	5 mm × 0.8 mm
C1	stripline	1.2 mm × 3.5 mm
L2	stripline	capacitor pad: 1 mm × 1 mm (1×)
		curve: width 0.8 mm; angle 90°; radius 0.8 mm (10×)
		vertical: 3.9 mm × 0.8 mm (2×)
		vertical: 9.4 mm × 0.8 mm (3×)
		horizontal: 0.5 mm × 0.8 mm (4×)
L3	stripline	3 mm × 2 mm
C2	stripline	4 mm × 6.5 mm
L4	stripline	5 mm × 1 mm
C3	stripline	8.8 mm × 30 mm + 0.2 mm × 13 mm
Output circuit		
C4	stripline	0.2 mm × 13 mm + 19 mm × 17.1 mm
L5	stripline	2.5 mm × 2.3 mm
L6	stripline	4 mm × 1 mm
C5	stripline	3 mm × 6.6 mm
L7	stripline	curve: width 0.8 mm; angle 90°; radius 0.8 mm (6×)
		vertical: 2.2 mm × 0.8 mm (2×)
		vertical: 6 mm × 0.8 mm (1×)
		horizontal: 1 mm × 0.8 mm (2×)
L8	stripline	2.5 mm × 0.8 mm
1/4 λ line	stripline	curve: width 1 mm; angle 90°; radius 0.8 mm
		vertical: 5 mm × 1 mm
		horizontal: 19 mm × 1 mm



Dimensions in mm.

See Table 10 for list of components.

Fig 3. Component layout for class-AB application circuit

Table 10. List of components

See Figure 3.

Component	Description	Value		Remarks
C1, C3, C9	multilayer ceramic chip capacitor	1 nF	[1]	
C2, C6, C10	multilayer ceramic chip capacitor	22 pF	[2]	
C4	tantalum SMD capacitor	47 μF; 20 V		KEMET: T491D476M020AS
C5	multilayer ceramic chip capacitor	56 pF	[2]	
C7	multilayer ceramic chip capacitor	47 pF	[2]	
C8	tantalum SMD capacitor	22 μF; 63 V		
R1	SMD resistor	51 Ω		0805
R2	resistor	49.9 Ω		

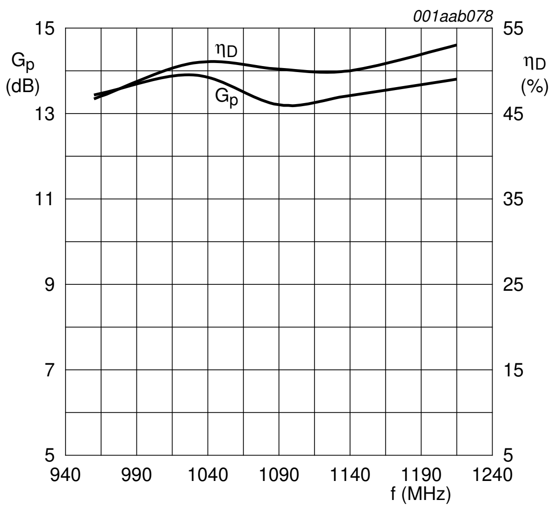
[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.

8. Test information

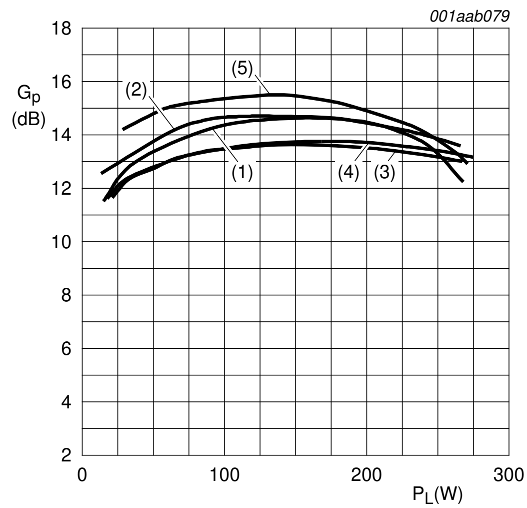
8.1 RF performance

Typical RF performance measured in common source class-AB test circuit at P_L = 250 W and 960 MHz to 1215 MHz frequency band. T_h = 25 °C; $Z_{th(j-h)}$ = 0.15 K/W; unless otherwise specified.



T_h = 25 °C; V_{DS} = 36 V; I_{Dq} = 150 mA; class-AB;
t_p = 100 µs; δ = 10 %.

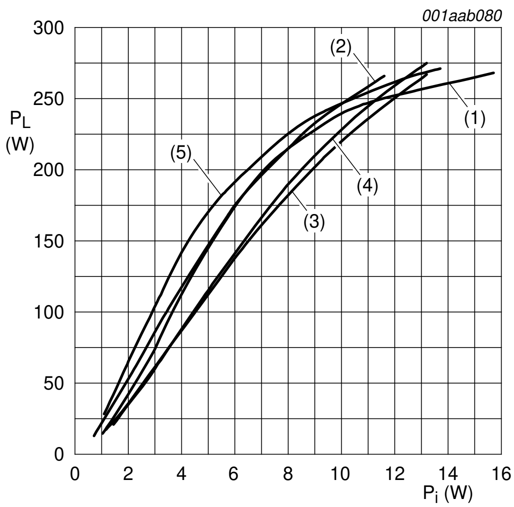
Fig 4. Power gain and drain efficiency as function of frequency; typical values



T_h = 25 °C; V_{DS} = 36 V; I_{Dq} = 150 mA; class-AB;
t_p = 100 µs; δ = 10 %.

(1) f = 960 MHz
(2) f = 1030 MHz
(3) f = 1090 MHz
(4) f = 1140 MHz
(5) f = 1215 MHz

Fig 5. Power gain as a function of load power; typical values



T_h = 25 °C; V_{DS} = 36 V; I_{Dq} = 150 mA; class-AB;
t_p = 100 μs; δ = 10 %.

(1) f = 960 MHz

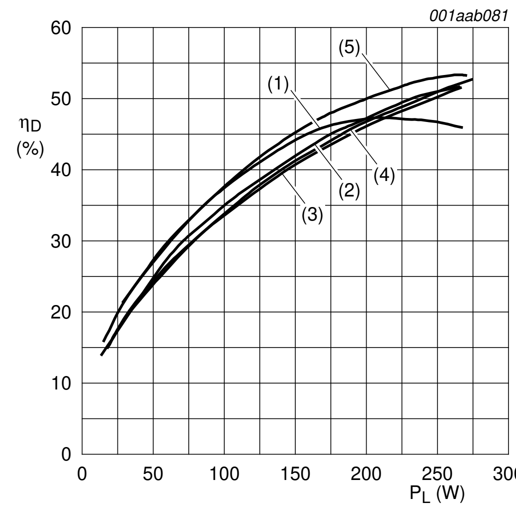
(2) f = 1030 MHz

(3) f = 1090 MHz

(4) f = 1140 MHz

(5) f = 1215 MHz

Fig 6. Load power as a function of input power; typical values



T_h = 25 °C; V_{DS} = 36 V; I_{Dq} = 150 mA; class-AB;
t_p = 100 μs; δ = 10 %.

(1) f = 960 MHz

(2) f = 1030 MHz

(3) f = 1090 MHz

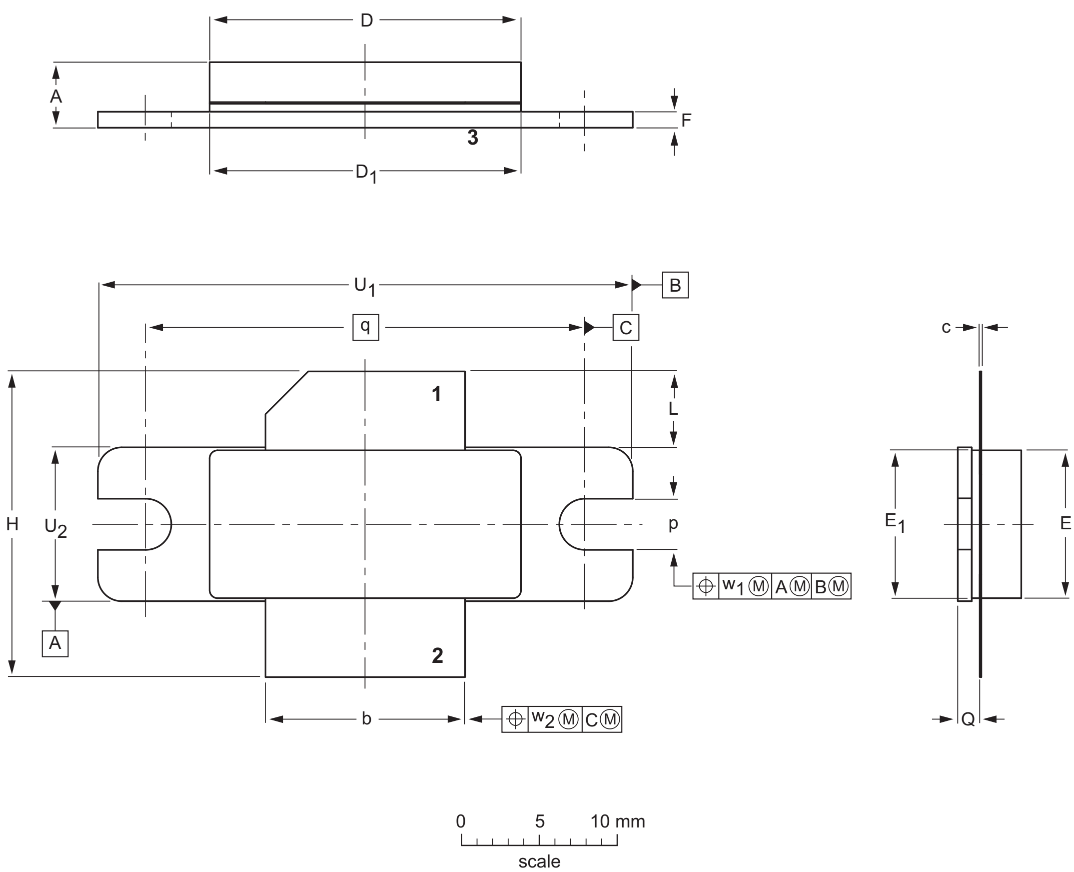
(4) f = 1140 MHz

(5) f = 1215 MHz

Fig 7. Efficiency as a function of load power; typical values

9. Package outline

Flangeed ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 8. Package outline SOT502A

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
DC	Direct Current
DME	Distance Measuring Equipment
JTIDS	Joint Tactical Information Distribution System
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
Mode-S	Mode Select
RF	Radio Frequency
SMD	Surface Mounted Device
TACAN	TACtical Air Navigation
TCAS	Traffic Collision Avoidance System
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA0912-250#4	20150901	Product data sheet	-	BLA0912-250 v.3
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLA0912-250 v.3	20101126	Product data sheet	-	BLA0912-250_2
BLA0912-250_2	20040722	Product data sheet	-	BLA0912-250_N_1
BLA0912-250_N_1	20031024	Preliminary data sheet	-	9397 750 12224

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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