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1. Product profile

1.1 General description

Silicon N-channel enhancement mode LDMOS transistor encapsulated in a 2-lead flangeless package (SOT538A) with a ceramic cap. The common source is connected to the mounting base.

Table 1. Typical performance

RF performance at Th = 25 °C in a common source test circuit.

Mode of operation	f	V _{DS}	PL	G _p
	(MHz)	(V)	(W)	(dB)
Pulsed class-AB; t_{p} = 50 $\mu s;$ δ = 2%	1030 to 1090	36	2	>16

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

- High power gain
- Easy power control

- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

1.3 Applications

Avionics applications in the 1030 to 1090 MHz frequency range.

2. Pinning information

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		1 لــــار
3	source, connected to mounting base		2 – – – 3 sym112

3. Ordering information

Table 3. Ordering information				
Type number	Package			
	Name	Description	Version	
BLA1011-2	-	ceramic surface mounted package; 2 leads	SOT538A	

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage		-	75	V
V _{GS}	gate-source voltage		-	±15	V
I _D	drain current (DC)		-	2.2	А
P _{tot}	total power dissipation	$T_h \le 25 \ ^\circ C$		10	W
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	200	°C

5. Thermal characteristics

Table 5.	Thermal characteristics			
Symbol	Parameter	Conditions	Тур	Unit
Z _{th(j-mb)}	thermal impedance from junction to mounting base		<u>[1]</u> 1	K/W
R _{th(mb-h)}	thermal resistance from mounting base to heatsink		[2] 6.5	K/W

[1] Thermal impedance is determined under RF operating conditions with pulsed bias and T_h = 25 °C.

[2] Typical value for mounting on PCB with 32 0.4 mm thermal vias with 20 μ m tin plating and thermal compound between PCB and heatsink.

6. Characteristics

Table 6.Characteristics

 $T_i = 25 \ ^{\circ}C$ unless otherwise specified.

J	umess otherwise specified.						
Symbol	Parameter	Conditions	Min	Тур	Мах	Unit	
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0; I _D = 0.2 mA	75	-	-	V	
V _{GSth}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 20 mA	2	-	5	V	
I _{DSS}	drain-source leakage current	V _{GS} = 0; V _{DS} = 26 V	-	-	0.1	mA	
I _{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9 V;$ $V_{DS} = 10 V$	2.8	-	-	А	
I _{GSS}	gate leakage current	V _{GS} = ±15 V; V _{DS} = 0	-	-	40	nA	

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1 = 25 01	unless otherwise specified.					
Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 0.75 A	-	0.5	-	S
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 0.75 A	-	1.2	-	Ω
C _{is}	input capacitance	V _{GS} = 0 V; V _{DS} = 26 V; f = 1 MHz	-	11	-	pF
C _{os}	output capacitance	V _{GS} = 0 V; V _{DS} = 26 V; f = 1 MHz	-	9	-	pF
C _{rs}	feedback capacitance	V _{GS} = 0 V; V _{DS} = 26 V; f = 1 MHz	-	0.5	-	pF

Table 6. Characteristics ... continued

Application information 7.

Table 7. RF performance in a common source class-AB circuit T_h

Mode of operation	f	V _{DS}	I _{DQ}	PL	Gp	t _r	t _f	Pulse droop
	(MHz)	(V)	(mA)	(W)	(dB)	(ns)	(ns)	(dB)
Pulsed class-AB; t_p = 50 μ s; δ = 2%	1030 to 1090	36	50	2	>16	<15	<15	<0.5

7.1 Ruggedness in class-AB operation

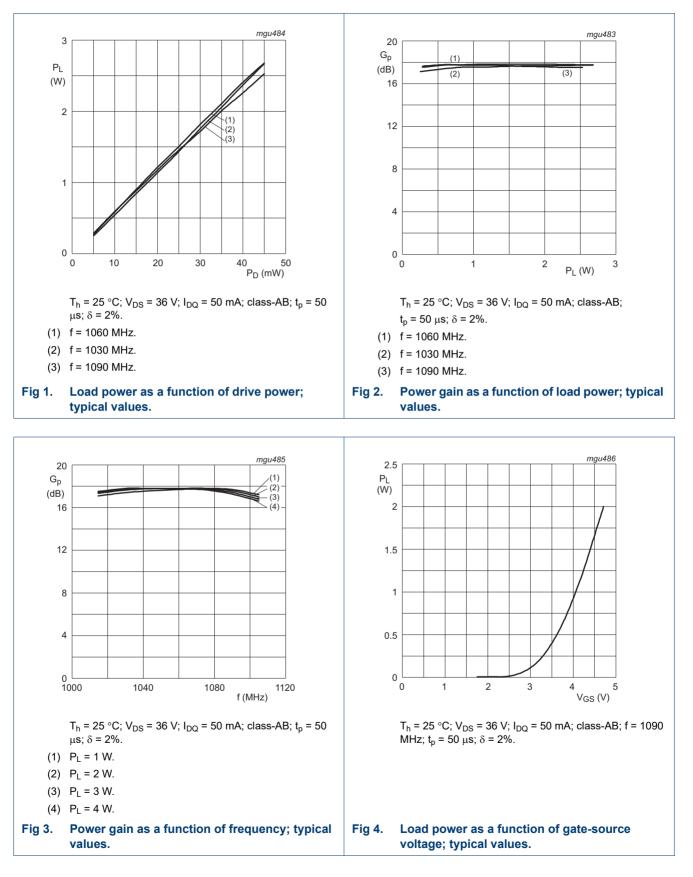
The BLA1011-2 is capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the operating conditions.

Table 0. Typical impedance	e values	
Frequency	Z _S	ZL
(MHz)	(Ω)	(Ω)
1030	1.51 + j 11.76	6.9 + j 5
1060	1.51 + j 11.26	6.7 + j 5.9
1090	1.52 + j 10.77	5.1 + j 6.6

Table 8 Typical impedance values

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BLA1011-2 Avionics LDMOS transistor



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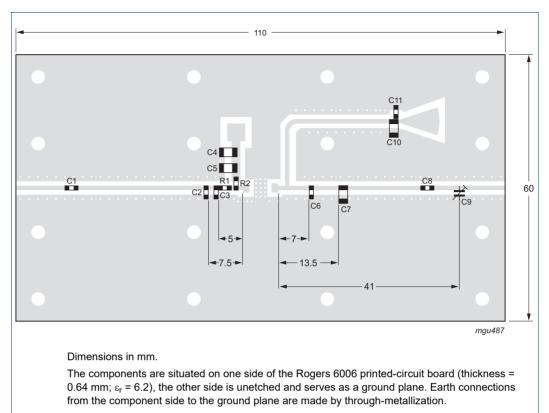


Fig 5. Printed-circuit board for class-AB test circuit.

8. Test information

Table 9. List of components for class-AB test circuit

(see <u>Figure 5</u>)		
Component	Description	Value
C1, C8	multilayer ceramic chip capacitor	[<u>1]</u> 56 pF
C2	multilayer ceramic chip capacitor	[<u>1]</u> 7.5 pF
C3	multilayer ceramic chip capacitor	<u>[1]</u> 1.8 pF
C4, C10	multilayer ceramic chip capacitor	20 nF
C5	multilayer ceramic chip capacitor	[<u>3]</u> 33 pF
C6	multilayer ceramic chip capacitor	[<u>1]</u> 5.6 pF
C7	multilayer ceramic chip capacitor	[3] 6.2 pF
C9	tekelec trimmer; type 37283	0.4 to 2.5 pF
C11	multilayer ceramic chip capacitor	[<u>1]</u> 33 pF
R1	SMD resistor	2.2 Ω (2 in parallel)
R2	SMD resistor	22 Ω

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 200B or capacitor of same quality.

[3] American Technical Ceramics type 100B or capacitor of same quality.

9. Package outline

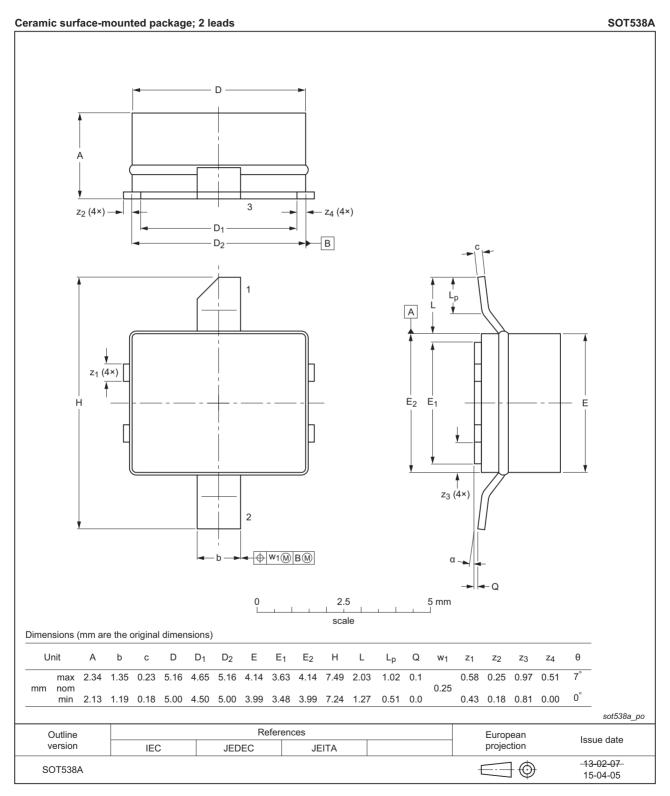


Fig 6. Package outline SOT538A

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10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA1011-2#7	20150901	Product data sheet	-	BLA1011-2 v.6
Modifications:	 The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. 			
BLA1011-2 v.6	20130506	Product data sheet	_	BLA1011-2 v.5
BLA1011-2 v.5	20031119	Product specification	-	BLA1011-2 v.4

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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