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# BLC2425M8LS300P

Power LDMOS transistor

Rev. 3 — 17 June 2016

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

300 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLC2425M8LS300P is designed for high-power CW applications and is assembled in a high performance plastic package.

**Table 1. Typical performance**

*RF performance at  $V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 20\text{ mA}$ ;  $T_{case} = 25\text{ °C}$  in a class-AB application circuit.*

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	32	300	17.0	58.0
CW pulsed [1]	2450	32	300	17.5	61.0

[1]  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\text{ %}$

### 1.2 Features and benefits

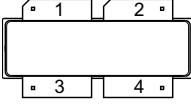
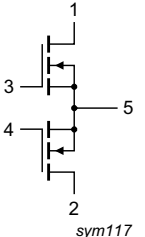
- High efficiency
- Easy power control
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally matched
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for CW applications in the 2400 MHz to 2500 MHz frequency range such as ISM applications and heating

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
flange	source		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC2425M8LS300P	-	air cavity plastic earless flanged package; 4 leads	SOT1250-1

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 300\text{ W}$	0.2	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ }^\circ\text{C}$ , per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.2\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 220\text{ mA}$	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	39	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 11\text{ A}$	-	16	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 7.7\text{ A}$	-	0.08	-	$\Omega$

**Table 7. RF characteristics**

Test signal: CW at 2450 MHz; RF performance at  $V_{DS} = 32\text{ V}; I_{Dq} = 20\text{ mA}; T_{case} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 300\text{ W}$	16.3	17.5	-	dB
$RL_{in}$	input return loss	$P_L = 300\text{ W}$	-	-14	-7	dB
$\eta_D$	drain efficiency	$P_L = 300\text{ W}$	49	54.5	-	%

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLC2425M8LS300P is capable of withstanding a load mismatch corresponding to  $VSWR = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 32\text{ V}; I_{Dq} = 20\text{ mA}; P_L = 300\text{ W (CW)}; f = 2450\text{ MHz}$ .

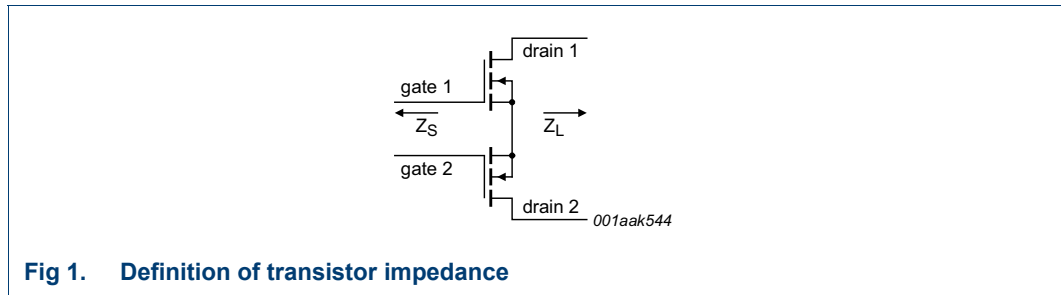
### 7.2 Impedance information

**Table 8. Typical impedance**

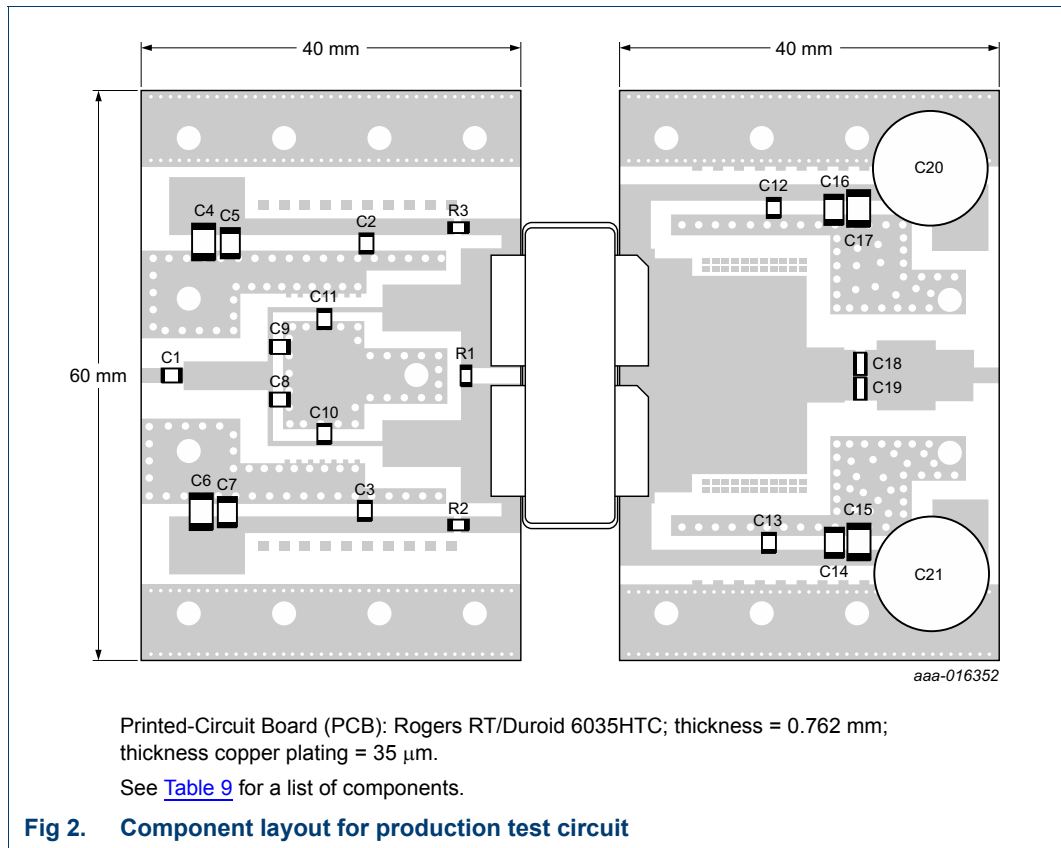
Measured load-pull data half device. Typical values unless otherwise specified.  $I_{Dq} = 20\text{ mA}; V_{DS} = 32\text{ V}$ .

f (MHz)	$Z_S$ [1] ( $\Omega$ )	$Z_L$ [1] ( $\Omega$ )
2400	1.2 – 5.9j	3.7 – 2.8j
2450	1.3 – 5.0j	3.2 – 2.5j
2500	3.3 – 7.0j	3.1 – 2.3j

[1]  $Z_S$  and  $Z_L$  defined in [Figure 1](#).



### 7.3 Test circuit



**Table 9. List of components**

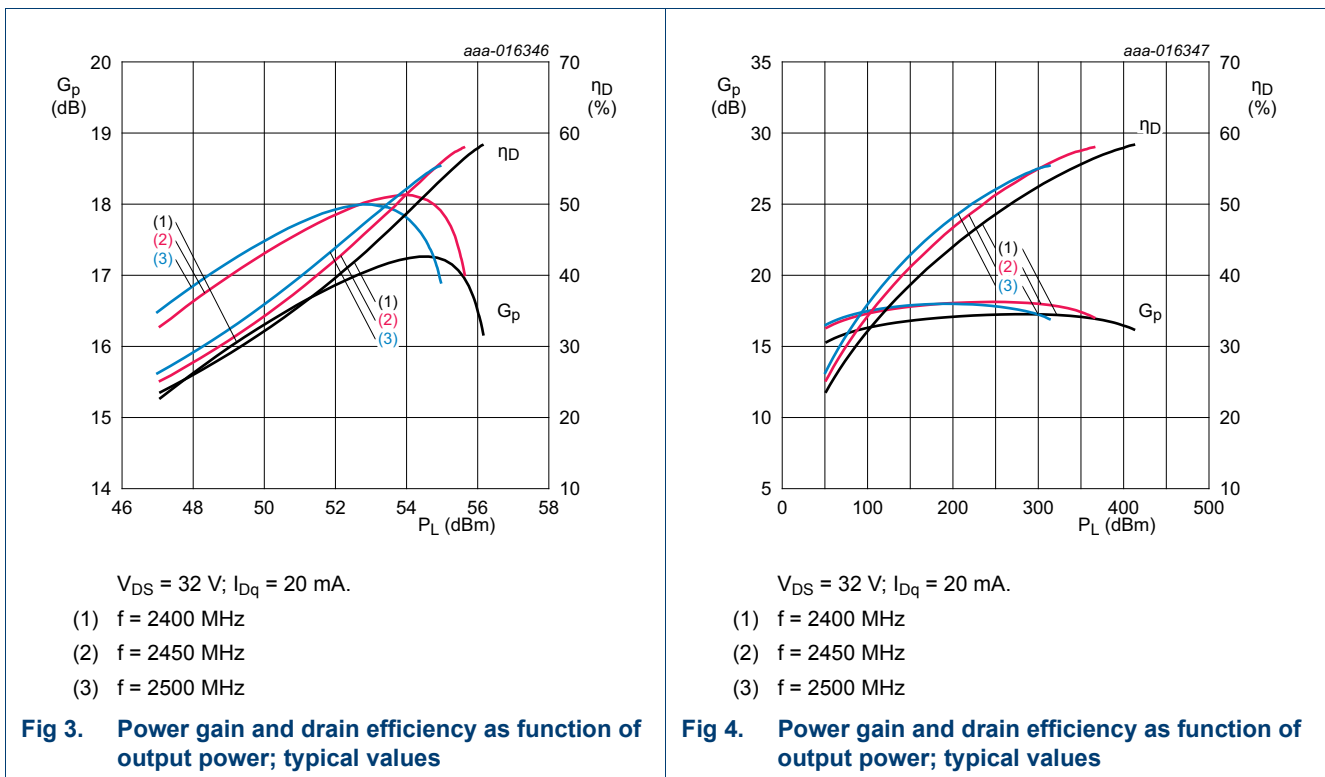
See [Figure 2](#) for component layout.

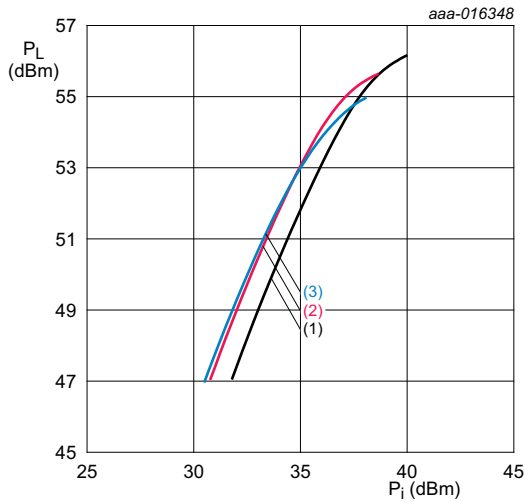
Component	Description	Value	Remarks
C1, C2, C3, C12, C13	multilayer ceramic chip capacitor	36 pF	ATC 800B
C4, C6, C15, C17	multilayer ceramic chip capacitor	10 μF, 50 V	
C5, C7, C14, C16	multilayer ceramic chip capacitor	470 nF, 50 V	
C8, C9	multilayer ceramic chip capacitor	1.4 pF	ATC 100B
C10, C11	multilayer ceramic chip capacitor	1.8 pF	ATC 100B
C18, C19	multilayer ceramic chip capacitor	24 pF	ATC 800R

**Table 9. List of components ...continued**  
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C20, C21	electrolytic capacitor	470 $\mu$ F, 63 V	
R1	resistor	9.1 $\Omega$	SMD 0805
R2, R3	resistor	5.1 $\Omega$	SMD 0805

### 7.4 Graphical data

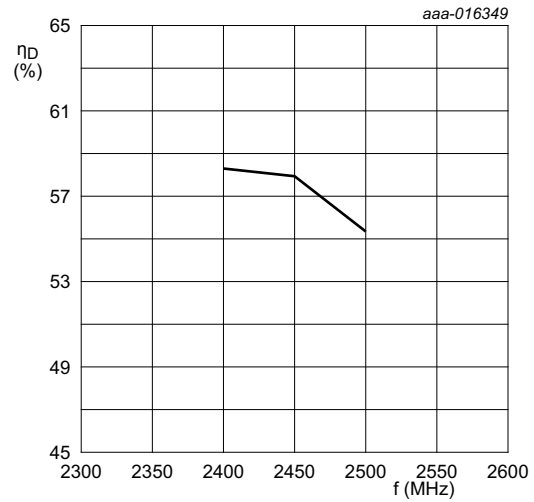




$V_{DS} = 32\text{ V}; I_{Dq} = 20\text{ mA}.$

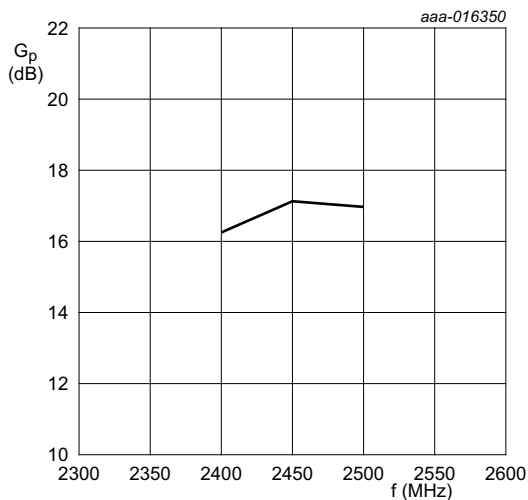
- (1)  $f = 2400\text{ MHz}$
- (2)  $f = 2450\text{ MHz}$
- (3)  $f = 2500\text{ MHz}$

**Fig 5. Output power as a function of input power; typical values**



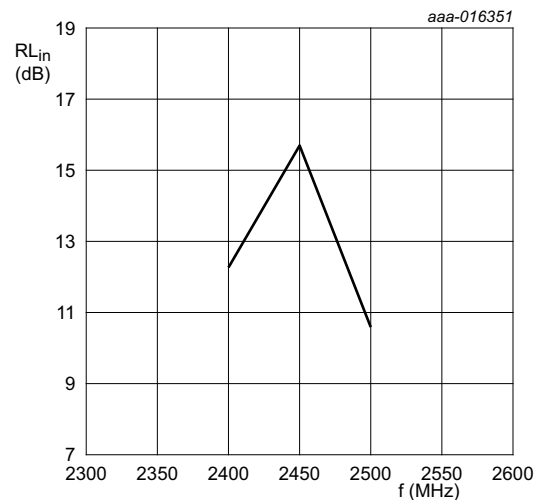
$V_{DS} = 32\text{ V}; I_{Dq} = 20\text{ mA}.$

**Fig 6. Drain efficiency as a function of frequency; typical values**



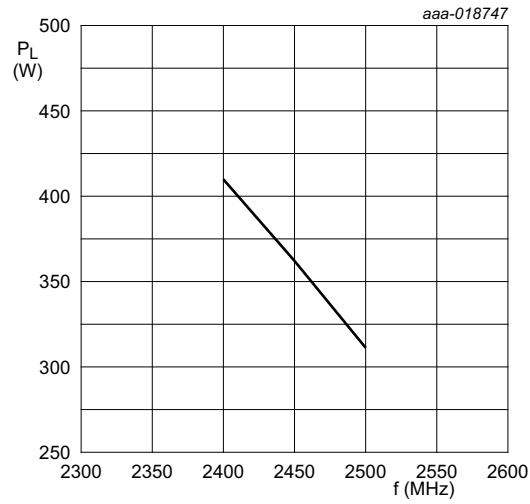
$V_{DS} = 32\text{ V}; I_{Dq} = 20\text{ mA}.$

**Fig 7. Power gain as a function of frequency; typical values**



$V_{DS} = 32\text{ V}; I_{Dq} = 20\text{ mA}.$

**Fig 8. Input return loss as a function of frequency; typical values**



V<sub>DS</sub> = 32 V; I<sub>Dq</sub> = 20 mA.

**Fig 9. Output power as a function of frequency; typical values**



8. Package outline

Plastic earless flanged cavity package; 4 leads

SOT1250-1

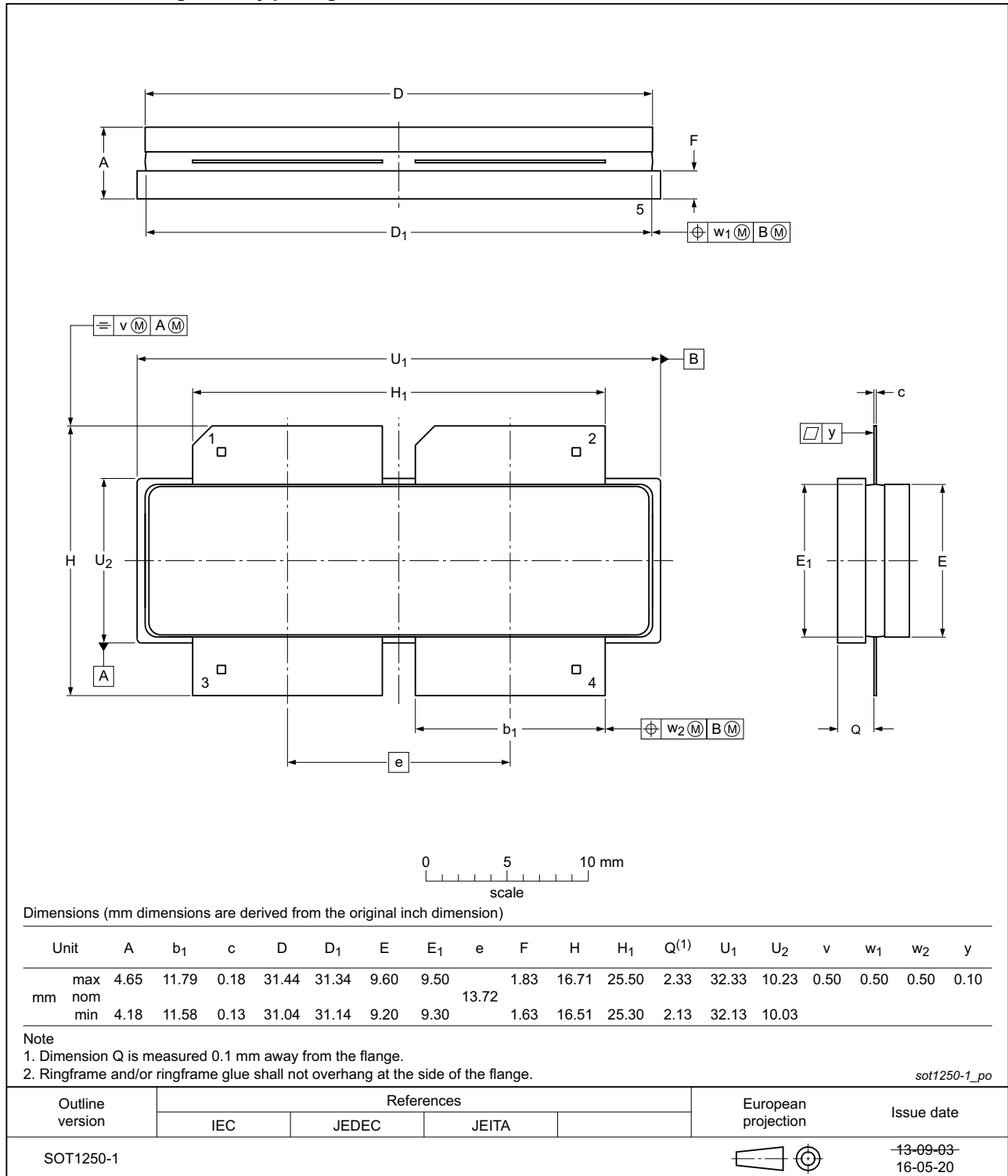



Fig 10. Package outline SOT1250-1

## 9. Handling information

CAUTION	
	<p>This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.</p> <p>Such precautions are described in the <i>ANSI/ESD S20.20</i>, <i>IEC/ST 61340-5</i>, <i>JESD625-A</i> or equivalent standards.</p>

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC2425M8LS300P v.3	20160617	Product data sheet	-	BLC2425M8LS300P#2
Modifications	<ul style="list-style-type: none"> <li><a href="#">Table 7 on page 3</a>: table updated</li> <li><a href="#">Figure 10 on page 8</a>: figure updated</li> </ul>			
BLC2425M8LS300P#2	20150901	Objective data sheet	-	BLC2425M8LS300P v.1
BLC2425M8LS300P v.1	20150703	Objective data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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