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BLC8G22LS-450AV

Power LDMOS transistor

AMPLEON

Rev. 5 — 2 December 2016

Product data sheet

1. Product profile

1.1 General description

450 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2110 MHz to 2170 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty production test circuit. V_{DS} = 28 V; I_{Dq} = 1000 mA (main); $V_{GS(amp)peak}$ = 0.50 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2110 to 2170	28	85	14	41	–33 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

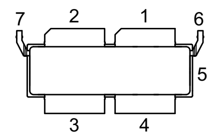
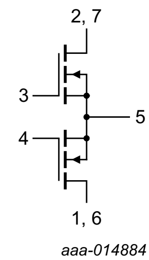
- Excellent ruggedness
- High-efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2110 MHz to 2170 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC8G22LS-450AV	-	air cavity plastic earless flanged package; 6 leads	SOT1258-3

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–0.5	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
T_{case}	case temperature		–40	+125	°C

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 28 V; I_{Dq} = 800 mA (main); $V_{GS(amp)peak}$ = 0.60 V; T_{case} = 80 °C		
		P_L = 85 W	0.29	K/W
		P_L = 110 W	0.27	K/W

7. Characteristics

Table 7. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.2 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 220 mA	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 900 mA	1.7	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	40	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 11 A	-	14.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 7.7 A	-	72	107	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 350 mA	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 2200 mA	1.7	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	58	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 17.5 A	-	23	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 12.25 A	-	47	69	mΩ

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 2112.5 MHz; f_2 = 2167.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1000 mA (main); $V_{GS(amp)peak}$ = 0.50 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 2110 MHz to 2170 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 85 W	13	14	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 85 W	-	−12	−7	dB
η_D	drain efficiency	$P_{L(AV)}$ = 85 W	37	41	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 85 W	-	−33	−27	dBc

Table 9. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f = 2115 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1000 mA (main); $V_{GS(amp)peak}$ = 0.50 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at a frequency of 2112.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 115 W	5.9	6.5	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 115 W	437	510	-	W

8. Test information

8.1 Ruggedness in Doherty operation

The BLC8G22LS-450AV is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:

- V_{DS} = 28 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 0.50 V; f = 2112.5 MHz: 1-carrier W-CDMA; P_L = 141 W (5 dB OBO); 100 % clipping
- V_{DS} = 32 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 0.50 V; f = 2112.5 MHz: 1-carrier W-CDMA; P_L = 141 W (5 dB OBO); 100 % clipping

8.2 Impedance information

Table 10. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 1300 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2110	1.2 – j5.1	0.7 – j4.4	217	49.1	16.8
2140	1.7 – j5.4	0.8 – j4.6	214	49.2	17.1
2170	1.9 – j5.6	0.8 – j4.7	207	48.8	17.3
Maximum drain efficiency load					
2110	1.2 – j5.1	1.4 – j3.4	166	58.1	18.9
2140	1.7 – j5.4	1.4 – j4.0	159	57.4	19.1
2170	1.9 – j5.6	1.4 – j4.0	151	56.4	19.4

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 11. Typical impedance of peak device

Measured load-pull data of main device; I_{Dq} = 2300 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2110	0.7 – j5.8	2.1 – j6.2	351	50.0	16.9
2140	0.9 – j6.0	2.1 – j6.3	346	51.0	17.3

Table 11. Typical impedance of peak device *...continued*

Measured load-pull data of main device; I_{Dq} = 2300 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2170	1.3 – j6.4	2.4 – j6.6	342	49.1	17.2
Maximum drain efficiency load					
2110	0.7 – j5.8	1.6 – j5.1	274	58.0	18.8
2140	0.9 – j6.0	1.6 – j5.1	261	57.5	19.0
2170	1.3 – j6.4	1.7 – j5.4	270	56.6	18.9

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

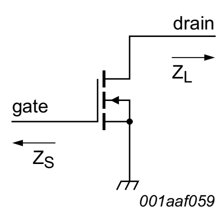


Fig 1. Definition of transistor impedance

8.3 Recommended impedances for Doherty design

Table 12. Typical impedance of main at 1 : 1 load

Measured load-pull data of main device; I_{Dq} = 1300 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$ [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	1.2 – j5.1	1.0 – j4.5	182	45	17.0
2140	1.7 – j5.4	1.0 – j4.5	182	45	17.1
2170	1.9 – j5.6	1.0 – j4.7	182	45	17.3

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 85 W.

Table 13. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; I_{Dq} = 1300 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$ [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	1.2 – j5.1	1.8 – j3.6	100	45	19.0
2140	1.7 – j5.4	2.0 – j3.6	100	45	19.0
2170	1.9 – j5.6	2.1 – j3.6	100	45	19.0

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 85 W.

Table 14. Typical impedance of peak device at 1 : 1 load

Measured load-pull data of main device; I_{Dq} = 2300 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$ [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	0.7 – j5.8	2.2 – j6.4	309	54.0	16.9
2140	0.9 – j6.0	2.2 – j6.2	309	54.0	17.3
2170	1.3 – j6.4	2.2 – j6.1	309	54.0	17.2

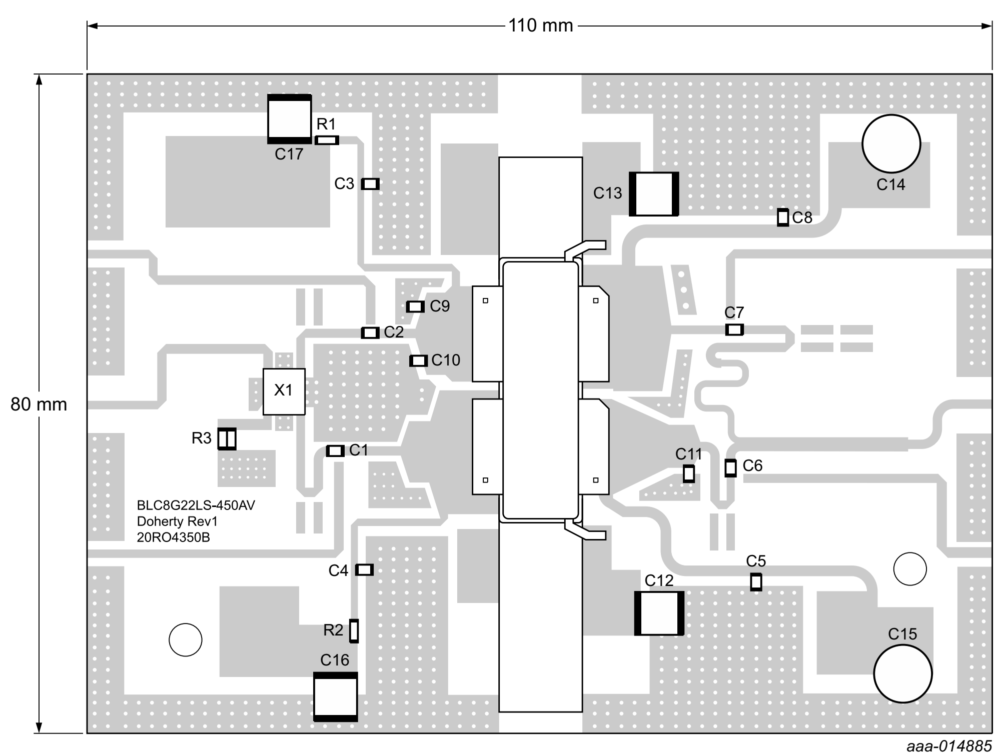
[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 15. Off-state impedances of peak device

f	Z_{off}
(MHz)	(Ω)
2110	0.5 – j3.4
2140	0.5 – j3.6
2170	0.5 – j3.8

8.4 Test circuit



Printed-Circuit Board (PCB): Rogers 4350B: ε_r = 3.66; thickness = 0.508 mm; thickness copper plating = 35 μm. See Table 16 for a list of components.

Fig 2. Component layout

Table 16. List of components

See Figure 2 for component layout.

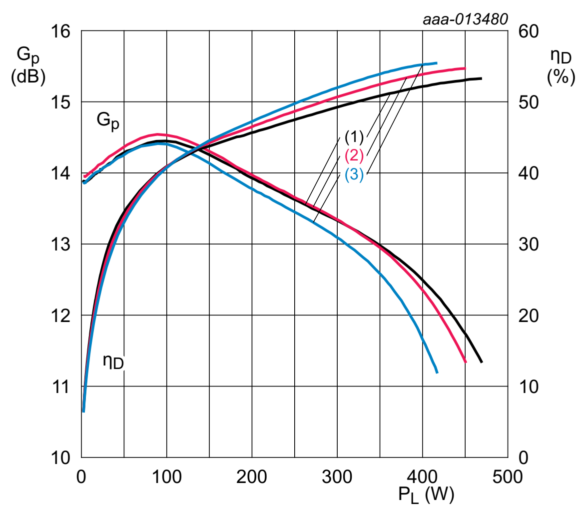
Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6, C7, C8	multilayer ceramic chip capacitor	10 pF [1]	ATC 800B
C9, C10	multilayer ceramic chip capacitor	1.0 pF [1]	ATC 800B
C11	multilayer ceramic chip capacitor	0.2 pF [1]	ATC 800B
C12, C13	multilayer ceramic chip capacitor	4.7 μF, 100 V [2]	Murata
C14, C15	electrolytic capacitor	470 μF, 63 V	
C16, C17	multilayer ceramic chip capacitor	10.0 μF, 50 V [2]	Murata
R1, R2	SMD resistor	4.7 Ω	SMD 1206, Philips
R3	SMD resistor	50 Ω, 10 W	SMD 1206, Philips
X1	transistor	-	Anaren X3C21P1-04S

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] Murata or capacitor of same quality.

8.5 Graphical data

8.5.1 Pulsed CW



V_{DS} = 28 V; I_{Dq} = 1000 mA; $V_{GS(amp)peak}$ = 0.50 V; t_p = 100 μs; δ = 10 %.

(1) f = 2110 MHz

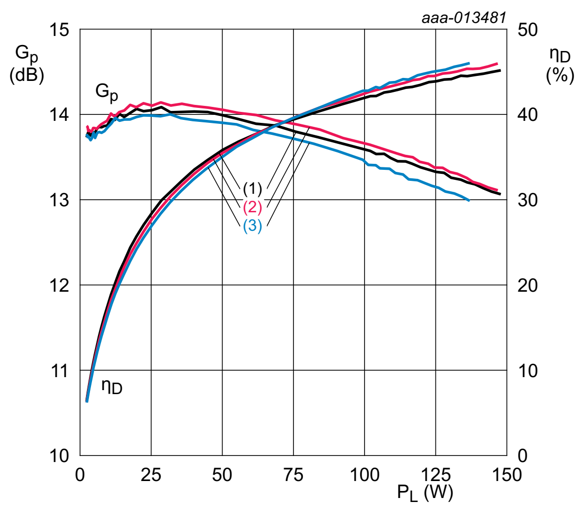
(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

8.5.2 1-Carrier W-CDMA

PAR = 9.6 dB per carrier at 0.01 % probability on the CCDF; 3GPP test model 1 with 64 DPCH (100 % clipping).



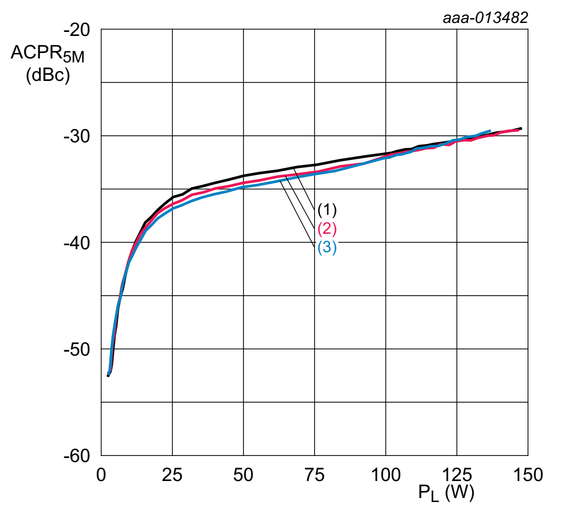
V_{DS} = 28 V; I_{Dq} = 1000 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 2112.5 MHz

(2) f = 2140.0 MHz

(3) f = 2167.5 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



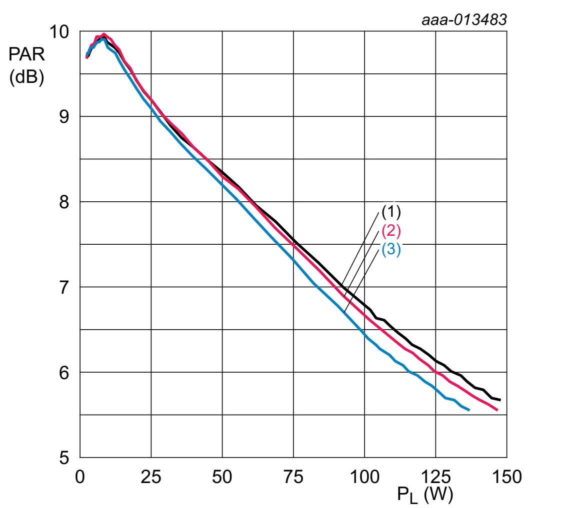
V_{DS} = 28 V; I_{Dq} = 1000 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 2112.5 MHz

(2) f = 2114.0 MHz

(3) f = 2167.5 MHz

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



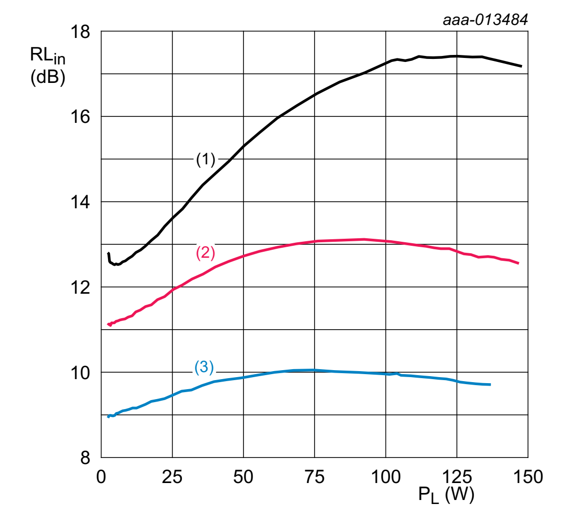
V_{DS} = 28 V; I_{Dq} = 1000 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 2112.5 MHz

(2) f = 2114.0 MHz

(3) f = 2167.5 MHz

Fig 6. Peak-to-average power ratio as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 1000 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 2112.5 MHz

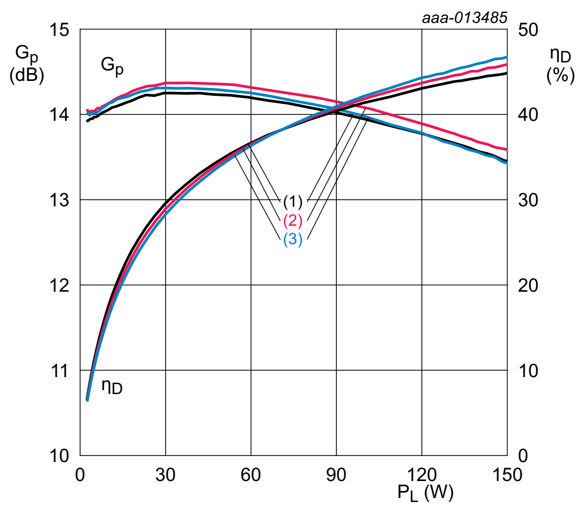
(2) f = 2114.0 MHz

(3) f = 2167.5 MHz

Fig 7. Input return loss as a function of output power; typical values

8.5.3 2-Carrier W-CDMA

PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1 with 64 DPCH (46 % clipping).



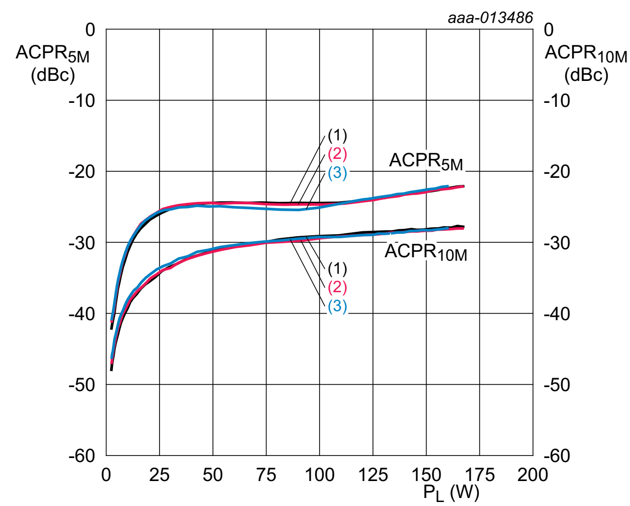
V_{DS} = 28 V; I_{Dq} = 1000 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 2112.5 MHz

(2) f = 2140.0 MHz

(3) f = 2167.5 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values



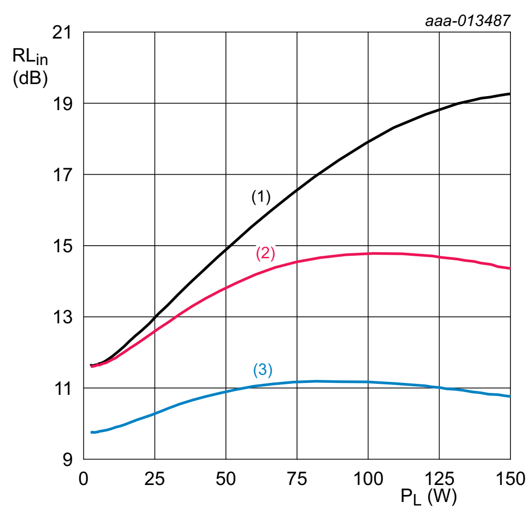
V_{DS} = 28 V; I_{Dq} = 1000 mA; $V_{GS(amp)peak}$ = 0.50 V.

(1) f = 2112.5 MHz

(2) f = 2114.0 MHz

(3) f = 2167.5 MHz

Fig 9. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 1000 mA; $V_{GS(amp)peak}$ = 0.50 V.

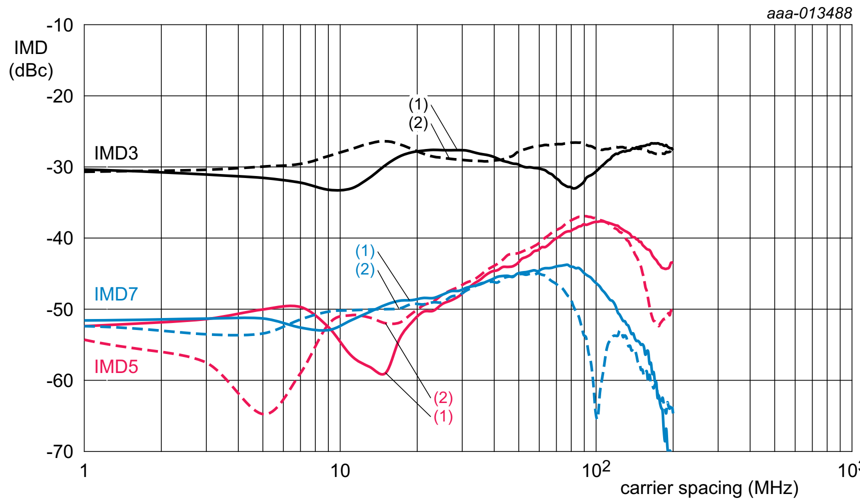
(1) f = 2112.5 MHz

(2) f = 2114.0 MHz

(3) f = 2167.5 MHz

Fig 10. Input return loss as a function of output power; typical values

8.5.4 2-Tone VBW



V_{DS} = 28 V; I_{Dq} = 1000 mA; $V_{GS(amp)peak}$ = 0.50 V; f = 2114 MHz.

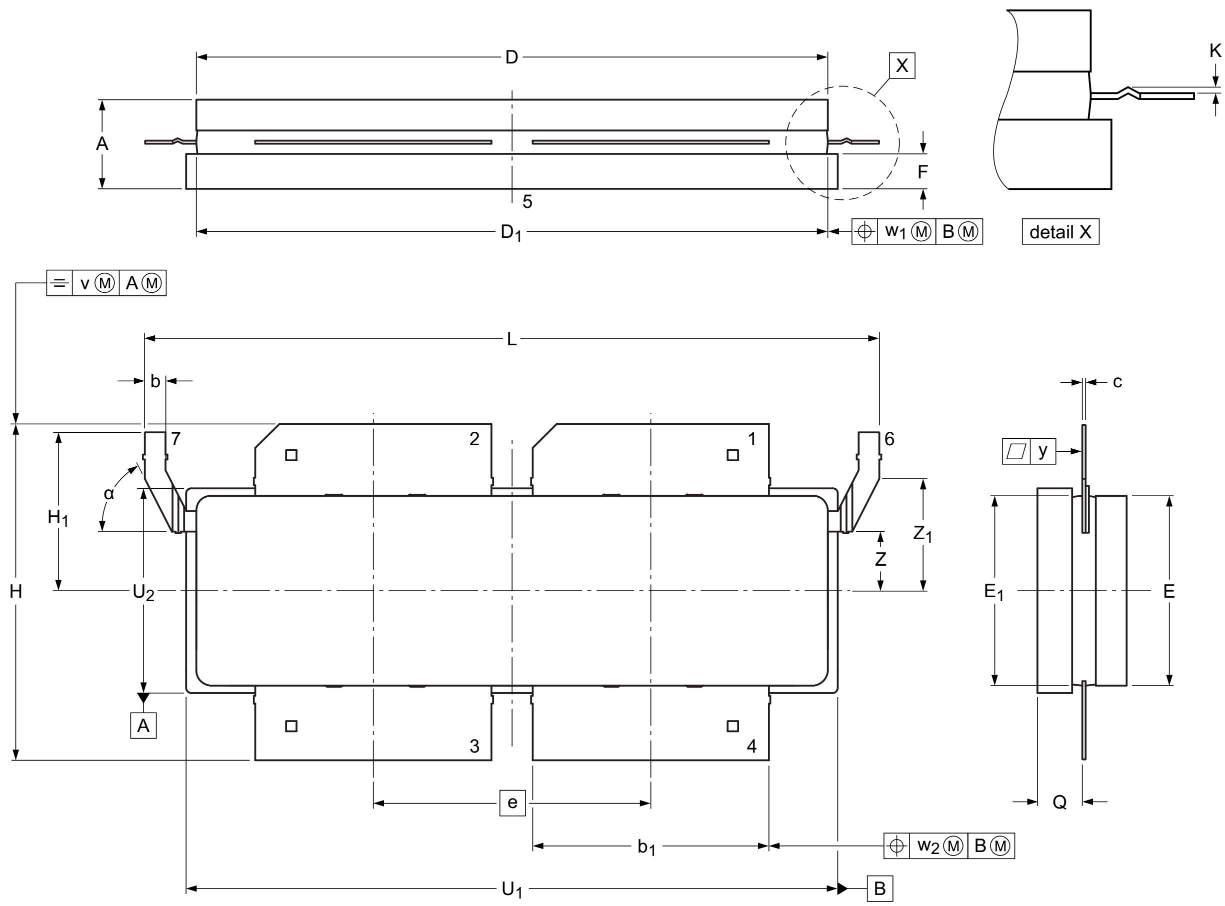
(1) IMD low

(2) IMD high

Fig 11. VBW capability

9. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1258-3**



K	y	α	Z	Z_1
0.17	0.1	65°	3.17	5.79
		61°	2.67	5.29

0 10 mm
scale

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	L	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2
mm	max	4.65	1.12	11.78	0.2	31.44	31.34	9.60	9.50		36.42	1.83	16.71	8.12	2.33	32.33	10.23	0.5	0.5	0.5
	nom									13.72										
	min	4.18	0.91	11.58	0.1	31.04	31.14	9.20	9.30		36.22	1.63	16.51	7.62	2.13	32.13	10.03			

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1258-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1258-3						~~14-12-19~~ 16-10-03

Fig 12. Package outline SOT1258-3

 All information provided in this document is subject to legal disclaimers.

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 17. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

11. Abbreviations

Table 18. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back-Off
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC8G22LS-450AV v.5	20161202	Product data sheet	-	BLC8G22LS-450AV v.4
Modifications:	• Figure 12 on page 11: updated package outline drawing SOT1258-3 • Section 10 on page 12: updated Handling information			
BLC8G22LS-450AV v.4	20150901	Product data sheet	-	BLC8G22LS-450AV v.3
BLC8G22LS-450AV v.3	20150602	Product data sheet	-	BLC8G22LS-450AV v.2
BLC8G22LS-450AV v.2	20150515	Product data sheet	-	BLC8G22LS-450AV v.1
BLC8G22LS-450AV v.1	20140929	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contact information

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For sales office addresses, please visit: **http://www.ampleon.com/sales**

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