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# BLC9G21LS-60AV

Power LDMOS transistor

Rev. 1 — 6 July 2017

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

60 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1805 MHz to 2200 MHz.

**Table 1. Typical performance**

*Typical RF performance at  $T_{case} = 25\text{ °C}$  in the Doherty demo board.*

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1930 to 1990	28	2.5	17.5	30	-39 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01% probability on CCDF per carrier.

### 1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Asymmetric design to achieve optimum efficiency across the band
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 2200 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	video decoupling (main)		
6	video decoupling (peak)		
7	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G21LS-60AV	-	air cavity plastic earless flanged package; 6 leads	SOT1275-1

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$		
		$P_L = 2.5\text{ W}$	0.92	K/W
		$P_L = 9.5\text{ W}$	0.97	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Main device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.2\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 20\text{ mA}$	1.5	2	2.5	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 100\text{ mA}$	1.7	2.2	2.7	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	4	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 1.0\text{ A}$	-	1.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 0.7\text{ A}$	-	624	1135	$\text{m}\Omega$
<b>Peak device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.3\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 30\text{ mA}$	1.5	2	2.5	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 150\text{ mA}$	1.7	2.2	2.7	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	6	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 1.5\text{ A}$	-	2.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 1.05\text{ A}$	-	420	760	$\text{m}\Omega$

**Table 7. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 100\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.8\text{ V}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1930 MHz to 1990 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 2.5\text{ W}$	16.3	17.5	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 2.5\text{ W}$	-	-10	-7	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 2.5\text{ W}$	26	30	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 2.5\text{ W}$	-	-39	-34	dBc

**Table 8. RF characteristics**

Test signal: pulsed CW;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\text{ %}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 100\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.8\text{ V}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1930 MHz to 1990 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(M)}$	peak output power		53	60	-	W

## 7. Test information

### 7.1 Ruggedness in Doherty operation

The BLC9G21LS-60AV is capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 100\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.8\text{ V}$ ;  $P_L = 38\text{ W}$  (CW);  $f_1 = 1805\text{ MHz}$ ;  $f_2 = 1930\text{ MHz}$ .

### 7.2 Impedance information

**Table 9. Typical impedance of main device**

Measured load-pull data of main device;  $I_{Dq} = 100\text{ mA}$  (main);  $V_{DS} = 28\text{ V}$ .

f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)	P <sub>L</sub> [2] (W)	η <sub>D</sub> [2] (%)	G <sub>p</sub> [2] (dB)
<b>Maximum power load</b>					
1805	2.4 – j6.9	12.0 – j9.4	30.7	63.9	16.4
1842	2.3 – j7.1	12.0 – j9.4	30.2	63.5	16.5
1880	2.6 – j7.9	11.0 – j8.0	29.3	61.2	16.2
1930	2.6 – j9.3	12.0 – j9.4	27.8	60.1	16.6
1960	3.2 – j9.0	12.0 – j9.4	28.4	60.6	16.5
1990	3.4 – j9.6	12.0 – j9.4	27.4	59.1	16.6
2110	4.7 – j15.9	9.7 – j8.8	29.2	60.6	18.0
2140	6.7 – j15.3	9.7 – j8.8	28.1	58.9	18.0
2170	5.3 – j19.6	9.7 – j8.8	29.1	61.7	18.3
<b>Maximum drain efficiency load</b>					
1805	2.4 – j6.9	23.6 – j0.0	20.5	73.3	18.2
1842	2.3 – j7.1	20.0 – j0.0	21.7	73.0	18.0
1880	2.6 – j7.9	19.6 – j3.1	18.9	71.5	18.4
1930	2.6 – j9.3	17.0 – j2.4	18.5	67.9	18.5
1960	3.2 – j9.0	14.8 – j2.0	19.7	69.3	18.3
1990	3.4 – j9.6	15.0 – j0.0	20.0	66.4	18.3
2110	4.7 – j15.9	13.0 – j1.6	17.7	69.4	20.6
2140	6.7 – j15.3	11.2 – j2.7	21.9	66.2	19.5
2170	5.3 – j19.6	11.6 – j1.4	20.7	70.6	20.5

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] at 3 dB gain compression.

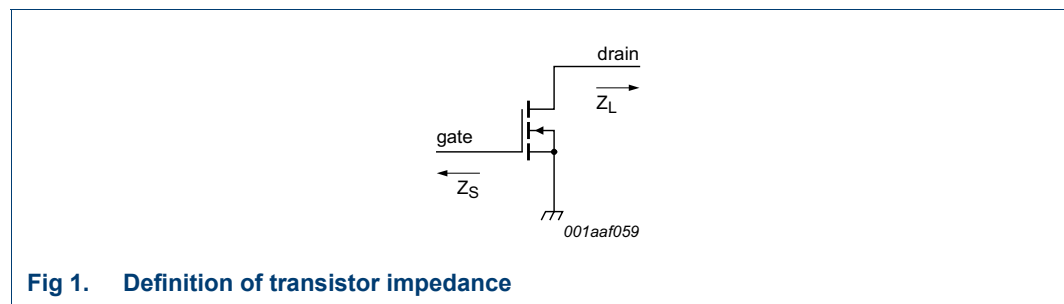
**Table 10. Typical impedance of peak device**

Measured load-pull data of peak device;  $I_{Dq} = 150 \text{ mA (peak)}$ ;  $V_{DS} = 28 \text{ V}$ .

f (MHz)	$Z_S$ [1] ( $\Omega$ )	$Z_L$ [1] ( $\Omega$ )	$P_L$ [2] (W)	$\eta_D$ [2] (%)	$G_P$ [2] (dB)
<b>Maximum power load</b>					
1805	2.2 – j6.6	6.5 – j7.7	46.2	63.4	15.9
1842	1.8 – j6.9	6.5 – j7.7	44.8	63.0	16.4
1880	2.5 – j7.0	6.5 – j7.7	43.0	61.4	16.2
1930	2.5 – j7.9	6.5 – j7.7	41.8	60.9	16.4
1960	2.8 – j8.0	6.9 – j8.6	41.9	60.1	16.3
1990	2.8 – j8.4	6.9 – j8.6	43.8	62.4	16.3
2110	5.1 – j12.6	5.7 – j8.0	43.8	62.5	17.7
2140	4.9 – j12.6	5.9 – j8.9	42.2	59.0	17.6
2170	5.8 – j14.8	5.9 – j8.9	43.1	60.9	17.8
<b>Maximum drain efficiency load</b>					
1805	2.2 – j6.6	10.3 – j1.2	32.0	74.9	17.8
1842	1.8 – j6.9	9.2 – j1.0	31.1	74.5	18.1
1880	2.5 – j7.0	9.0 – j2.0	30.4	69.8	18.2
1930	2.5 – j7.9	7.3 – j1.5	28.6	69.6	18.3
1960	2.8 – j8.0	7.1 – j2.3	29.6	68.5	18.1
1990	2.8 – j8.4	7.3 – j1.5	28.6	72.7	18.8
2110	5.1 – j12.6	7.0 – j4.0	32.0	70.3	19.8
2140	4.9 – j12.6	6.0 – j4.1	30.4	67.8	19.7
2170	5.8 – j14.8	6.0 – j4.1	30.6	70.5	20.2

[1]  $Z_S$  and  $Z_L$  defined in [Figure 1](#).

[2] at 3 dB gain compression.



**Fig 1. Definition of transistor impedance**

### 7.3 Recommended impedances for Doherty design

**Table 11. Typical impedance of main device at 1 : 1 load**

Measured load-pull data of main device;  $I_{Dq} = 100 \text{ mA (main)}$ ;  $V_{DS} = 28 \text{ V}$ .

f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)	P <sub>L</sub> [2] (W)	η <sub>D</sub> [3] (%)	G <sub>p</sub> [3] (dB)
1805	2.4 – j6.9	13.6 – j8.2	30.2	67.0	19.7
1842	2.3 – j7.1	13.6 – j8.2	29.4	66.6	19.9
1880	2.6 – j7.9	13.6 – j8.2	28.6	65.6	20.0
1930	2.6 – j9.3	13.6 – j8.2	26.8	62.8	20.1
1960	3.2 – j9.0	13.6 – j8.2	27.5	63.6	20.0
1990	3.4 – j9.6	12.2 – j6.9	26.6	61.9	19.9
2110	4.7 – j15.9	12.2 – j6.9	27.4	66.4	21.9
2140	6.7 – j15.3	10.1 – j6.8	27.5	62.6	21.5
2170	5.3 – j19.6	11.0 – j8.0	28.5	64.9	21.8

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] at 3 dB gain compression.

[3] at P<sub>L(AV)</sub> = 34 dBm.

**Table 12. Typical impedance of main device at 1 : 2.7 load**

Measured load-pull data of main device;  $I_{Dq} = 100 \text{ mA (main)}$ ;  $V_{DS} = 28 \text{ V}$ .

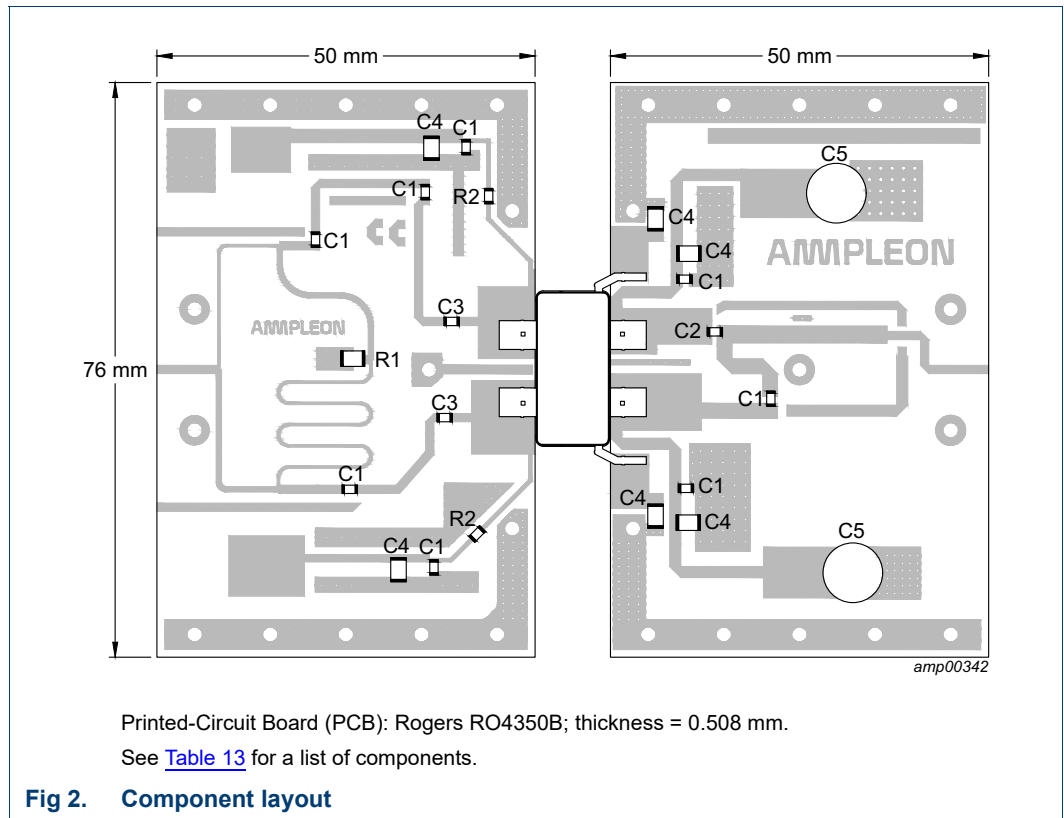
f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)	P <sub>L</sub> [2] (W)	η <sub>D</sub> [3] (%)	G <sub>p</sub> [3] (dB)
1805	2.4 – j6.9	23.6 – j0.0	20.5	73.3	21.2
1842	2.3 – j7.1	20.0 – j0.0	21.7	73.0	21.2
1880	2.6 – j7.9	19.6 – j3.1	18.9	71.5	21.4
1930	2.6 – j9.3	17.0 – j2.4	18.5	67.9	21.5
1960	3.2 – j9.0	14.8 – j2.0	19.7	69.3	21.3
1990	3.4 – j9.6	15.0 – j0.0	20.0	66.4	21.3
2110	4.7 – j15.9	13.0 – j1.6	17.7	69.4	23.6
2140	6.7 – j15.3	11.2 – j2.7	21.9	66.2	22.5
2170	5.3 – j19.6	11.6 – j1.4	20.7	70.6	23.5

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] at 3 dB gain compression.

[3] at P<sub>L(AV)</sub> = 34 dBm.

7.4 Test circuit



**Table 13. List of components**

See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	30 pF <a href="#">[1]</a>	
C2	multilayer ceramic chip capacitor	20 pF <a href="#">[1]</a>	
C3	multilayer ceramic chip capacitor	3.9 pF <a href="#">[1]</a>	
C4	multilayer ceramic chip capacitor	10 μF, 50 V <a href="#">[2]</a>	
C5	electrolytic capacitor	2200 μF, 63 V	
R1	resistor	50 Ω	SMD 2512
R2	resistor	5.1 Ω	SMD 0805

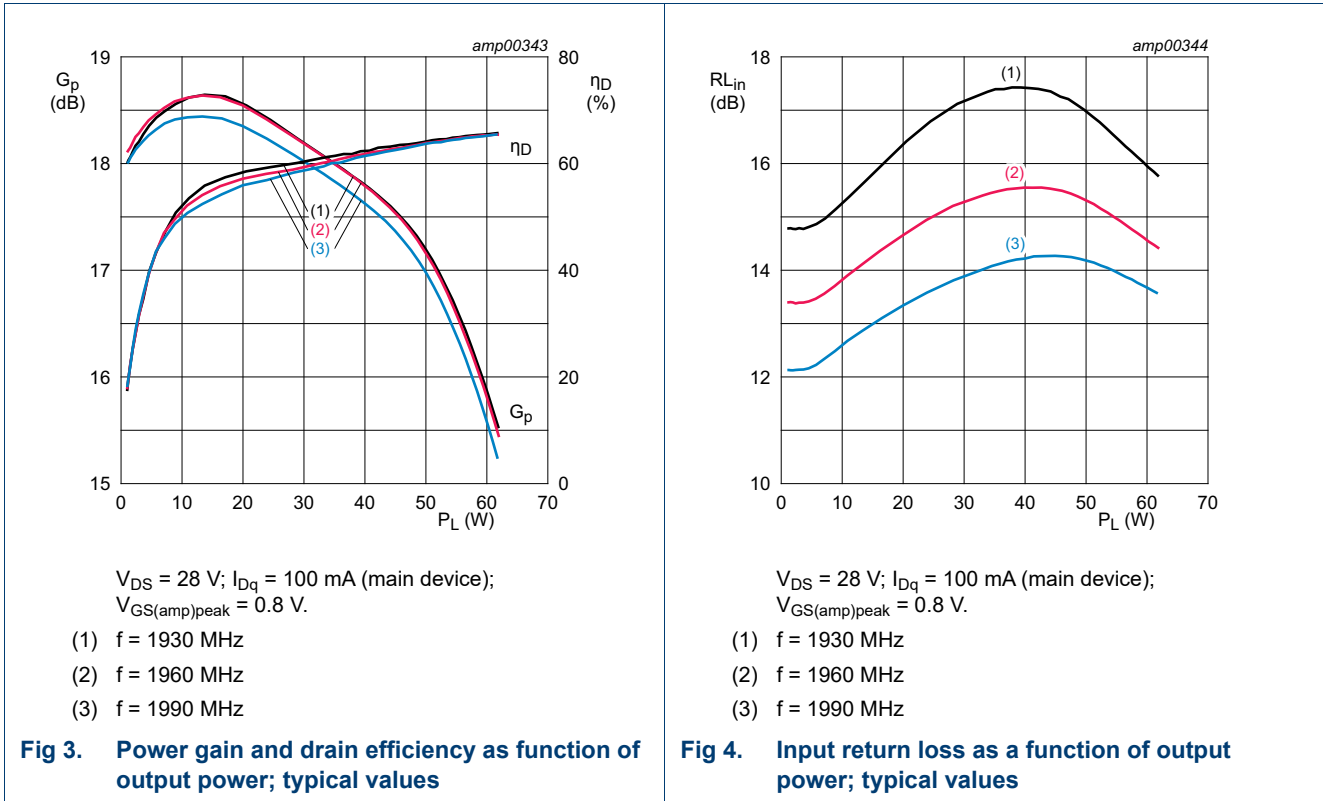
[1] American Technical Ceramics type 600F or capacitor of same quality.

[2] Murata or capacitor of same quality.

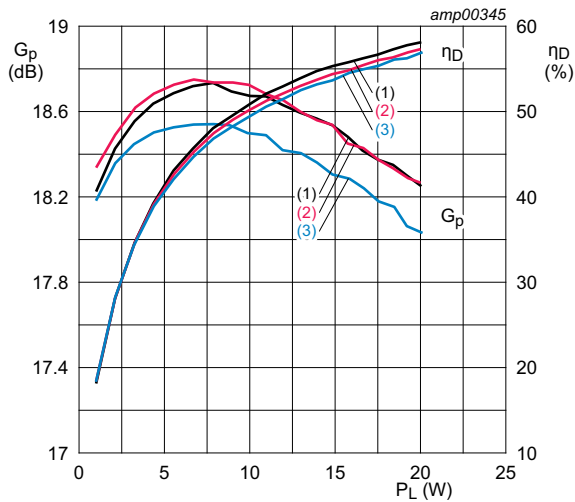


7.5 Graphical data

7.5.1 Pulsed CW

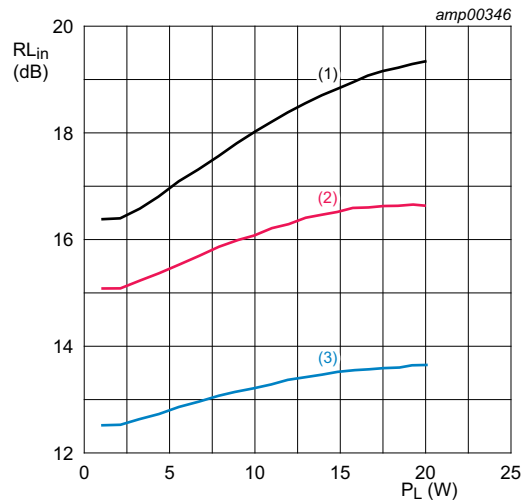


7.5.2 1-Carrier W-CDMA



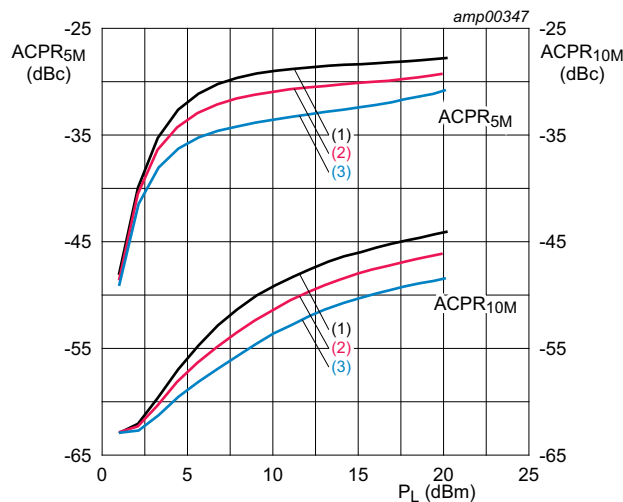
$V_{DS} = 28\text{ V}; I_{Dq} = 100\text{ mA}$  (main device);  
 $V_{GS(amp)peak} = 0.8\text{ V}$ .  
 (1)  $f = 1930\text{ MHz}$   
 (2)  $f = 1960\text{ MHz}$   
 (3)  $f = 1990\text{ MHz}$

**Fig 5. Power gain and drain efficiency as function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 100\text{ mA}$  (main device);  
 $V_{GS(amp)peak} = 0.8\text{ V}$ .  
 (1)  $f = 1930\text{ MHz}$   
 (2)  $f = 1960\text{ MHz}$   
 (3)  $f = 1990\text{ MHz}$

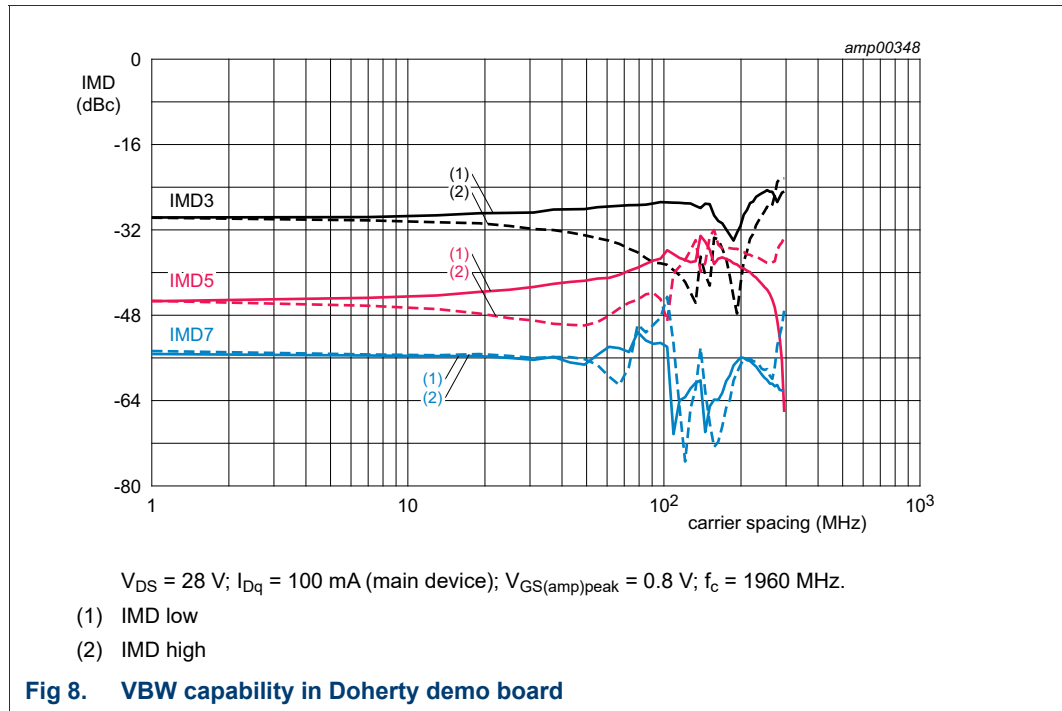
**Fig 6. Input return loss as a function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 100\text{ mA}$  (main device);  $V_{GS(amp)peak} = 0.8\text{ V}$ .  
 (1)  $f = 1930\text{ MHz}$   
 (2)  $f = 1960\text{ MHz}$   
 (3)  $f = 1990\text{ MHz}$

**Fig 7. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as function of output power; typical values**

7.5.3 2-Tone VBW



8. Package outline

Air cavity plastic earless flanged package; 6 leads

SOT1275-1

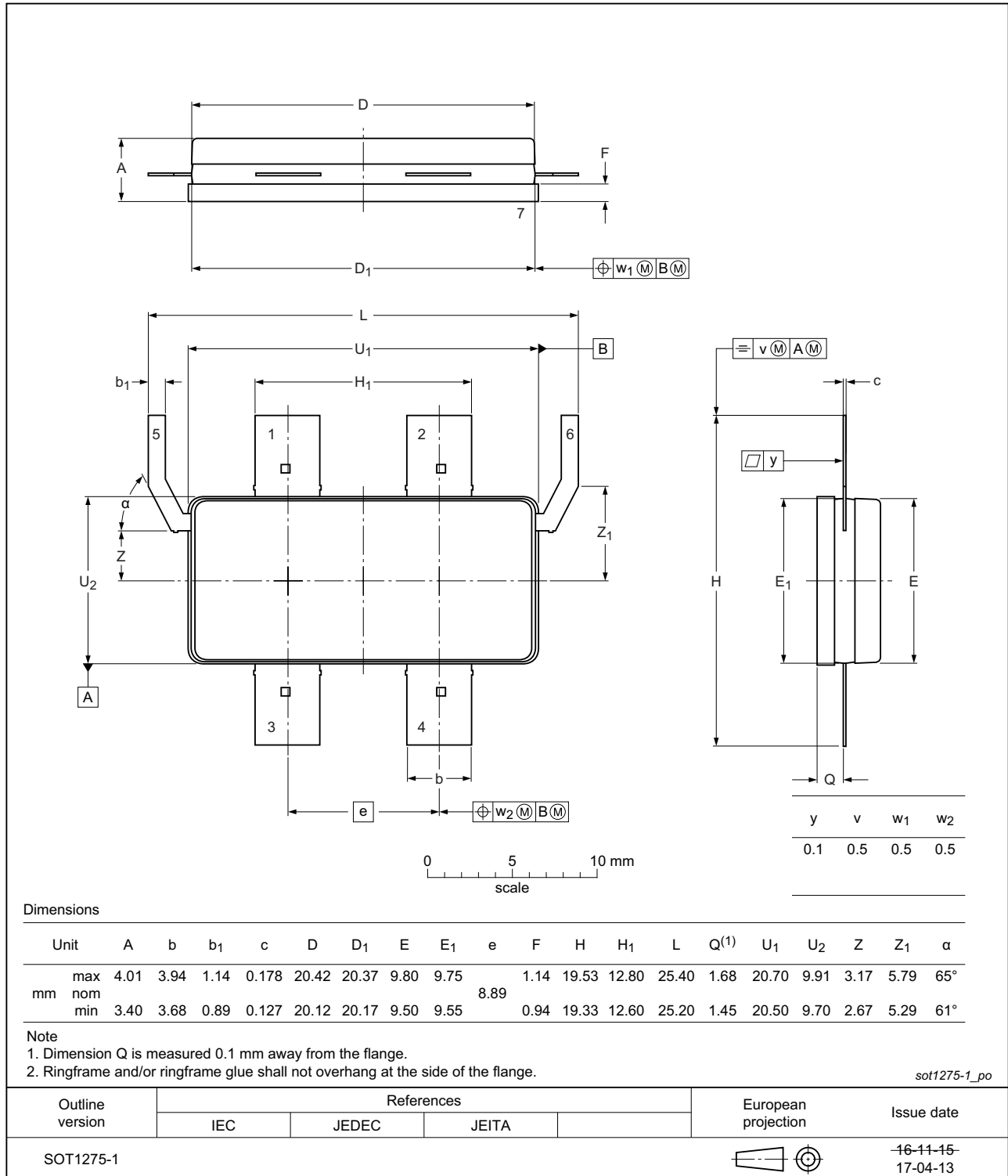


Fig 9. Package outline SOT1275-1

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 14. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 10. Abbreviations

**Table 15. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video Bandwidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

**Table 16. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G21LS-60AV v.1	20170706	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

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## 13. Contact information

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