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BLE112

DATA SHEET

Thursday, 10 December 2015

Version 1.48

VERSION HISTORY

Version	Comment
1.0	Certification information updated. Layout guide for BLE112-N added.
1.1	RF pin dimensions added
1.11	Absolute maximum supply corrected
1.2	Certification information updated
1.21	Current consumption added
1.22	Current consumption profiles added
1.23	Typo corrected on table 2
1.24	UART chapter, I/O Ports chapter, DC characteristics
1.25	Updated product codes
1.26	Note about P1_0 and P1_1 in chapter 2.1
1.27	Design check list, peripheral pull-up/pull-down requirements
1.28	Updating “Alternate” configuration table for clarity
1.29	Absolute maximum ratings: all supply nets must have the same voltage. Opamp and comparator removed from the peripherals table.
1.3	MIC Japan information updated
1.4	Updated contact information
1.41	CE info updated
1.42	TXP vs HW config added
1.43	Peripheral mapping table: analog comparator added
1.44	Product codes updates
1.45	CE info updated
1.46	Layout examples added
1.47	Contact info updated

1.48	Updated op-amp description

TABLE OF CONTENTS

BLE112 *Bluetooth®* low energy single mode module

DESCRIPTION

BLE112, *Bluetooth* low energy single mode module is a single mode device targeted for low power sensors and accessories.

BLE112 offers all *Bluetooth* low energy features: radio, stack, profiles and application space for customer applications, so no external processor is needed. The module also provides flexible hardware interfaces to connect sensors, simple user interfaces or even displays directly to the module.

BLE112 can be powered directly with a standard 3V coin cell batteries or pair of AAA batteries. In lowest power sleep mode it consumes only 400nA and will wake up in few hundred microseconds.

APPLICATIONS:

- Heart rate sensors
- Pedometers
- Watches
- Blood pressure and glucose meters
- Weight scales
- Key fobs
- Households sensors and collector devices
- Security tags
- Wireless keys (keyless go)
- Proximity sensors
- HID keyboards and mice
- Indoor GPS broadcasting devices

KEY FEATURES:

- *Bluetooth v.4.0*, single mode compliant
  - Supports master and slave modes
  - 4+ simultaneous connection in master mode
- Integrated *Bluetooth* low energy stack
  - GAP, GATT, L2CAP, SMP
  - *Bluetooth* low energy profiles
- Radio performance
  - TX power: +3dBm to -23dBm
  - RX sensitivity: -85dBm to -91dBm
- Ultra low current consumption
  - Transmit: 27mA (0dBm)
  - Sleep mode 3: 0.4uA
- Programmable 8051 processor for embedding full applications
- *Bluetooth* qualified
- CE qualified
- Modular certification for FCC, IC and KCC
- MIC Japan compatibility fully tested with ARIB STD-T66

1 BLE112 Product numbering

Product code	Description
BLE112-A-v1	BLE112 with integrated chip antenna and software version 1.0
BLE112-E-v1	BLE112 with U.FL connector and software version 1.0

2 Pinout and Terminal Description

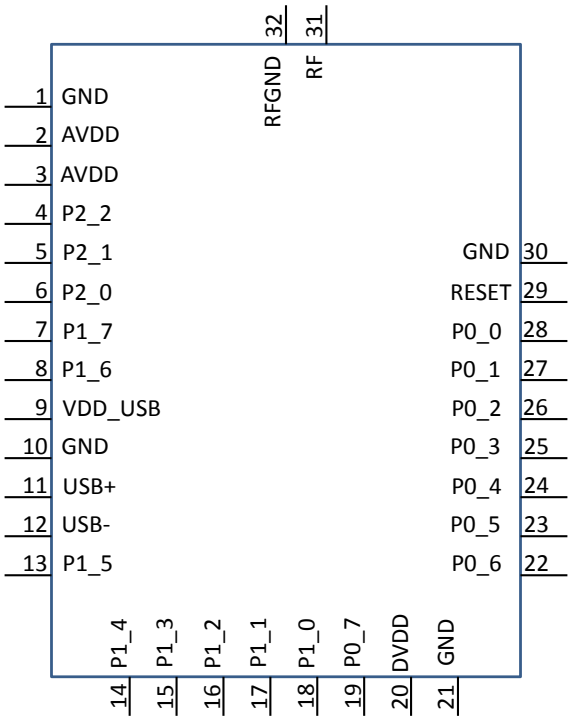

Figure 1: BLE112

	PIN NUMBER	PAD TYPE	DESCRIPTION
RESET	29		Active low reset.
GND	1, 10, 21, 30	GND	GND
RF	31	RF (*	RF output/input for BLE112-N. With BLE112-A and BLE112-E do not connect.
RFGND	32	GND	RF ground. Connected to GND internally in the module. With BLE112-A and BLE112-E leave floating or connect to a solid GND plane.
DVDD	20	Supply voltage	Supply voltage 2V - 3.6V
AVDD	2, 3	Supply voltage	Supply voltage 2V - 3.6V
VDD_USB	9	Supply voltage	Supply voltage 2V - 3.6V

*) RF pin is not connected in BLE112-A and BLE112-E. To use RF pin with BLE112-B please see the design guide.

Table 1: Supply and RF Terminal Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	DESCRIPTION
4	P2_2	Digital I/O	Configurable I/O port, See table 3
5	P2_1	Digital I/O	Configurable I/O port, See table 3
6	P2_0	Digital I/O	Configurable I/O port, See table 3
7	P1_7	Digital I/O	Configurable I/O port, See table 3
8	P1_6	Digital I/O	Configurable I/O port, See table 3
11	USB+	USB+	USB data plus
12	USB-	USB-	USB data minus
13	P1_5	Digital I/O	Configurable I/O port, See table 3
14	P1_4	Digital I/O	Configurable I/O port, See table 3
15	P1_3	Digital I/O	Configurable I/O port, See table 3
16	P1_2	Digital I/O	Configurable I/O port, See table 3
17	P1_1	Digital I/O	Configurable I/O port with 20mA driving capability, See table 3
18	P1_0	Digital I/O	Configurable I/O port with 20mA driving capability, See table 3
19	P0_7	Digital I/O	Configurable I/O port, See table 3
22	P0_6	Digital I/O	Configurable I/O port, See table 3
23	P0_5	Digital I/O	Configurable I/O port, See table 3
24	P0_4	Digital I/O	Configurable I/O port, See table 3
25	P0_3	Digital I/O	Configurable I/O port, See table 3
26	P0_2	Digital I/O	Configurable I/O port, See table 3
27	P0_1	Digital I/O	Configurable I/O port, See table 3
28	P0_0	Digital I/O	Configurable I/O port, See table 3

Table 2: Terminal Descriptions

*) BLE112 is configurable as either SPI master or SPI slave

PERIPHERAL / FUNCTION		P0								P1								P2			HARDWARE.XML Example (*
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	2	1	0	
Analog Comparator				+	-																(***
ADC		A7	A6	A5	A4	A3	A2	A1	A0												(***
USART 0 SPI (**	Alt.1			C	SS	MO	MI														<usart channel="0" mode="spi_master" alternate="1" ...
	Alt.2											MO	MI	C	SS						<usart channel="0" mode="spi_master" alternate="2" ...
USART 0 UART	Alt.1			RT	CT	TX	RX														<usart channel="0" mode="uart" alternate="1" ...
	Alt.2											TX	RX	RT	CT						<usart channel="0" mode="uart" alternate="2" ...
USART 1 SPI (**	Alt.1			MI	MO	C	SS														<usart channel="1" mode="spi_master" alternate="1" ...
	Alt.2									MI	MO	C	SS								<usart channel="1" mode="spi_master" alternate="2" ...
USART 1 UART	Alt.1			RX	TX	RT	CT														<usart channel="1" mode="uart" alternate="1" ...
	Alt.2									RX	TX	RT	CT								<usart channel="1" mode="uart" alternate="2" ...
TIMER 1	Alt.1		4	3	2	1	0														<timer index="1" alternate="1" ...
	Alt.2	3	4												0	1	2				<timer index="1" alternate="2" ...
TIMER 3	Alt.1												1	0							<timer index="3" alternate="1" ...
	Alt.2									1	0										<timer index="3" alternate="2" ...
TIMER 4	Alt.1															1	0				<timer index="4" alternate="1" ...
	Alt.2																			0	<timer index="4" alternate="2" ...
DEBUG																		DC	DD		
OBSSEL												5	4	3	2	1	0				

*) Refer to Profile Toolkit Developer Guide for detailed settings

**) SS is the slave select signal when BLE113 is set as SPI slave. When set as SPI master, any available I/O can be used as chip select signal of BLE113

***) The analog comparator and the ADC will be turned on automatically when taken in use and the configuration is done using API (Application Programming Interface). Refer to Bluetooth Smart Software API Reference

Table 3:Peripheral I/O Pin Mapping

2.1 I/O Ports

Each I/O port, except pins P1_0 and P1_1, can be configured as an input with either internal pull-up or pull-down, or tri-state. Pull-down or pull-up can only be configured to whole port, not individual pins. Unused I/O pins should have defined level and not be floating. To avoid excessive leakage current P1_0 and P1_1 must be configured either as outputs or as inputs using external pull-up or pull-down resistors. See the Profile Toolkit developer guide for more information about the configuration. During reset the I/O pins are configured as inputs with pull-ups. P1_0 and P1_1 are inputs but do not have pull-up or pull-down.

The pins configured as peripheral I/O signals do not have pull-up/pull-down capability, even if the peripheral function is an input. In power modes PM1, PM2, and PM3, the I/O pins retain the I/O mode and output value (if applicable) that was set when PM1/PM2/PM3 was entered. All the IO's set as input must have an external pull-up or pull-down resistor to avoid excessive leakage current.

2.2 UART

UART baud rate can be configured up 2 Mbps. See the Profile Toolkit developer guide for more information. Following table lists commonly used baud rates for BLE112

Baud rate (bps)	Error (%)
2400	0.14
4800	0.14
9600	0.14
14 400	0.03
19 200	0.14
28 800	0.03
38 400	0.14
57 600	0.03
76 800	0.14
115 200	0.03
230 400	0.03

Table 4: Commonly used baud rates for BLE112

2.3 Electrical Characteristics

2.4 Absolute Maximum Ratings

Note: These are absolute maximum ratings beyond which the module can be permanently damaged. These are not maximum operating conditions. The maximum recommended operating conditions are in the table 6.

Rating	Min	Max	Unit
Storage Temperature	-40	85	°C
AVDD,DVDD, VDD_USB (*	-0.3	3.9	V
Other Terminal Voltages	VSS-0.4	VDD+0.4	V

*) All supply nets must have the same voltage

Table 5: Absolute Maximum Ratings

2.5 Recommended Operating Conditions

Rating	Min	Max	Unit
Operating Temperature Range	-40	85	°C
AVDD, DVDD, VDD_USB (*	2.0	3.6	V

*) Supply voltage noise should be less than 10mVpp. Excessive noise at the supply voltage will reduce the RF performance.

Table 6: Recommended Operating Conditions

2.6 DC Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.5			V
Logic-0 input current	Input equals 0V	-50		50	nA
Logic-1 input current	Input equals VDD	-50		50	nA
I/O pin pull-up and pull-down resistors			20		kΩ
Logic-0 output volatge, 4 mA pins	Output load 4 mA			0.5	V
Logic-1 output voltage, 4 mA pins	Outoput load 4 mA	2.4			V

For detailed I/O terminal characteristic and timings refer to the CC2540 datasheet available in (http://www.ti.com/lit/ds/symlink/cc2540.pdf)

2.7 Current Consumption

Power mode	Min	Typ	Max	Unit
Active mode TX 2 dBm			36	mA
Active mode TX -2 dBm			30	mA
Active mode TX -6 dBm			28	mA
Active mode RX			25	mA
Power mode 1		235		uA
Power mode 2		0.9		uA
Power mode 3		0.4		uA

Table 7: Current consumption of BLE112

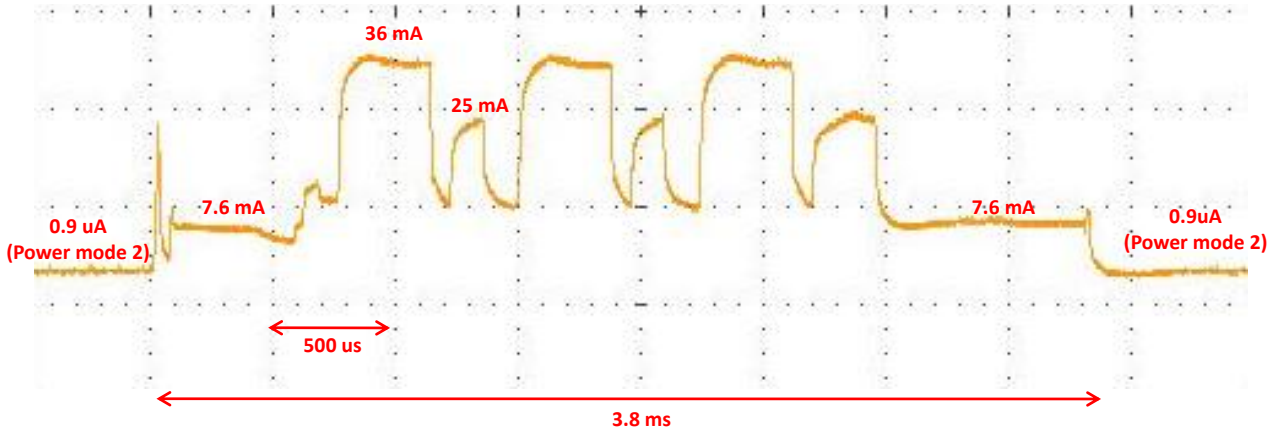

Figure 2: Typical current consumption profile during advertising in slave mode

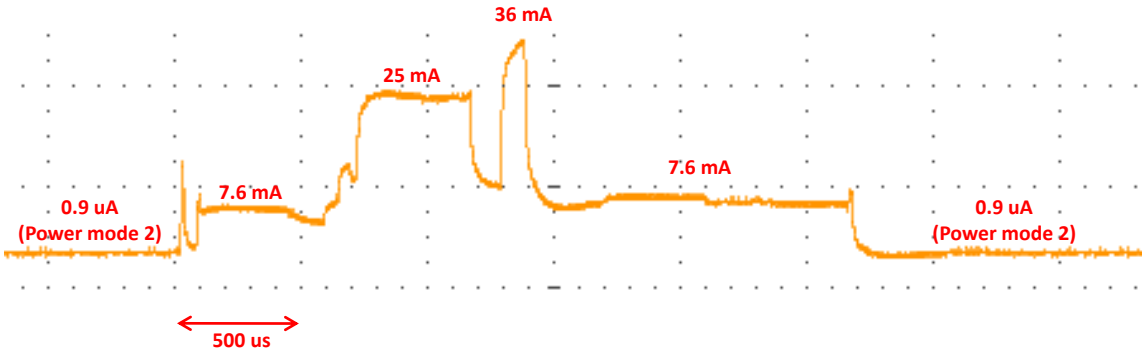

Figure 3: Typical current consumption profile during data connection in slave mode

2.8 RF Characteristics

2.8.1 TX Power vs HW Configuration

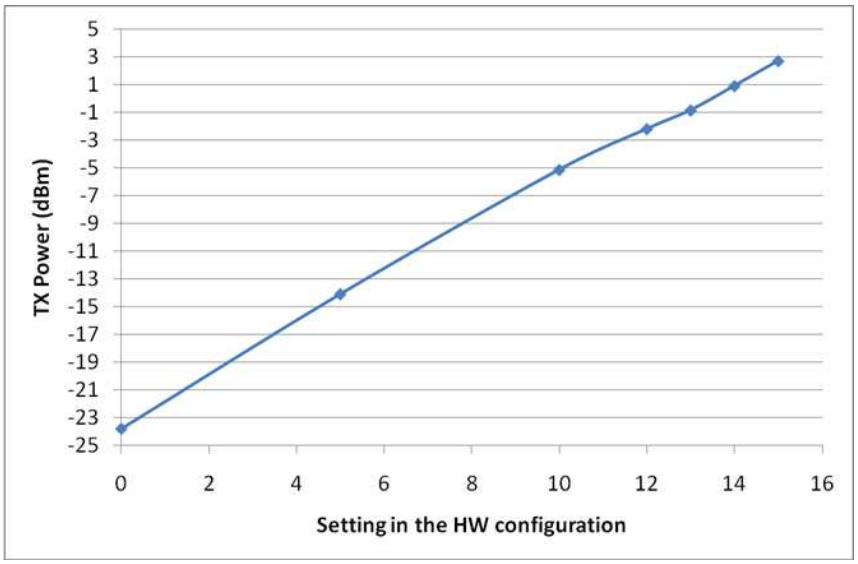

Figure 4: TXP vs HW Configuration

2.8.2 Antenna characteristics

The antenna radiation pattern is depends on the mother board layout. Following characteristics are measured from a test board based on the layout guide given in chapter 5.3.

- Efficiency 33% (-4.8 dB)
- Peak gain 0 dBi

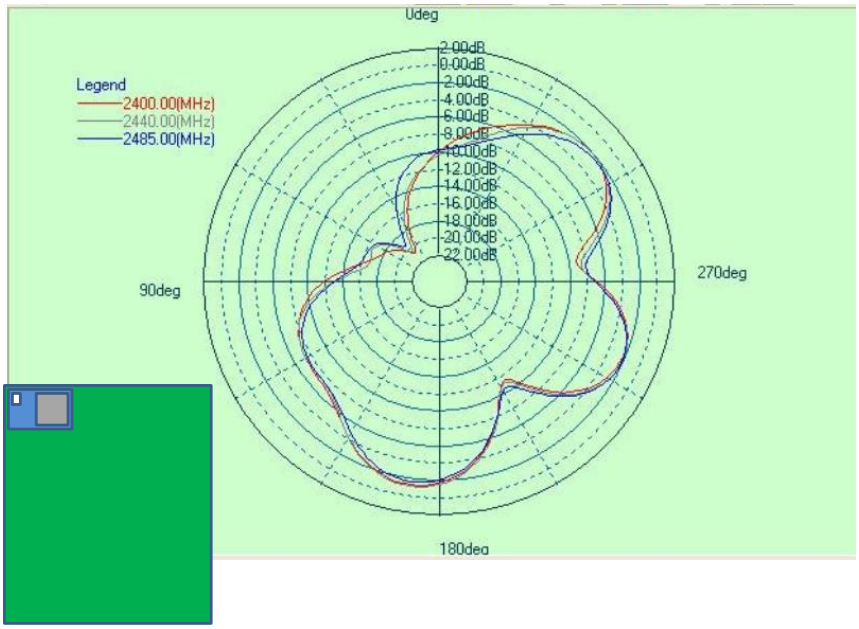

Figure 5: Radiation pattern of BLE112, top view

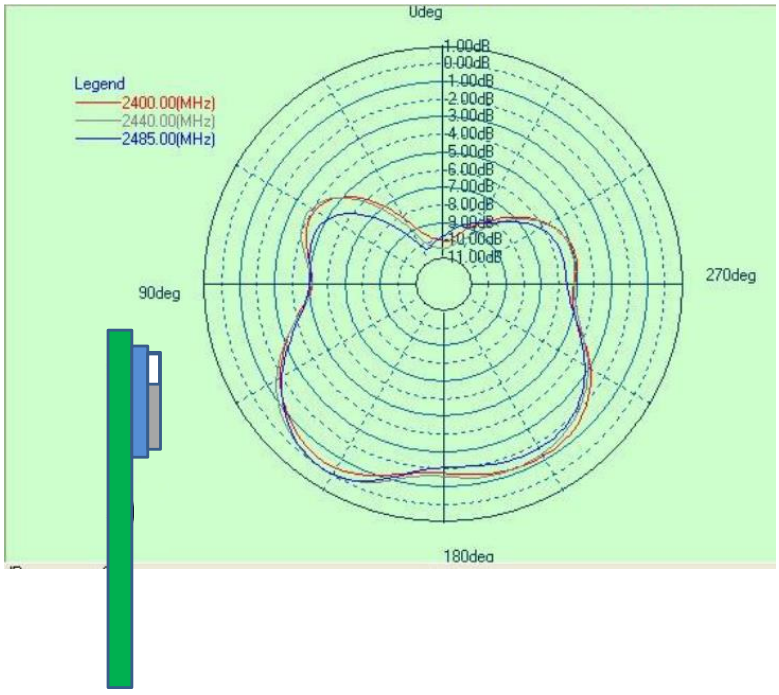

Figure 6: Radiation pattern of BLE112, front view

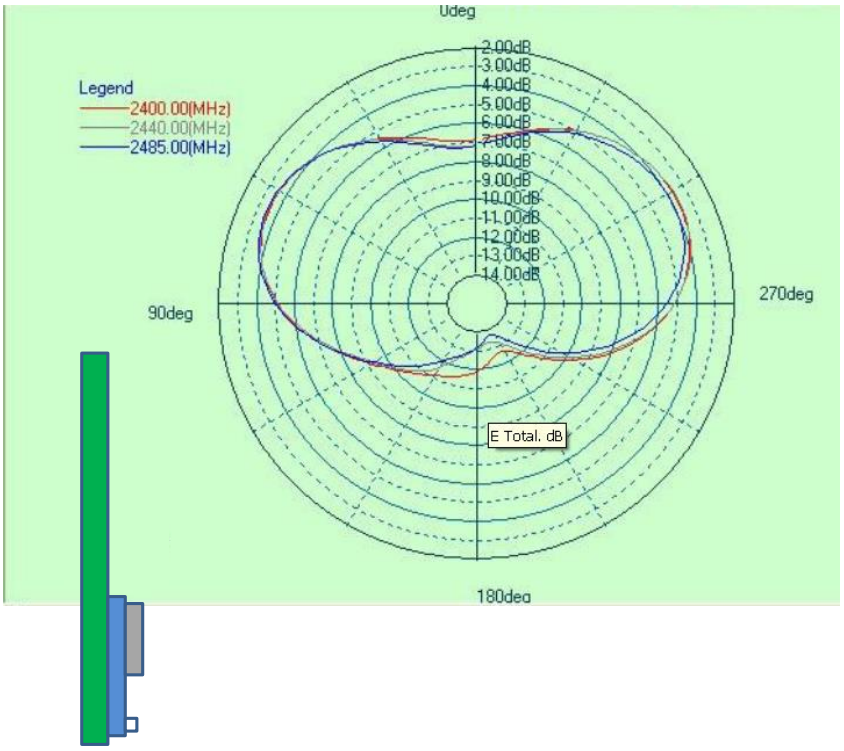

Figure 7: Radiation pattern of BLE112, side view

3 Physical Dimensions

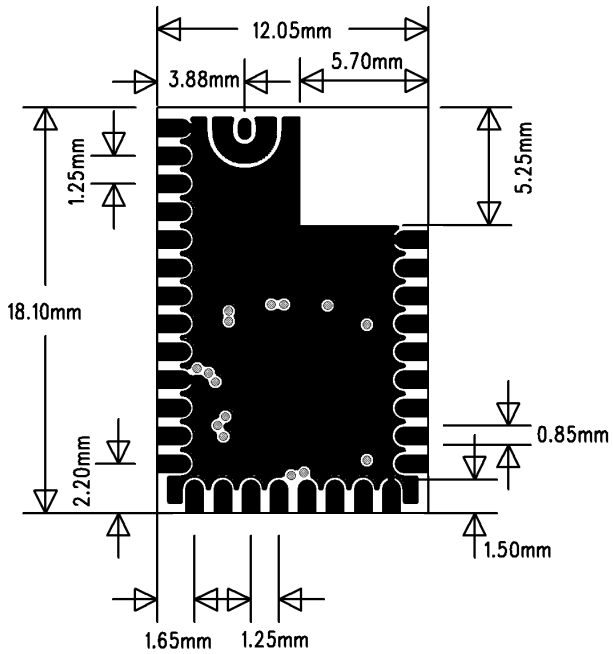

Figure 8: Physical dimensions and pinout (top view)

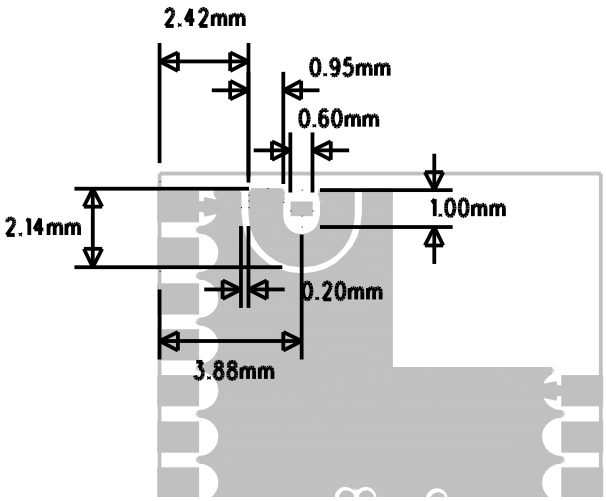

Figure 9: Dimensions for the RF pin

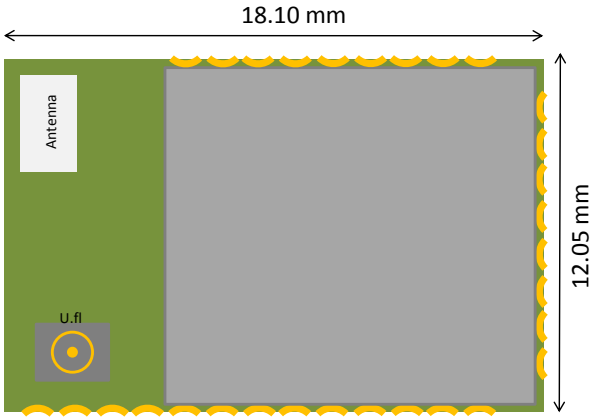

Figure 10: Physical dimensions (top view)

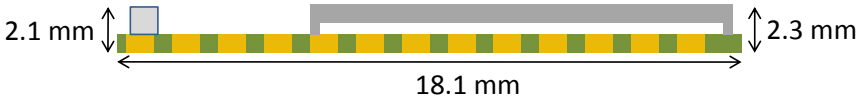

Figure 11: Physical dimensions (side view)

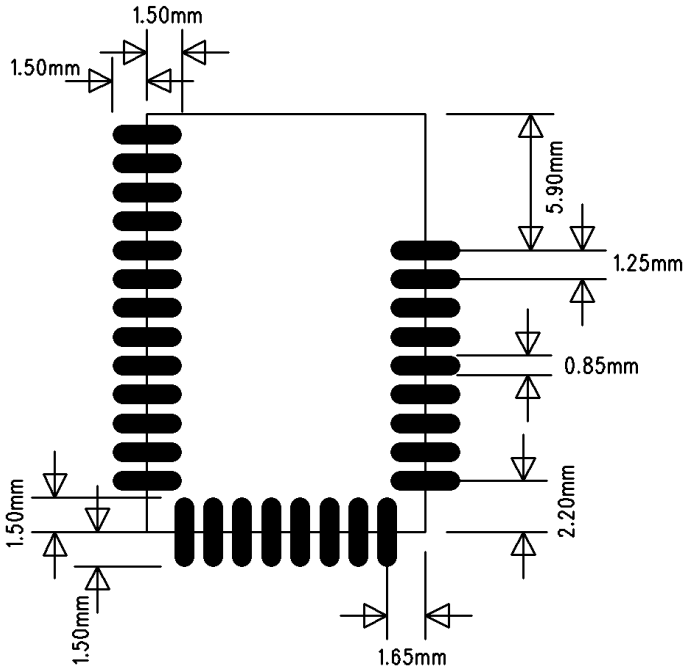

Figure 12: Recommended land pattern for BLE112-A and BLE112-E

4 Power-On Reset and Brownout Detector

BLE112 includes a power-on reset (POR), providing correct initialization during device power on. It also includes a brownout detector (BOD) operating on the regulated 1.8-V digital power supply only. The BOD protects the memory contents during supply voltage variations which cause the regulated 1.8-V power to drop below the minimum level required by digital logic, flash memory, and SRAM. When power is initially applied, the POR and BOD hold the device in the reset state until the supply voltage rises above the power-on-reset and brownout voltages.

5 Design Guidelines

5.1 General Design Guidelines

BLE112 can be used directly with a coin cell battery. Due to relatively high internal resistance of a coin cell battery it is recommended to place a 100uF capacitor in parallel with the battery. The internal resistance of a coin cell battery is initially in the range of 10 ohms but the resistance increases rapidly as the capacity is used. Basically the higher the value of the capacitor the higher is the effective capacity of the battery and thus the longer the life time for the application. The minimum value for the capacitor depends on the end application and the maximum transmit power used. The leakage current of a 100uF capacitor is in the range of 0.5 uA to 3 uA and generally ceramic capacitors have lower leakage current than tantalum or aluminum electrolytic capacitors.

Optionally TI's TPS62730 can be used to reduce the current consumption during TX/RX and data processing stages. TPS62730 is an ultra low power DC/DC converter with by-pass mode and will reduce the current consumption during transmission nominally by ~20% when using 3V coin cell battery.

A ferrite bead is recommended to be used to filter any excessive noise in the power supply lines to guarantee the radio performance.

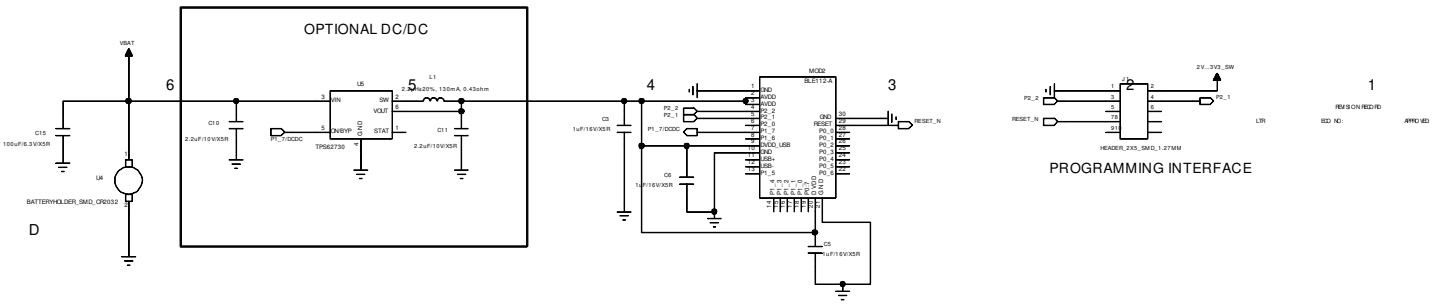

Figure 13: Example schematic for BLE112 with a coin cell battery

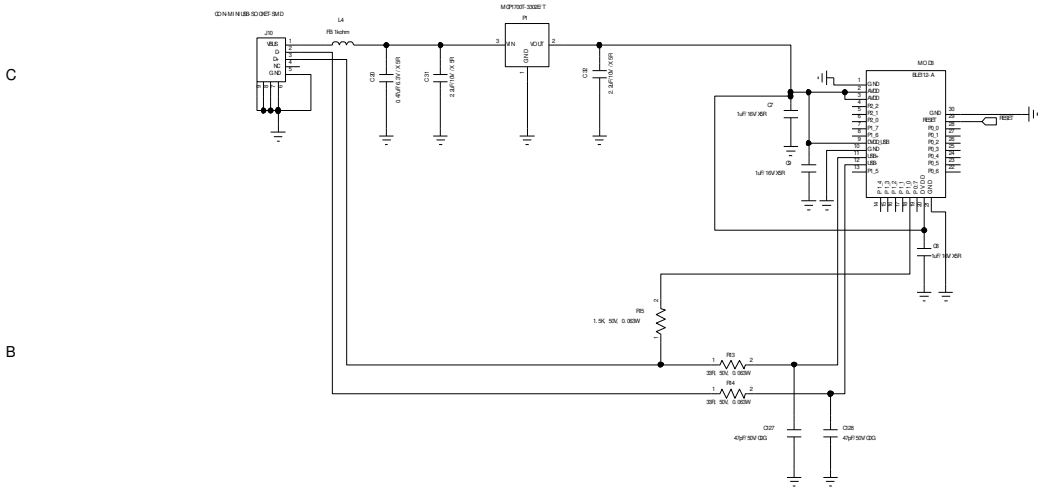

Figure 14: Example schematic for BLE112 with USB

5.2 Layout Guide Lines

Use good layout practices to avoid excessive noise coupling to supply voltage traces or sensitive analog signal traces. If using overlapping ground planes use stitching vias separated by max 3 mm to avoid emission from the edges of the PCB. Connect all the GND pins directly to a solid GND plane and make sure that there is a low impedance path for the return current following the signal and supply traces all the way from start to the end.

A good practice is to dedicate one of the inner layers to a solid GND plane and one of the inner layers to supply voltage planes and traces and route all the signals on top and bottom layers of the PCB. This arrangement will make sure that any return current follows the forward current as close as possible and any loops are minimized.

Figure 15: Typical 4-layer PCB construction

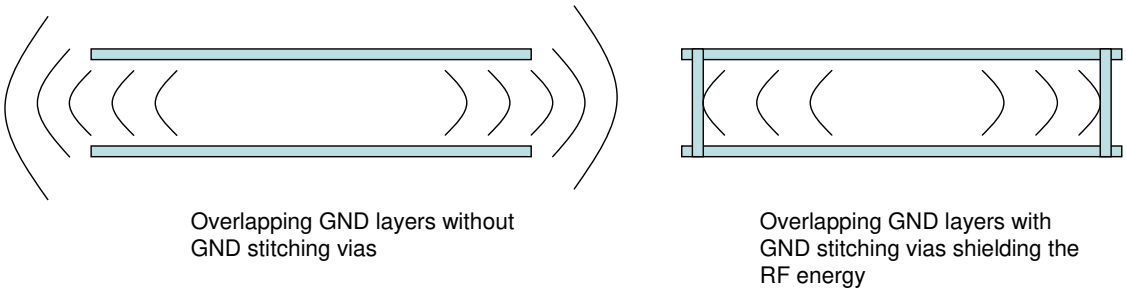

Figure 16: Use of stitching vias to avoid emissions from the edges of the PCB

5.3 BLE112-A Layout Guide

For optimal performance of the antenna place the module at the corner of the PCB as shown in the Figure 17. Do not place any metal (traces, components, battery etc.) within the clearance area of the antenna. Connect all the GND pins directly to a solid GND plane. Place the GND vias as close to the GND pins as possible. Use good layout practices to avoid any excessive noise coupling to signal lines or supply voltage lines. Avoid placing plastic or any other dielectric material closer than 5 mm from the antenna. Any dielectric closer than 5 mm from the antenna will detune the antenna to lower frequencies.

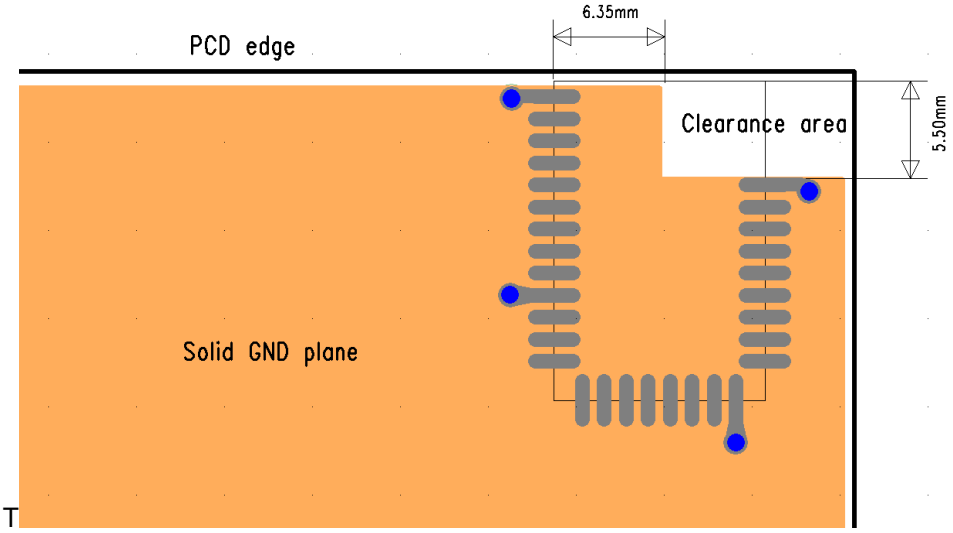

Figure 17: Recommended layout for BLE112-A

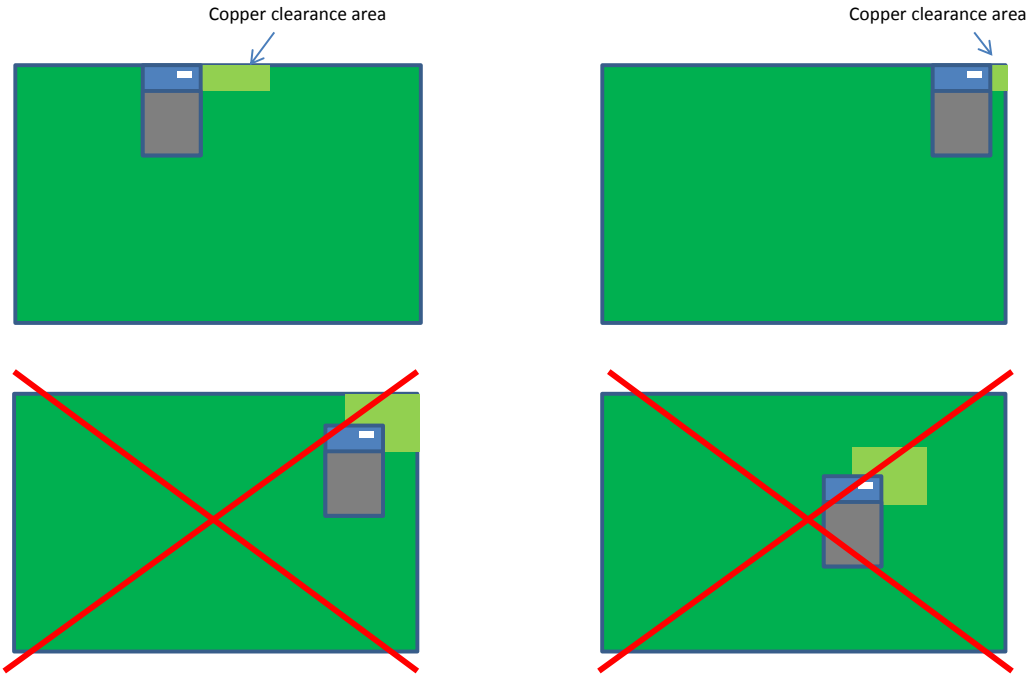

Figure 18: Layout examples for BLE112

5.4 BLE112-N Layout Guide

Use 50 ohm transmission line to trace the signal from RF pin to an external RF connector. Figure 19 shows a layout example for BLE112-N with an external SMA connector.

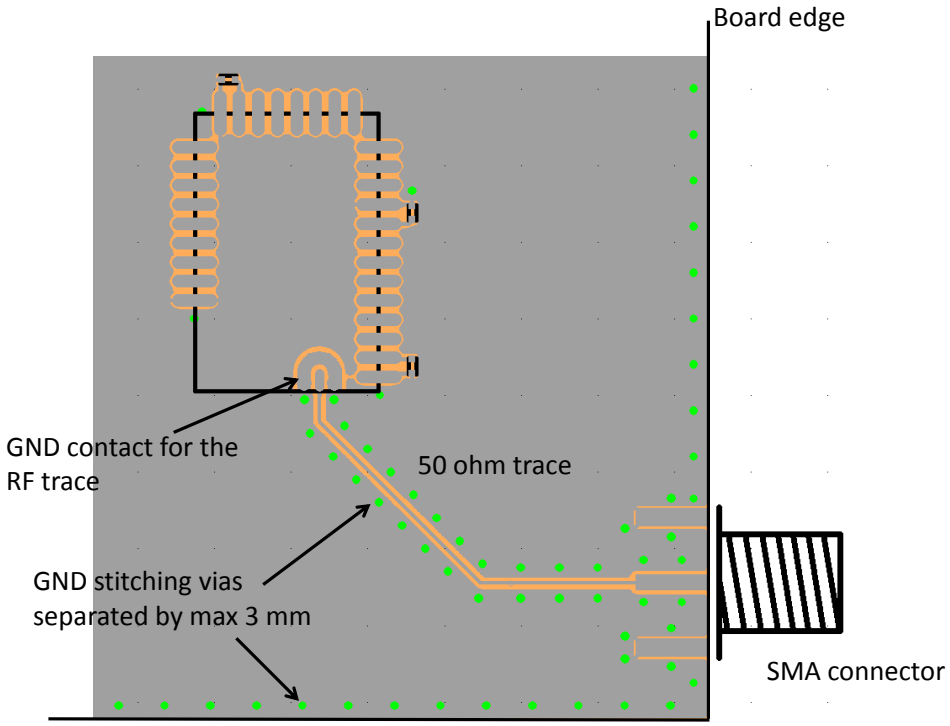

Figure 19: Example layout for BLE112-N

A transmission line impedance calculator, such as TX-Line made by AWR, can be used to approximate the dimensions for the 50 ohm transmission line. Figure 20 shows an example for two different 50 ohm transmission lines.

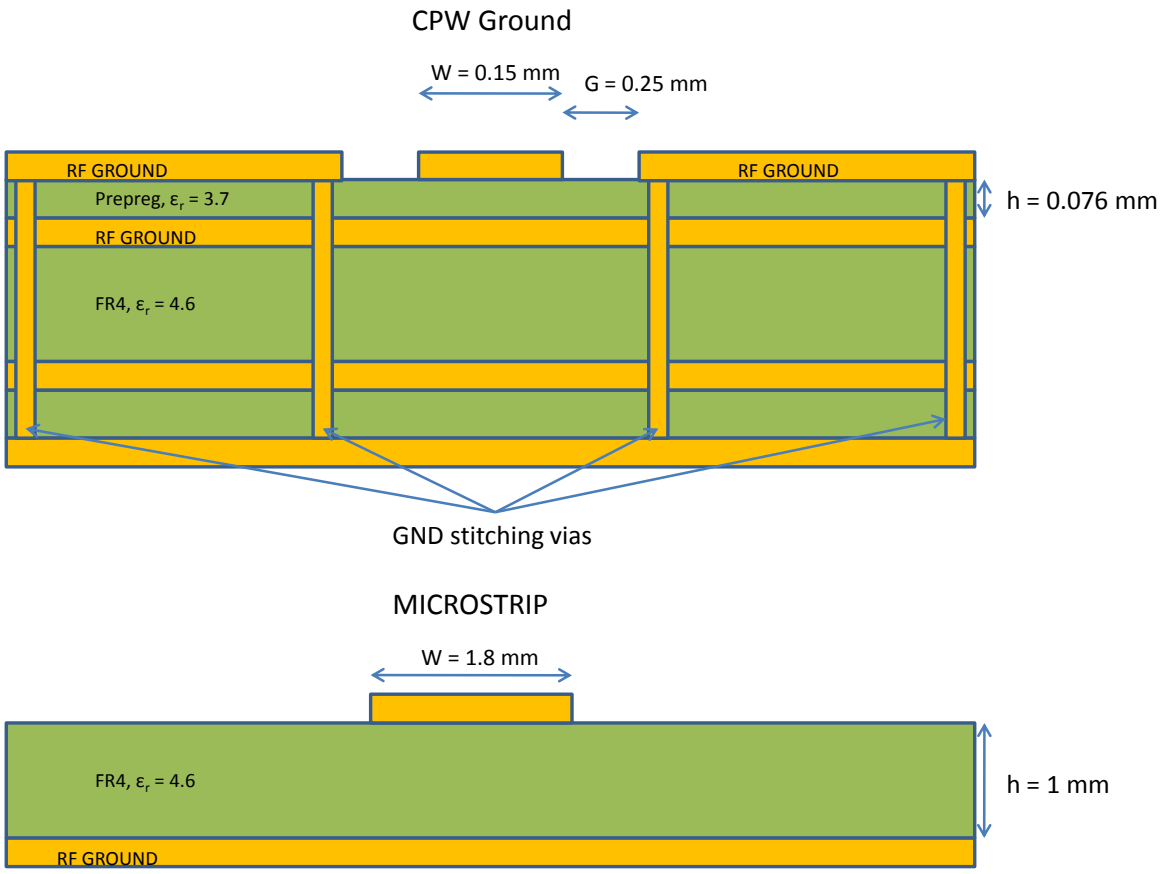

Figure 20: Example cross section of two different 50 ohm transmission line

5.5 Design Check List

- Antenna is placed at the edge of a PCB, preferably to a corner
- Antenna has sufficient clearance area around it and it is not covered by metal
- All the GND pins are connected to a solid GND plane
- All the IOs are in a known state and there are no leakage paths from the IOs
    - UART and SPI inputs must have external pull-up or pull-down
    - P1_0 and P1_1 must have either external pull-up or pull-down or configured as output
- TX power is set not higher than required for each application
- By-pass capacitor (47 uF… 100uF) is placed parallel with a coin cell battery to compensate the high series resistance of a coin cell
- Current test point is placed to measure the sleep current

6 Soldering Recommendations

BLE112 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Bluegiga Technologies will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

- Refer to technical documentations of particular solder paste for profile configurations
- Avoid using more than one flow.
- Reliability of the solder joint and self-alignment of the component are dependent on the solder volume. Minimum of 150μm stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.
- A low residue, “no clean” solder paste should be used due to low mounted height of the component.

7 Block diagram

BLE112 is based on TI's CC2540 chip. Embedded 32 MHz and 32.678 kHz crystals are used for clock generation. Matched balun and low pass filter provide optimal radio performance with extremely low spurious emissions. Small ceramic chip antenna gives good radiation efficiency even when the module is used in layouts with very limited space.

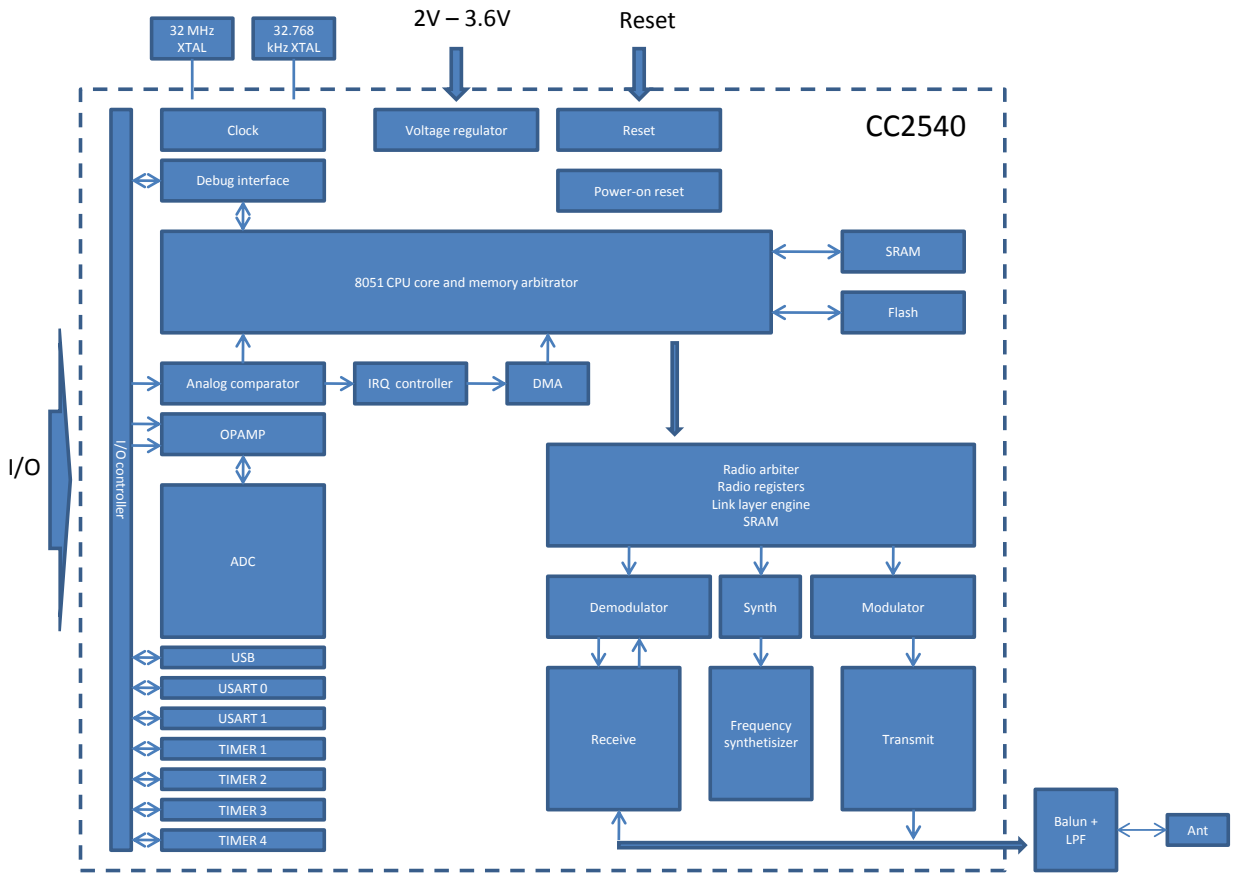

Figure 21: Simplified block diagram of BLE112

CPU and Memory

The 8051 CPU core is a single-cycle 8051-compatible core. It has three different memory access buses (SFR, DATA, and CODE/XDATA), a debug interface, and an 18-input extended interrupt unit.

The memory arbiter is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The SFR bus is a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.