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BLE121LR

DATA SHEET

Tuesday, 09 September 2014

Version 1.2

bluegiga

VERSION HISTORY

Version	Comment
1.1	First release
1.2	Standard gain mode option for the receiver added. Figure 22 corrected. Ceritification info updated. Footprint and PCB land pattern figures revised. Design check list added. Layout guide updated. Range chapter added.

TABLE OF CONTENTS

BLE121LR *Bluetooth®* Smart Module

DESCRIPTION

BLE121LR is a Bluetooth Smart Long Range module targeted for *Bluetooth* Smart applications where the best possible RF performance and range are required. At +8 dBm TX power and -98 dBm sensitivity BLE121LR has best-in-class RF performance and can provide *Bluetooth* Smart connectivity up to 450 meters. BLE121LR integrates all features required for a *Bluetooth* Smart application: *Bluetooth* radio, software stack and GATT based profiles. and it can also host end user applications, which means no external micro controller is required in size, price or power constrained devices. BLE121LR*Bluetooth* Smart module also has flexible hardware interfaces to connect to different peripherals or sensors. Although BLE121LR *Bluetooth* Smart Long Range Module is target for applications requiring high RF performance, it is still has relatively low power consumption and can be power using a standard 3V coin cell batteries.

APPLICATIONS:

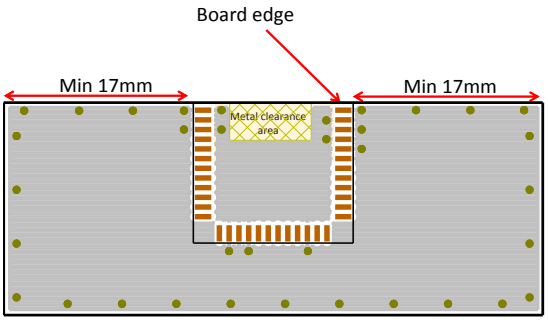
- Smart home accessories
- beacon devices
- Health and fitness sensors
- Medical sensors
- iPhone and iPad accessories
- Security and proximity tags

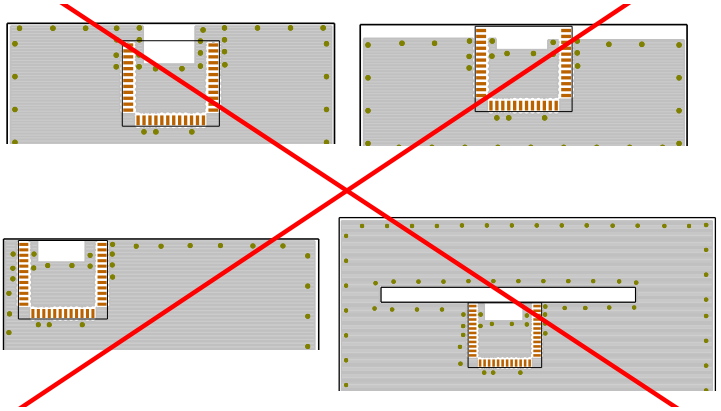
KEY FEATURES:

- *Bluetooth* v. 4.0 Single Mode Compliant
  - Master and slave modes
  - Up to eight connections
- Integrated *Bluetooth* Smart Stack
  - GAP, ATT and GATT
  - *Bluetooth* Smart profiles
- Best-in-Class RF Performance
  - Transmit power : +8 dBm
  - Receiver sensitivity: -98 dBm
  - Range up to 450 meters
- Low Current Consumption
  - Transmit: 36 mA (+8 dBm)
  - Receive: 33 mA (-98 dBm)
  - Power mode 3: 0.5 uA
- Flexible Peripheral Interfaces
  - UART and SPI
  - I2C, PWM and GPIO
  - 12-bit ADC
- Host Interfaces:
  - UART
- Programmable 8051 Processor for Stand-alone Operation
  - Simple Bluegiga BGScript™ scripting language for quick application development
  - Bluegiga Profile Toolkit™ allowing the quick development of GATT based profiles
- Dimensions: 14.7 x 13.0 x 1.8 mm
- *Bluetooth*, CE, FCC, IC, South Korea and Japan qualified

1 Design Check List

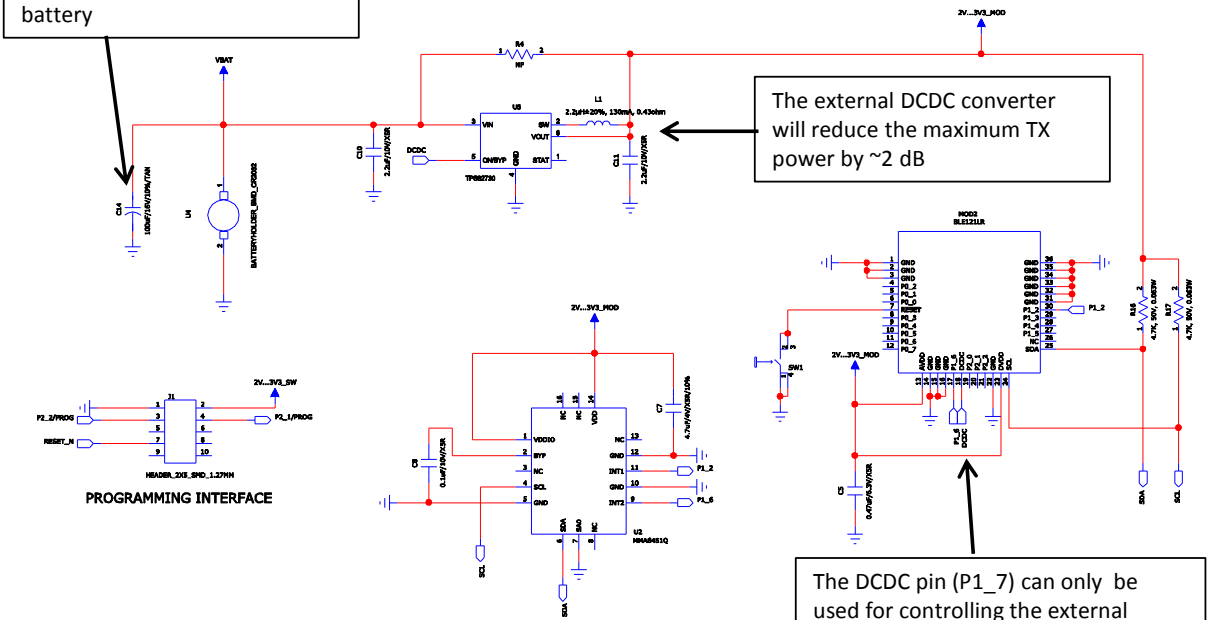
- Make sure that the programing interface (P2_, P2_2, reset) is available for debugging or FW updates
- Add test points for testing the current consumption
- Make sure that all the IO's are in a known state
- Make sure that the layout under the antenna is done as instructed





Place large capacitor in parallel with the battery to reduce the peak current drawn from the battery

The external DCDC converter will reduce the maximum TX power by ~2 dB



The DCDC pin (P1_7) can only be used for controlling the external DCDC. The operation of P1_7 must not be altered by SW.

2 BLE121LR Product numbering

Available products and product codes

Product code	Description
BLE121LR-A-M256K	BLE121LR with an embedded chip antenna and with 256k internal flash

3 Pinout and Terminal Description

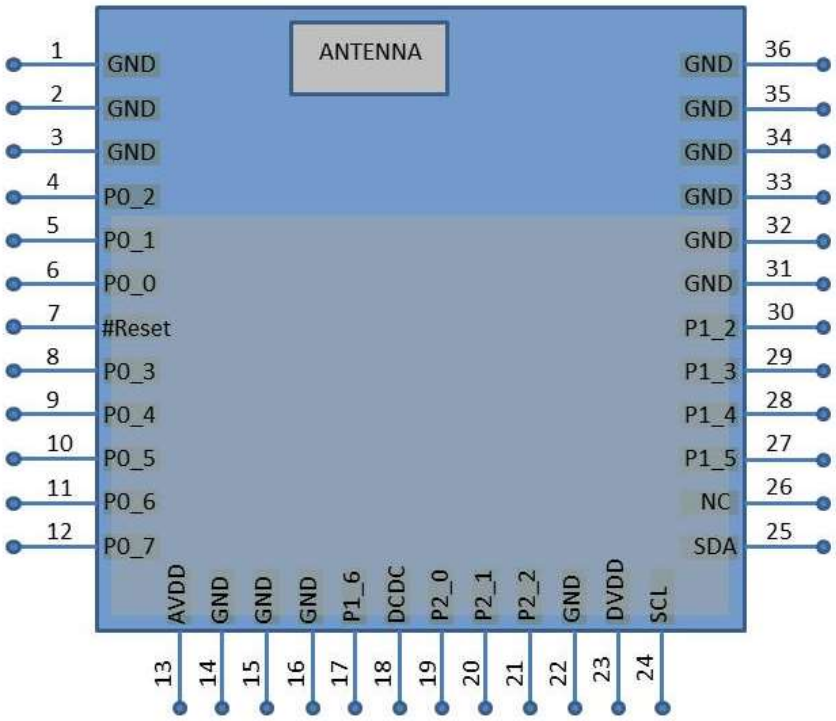


Figure 1: BLE121LR

Pin Number	Pin Name	Pad Type	Description
1-3, 14, 15, 22 31-36	GND	GND	GND
13	AVDD	Supply voltage	
23	DVDD	Supply voltage	
7	Reset	Reset	Active low reset. Internal pull-up.

Table 1: Supply and RF Terminal Descriptions

Pin Number	Pin Name	Pad Type	Description
6	P0_0	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
5	P0_1	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
4	P0_2	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
8	P0_3	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping

9	P0_4	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
10	P0_5	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
11	P0_6	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
12	P0_7	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
30	P1_2	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
29	P1_3	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
28	P1_4	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
27	P1_5	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
17	P1_6	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
19	P2_0	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
20	P2_1	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping
21	P2_2	I/O	Configurable Input/Output. See Table 4: Peripheral I/O Pin Mapping

Table 2: Configurable I/O Terminals

Pin Number	Pin Name	Pad Type	Description
24	SCL	I2C clock	
25	SDA	I2C data	
18	DCDC_CNTRL	Output	On / by-pass control for an external DCDC converter

Table 3: Non-configurable Terminals

PERIPHERAL / FUNCTION		P0								P1								P2			HARDWARE.XML Example (*
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	2	1	0	
ADC		A7	A6	A5	A4	A3	A2	A1	A0	DCDC CONTROL						RESERVED	RESERVED				
USART 0 SPI (**	Alt.1			C	SS	MO	MI														<usart channel="0" mode="spi_master" alternate="1" ...
	Alt.2											MO	MI	C	SS						<usart channel="0" mode="spi_master" alternate="2" ...
USART 0 UART	Alt.1			RT	CT	TX	RX														<usart channel="0" mode="uart" alternate="1" ...
	Alt.2											TX	RX	RT	CT						<usart channel="0" mode="uart" alternate="2" ...
USART 1 SPI (**	Alt.1			MI	MO	C	SS														<usart channel="1" mode="spi_master" alternate="1" ...
USART 1 UART	Alt.1			RX	TX	RT	CT														<usart channel="1" mode="uart" alternate="1" ...
TIMER 1	Alt.1		4	3	2	1	0														<timer index="1" alternate="1" ...
	Alt.2	3	4												0						<timer index="1" alternate="2" ...
TIMER 3	Alt.1												1	0							<timer index="3" alternate="1" ...
	Alt.2									0											<timer index="3" alternate="2" ...
TIMER 4	Alt.1																				<timer index="4" alternate="1" ...
	Alt.2																			0	<timer index="4" alternate="2" ...
DEBUG																		DC	DD		
OBSSEL												5	4	3	2						

*) Refer to BLE Configuration Guide for detailed settings

**) SS is the slave select signal when BLE121LR is set as SPI slave. When set as SPI master, any available I/O can be used as chip select signal of BLE121LR

NOTE: Pins configured as peripheral I/O signals do not have pull-up / -down capability

Table 4: Peripheral I/O Pin Mapping

3.1 I/O Ports

3.1.1 I/O Configurations

Each I/O port can be configured as an input or output. When configured as input, each I/O port can also be configured with internal pull-up, pull-down or tri-state. Pull-down or pull-up can only be configured to whole port, not individual pins. Unused I/O pins should have defined level and not be floating. See the BLE Configuration Guide for more information about the configuration.

During reset the I/O pins are configured as inputs with pull-ups.

Note: Pins configured as peripheral I/O signals do not have pull-up / -down capability

3.1.2 Reserved I/O's

The high current driving pins P1_0 and P1_1 are reserved for the internal RF front end control. These pins are not exposed in BLE121LR and they can't be used for application purposes.

P1_7 is also used for the RF front end control but as an output it can be used to control the external DCDC for lowering the peak current drawn from the battery. The function of P1_7 can't be altered. If external DCD is not used then P1_7 should be left not connected.

3.2 UART

UART baud rate can be configured up 2 Mbps. See the BLE Configuration Guide for more information. Following table lists commonly used baud rates for BLE121LR

Baud rate (bps)	Error (%)
2400	0.14
4800	0.14
9600	0.14
14 400	0.03
19 200	0.14
28 800	0.03
38 400	0.14
57 600	0.03
76 800	0.14
115 200	0.03
230 400	0.03

Table 5: Commonly used baud rates for BLE121LR

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Note: These are absolute maximum ratings beyond which the module can be permanently damaged. These are not maximum operating conditions. The maximum recommended operating conditions are in the Table 7.

Rating	Min	Max	Unit
Storage Temperature	-40	+85	°C
AVDD, DVDD	-0.3	3.9	V
Other Terminal Volatages	VSS-0.4	VDD+0.4	V

Table 6: Absolute Maximum Ratings

4.2 Recommended Operating Conditions

Rating	Min	Max	Unit
Operationg Temperature Range	-40	+85	°C
AVDD, DVDD (*,**,***	2.0	3.6	V

Table 7: Recommended Operating Conditions

*) All supply nets must have the same voltage
**) Supply voltage noise should be less than 10mVpp. Excessive noise at the supply voltage will reduce the RF performance.
***) The supply voltage has an impact on the TX power, see Figure 7.

4.3 DC Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage	DVDD =3V0	2.5			V
Logic-0 input current	Input equals 0V	-50		50	nA
Logic-1 input current	Input equals VDD	-50		50	nA
I/O pin pull-up and pull-down resistors			20		kΩ

For detailed I/O terminal characteristic and timings refer to the CC2541 datasheet available in (http://www.ti.com/lit/ds/symlink/cc2541.pdf)

Table 8: DC Characteristic

4.4 Current Consumption

Power mode	hardware.xml	Min	Typ	Max	Unit
Transmit (3V0 supply, without DCDC)	<txpower power = ”1”/> <slow clock enable = ”true”/>		25		mA
	<txpower power = ”9”/> <slow clock enable = ”true”/>		36		mA
	<txpower power = ”9”/> <slow clock enable = ”false”/>		39		mA
Transmit (With DCDC)	<txpower power = ”9”/> <slow clock enable = ”true”/>		32 **		mA
	<txpower power = ”9”/> <slow clock enable = ”false”/>		35 **		mA
Receive	<slow clock enable = ”true”/>		28		mA
	<slow clock enable = ”false”/>		33		mA
Power mode 1	<sleeposc enable="true" ppm="30" />		2.7		mA
Power mode 2	<sleeposc enable="true" ppm="30" />		1.3		µA
Power mode 3	***		0.5		µA

**) Using DCDC reduces transmit power by ~2 dB and thus lowers also the peak current drawn by the module

***) To enter PM1 and PM2 sleep oscillator must be enabled in the hardware.xml. PM3 is not dependent on the sleep clock. The module will enter PM3 automatically when there is no activity which would require clock. PM3 can be disabled in hardware.xml, for example <sleep enable=“true” max_mode=”2” />

Figure 2: BLE121LR TX peak current as a function of the setting in the HW configuration file

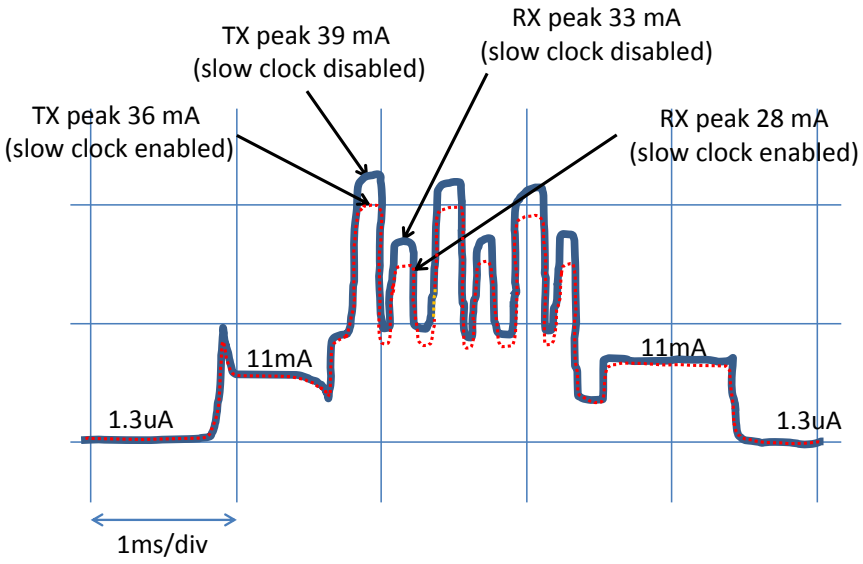


Figure 3: Typical current consumption profile while advertising

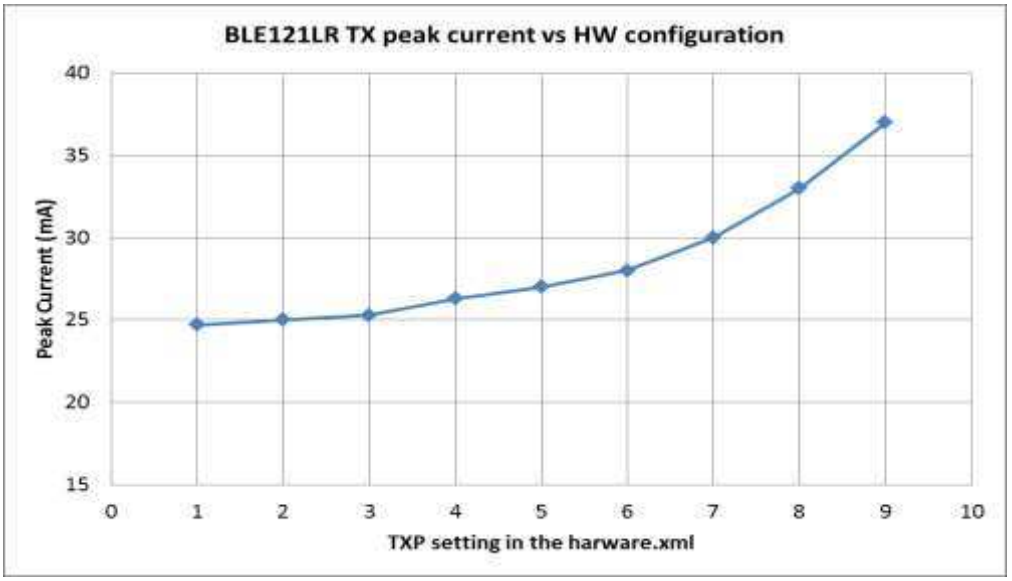


Figure 4: BLE121LR TX peak current as a function of hardware.xml TXP setting (Example: `<txpower power="9" bias="5" />`)

4.4.1 Current Consumption When Using TPS62730 DCDC Converter

TPS62730 DCDC converter provides 20% reduction to the peak current drawn from 3.0V supply and 15% reduction to the peak current drawn from 2.7V supply. This is achieved by converting higher power supply down to 2.1V supply with a switching mode regulator. The module turns the DCDC on when the processor is active and off (by-pass mode) when the processor is not active.

Because the TX power of BLE121LR depends on the supply voltage, the TX power is reduced when using TPS62730 DCDC converter. The reduced TX power in turn reduces the peak current drawn by the module. Thus when using TPS62730 with BLE121LR from 3.0V supply, the peak current is reduced in total by:

- ~4 mA because of lower TX power
- -20% because of the switching mode regulator converting from 3.0V down to 2.1V

➔ Peak current drawn from 3.0V supply in total (Max TXP, slow clock enabled):
(36 mA – 4 mA) * 0.8 = 25.6 mA

4.5 RF Characteristics

Rating	Min	Typ	Max	Unit
Transmit power		8		dBm
Transmit power variation within BT band		1	1.8	dB
Transmit power variation within the temperature range		+/-1.5		dB
Sensitivity (Default, high gain mode, PER 30.8%)		-98		dBm
Sensitivity (standard gain mode, PER 30.8%) (*		-92		dBm

*) Standard gain mode can be set using an API command. Please refer to the Bluetooth Smart Software API Reference document.

Figure 5: BLE121LR RF characteristics

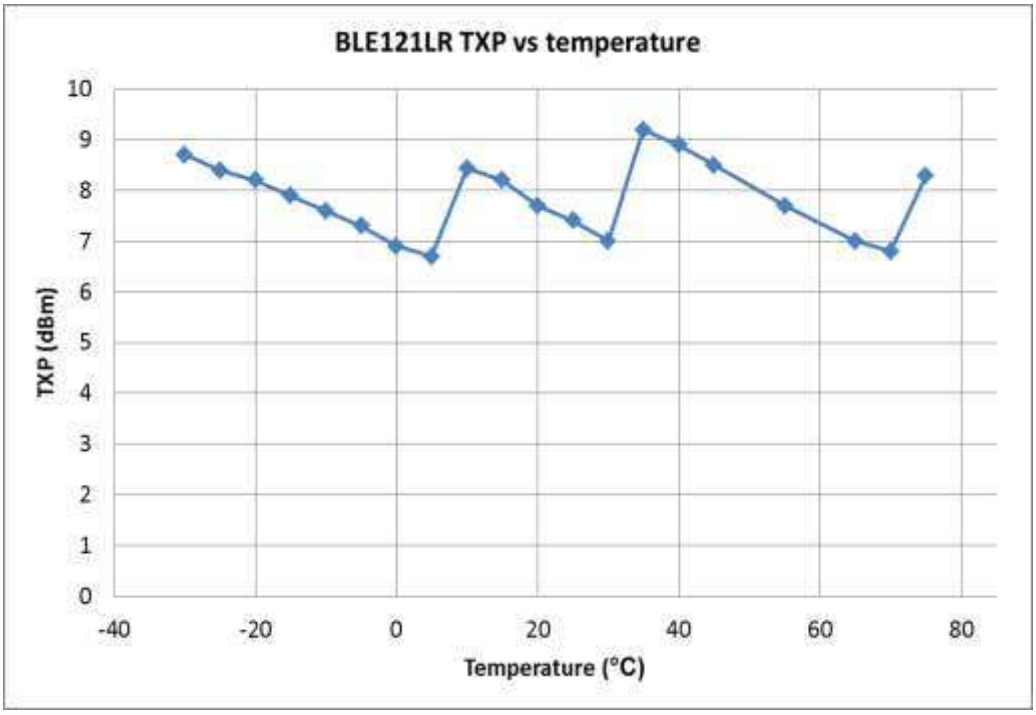


Figure 6: Typical transmit power as a function of temperature

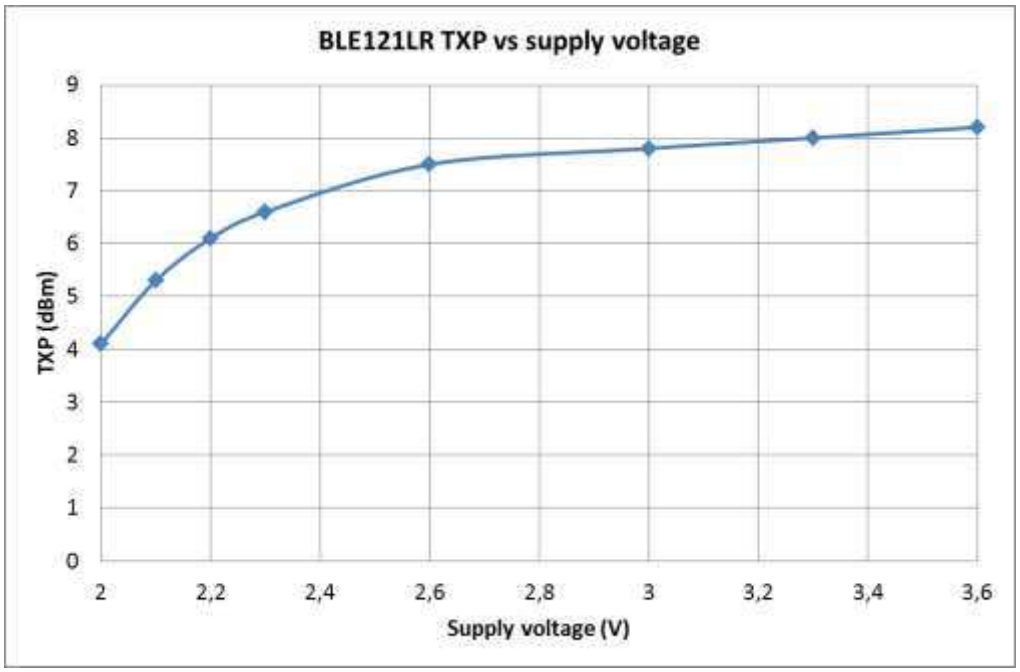


Figure 7: BLE121LR transmit power as a function of supply voltage

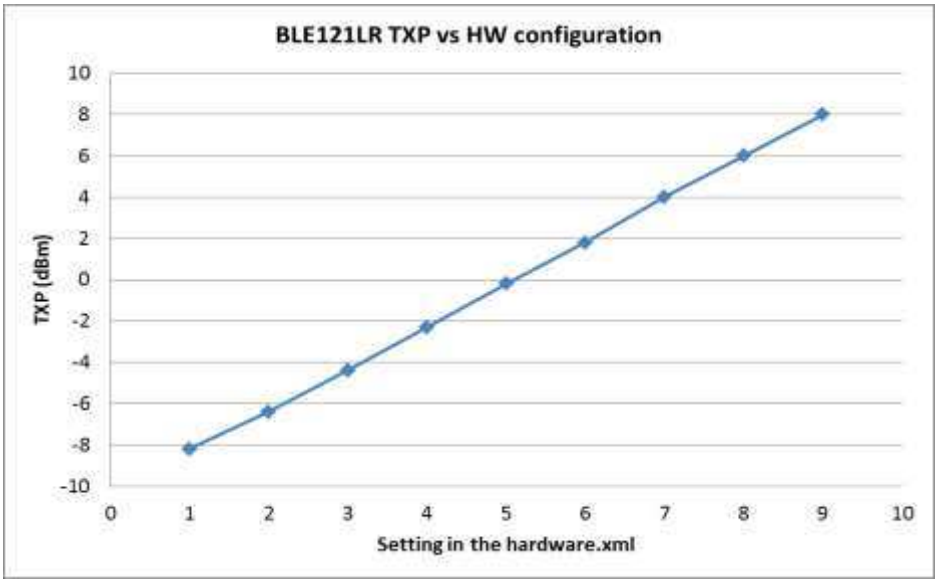


Figure 8: BLE121LR TX power as a function of the setting in the HW configuration file (Example: `<txpower power="9" bias="5" />`)

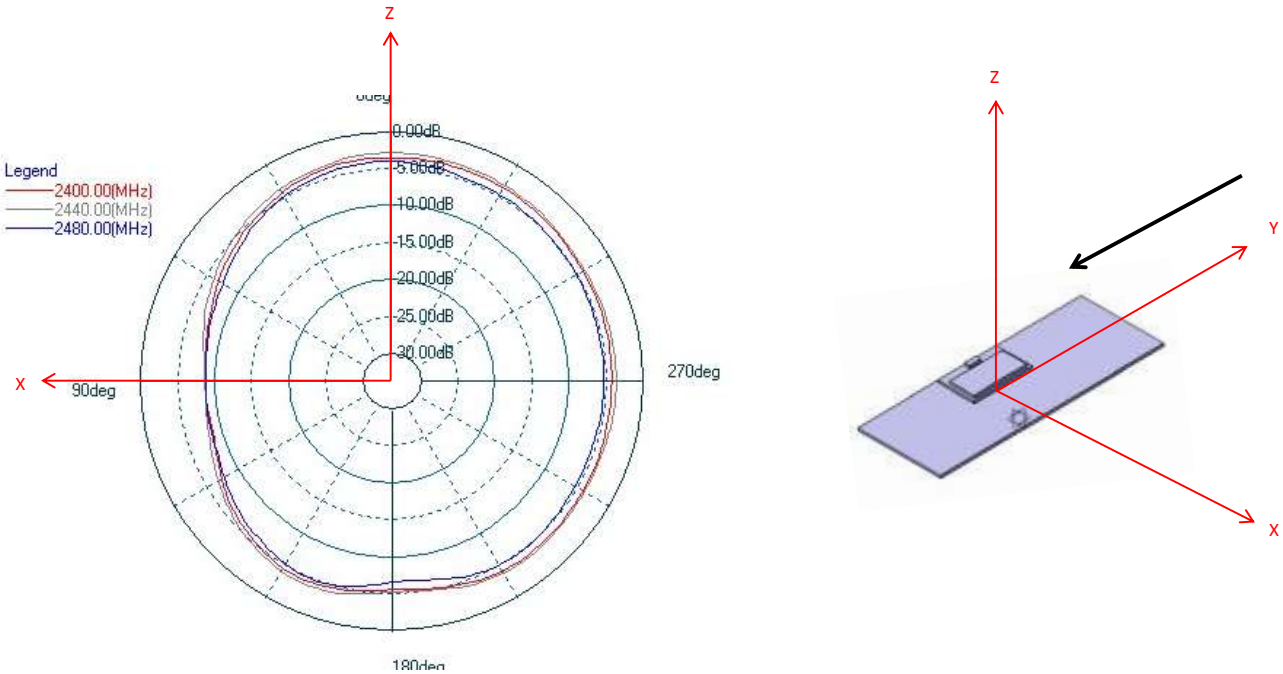


Figure 9: Radiation pattern of BLE121LR when mounted to a carrier board

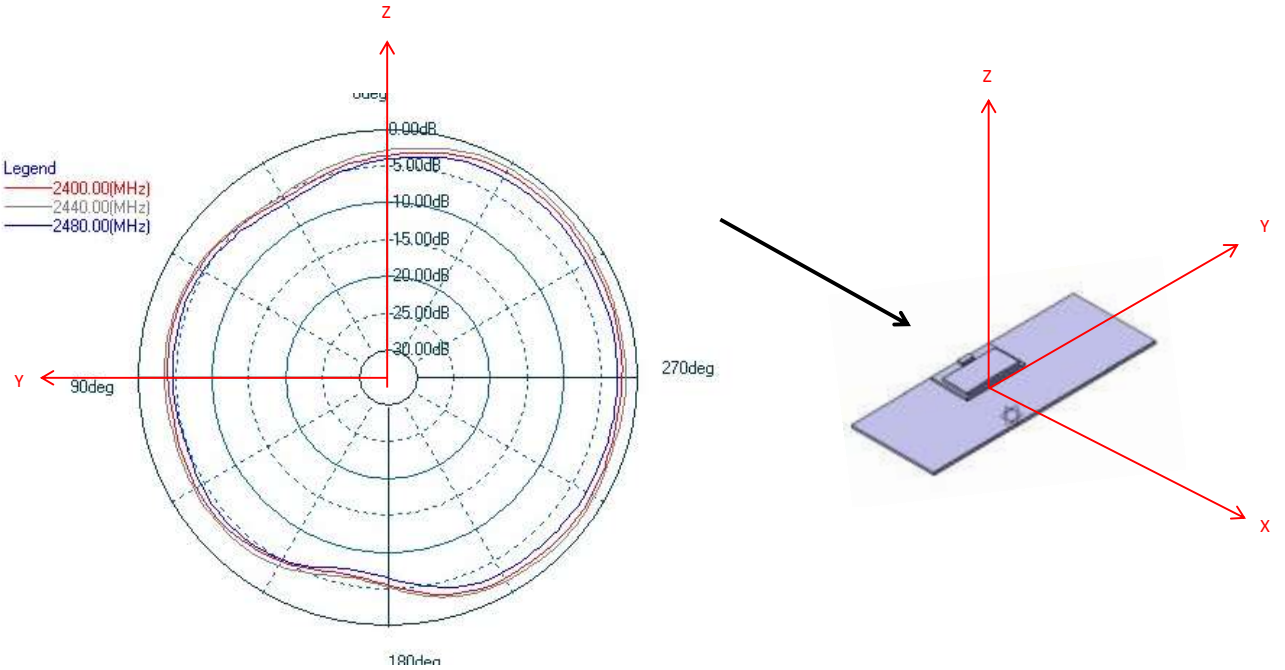


Figure 10: Radiation pattern of BLE121LR when mounted to a carrier board

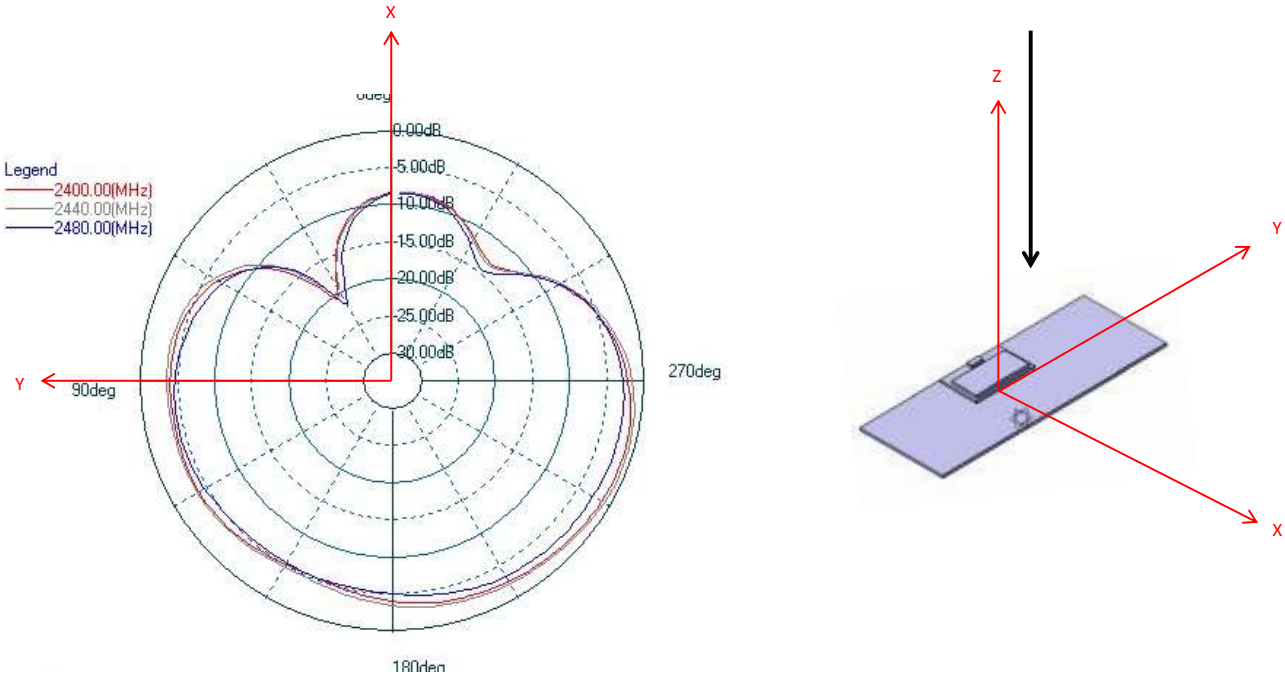


Figure 11: Radiation pattern of BLE121LR when mounted to a carrier board

4.6 Range of BLE121LR

Module	Typical TXP	Sensitivity	Direction	Antenna Attenuation	Link Budget	Calculated Range	Tested Range
BLE121LR	8 dBm	-98 dBm	Front	-3 dB	100 dB	470m	450m
BLE121LR	8 dBm	-98 dBm	Back	-7 dB	92 dB	300m	300m
BLE121LR	8 dBm	-98 dBm	Side	-5 dB	96 dB	370m	340m

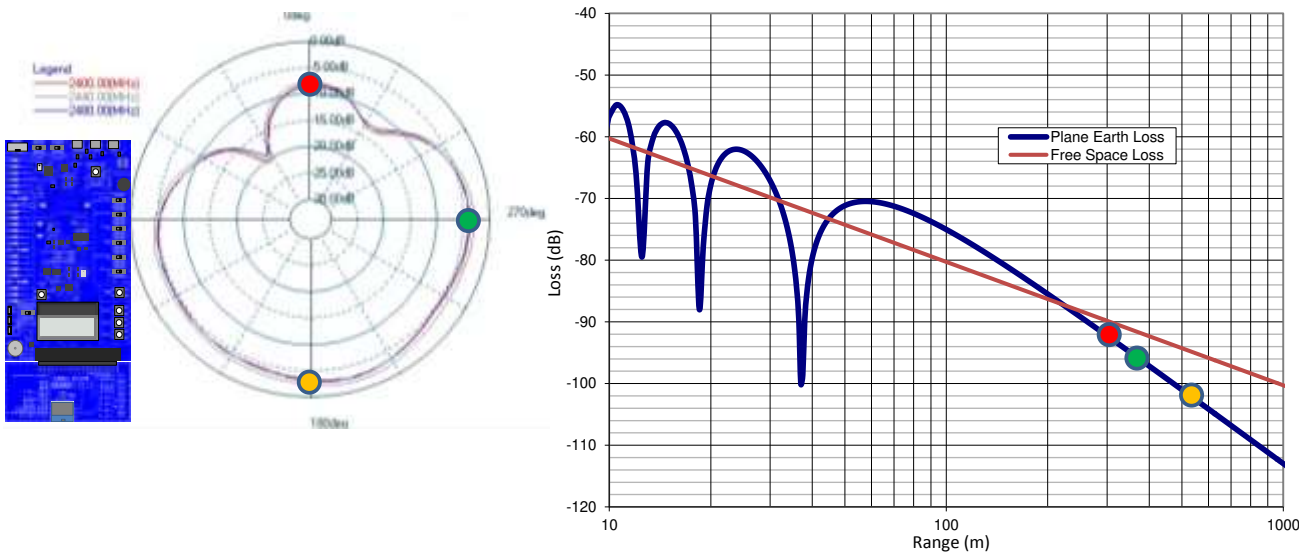


Figure 12: Range of BLE121LR vs BLE121LR when antennas are 1.5m above GND

The range of BLE121LR is dependent on the mother board layout, height of the antennas above GND and any obstacles within the RF path or near the RF path (multipath propagation). See Figure 25 how the layout impacts to the range of BLE121LR.

In an open field the received power is a sum of the line-of-sight wave and the ground-reflected wave. Depending on the phase of the ground-reflected wave, it either amplifies or attenuates the total received power. Figure 14 shows how the antenna height from ground impacts to the RF path loss and range in an open field.

RF power propagates in free space within a virtual “pipe” which can be defined by so called Fresnel ellipsoid. Any obstacles within the area of this “pipe” will attenuate the RF power and thus decrease the actual range of the link. The radius of the “pipe” can be approximated by

$$R = \sqrt{\frac{D \times \lambda}{12}}$$

Where R is the radius, D is the distance between the antennas and lambda is the wave length (12.2 cm).

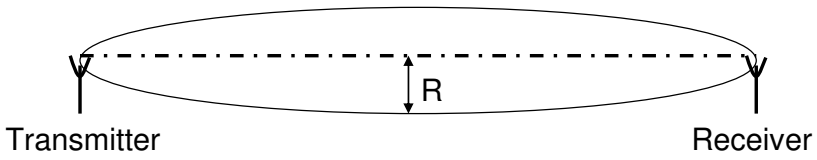


Figure 13: RF propagation area between TX and RX

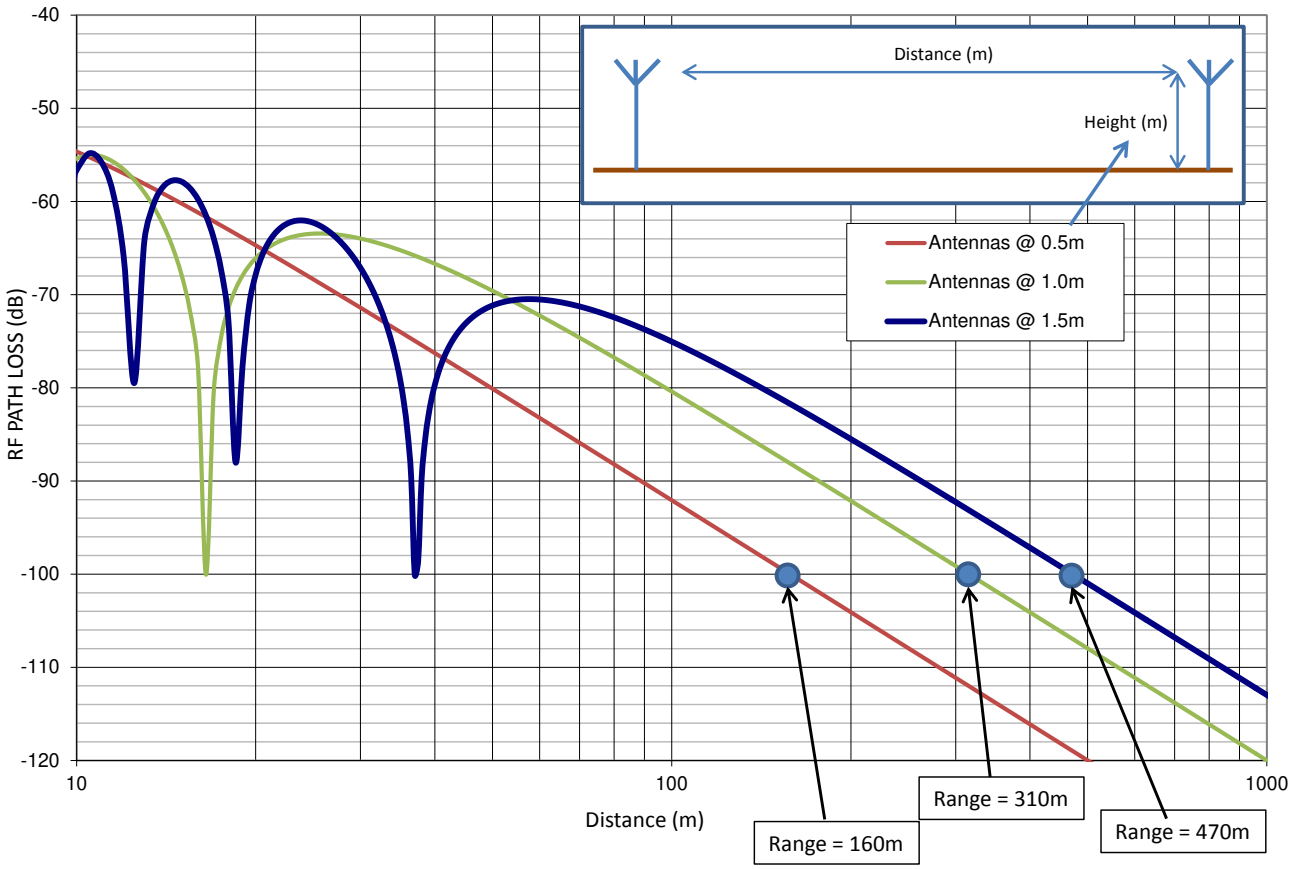


Figure 14: Impact of module height above GND to RF path loss

5 Physical Dimensions

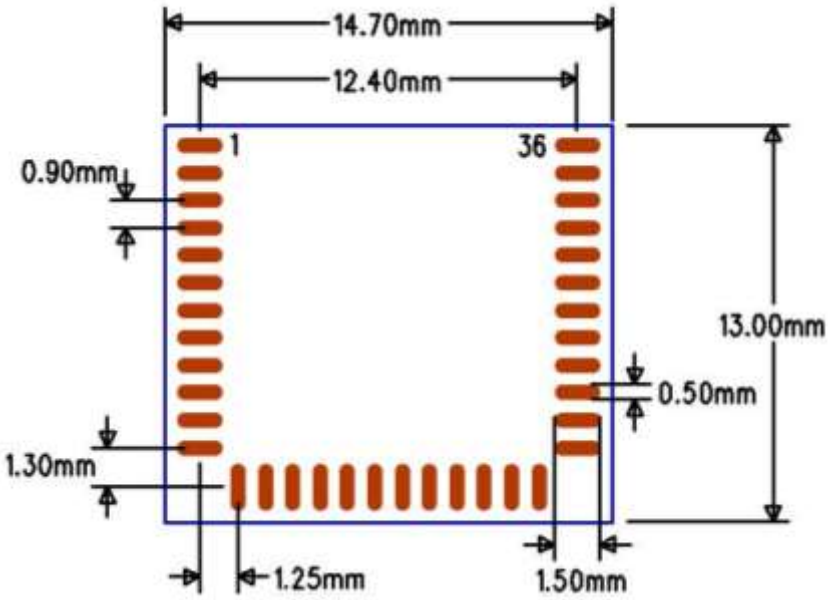


Figure 15: Footprint of BLE121LR (top view)

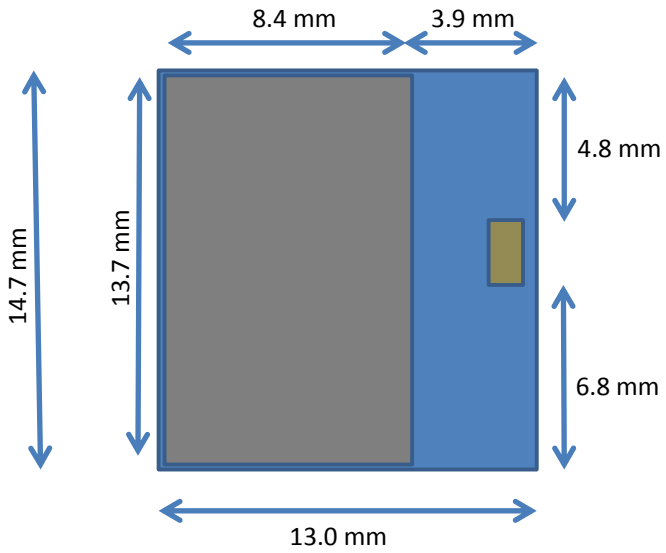


Figure 16: Physical dimensions (top view)

Figure 17: Physical dimensions (side view)

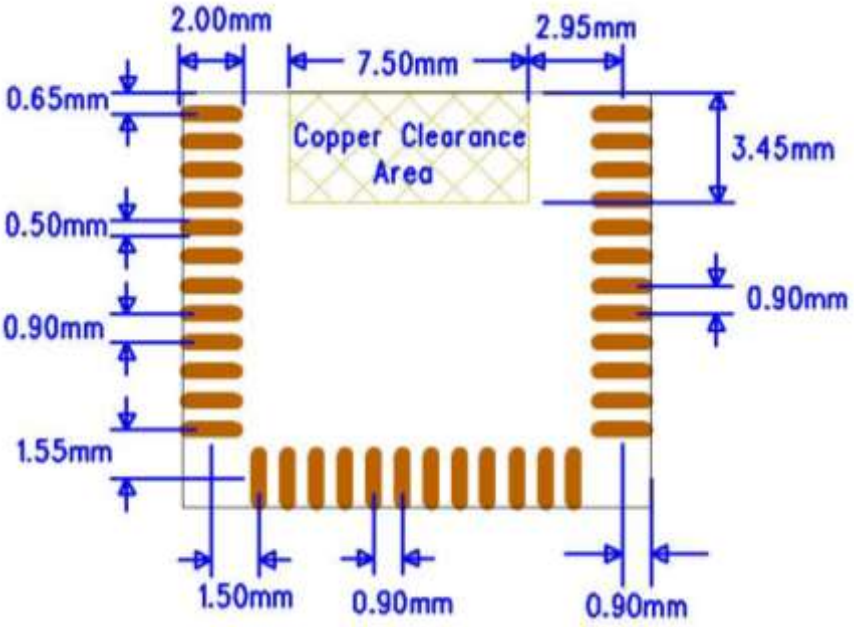


Figure 18: Recommended land pattern for BLE121LR-A

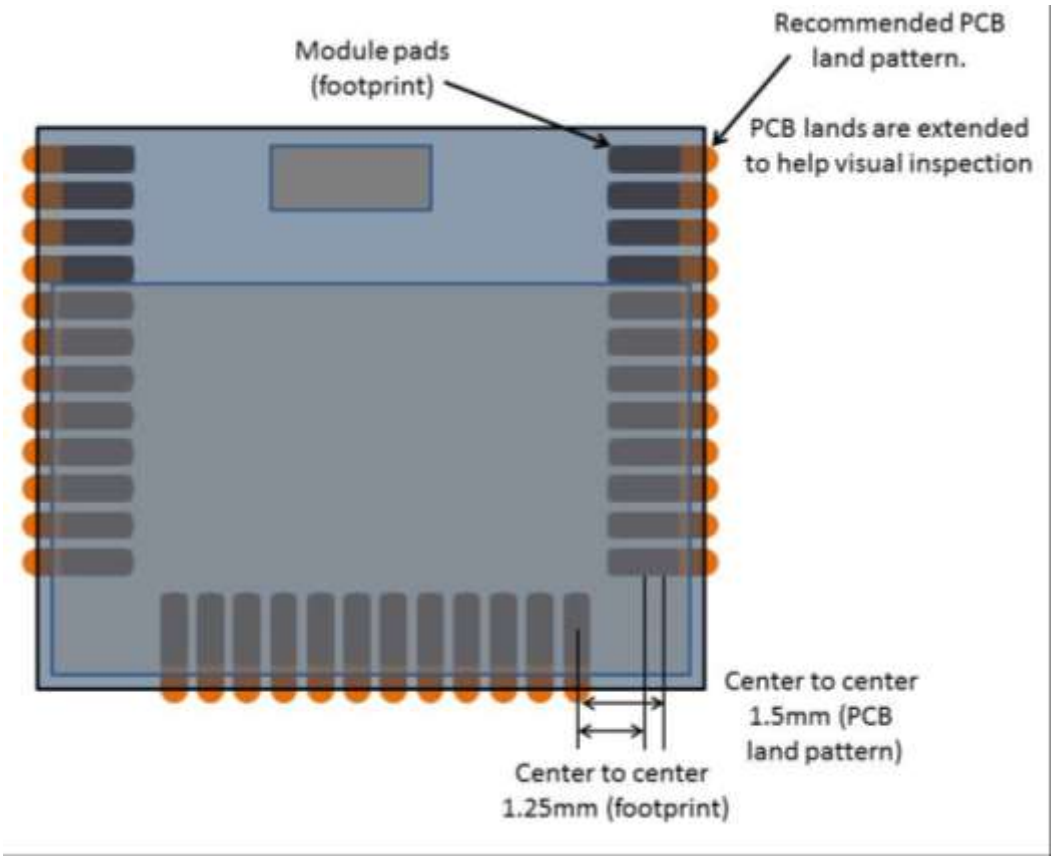


Figure 19: Module placed on the recommended PCB land pattern

6 Power-On Reset and Brownout Detector

BLE121LR includes a power-on reset (POR), providing correct initialization during device power on. It also includes a brownout detector (BOD) operating on the regulated 1.8-V digital power supply only. The BOD protects the memory contents during supply voltage variations which cause the regulated 1.8-V power to drop below the minimum level required by digital logic, flash memory, and SRAM. When power is initially applied, the POR and BOD hold the device in the reset state until the supply voltage rises above the power-on-reset and brownout voltages.

7 Design Guidelines

7.1 General Design Guidelines

BLE121LR can be used directly with a coin cell battery. Due to relatively high internal resistance of a coin cell battery it is recommended to place a 100uF capacitor in parallel with the battery. The internal resistance of a coin cell battery is initially in the range of 10 ohms but the resistance increases rapidly as the capacity is used. Basically the higher the value of the capacitor the higher is the effective capacity of the battery and thus the longer the life time for the application. The minimum value for the capacitor depends on the end application and the maximum transmit power used. The leakage current of a 100uF capacitor is in the range of 0.5 uA to 3 uA and generally ceramic capacitors have lower leakage current than tantalum or aluminum electrolytic capacitors.

Optionally TI's TPS62730 can be used to reduce the current consumption during TX/RX and data processing stages. TPS62730 is an ultra-low power DC/DC converter with by-pass mode and will reduce the current consumption during transmission nominally by ~20% when using 3V coin cell battery. Because, unlike with BLE112 and BLE113, the TX power of BLE121LR is dependent on the power supply, the DCDC reduces the TX power by ~2dB, which provides additional saving in the peak current. So in total the peak current can be reduced by approximately 30% with the cost of 2 dB lower TX power.

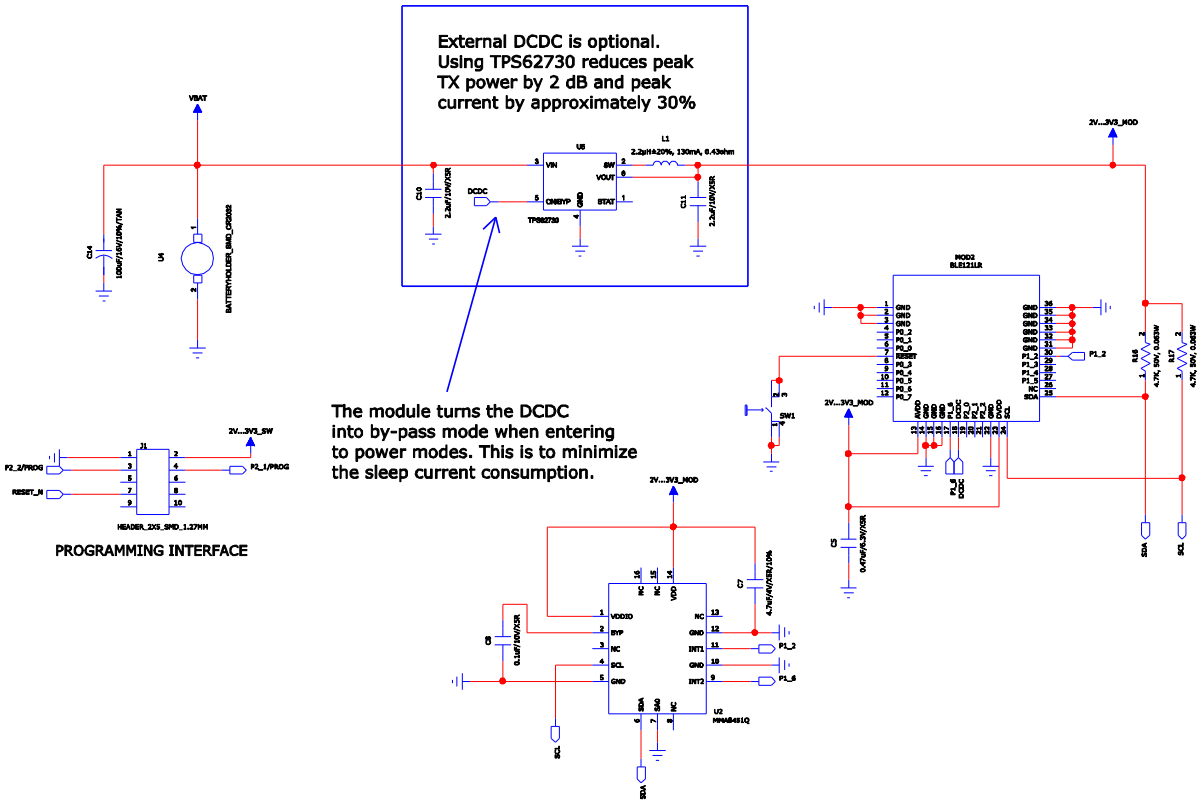


Figure 20: Example schematic for BLE121LR with a coin cell battery, TPS62730 DCDC converter and an I2C accelerometer

7.2 Layout Guide Lines

Use good layout practices to avoid excessive noise coupling to supply voltage traces or sensitive analog signal traces. If using overlapping ground planes use stitching vias separated by max 3 mm to avoid emission

from the edges of the PCB. Connect all the GND pins directly to a solid GND plane and make sure that there is a low impedance path for the return current following the signal and supply traces all the way from start to the end.

A good practice is to dedicate one of the inner layers to a solid GND plane and one of the inner layers to supply voltage planes and traces and route all the signals on top and bottom layers of the PCB. This arrangement will make sure that any return current follows the forward current as close as possible and any loops are minimized.

Figure 21: Typical 4-layer PCB construction

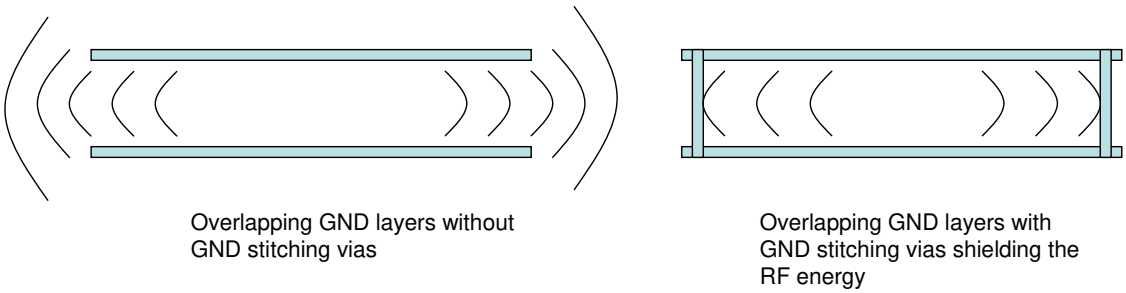


Figure 22: Use of stitching vias to avoid emissions from the edges of the PCB

7.3 BLE121LR-A Layout Guide

For optimal performance of the antenna place the module at the edge of the PCB as shown in the Figure 23. Do not place any metal (traces, components, battery etc.) within the clearance area of the antenna. Connect all the GND pins directly to a solid GND plane. Place the GND vias as close to the GND pins as possible. Use good layout practices to avoid any excessive noise coupling to signal lines or supply voltage lines. Do not place plastic or any other dielectric material in touch with the antenna.

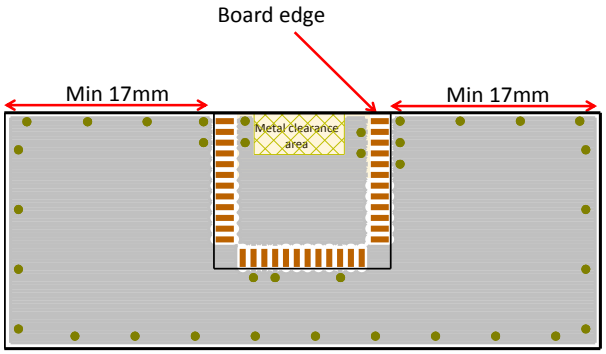


Figure 23: Recommended layout for BLE121LR-A

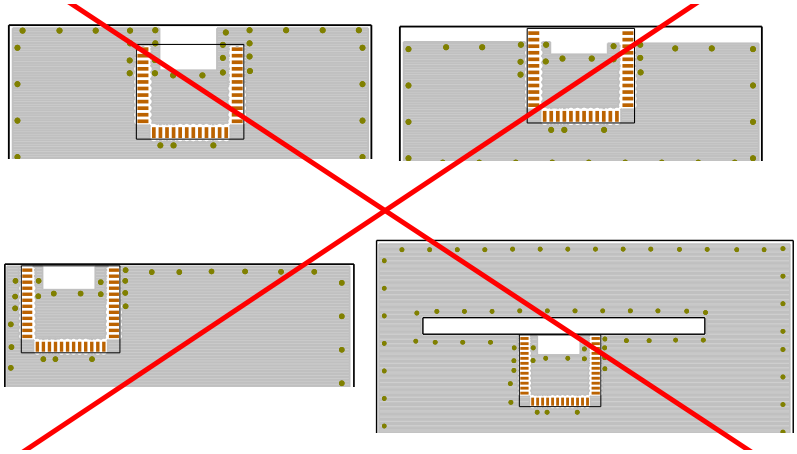


Figure 24: Poor layouts for BLE121LR

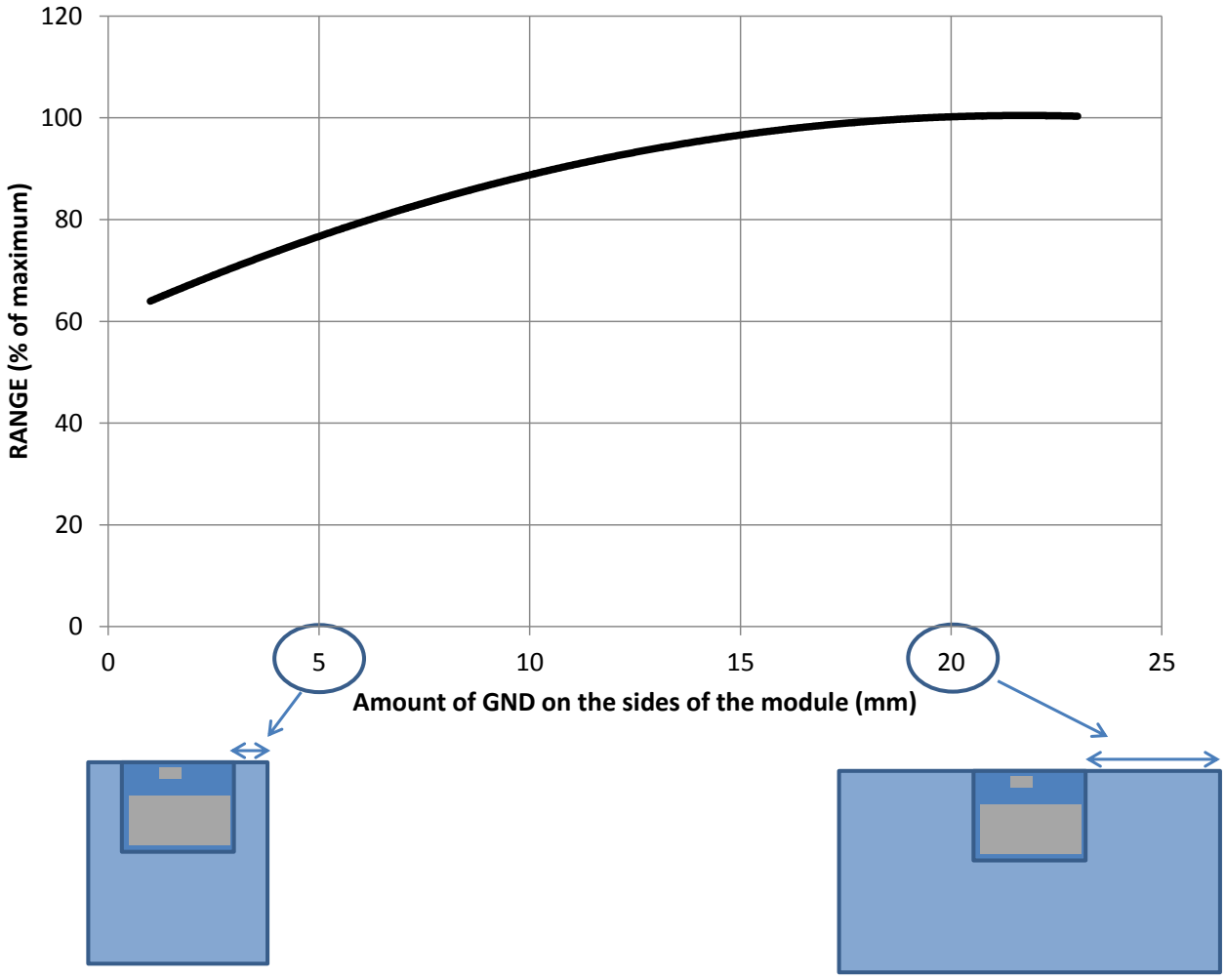


Figure 25: Impact of the size of GND plane to the range of BLE121LR