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Power LDMOS transistor

Rev. 2 — 1 September 2015

AMPLEON Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for ISM applications at frequencies from 700 MHz to 1000 MHz.

Table 1.Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f	V _{DS}	P _{L(AV)}	Gp	η _D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	869 to 894	28	40	20	28.5	-39 <mark>[1]</mark>

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (700 MHz to 1000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

 RF power amplifiers for ISM applications in the 700 MHz to 1000 MHz frequency range.

Power LDMOS transistor

2. Pinning information

Pin	Description		Simplified outline	Graphic symbol
BLF10M6	200 (SOT502A)			
1	drain			
2	gate		$\int \int \int]$	ر لـــــار
3	source	<u>[1]</u>		
				sym112
BLF10M6	LS200 (SOT502B)			
1	drain			
2	gate			1 لــــا
3	source	<u>[1]</u>		
				3
				sym112

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information					
Type number	Packag	je			
	Name	Description	Version		
BLF10M6200	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A		
BLF10M6LS200	-	earless flanged ceramic package; 2 leads	SOT502B		

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage		-	65	V
V _{GS}	gate-source voltage		-0.5	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		<u>[1]</u> _	225	°C

[1] Continuous use at maximum temperature will affect the reliability

5. Thermal characteristics

Table 5.	Thermal characteristics				
Symbol	Parameter	Conditions	Туре	Тур	Unit
R _{th(j-case)}	thermal resistance from	T _{case} = 80 °C;	BLF10M6200	0.50	K/W
	junction to case	P _L = 40 W	BLF10M6LS200	0.35	K/W

BLF10M6200_BLF10M6LS200#2

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6. Characteristics

Table 6.DC characteristics

 $T_i = 25 \ ^{\circ}C$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	V_{GS} = 0 V; I _D = 0.9 mA	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V_{DS} = 10 V; I _D = 270 mA	1.4	2.0	2.4	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 1620 mA	1.7	2.2	2.7	V
I _{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	4.2	μA
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	48	-	A
I _{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	420	nA
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 9.45 A	-	18	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ $I_D = 9.45 A$	-	0.07	-	Ω

Table 7. AC characteristics

 $T_i = 25 \ ^{\circ}C$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	3	-	pF

Table 8. RF characteristics

Test signal: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 DPCH; $f_1 = 871.5$ MHz; $f_2 = 876.5$ MHz; $f_3 = 886.5$ MHz; $f_4 = 891.5$ MHz; RF performance at $V_{DS} = 28$ V; $I_{Dq} = 1400$ mA; $T_{case} = 25$ °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
G _p	power gain	$P_{L(AV)} = 40 W$	19	20	-	dB
η_D	drain efficiency	$P_{L(AV)} = 40 W$	25	28.5	-	%
RL _{in}	input return loss	$P_{L(AV)} = 40 W$	-	-6.4	-4.5	dB
ACPR	adjacent channel power ratio	$P_{L(AV)} = 40 W$	-	-39.4	-36	dBc

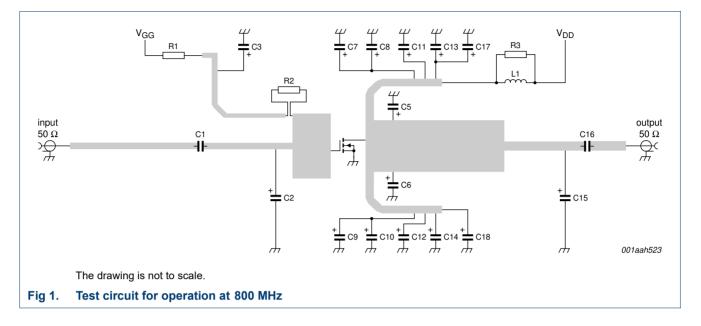
7. Test information

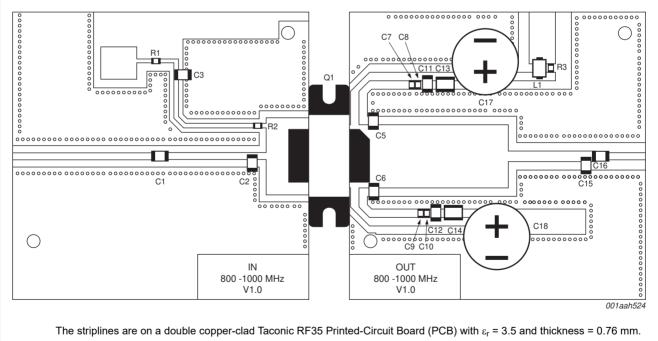
7.1 Ruggedness in class-AB operation

The BLF10M6200 and BLF10M6LS200 are enhanced rugged devices and capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28$ V; $I_{Dq} = 1400$ mA; $P_L = 200$ W; f = 894 MHz

Power LDMOS transistor

7.2 Test circuit





See Table 9 for list of components.

The drawing is not to scale.

Fig 2. Component layout

Power LDMOS transistor

Table 9. List of components

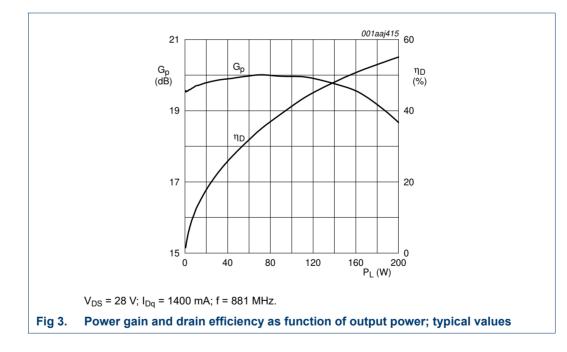
Component	Description	Value		Remarks
C1, C3, C11, C12, C16	multilayer ceramic chip capacitor	68 pF	[1]	solder vertically
C2	multilayer ceramic chip capacitor	13 pF	[1]	solder vertically
C5, C6	multilayer ceramic chip capacitor	10 pF	[1]	solder vertically
C7, C8, C9, C10	electrolytic capacitor	220 nF		Vishay VJ1206Y224KXB
C13, C14	multilayer ceramic chip capacitor	4.7 μF, 50 V	[2]	
C15	multilayer ceramic chip capacitor	1.5 pF	[1]	solder vertically
C17, C18	electrolytic capacitor	220 μF, 63 V		
L1	ferrite SMD bead	-		Ferroxcube BDS 3/3/4.6-4S2 or equivalent
Q1	BLF10M6200	-		
R1, R2, R3	SMD resistor	9.1 Ω, 0.1 W		

[1] American Technical Ceramics type 100B or capacitor of same quality.

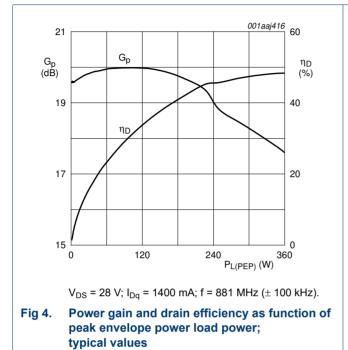
[2] TDK or capacitor of same quality.

7.3 Graphical data

7.3.1 One-tone CW

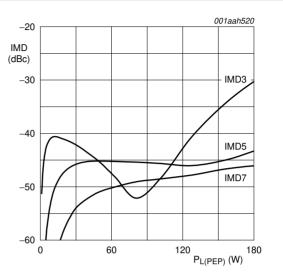


Power LDMOS transistor



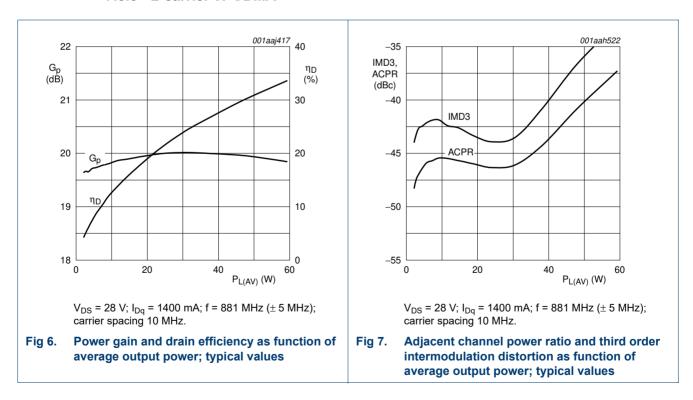
7.3.2 Two-tone CW





V_{DS} = 28 V; I_{Dg} = 1400 mA; f = 881 MHz (± 100 kHz).

Fig 5. Intermodulation distortion as a function of peak envelope power load power; typical values



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BLF10M6200; BLF10M6LS200

Power LDMOS transistor

8. Package outline

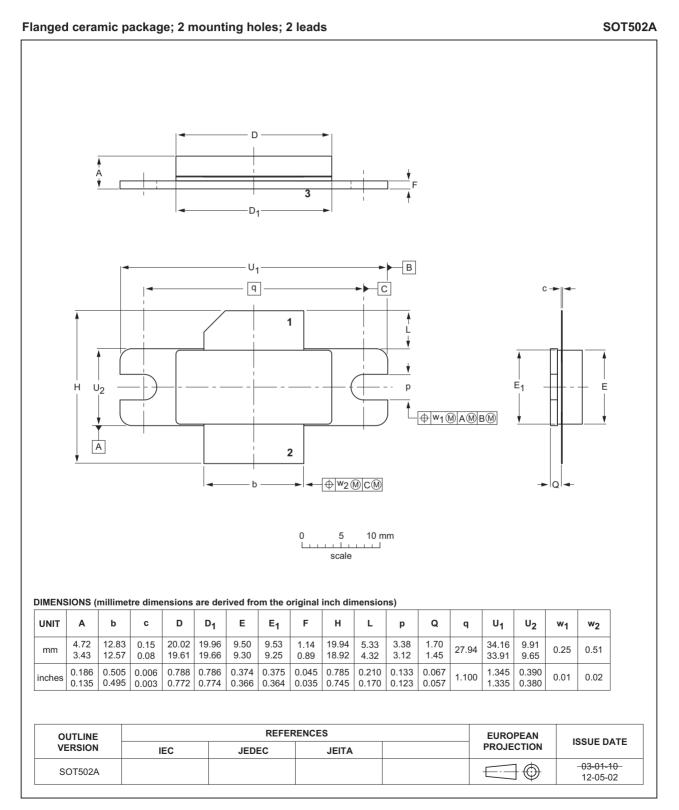


Fig 8. Package outline SOT502A

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BLF10M6200; BLF10M6LS200

Power LDMOS transistor

SOT502B

Earless flanged ceramic package; 2 leads

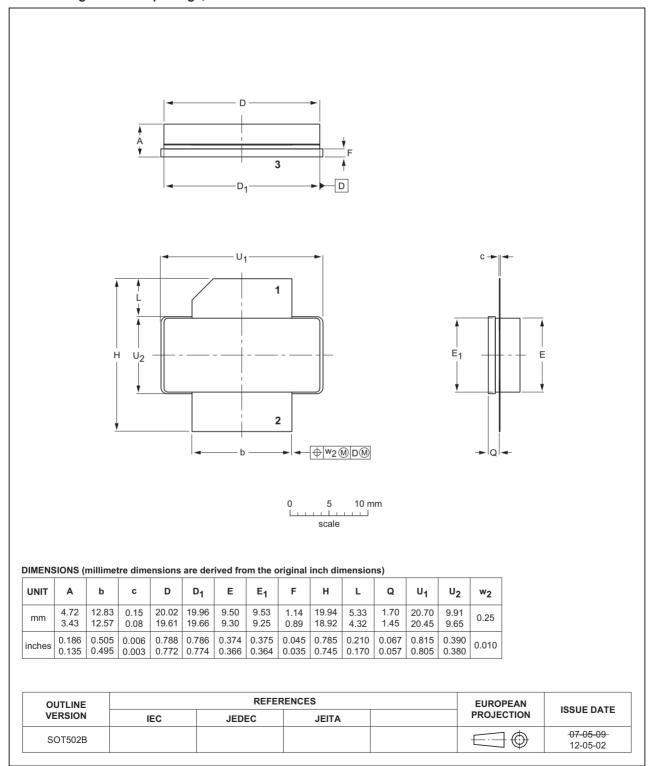


Fig 9. Package outline SOT502B

BLF10M6200_BLF10M6LS200#2

Product data sheet

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

10. Abbreviations

Table 10.	Abbreviations
Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11.Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
LF10M6200_BLF10M6LS200#2 20150901 Product data sheet		-	BLF10M6200_ BLF10M6LS20 0 v.1			
Modifications: • The format of this document has been redesigned to comply w identity guidelines of Ampleon.				nply with the new		
	 Legal texts have been adapted to the new company name where appropriate. 					
BLF10M6200_BLF10M6LS200 v.1	20130701	Product data sheet	-	-		

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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