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BLF184XR; BLF184XRS

Power LDMOS transistor

Rev. 4 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 700 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 600 MHz band.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	108	50	700	23.9	73.5
CW	108	50	750	23.5	81.9

1.2 Features and benefits

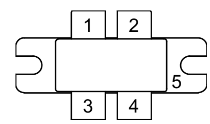
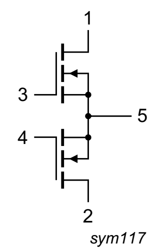
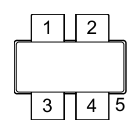
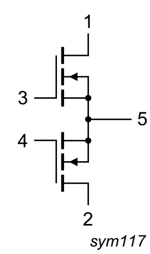
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 600 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF184XR (SOT1214A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF184XRS (SOT1214B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF184XR	-	flanged ceramic package; 2 mounting holes; 4 leads	SOT1214A
BLF184XRS	-	earless flanged ceramic package; 4 leads	SOT1214B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	135	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

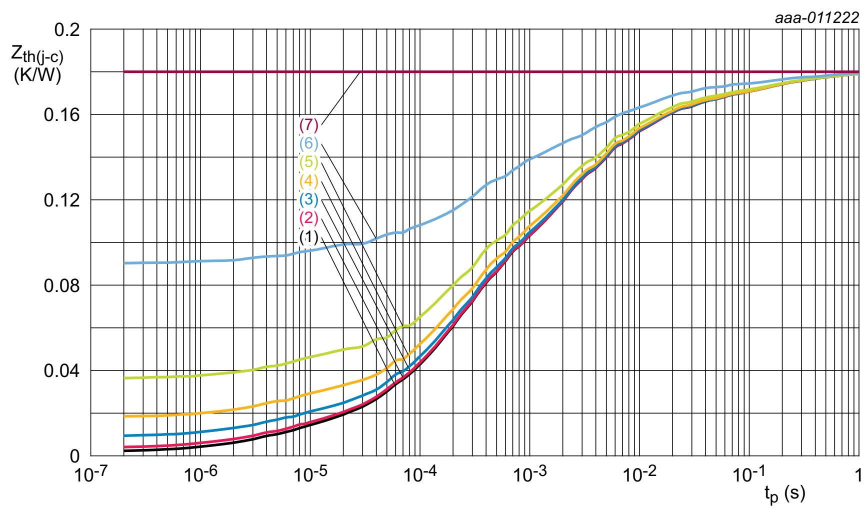
Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 150 °C	[1][2]	0.18	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_j = 150 °C; t_p = 100 μs; δ = 20 %	[3]	0.065	K/W

[1] T_j is the junction temperature.

[2] $R_{th(j-c)}$ is measured under RF conditions.

[3] See Figure 3.



(1) δ = 1 %

(2) δ = 2 %

(3) δ = 5 %

(4) δ = 10 %

(5) δ = 20 %

(6) δ = 50 %

(7) δ = 100 % (DC)

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.75 mA	135	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 275 mA	1.25	1.9	2.25	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 50 mA	-	1.6	-	V

Table 6. DC characteristics *...continued*

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	38.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 3.75 V; I_D = 9.625 A	-	0.16	-	Ω

Table 7. AC characteristics

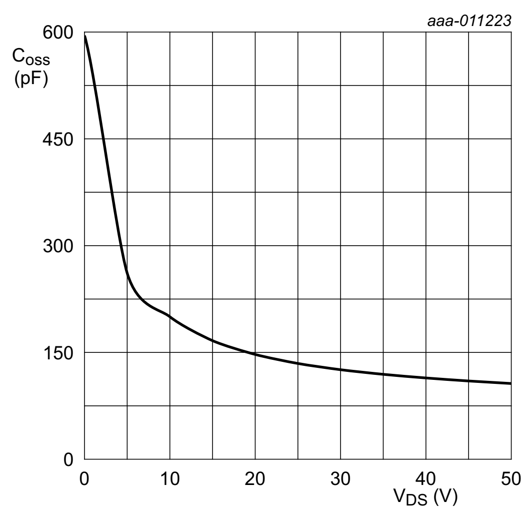
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	3.1	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	292	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	107	-	pF

Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μs; δ = 20 %; f = 108 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 700 W	22.8	23.9	-	dB
RL_{in}	input return loss	P_L = 700 W	-	−20	−13	dB
η_D	drain efficiency	P_L = 700 W	71	73.5	-	%



V_{GS} = 0 V; f = 1 MHz.

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

7. Test information

7.1 Ruggedness in class-AB operation

The BLF184XR and BLF184XRS are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 100 mA; P_L = 700 W pulsed; f = 108 MHz.

7.2 Impedance information

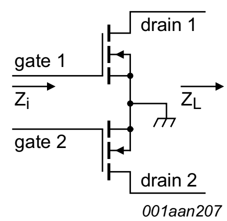


Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 50 V and P_L = 700 W.

f	Z_i	Z_L
(MHz)	**(Ω)**	**(Ω)**
108	5.8 – j19.1	5.5 + j1.0

7.3 UIS avalanche energy

Table 10. Typical avalanche data per section

T_{amb} = 25 °C; typical test data; test jig without water cooling.

I_{AS}	E_{AS}
(A)	**(J)**
15	4.3
20	2.1
25	1.3

For information see application note *AN10273*.

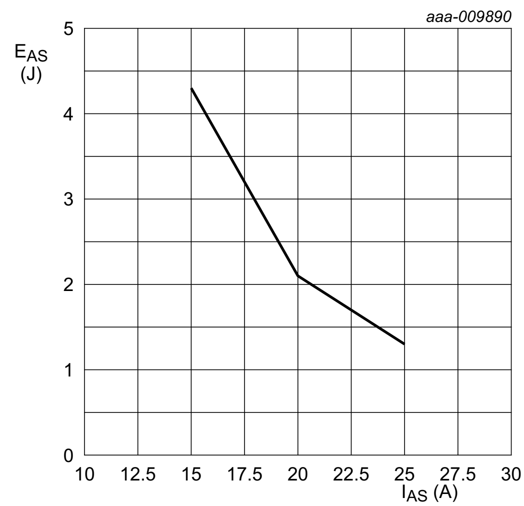
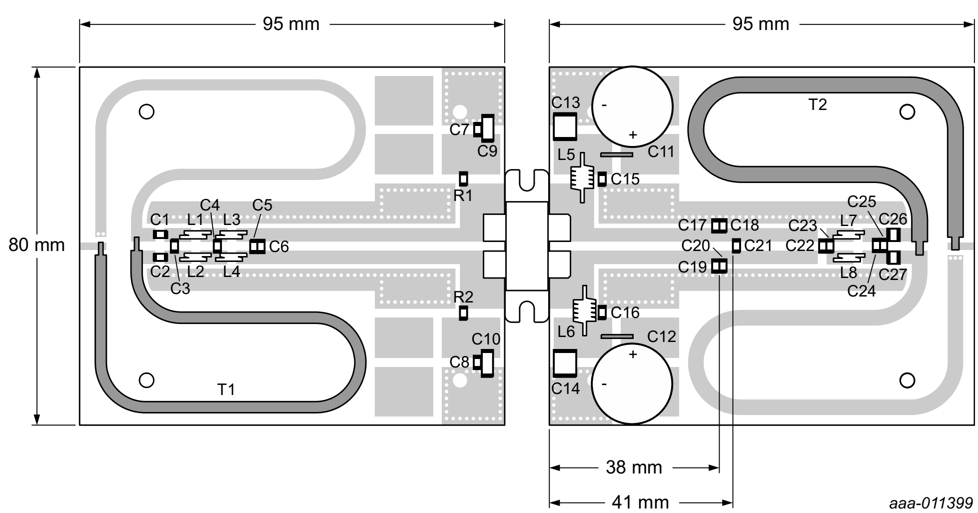


Fig 4. Non-repetitive avalanche energy as a function of single pulse avalanche current, typical values

7.4 Test circuit



Printed-Circuit Board (PCB): Taconic RF-35; ε_r = 3.5 F/m; thickness = 0.765 mm; thickness copper plating = 35 μm, gold plated.

See Table 11 for a list of components.

Fig 5. Component layout for class-AB production test circuit

Table 11. List of components

For test circuit see Figure 5.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	910 pF [1]	
C3	multilayer ceramic chip capacitor	47 pF [1]	
C4	multilayer ceramic chip capacitor	51 pF [1]	

Table 11. List of components *…continued*

For test circuit see Figure 5.

Component	Description	Value	Remarks
C5	multilayer ceramic chip capacitor	100 pF [1]	
C6, C23	multilayer ceramic chip capacitor	20 pF	
C7, C8, C15, C16	multilayer ceramic chip capacitor	820 pF [1]	
C9, C10, C13, C14	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK C5750X7R2A475KT
C11, C12	electrolytic capacitor	1000 μF, 63 V	
C17, C19	multilayer ceramic chip capacitor	39 pF [1]	
C18, C20	multilayer ceramic chip capacitor	27 pF [1]	
C21	multilayer ceramic chip capacitor	7.5 pF [1]	
C22	multilayer ceramic chip capacitor	22 pF [1]	
C24, C25	multilayer ceramic chip capacitor	27 pF [1]	
C26, C27	multilayer ceramic chip capacitor	1 nF [2]	
L1, L2, L3, L4	1.5 turn 0.8 mm copper wire	D = 2.8 mm	
L5, L6	5.5 turn 0.8 mm copper wire	D = 3.6 mm	
L7, L8	1 turn 1.5 mm copper wire	D = 4 mm	
R1, R2	resistor	10 Ω	SMD 1206
T1	semi rigid coax	25 Ω, length = 160 mm	Micro-Coax UT-090C-25
T2	semi rigid coax	25 Ω, length = 160 mm	Micro-Coax UT-141C-25

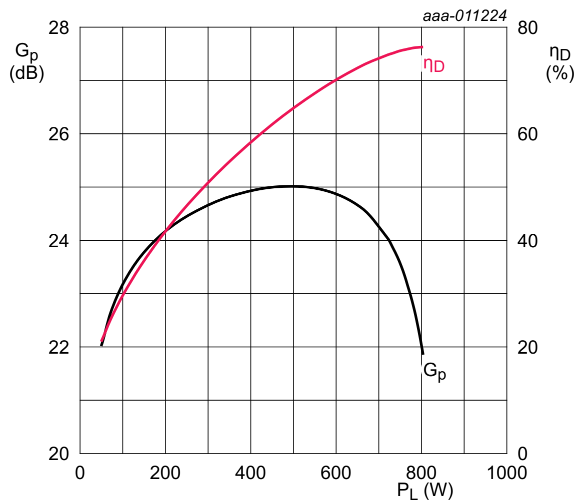
[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

7.5 Graphical data

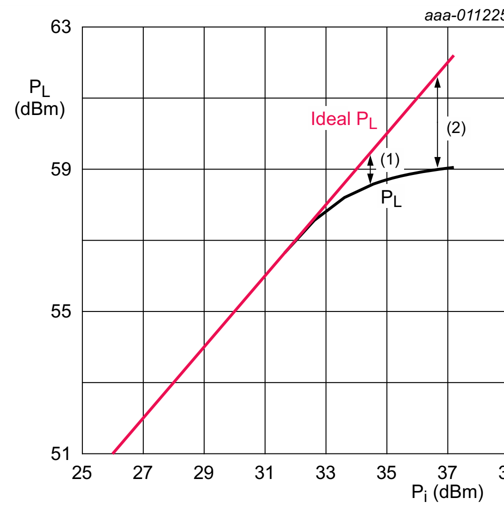
The following figures are measured in a class-AB production test circuit.

7.5.1 1-Tone CW pulsed



V_{DS} = 50 V; I_{Dq} = 100 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

Fig 6. Power gain and drain efficiency as function of output power; typical values

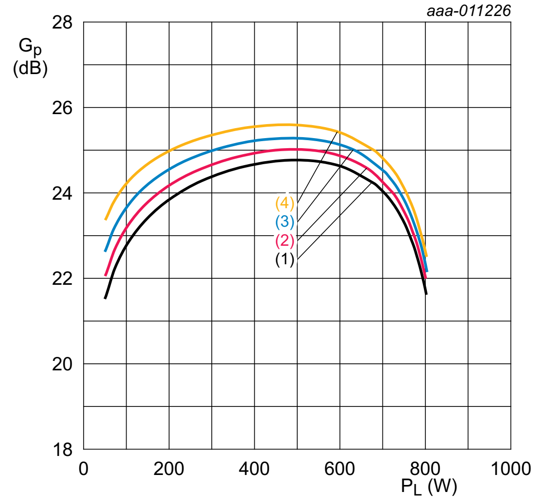


V_{DS} = 50 V; I_{Dq} = 100 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) $P_{L(1dB)}$ = 58.6 dBm (720 W)

(2) $P_{L(3dB)}$ = 59 dBm (800 W)

Fig 7. Output power as a function of input power; typical values



V_{DS} = 50 V; f = 108 MHz; t_p = 100 μs; δ = 20 %.

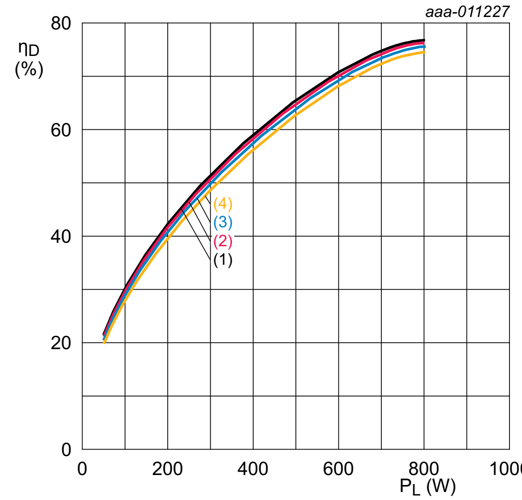
(1) I_{Dq} = 50 mA

(2) I_{Dq} = 100 mA

(3) I_{Dq} = 200 mA

(4) I_{Dq} = 400 mA

Fig 8. Power gain as a function of output power; typical values



V_{DS} = 50 V; f = 108 MHz; t_p = 100 μs; δ = 20 %.

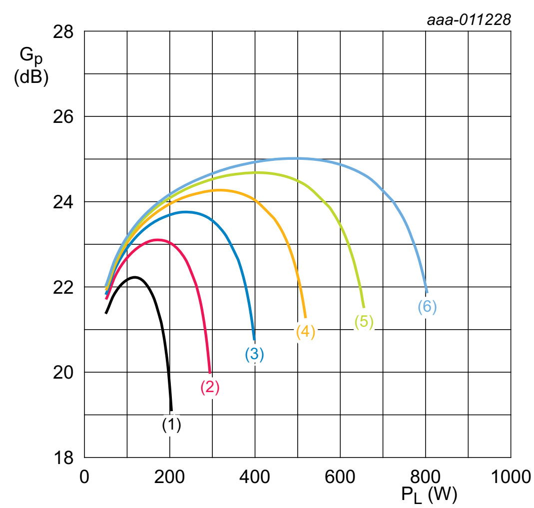
(1) I_{Dq} = 50 mA

(2) I_{Dq} = 100 mA

(3) I_{Dq} = 200 mA

(4) I_{Dq} = 100 mA

Fig 9. Drain efficiency as a function of output power; typical values



I_{Dq} = 100 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 25 V

(2) V_{DS} = 30 V

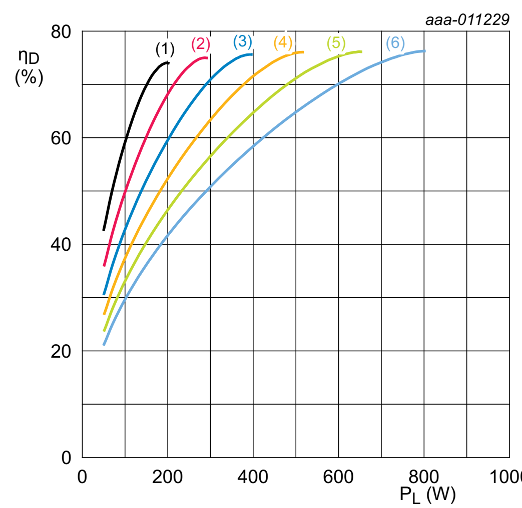
(3) V_{DS} = 35 V

(4) V_{DS} = 40 V

(5) V_{DS} = 45 V

(6) V_{DS} = 50 V

Fig 10. Power gain as a function of output power; typical values



I_{Dq} = 100 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 25 V

(2) V_{DS} = 30 V

(3) V_{DS} = 35 V

(4) V_{DS} = 40 V

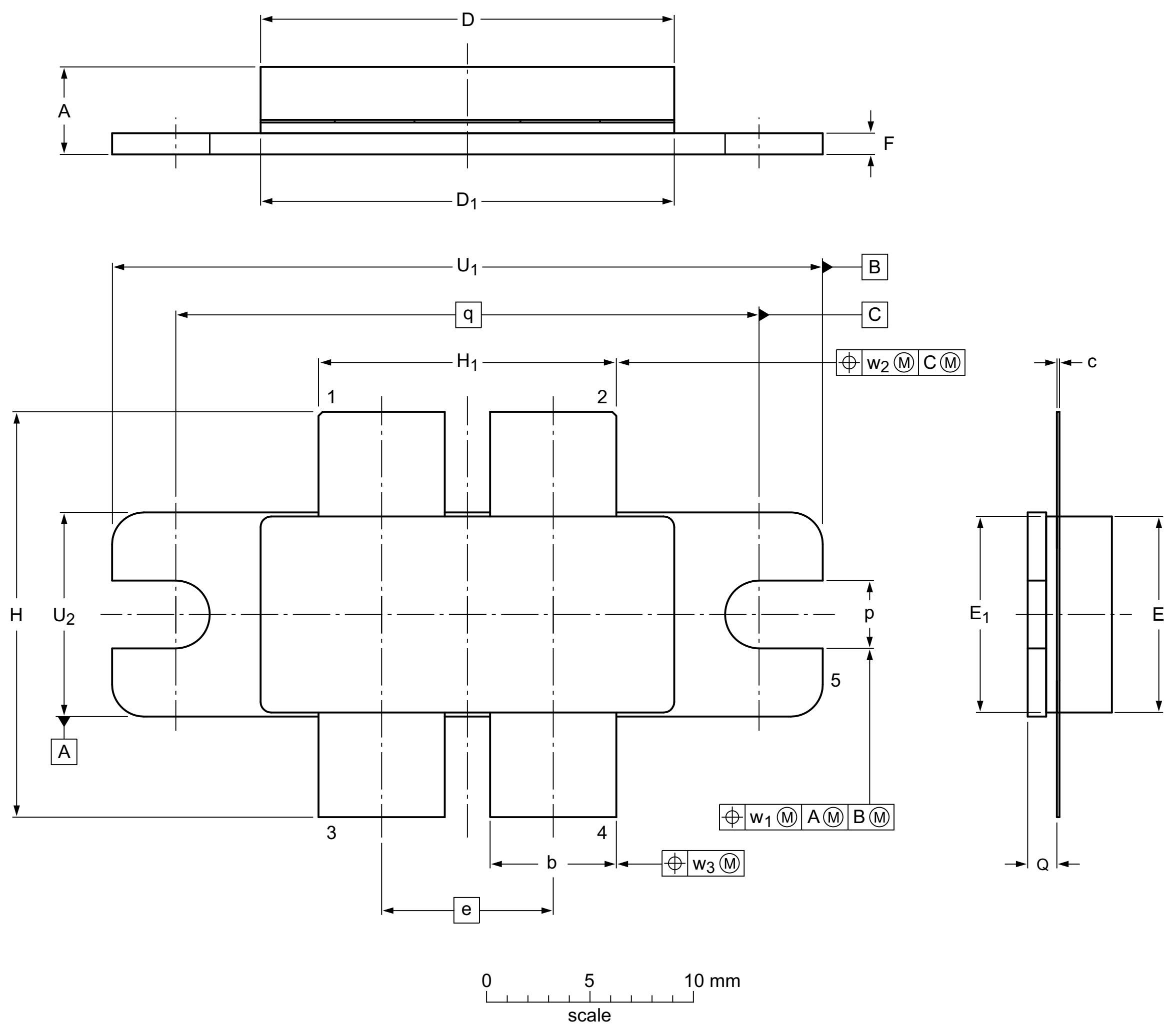
(5) V_{DS} = 45 V

(6) V_{DS} = 50 V

Fig 11. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 4 leads **SOT1214A**



Dimensions

Unit(1)		A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q(2)	q	U_1	U_2	w_1	w_2	w_3
mm	max	4.72	6.17	0.15	20.02	19.96		9.53	9.50	1.14	19.94		3.38	1.70		34.16	9.91			
	nom						8.21					14.24			27.94			0.25	0.51	0.25
	min	3.43	5.92	0.08	19.61	19.66		9.27	9.29	0.89	18.92		3.12	1.45		33.91	9.65			
inches	max	0.187	0.243	0.006	0.788	0.786		0.375	0.374	0.045	0.785		0.133	0.067		1.345	0.39			
	nom						0.323					0.56			1.10			0.01	0.02	0.01
	min	0.135	0.233	0.003	0.772	0.774		0.365	0.366	0.035	0.745		0.123	0.057		1.335	0.38			

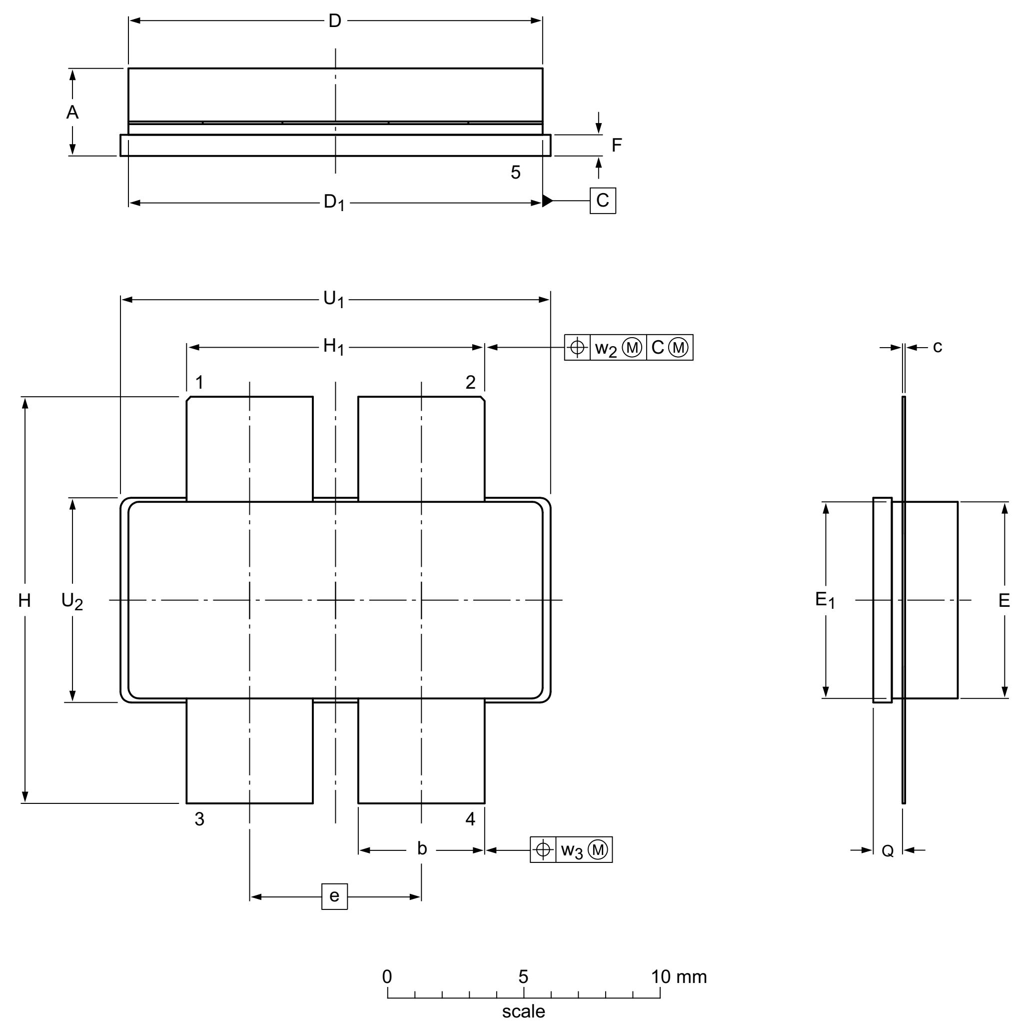
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from body.

sot1214a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1214A					[projection symbol]	~~12-08-16~~ 12-10-10

Fig 12. Package outline SOT1214A

Earless flanged ceramic package; 4 leads **SOT1214B**



Dimensions

Unit(1)		A	b	c	D	D_1	e	E	E_1	F	H	H_1	Q(2)	U_1	U_2	w_2	w_3
mm	max	4.72	6.17	0.15	20.02	19.96		9.53	9.50	1.14	19.94		1.70	20.70	9.91		
	nom						8.21					14.24				0.51	0.25
	min	3.43	5.92	0.08	19.61	19.66		9.27	9.29	0.89	18.92		1.45	20.45	9.65		
inches	max	0.187	0.243	0.006	0.788	0.786		0.375	0.374	0.045	0.785		0.067	0.815	0.39		
	nom						0.323					0.56				0.02	0.01
	min	0.135	0.233	0.003	0.772	0.774		0.365	0.366	0.035	0.745		0.057	0.805	0.38		

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from body.

sot1214b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1214B						~~12-10-10~~ 14-03-27

Fig 13. Package outline SOT1214B

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
UIS	Unclamped Inductive Switching
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF184XR_BLF184XRS v.4	20150901	Product data sheet	-	BLF184XR_BLF184XRS v.3
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLF184XR_BLF184XRS v.3	20140401	Product data sheet	-	BLF184XR_BLF184XRS v.2
BLF184XR_BLF184XRS v.2	20140227	Preliminary data sheet	-	BLF184XR_BLF184XRS v.1
BLF184XR_BLF184XRS v.1	20130506	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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13. Contact information

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