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Thank you for your cooperation and understanding,

Ampleon

VHF push-pull power MOS transistor BLF246B

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

Large signal applications in the VHF frequency range.

DESCRIPTION

Dual silicon N-channel enhancement mode vertical D-MOS push-pull transistor encapsulated in an 8-lead SOT161A balanced flange package with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT161A

PIN	DESCRIPTION
1	source
2	source
3	drain 1
4	gate 1
5	drain 2
6	gate 2
7	source
8	source

PIN CONFIGURATION

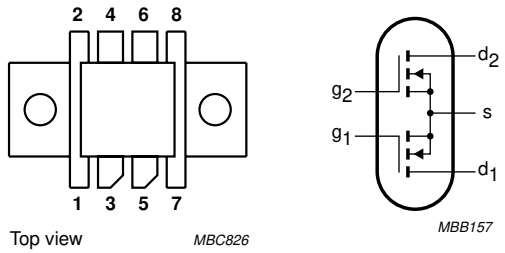


Fig.1 Simplified outline and symbol.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	175	28	60	>14	>55

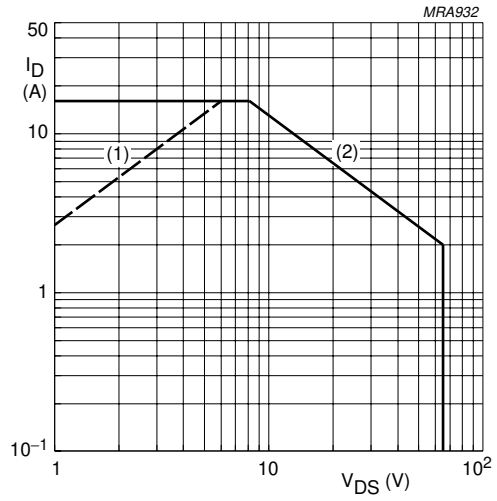
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section unless otherwise specified					
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	8	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C total device; both sections equally loaded	–	130	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

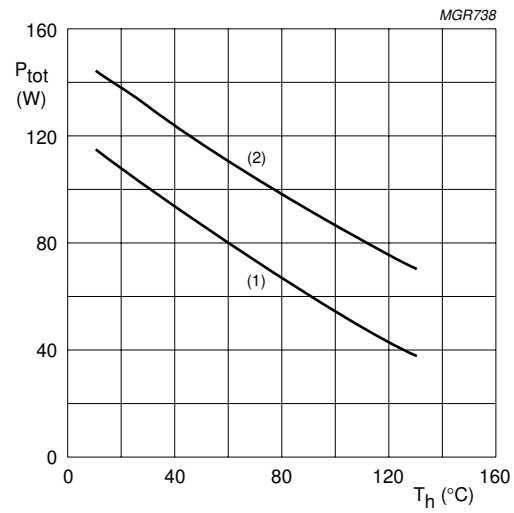
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	1.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25	K/W



(1) Current in this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power derating curves.

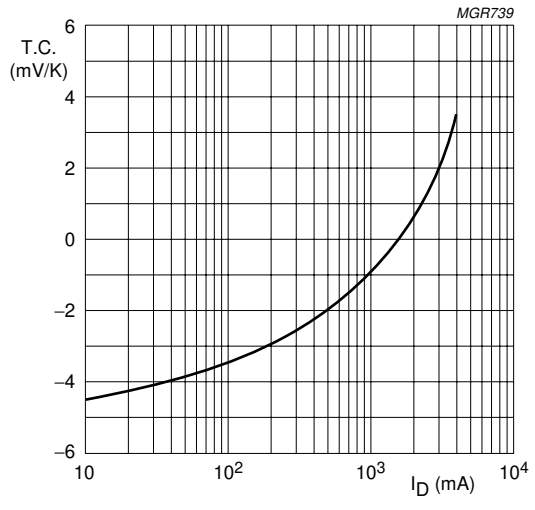
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 1.5 A; V_{DS} = 10 V	1.2	1.8	–	S
R_{DSon}	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	0.4	0.75	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	125	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	75	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	11	–	pF

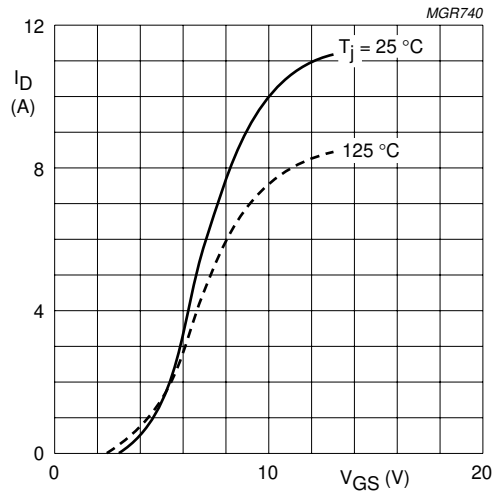
V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			



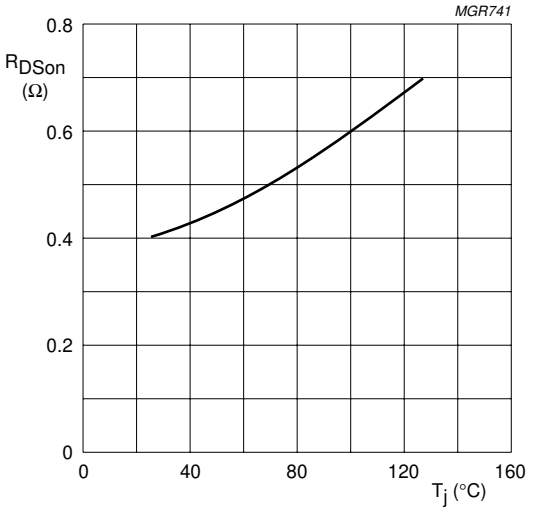
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values per section.



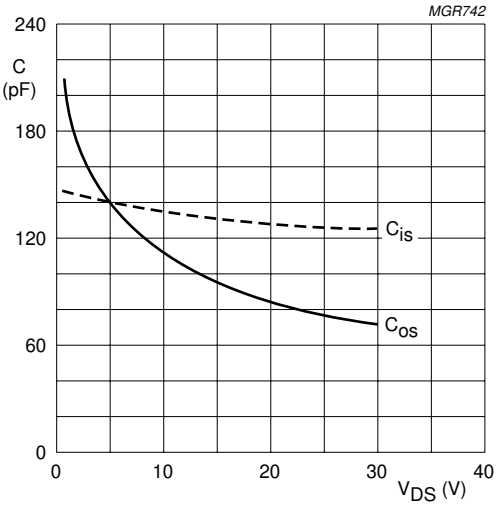
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage; typical values per section.



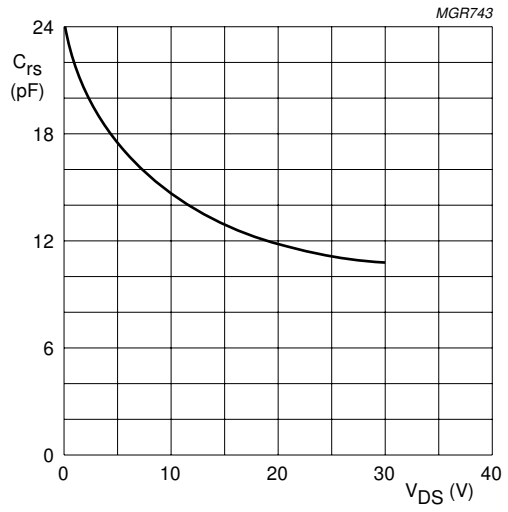
V_{GS} = 10 V; I_D = 1.5 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values per section.

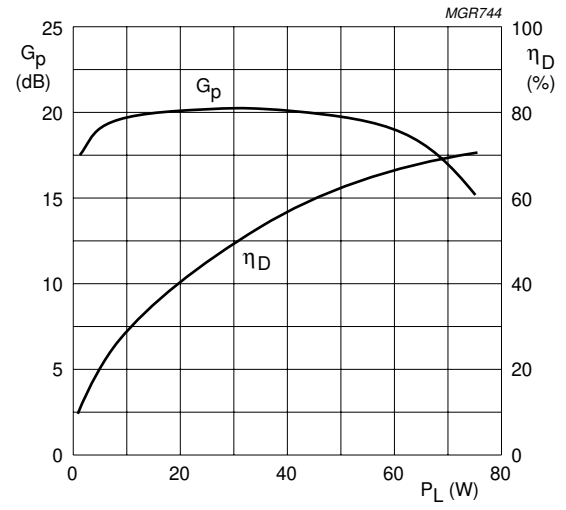
APPLICATION INFORMATION

RF performance in CW operation in a push-pull, common source, class-B circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.25 K/W; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	2×50	60	>14 typ. 19	>55 typ. 65

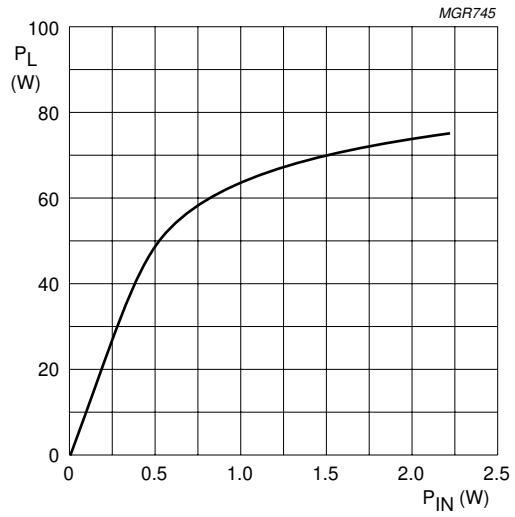
Ruggedness in class-B operation

The BLF246B is capable of withstanding a load mismatch corresponding to VSWR = 50 : 1 through all phases under the following conditions: V_{DS} = 28 V; f = 175 MHz at rated output power.



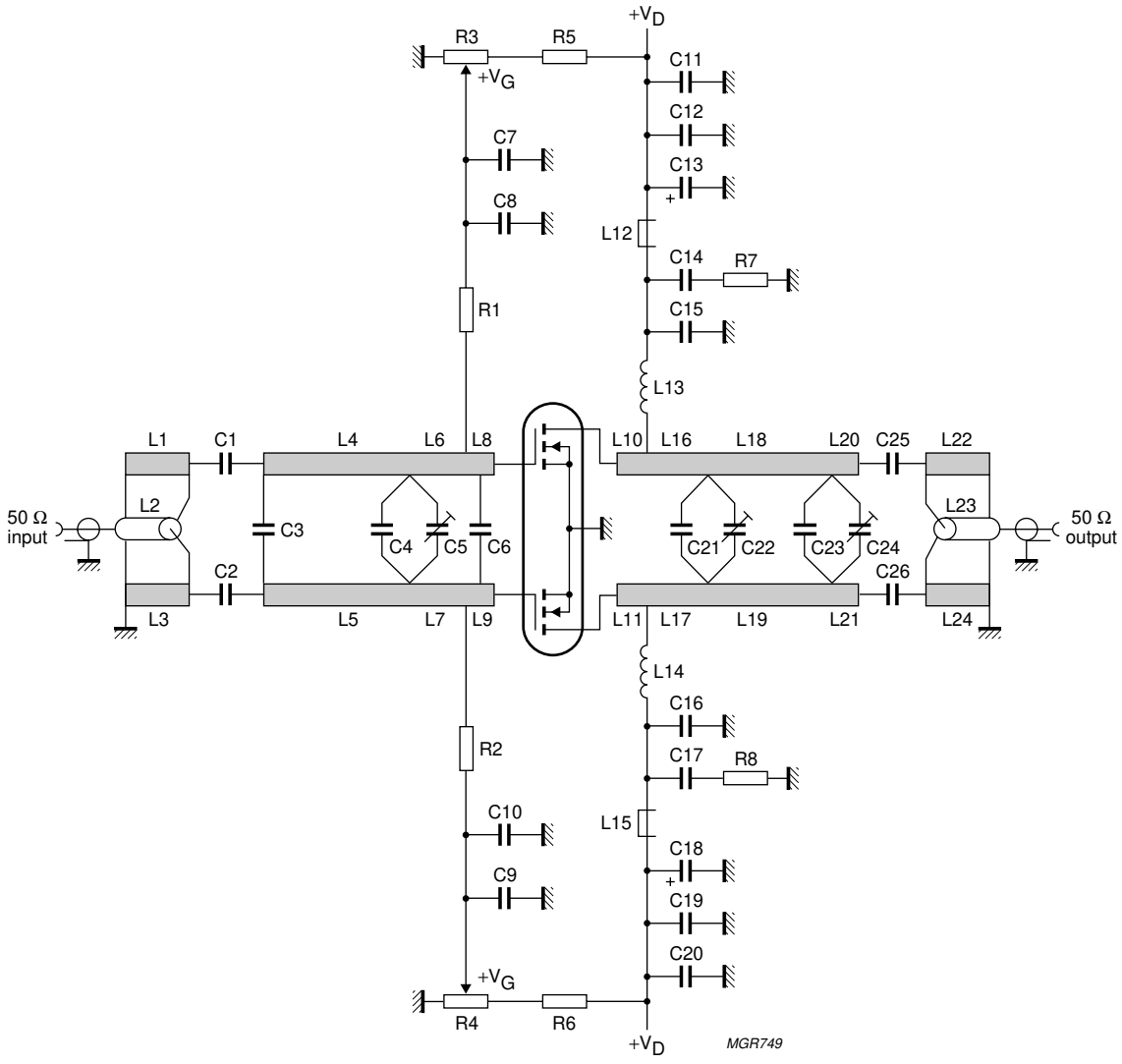
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 50 mA;
Z_L = 4.6 + j5 Ω; f = 175 MHz.

Fig.9 Power gain and efficiency as a function of load power; typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 50 mA;
Z_L = 4.6 + j5 Ω; f = 175 MHz.

Fig.10 Load power as a function of input power; typical values per section.



f = 175 MHz.

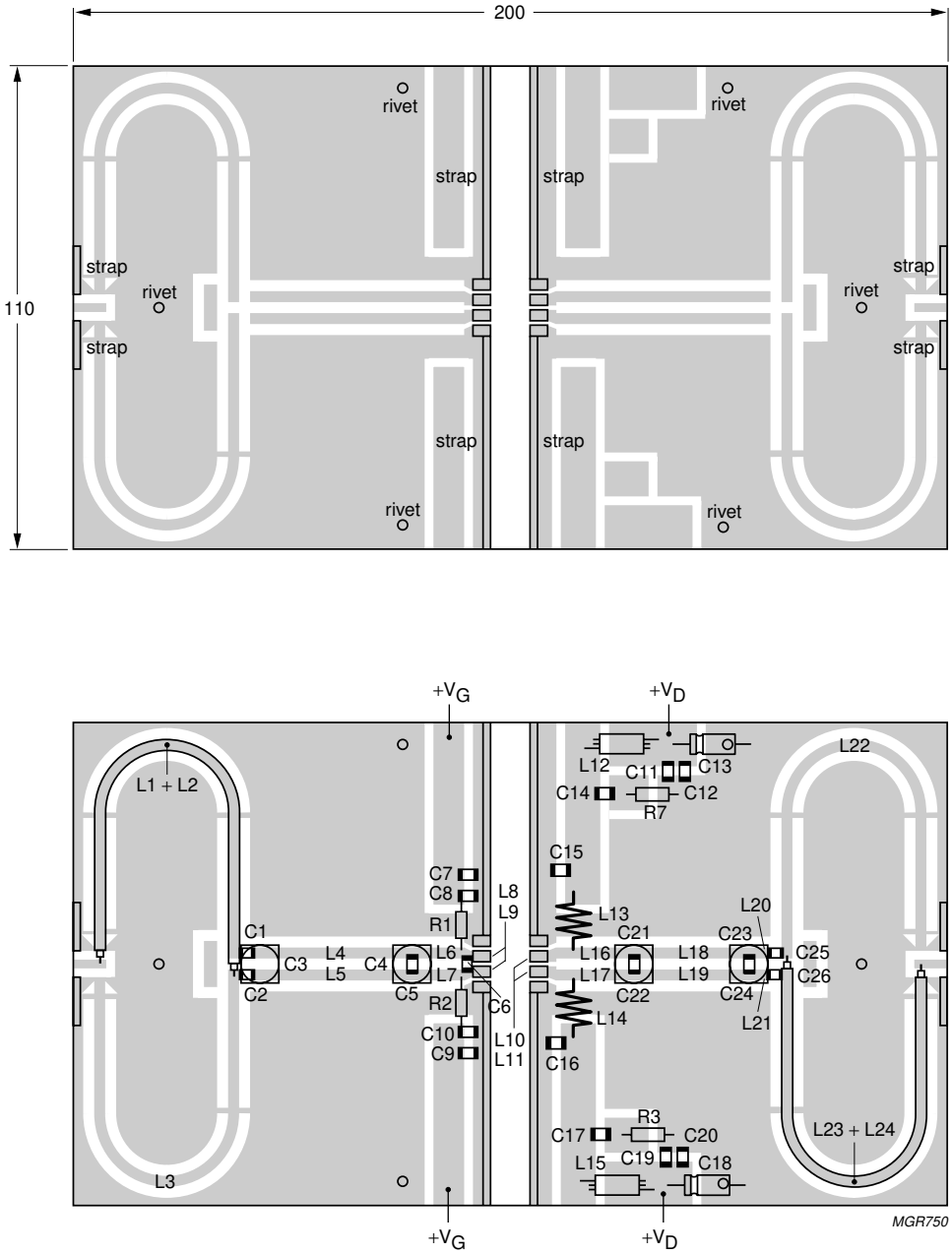
Fig.11 Test circuit for class-B operation.

List of components class-B test circuit (see Figs 11 and 12)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2, C25, C26	multilayer ceramic chip capacitor; note 1	91 pF		
C3	film dielectric trimmer	4 to 40 pF		2222 809 08002
C4	multilayer ceramic chip capacitor; note 1	180 pF		
C5, C22, C24	film dielectric trimmer	5 to 60 pF		2222 809 08003
C6	multilayer ceramic chip capacitor; note 2	100 pF		
C7, C9, C12, C14, C17, C19	multilayer ceramic chip capacitor; note 1	100 nF		2222 852 47104
C8, C10	multilayer ceramic chip capacitor; note 1	680 pF		
C11, C20	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C13, C18	electrolytic capacitor	10 μF, 63 V		
C15, C16, C21	multilayer ceramic chip capacitor; note 1	82 pF		
C23	multilayer ceramic chip capacitor; note 1	33 pF		
L1, L3, L22, L24	stripline; note 3	55 Ω	111 × 2.5 mm	
L2, L23	semi-rigid cable	50 Ω	length 111 mm ext. dia 2.2 mm	
L4, L5	stripline; note 3	50 Ω	38 × 2.8 mm	
L6, L7	stripline; note 3	50 Ω	9 × 2.8 mm	
L8, L9	stripline; note 3	50 Ω	8 × 2.8 mm	
L10, L11	stripline; note 3	50 Ω	11 × 2.8 mm	
L12, L15	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L13, L14	4 turns enamelled 1 mm copper wire	50 nH	length 6.5 mm int. dia. 4 mm leads 2 × 5 mm	
L16, L17	stripline; note 3	50 Ω	16 × 2.8 mm	
L18, L19	stripline; note 3	50 Ω	25 × 2.8 mm	
L20, L21	stripline; note 3	50 Ω	3 × 2.8 mm	
R1, R2	metal film resistor	0.4 W, 10 Ω		
R3, R4	10 turns potentiometer	50 kΩ		
R5, R6	metal film resistor	0.4 W, 205 kΩ		
R7, R8	metal film resistor	1 W, 21.5 Ω		

Notes

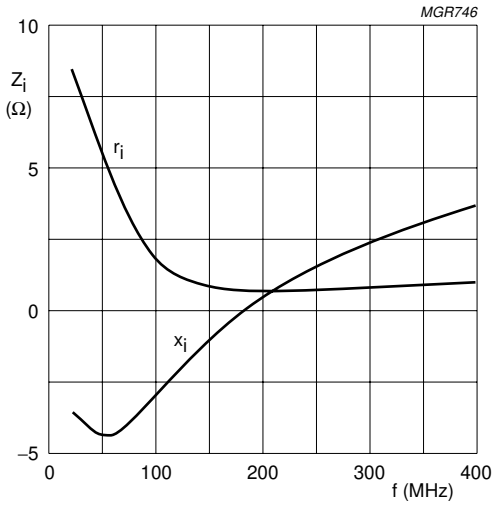
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed-circuit board with epoxy glass dielectric (ε_r = 4.5); thickness $^1/_{16}$ inch. The other side of the board is fully metallized and used as a ground plane. The ground planes on each side of the board are connected together by means of copper straps and hollow rivets.



Dimensions in mm.

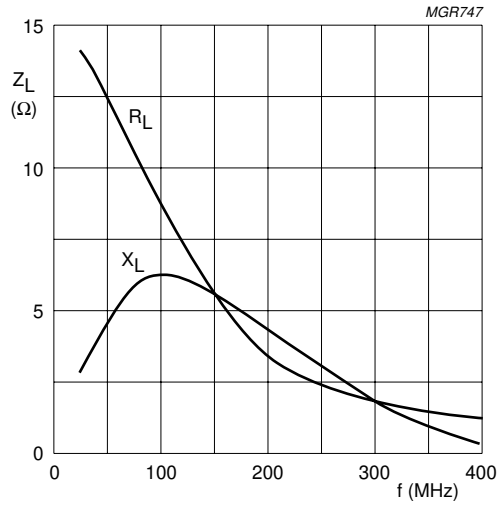
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 50 mA;
R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.13 Input impedance as a function of frequency (series components); typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 50 mA;
R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.14 Load impedance as a function of frequency (series components); typical values per section.

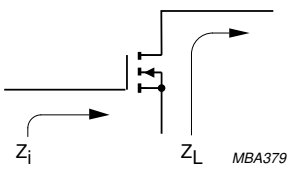
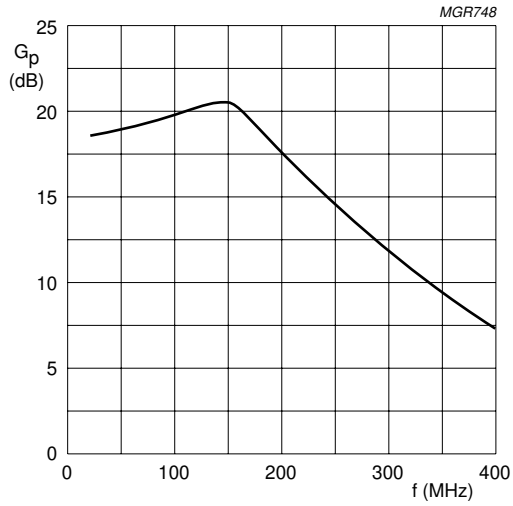


Fig.15 Definition of MOS impedance.

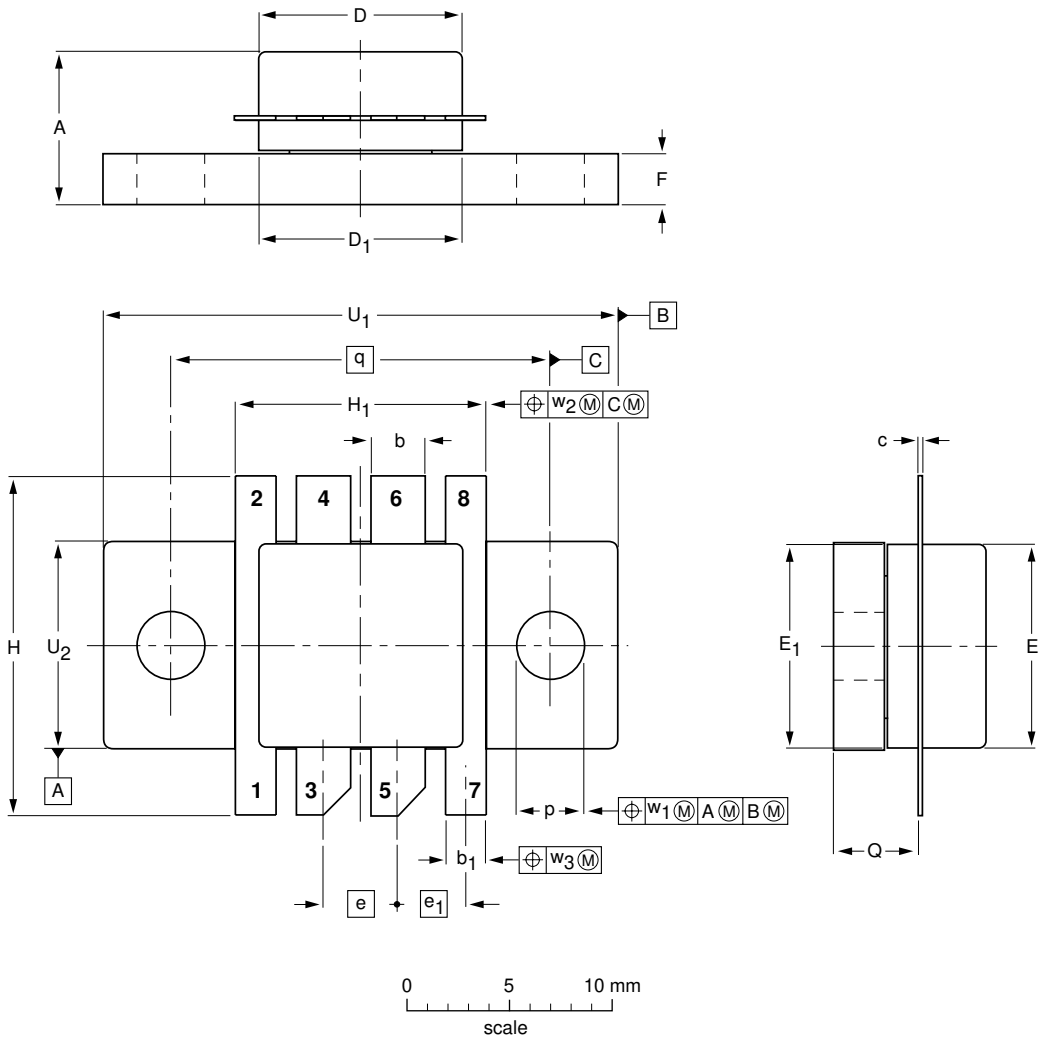


Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 50 mA;
R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.16 Power gain as a function of frequency; typical values per section.

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 8 leads **SOT161A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	e_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	7.27 6.47	2.93 2.66	2.04 1.77	0.18 0.10	10.22 10.00	10.21 9.94	10.21 10.00	10.21 9.94	3.80	3.50	2.70 2.08	16.81 16.21	12.83 12.57	3.33 3.07	4.32 4.06	18.42	24.97 24.71	10.34 10.08	0.25	0.51	0.25
inches	0.286 0.255	0.115 0.105	0.080 0.070	0.007 0.004	0.402 0.394	0.402 0.391	0.402 0.394	0.402 0.391	0.150	0.138	0.106 0.082	0.662 0.638	0.505 0.495	0.131 0.121	0.170 0.160	0.725	0.983 0.973	0.407 0.397	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT161A						~~99-03-29~~ 99-10-04

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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