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BLF6G20-180PN

Power LDMOS transistor

Rev. 4 — 1 September 2015



1. Product profile

1.1 General description

180 W LDMOS power transistor for base station applications at frequencies from 1800 MHz to 2000 MHz.

Table 1.Typical performance

RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Mode of operation	f	V _{DS}	P _{L(AV)}	Gp	η _D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	1805 to 1880	32	50	18	29.5	-35 <mark>[1]</mark>

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Typical 2-carrier W-CDMA performance at frequencies of 1805 MHz and 1880 MHz, a supply voltage of 32 V and an I_{Dq} of 1600 mA:
 - Average output power = 50 W
 - Power gain = 18 dB (typ)
 - Efficiency = 29.5 %
 - ♦ ACPR = -35 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1800 MHz to 2000 MHz)
- Internally matched for ease of use
- Qualified up to a supply voltage of 32 V
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

 RF power amplifiers for W-CDMA base stations and multicarrier applications in the 1800 MHz to 2000 MHz frequency range

2. Pinning information

Table 2.	Pinning		
Pin	Description	Simplified outline Graphic s	ymbol
1	drain1		
2	drain2		
3	gate1		- 1
4	gate2	3 4	5
5	source		
		'F	Ţ
			2 sym117

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information				
Type number Package				
	Name	Description	Version	
BLF6G20-180PN	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A	

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Мах	Unit
V _{DS}	drain-source voltage		-	65	V
V _{GS}	gate-source voltage		-0.5	+13	V
T _{stg}	storage temperature		-65	+150	°C
T _{case}	case temperature		-	150	°C
Tj	junction temperature		-	225	°C

5. Thermal characteristics

Table 6.

Table 5.	Thermal characteristics			
Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-case)}	thermal resistance from junction to case	T_{case} = 80 °C; $P_{L(AV)}$ = 50 W	0.45	K/W

6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.5 mA	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V_{DS} = 10 V; I _D = 144 mA	1.575	1.9	2.3	V
V _{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I _D = 800 mA	1.725	2.1	2.45	V
I _{DSS}	drain leakage current	$V_{GS} = 0 V$				
		V _{DS} = 28 V	-	-	3	μA
		V _{DS} = 60 V	-	-	5	μA
I _{DSX}	drain cut-off current	$\label{eq:VGS} \begin{array}{l} V_{\mathrm{GS}} = V_{\mathrm{GS}(\mathrm{th})} + 3.75 \ V; \\ V_{\mathrm{DS}} = 10 \ V \end{array}$	-	25	-	A
I _{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	300	nA
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 7.2 A	-	10	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ I _D = 5 A	-	0.1	0.165	Ω

7. Application information

Table 7. Application information

Characteristics

Mode of operation: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 PDPCH; $f_1 = 1802.5$ MHz; $f_2 = 1807.5$ MHz; $f_3 = 1872.5$ MHz; $f_4 = 1877.5$ MHz; RF performance at $V_{DS} = 32$ V; $I_{Dq} = 1600$ mA; $T_{case} = 25$ °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G _p	power gain	$P_{L(AV)} = 50 W$	16.8	18	19.2	dB
RLin	input return loss	$P_{L(AV)} = 50 W$	-	-10	-6.5	dB
η_D	drain efficiency	$P_{L(AV)} = 50 W$	26	29.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 50 W$	-	-35	-33	dBc

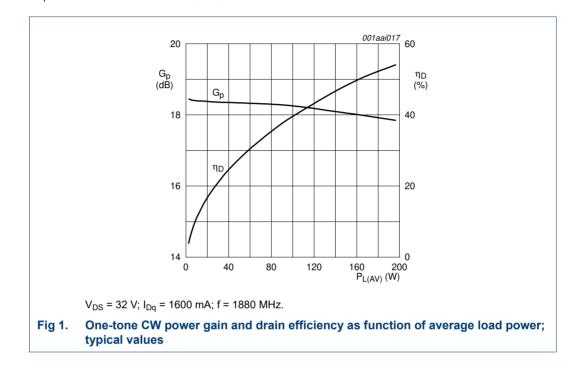
Table 8. Application information

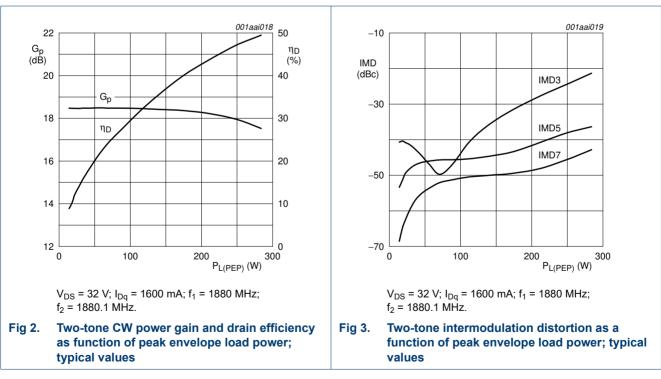
Mode of operation: 1-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 PDPCH; $f_1 = 1872.5$ MHz; $f_2 = 1877.5$ MHz; RF performance at $V_{DS} = 32$ V; $I_{Dg} = 1600$ mA; $T_{case} = 25$ °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
PARO	output peak-to-average ratio	P _{L(AV)} = 115 W; at 0.01 % probability on CCDF	4.1	4.3	-	dB

7.1 Ruggedness in class-AB operation

The BLF6G20-180PN is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dg} = 1600 mA; P_L = 180 W (CW); f = 1880 MHz.

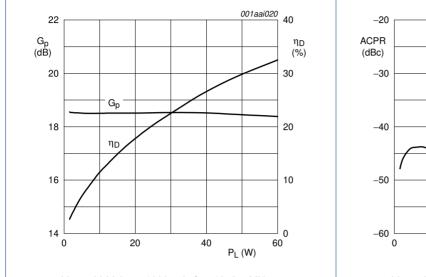




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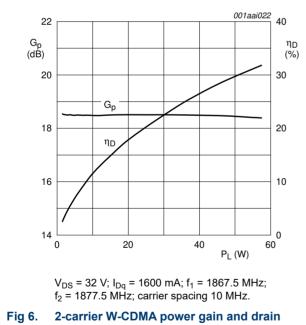
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Power LDMOS transistor

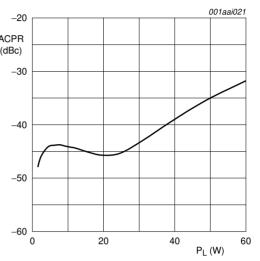


 V_{DS} = 32 V; I_{Dq} = 1600 mA; f_1 = 1872.5 MHz; f_2 = 1877.5 MHz; carrier spacing 5 MHz.



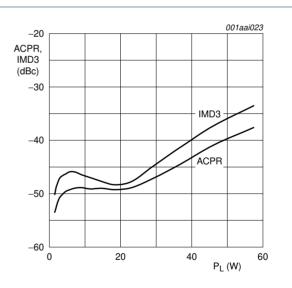


efficiency as function of load power; typical values



 V_{DS} = 32 V; I_{Dq} = 1600 mA; f_1 = 1872.5 MHz; f_2 = 1877.5 MHz; carrier spacing 5 MHz.

Fig 5. 2-carrier W-CDMA adjacent channel power ratio as a function of load power; typical values

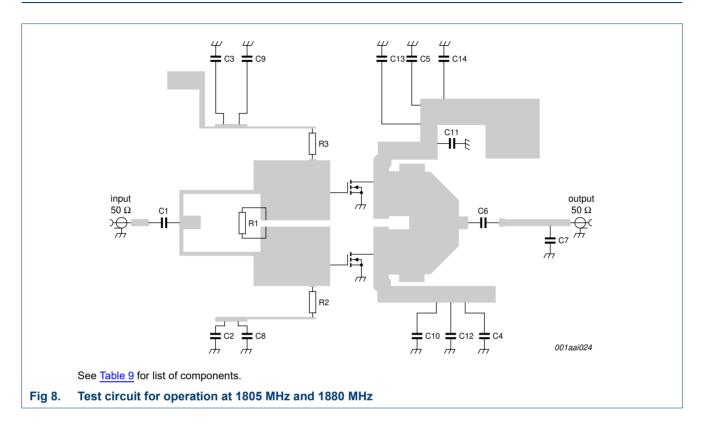


 V_{DS} = 32 V; I_{Dq} = 1600 mA; f₁ = 1867.5 MHz; f₂ = 1877.5 MHz; carrier spacing 10 MHz.

Fig 7. 2-carrier W-CDMA adjacent channel power ratio and third order intermodulation distortion as function of load power; typical values

Power LDMOS transistor

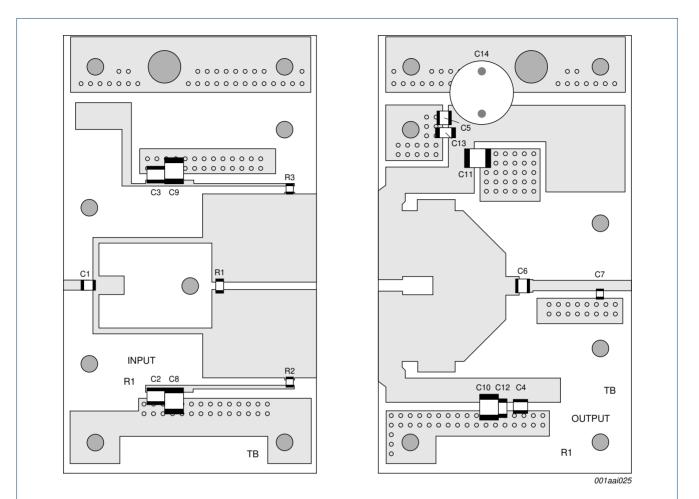
8. Test information



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Power LDMOS transistor



Striplines are on a double copper-clad Rogers R04350 Printed-Circuit Board (PCB) with ε_r = 3.5 and thickness = 0.76 mm. See Table 9 for list of components.

Fig 9. Component layout for 1805 MHz and 1880 MHz test circuit

Table 9.List of components

For test circuit, see Figure 8 and Figure 9.

Component	Description	Value	Remarks
C1	ATC multilayer ceramic chip capacitor	6.2 pF	<u>[1]</u>
C2, C3	ATC multilayer ceramic chip capacitor	16 pF	<u>[1]</u>
C4, C5, C6	ATC multilayer ceramic chip capacitor	18 pF	[2]
C7	ATC multilayer ceramic chip capacitor	1.1 pF	<u>[3]</u>
C8, C9, C10, C11	TDK multilayer ceramic chip capacitor	4.7 μF	
C12, C13	AVX multilayer ceramic chip capacitor	220 nF	
C14	electrolytic capacitor	100 μF; 63 V	[2]
R1	chip resistor	33 Ω	
R2, R3	chip resistor	8.2 Ω	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] American Technical Ceramics type 180R or capacitor of same quality.

[3] American Technical Ceramics type 100A or capacitor of same quality.

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Power LDMOS transistor

9. Package outline

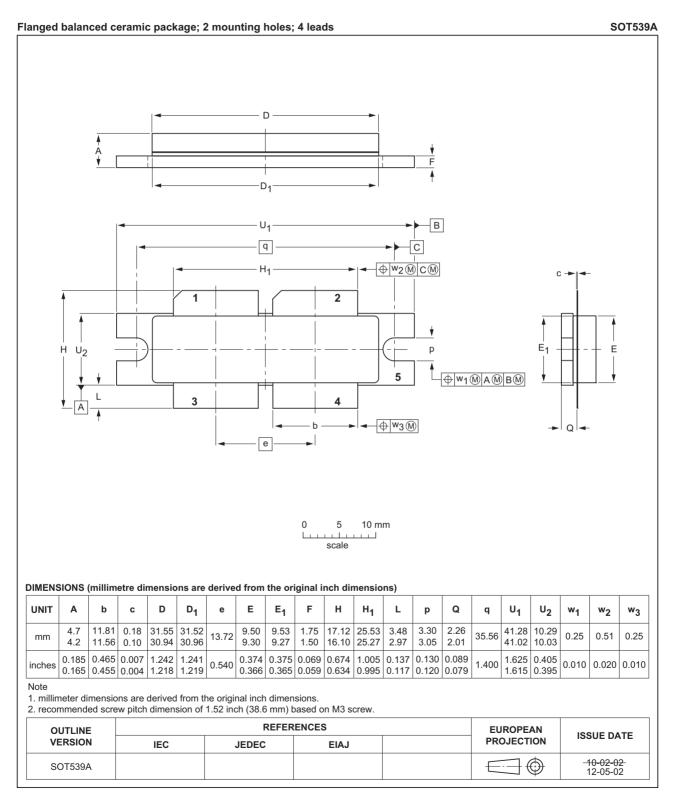


Fig 10. Package outline SOT539A

10. Abbreviations

Table 10. Abl	previations
Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
IMD	InterModulation Distortion
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11.Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G20-180PN#4	20150901	Product data sheet	-	BLF6G20-180PN_3
Modifications:	 The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. 			
BLF6G20-180PN_3	20090330	Product data sheet	-	BLF6G20-180PN_2
BLF6G20-180PN_2	20090121	Preliminary data sheet	-	BLF6G20-180PN_1
BLF6G20-180PN_1	20080428	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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