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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# BLF7G21L-160P; BLF7G21LS-160P

Power LDMOS transistor

Rev. 4 — 1 September 2015

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 1800 MHz to 2050 MHz, also suitable for operation at 1495 MHz to 1511 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in a common source class-AB production test circuit.

Mode of operation	f (MHz)	$I_{DQ}$ (mA)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	ACPR (dBc)
2-carrier W-CDMA	1930 to 1990	1080	28	45	18	34	-30 <a href="#">[1]</a>
1-carrier W-CDMA	1930 to 1990	1080	28	50	18.0	36	-34 <a href="#">[2]</a>

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

[2] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

### 1.2 Features and benefits

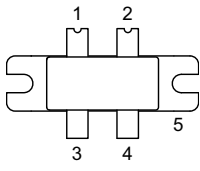
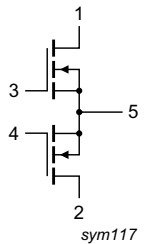
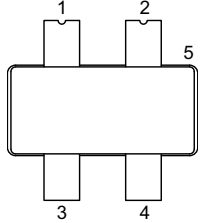
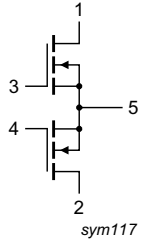
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation (1800 MHz to 2050 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1800 MHz to 2050 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF7G21L-160P (SOT1121A)</b>			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		
<b>BLF7G21LS-160P (SOT1121B)</b>			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G21L-160P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A
BLF7G21LS-160P	-	earless flanged ceramic package; 4 leads	SOT1121B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$I_D$	drain current		-	32.5	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 100\text{ W}$	0.41	K/W

## 6. Characteristics

**Table 6. Characteristics**

$T_j = 25\text{ °C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.9\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 90\text{ mA}$	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	14	-	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	200	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 4.5\text{ A}$	-	7	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 3.15\text{ A}$	-	0.15	-	$\Omega$

## 7. Test information

**Table 7. Application information**

Mode of operation: 2-carrier W-CDMA; PAR 8.4 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 PDPCH;  $f_1 = 1932.5\text{ MHz}$ ;  $f_2 = 1937.5\text{ MHz}$ ;  $f_3 = 1982.5\text{ MHz}$ ;  $f_4 = 1987.5\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 1080\text{ mA}$ ;  $T_{case} = 25\text{ °C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 45\text{ W}$	17.0	18.0	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 45\text{ W}$	-	-15	-8	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 45\text{ W}$	31	34	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)} = 45\text{ W}$	-	-30	-25	dBc
$ACPR_{10M}$	adjacent channel power ratio (10 MHz)	$P_{L(AV)} = 45\text{ W}$	-	-	-	dBc

**Table 8. Application information**

Mode of operation: 1-carrier W-CDMA; PAR 7.2 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 PDPCH;  $f_1 = 1932.5\text{ MHz}$ ;  $f_2 = 1987.5\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 1080\text{ mA}$ ;  $T_{case} = 25\text{ °C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$PAR_O$	output peak-to-average ratio	$P_{L(AV)} = 80\text{ W}$ ; at 0.01 % probability on CCDF	4.0	4.5	-	dB

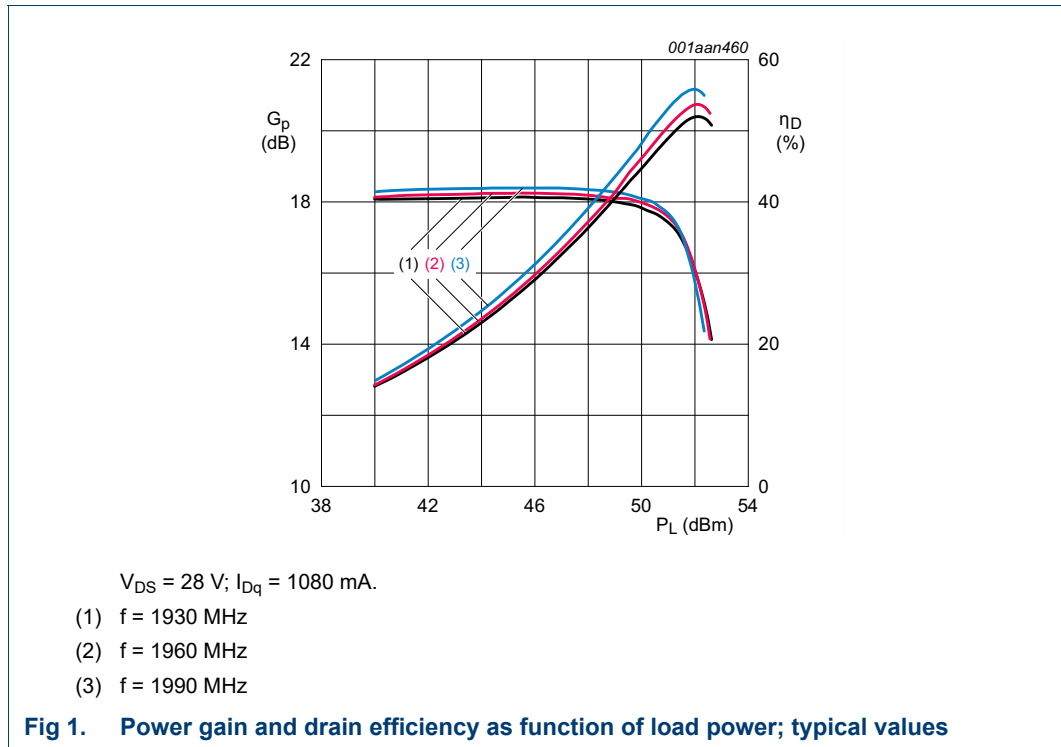
7.1 Ruggedness in class-AB operation

The BLF7G21L-160P and BLF7G21LS-160P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:

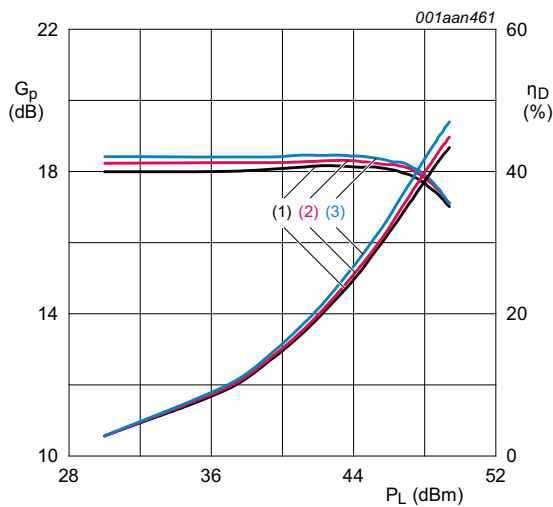
$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 1080\text{ mA}$ ;  $P_L = 160\text{ W (CW)}$ ,  $f = 1805\text{ MHz}$ ,

$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 350\text{ mA}$ ;  $P_L = 31.6\text{ W (IS-95)}$ ;  $P_L = 90\text{ W (pulsed CW, } \delta = 10\% \text{, } t_p = 100\text{ }\mu\text{s, per section)}$ ,  $f = 1495\text{ MHz}$ .

7.2 CW

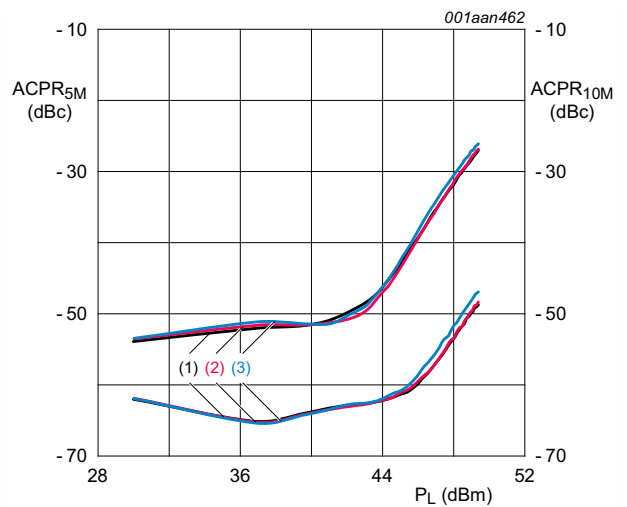


7.3 1-Carrier W-CDMA



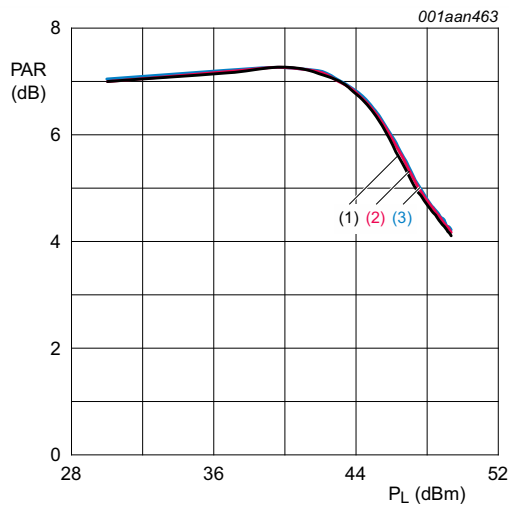
$V_{DS} = 28$  V;  $I_{Dq} = 1080$  mA.  
 (1)  $f = 1930$  MHz  
 (2)  $f = 1960$  MHz  
 (3)  $f = 1990$  MHz

**Fig 2. Power gain and drain efficiency as function of load power; typical values**



$V_{DS} = 28$  V;  $I_{Dq} = 1080$  mA.  
 (1)  $f = 1930$  MHz  
 (2)  $f = 1960$  MHz  
 (3)  $f = 1990$  MHz

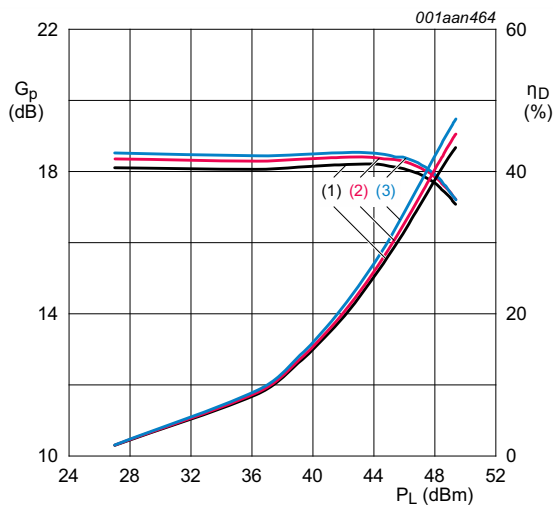
**Fig 3. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as a function of load power; typical values**



$V_{DS} = 28$  V;  $I_{Dq} = 1080$  mA.  
 (1)  $f = 1930$  MHz  
 (2)  $f = 1960$  MHz  
 (3)  $f = 1990$  MHz

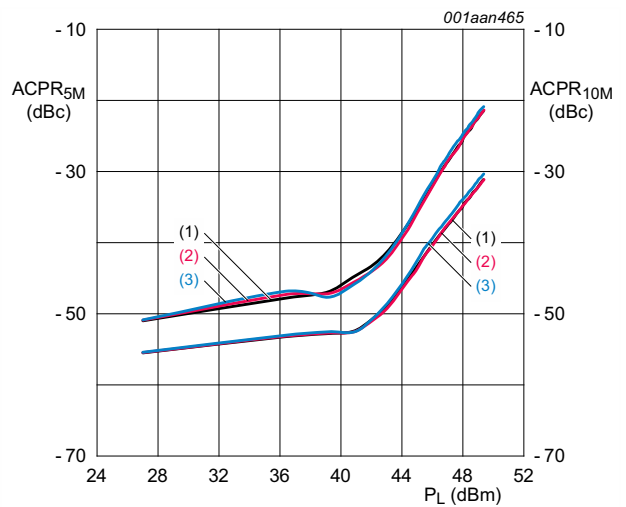
**Fig 4. Peak-to-average ratio as a function of load power; typical values**

7.4 2-Carrier W-CDMA 5 MHz



$V_{DS} = 28\text{ V}; I_{Dq} = 1080\text{ mA}$ .  
 (1)  $f = 1930\text{ MHz}$   
 (2)  $f = 1960\text{ MHz}$   
 (3)  $f = 1990\text{ MHz}$

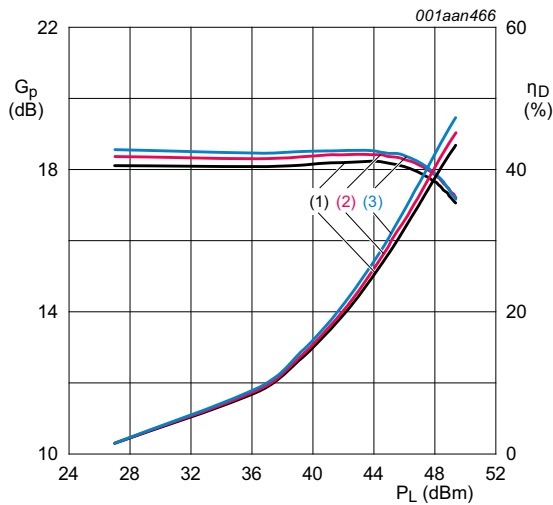
**Fig 5. Power gain and drain efficiency as function of load power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 1080\text{ mA}$ .  
 (1)  $f = 1930\text{ MHz}$   
 (2)  $f = 1960\text{ MHz}$   
 (3)  $f = 1990\text{ MHz}$

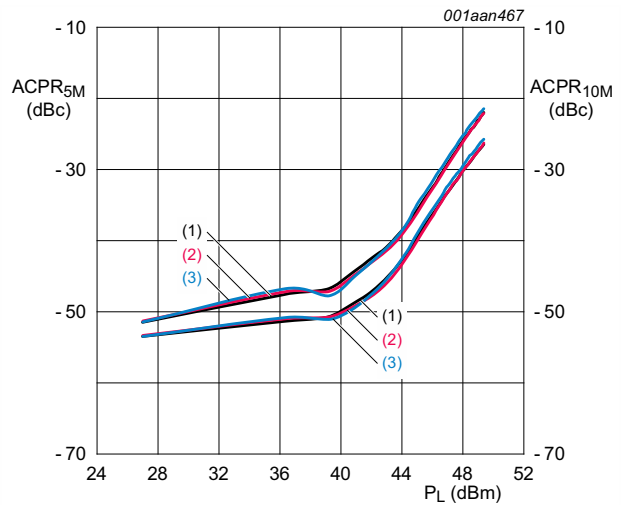
**Fig 6. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as a function of load power; typical values**

7.5 2-Carrier W-CDMA 10 MHz



$V_{DS} = 28\text{ V}; I_{Dq} = 1080\text{ mA}$ .  
 (1)  $f = 1930\text{ MHz}$   
 (2)  $f = 1960\text{ MHz}$   
 (3)  $f = 1990\text{ MHz}$

**Fig 7. Power gain and drain efficiency as function of load power; typical values**

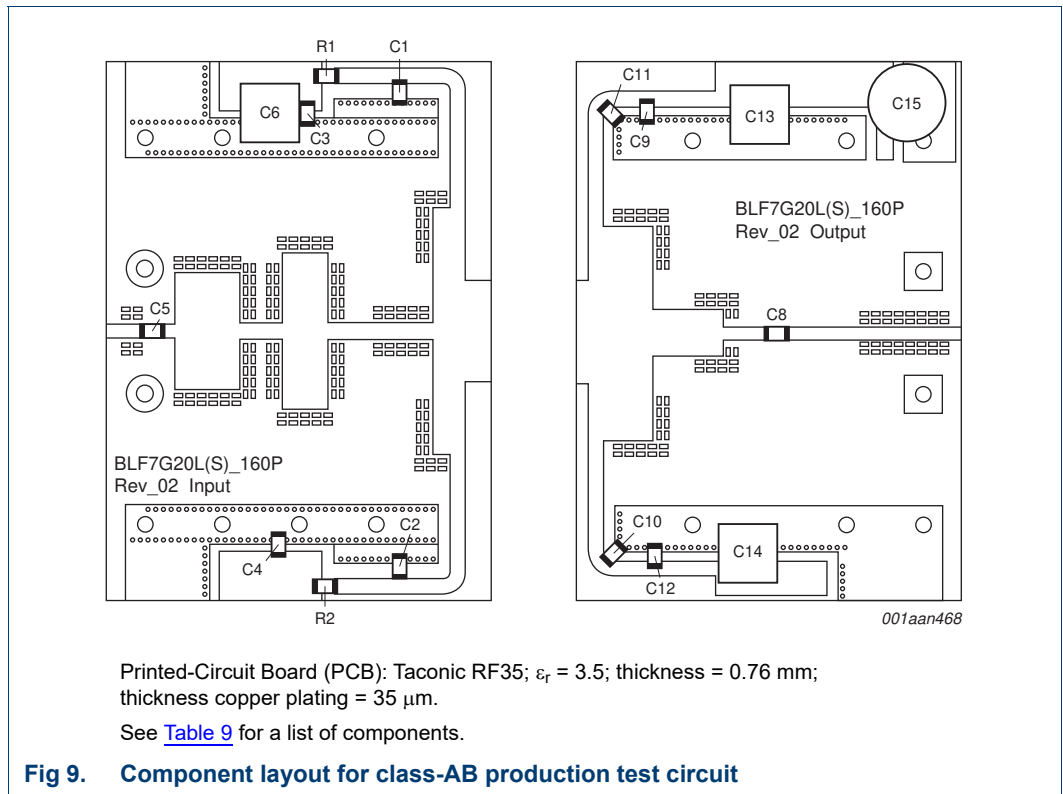


$V_{DS} = 28\text{ V}; I_{Dq} = 1080\text{ mA}$ .  
 (1)  $f = 1930\text{ MHz}$   
 (2)  $f = 1960\text{ MHz}$   
 (3)  $f = 1990\text{ MHz}$

**Fig 8. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as a function of load power; typical values**



7.6 Test circuit



**Table 9. List of components**

For test circuit see [Figure 9](#).

Component	Description	Value	Remarks
C1, C2, C5, C9, C10	multilayer ceramic chip capacitor	68 pF	[1]
C3, C4, C11, C12	multilayer ceramic chip capacitor	820 pF	[2]
C6, C13, C14	multilayer ceramic chip capacitor	10 $\mu\text{F}$	[3]
C8	multilayer ceramic chip capacitor	10 pF	[1]
C15	electrolytic capacitor	470 $\mu\text{F}$ ; 63 V	
R1, R2	SMD resistor	12 $\Omega$	Philips 1206

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.

[3] TDK or capacitor of same quality.

7.7 Impedance information

Table 10. Typical impedance

Typical values valid for both section in parallel unless otherwise specified.

f MHz	Z <sub>S</sub> Ω	Z <sub>L</sub> Ω
1750	0.99 – j4.09	2.32 – j2.35
1805	1.12 – j4.39	2.20 – j2.20
1840	1.23 – j4.58	2.08 – j2.14
1880	1.31 – j4.74	1.94 – j2.12
1930	1.49 – j5.01	1.76 – j2.15
1960	1.61 – j5.19	1.66 – j2.20
1990	1.75 – j5.36	1.56 – j2.26
2020	1.91 – j5.54	1.48 – j2.34
2050	2.13 – j5.75	1.4 – j2.42

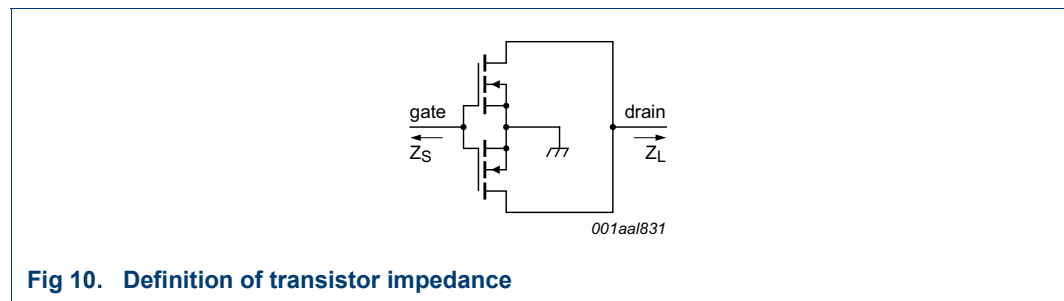
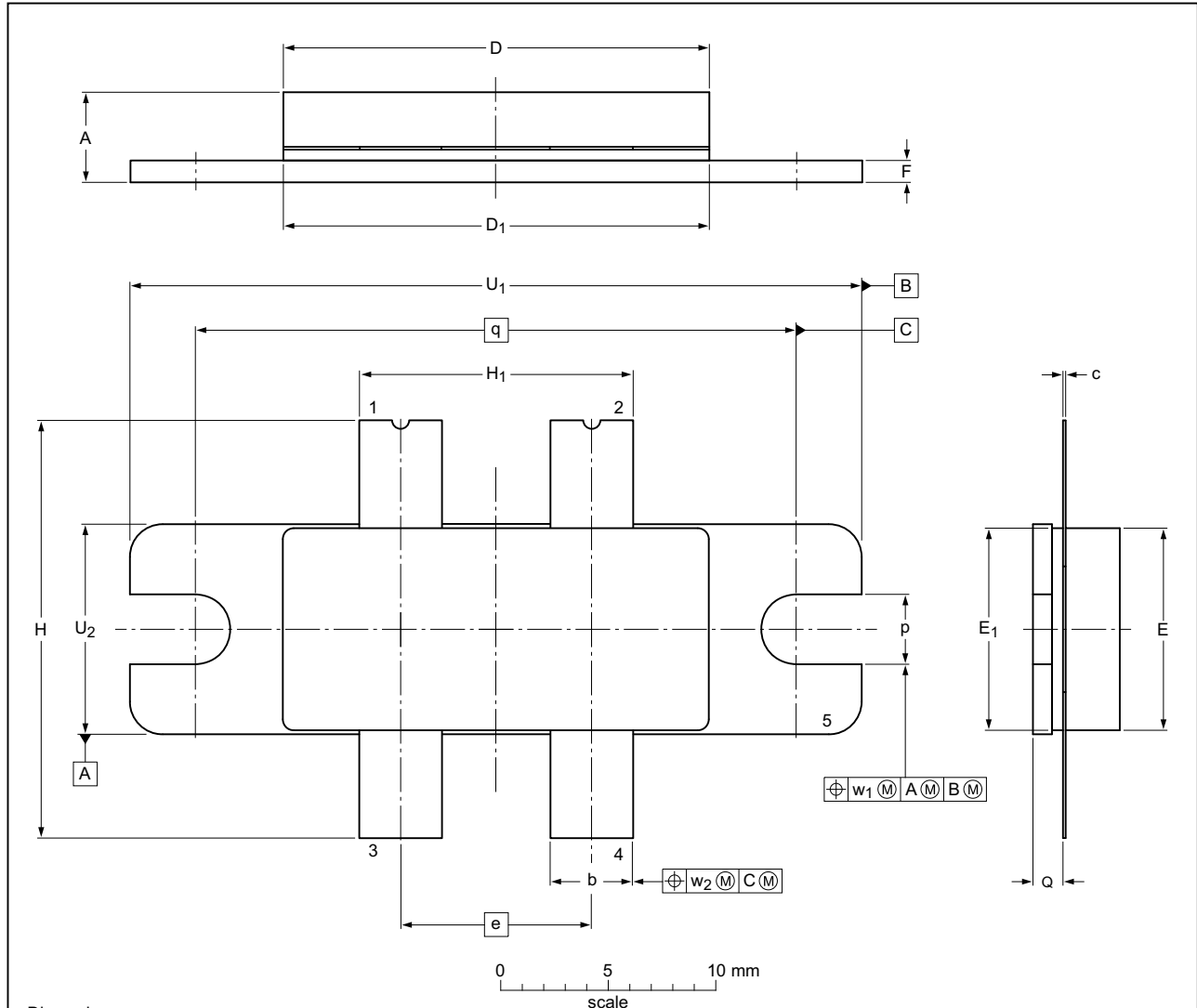


Fig 10. Definition of transistor impedance

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads

SOT1121A



Dimensions

Unit <sup>(1)</sup>	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	p	Q <sup>(2)</sup>	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	max 4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	3.38	1.70	34.16	9.91		0.25	0.51
	nom					8.89								27.94				
	min 3.45	3.68	0.10	19.61	19.66		9.27	9.27	0.89	18.92	12.57	3.12	1.45	33.91	9.65			
inches	max 0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.133	0.067	1.345	0.39		0.01	0.02
	nom					0.35								1.1				
	min 0.136	0.145	0.004	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.123	0.057	1.335	0.38			

Note

- 1. millimeter dimensions are derived from the original inch dimensions.
- 2. dimension is measured 0.030 inch (0.76 mm) from the body.

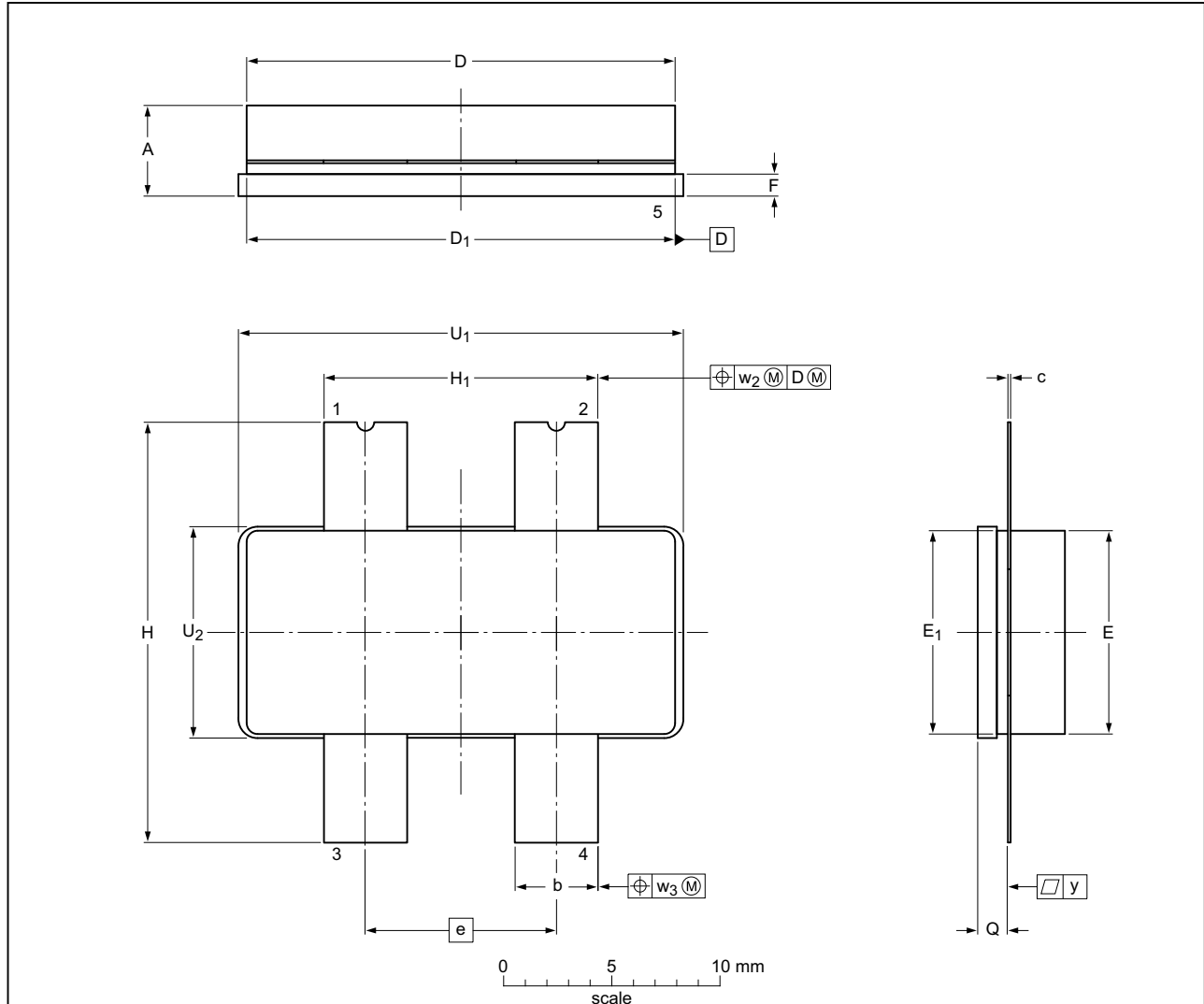
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Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1121A					09-10-12 10-02-02

Fig 11. Package outline SOT1121A

Earless flanged ceramic package; 4 leads

SOT1121B



Dimensions

Unit <sup>(1)</sup>	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	Q	U <sub>1</sub>	U <sub>2</sub>	w <sub>2</sub>	w <sub>3</sub>	y
mm	max	4.75	3.94	0.18	20.02	19.96	9.53	9.53	1.14	19.94	12.83	1.70	20.70	9.91	0.51	0.25	0.25
	nom					8.89											
	min	3.45	3.68	0.08	19.61	19.66	9.27	9.27	0.89	18.92	12.57	1.45	20.45	9.65			
inches	max	0.187	0.155	0.007	0.788	0.786	0.375	0.375	0.045	0.785	0.505	0.067	0.815	0.39	0.02	0.01	0.01
	nom					0.35											
	min	0.136	0.145	0.003	0.772	0.774	0.365	0.365	0.035	0.745	0.495	0.057	0.805	0.38			

Note

1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121b\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1121B					09-12-14 12-06-07

Fig 12. Package outline SOT1121B

## 9. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 10. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G21L-160P_7G21LS-160P#4	20150901	Product data sheet	-	BLF7G21L-160P_7G21LS-160P v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BLF7G21L-160P_7G21LS-160P v.3	20140210	Product data sheet	-	BLF7G21L-160P_7G21LS-160P v.2
BLF7G21L-160P_7G21LS-160P v.2	20111013	Product data sheet	-	BLF7G21L-160P_7G21LS-160P v.1
BLF7G21L-160P_7G21LS-160P v.1	20110401	Objective data sheet	-	-

## 11. Legal information

### 11.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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