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Ampleon

UHF power LDMOS transistor BLF861A

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Designed to withstand abrupt load mismatch errors
- Source on underside eliminates DC isolators; reducing common mode inductance
- Designed for broadband operation (UHF band)
- Internal input and output matching for high gain and optimum broadband operation.

APPLICATIONS

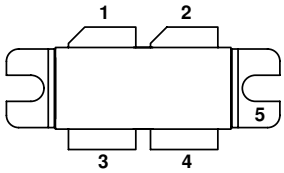
- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS push-pull transistor in a SOT540A package with ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT540A

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source connected to flange



Top view MBK777

Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source 860 MHz test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	ΔG_p (dB)
CW, class-AB	860	32	150	>13.5 typ. 14.5	>50	≤1
PAL BG (TV); class-AB	860 (ch 69)	32	>150 typ. 170 (peak sync)	>14	>40	note 1

Note

1. Sync compression: input sync ≥ 33%; output sync 27%.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±15	V
I_D	drain current (DC)		–	18	A
P_{tot}	total power dissipation	T_{mb} ≤ 25 °C	–	318	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 318 W	0.55	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.2	K/W

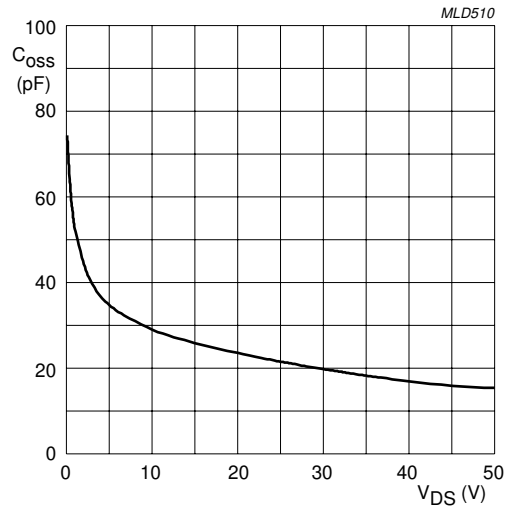
CHARACTERISTICS

T_j = 25 °C; per section; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 1.5 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 150 mA	4	–	5.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 32 V	–	–	2.2	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	18	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	25	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 4 A	–	4	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 4 A	–	160	–	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz (1)	–	82	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz (1)	–	40	–	pF
C_{rss}	feedback capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz (1)	–	6	–	pF

Note

1. Capacitance values without internal matching.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.2 Output capacitance as a function of drain-source voltage; typical values per section.

APPLICATION INFORMATION

RF performance in a common source 860 MHz test circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)	d_{Im} (dBc)	ΔG_p (dB)
CW; class-AB	860	32	1	150	>13.5 typ. 14.5	>50	–	≤1
2-tone; class-AB	f_1 = 860 f_1 = 860.1	32	1	150 (PEP)	>14	>40	≤–25	–
PAL BG (TV); class-AB	860 (ch 69)	32	1	> 150 typ. 170 (peak sync)	>14	>40	–	note 1

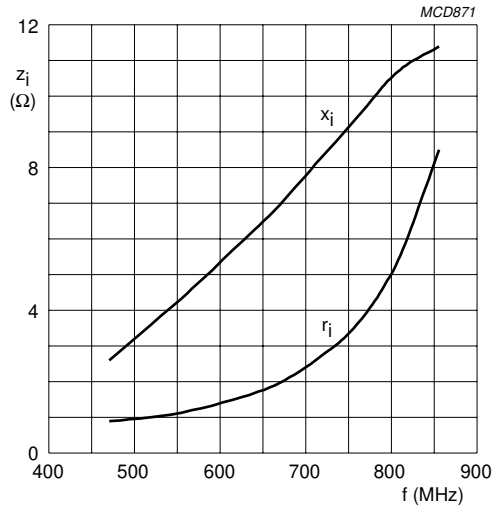
Note

1. Sync compression: input sync ≥ 33%; output sync 27% measured in an 860 MHz test circuit.

Ruggedness in class-AB operation

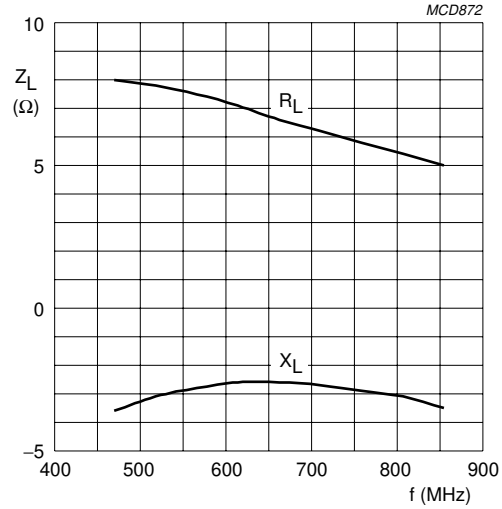
The BLF861A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; f = 860 MHz at rated load power.

The BLF861A is an improved version of the BLF861 on ruggedness and is capable to withstand abrupt source or load mismatch errors under the nominal power condition.



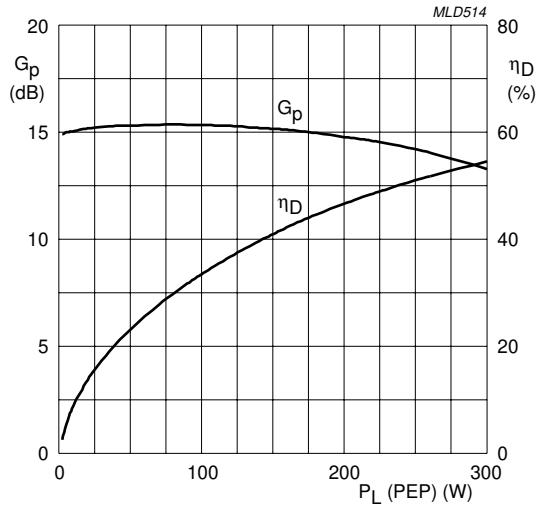
CW, class-AB operation; V_{DS} = 32 V; I_{DQ} = 1 A; P_L = 170 W (total device); T_h = 25 °C.

Fig.3 Input impedance as a function of frequency (series components); typical push-pull values.



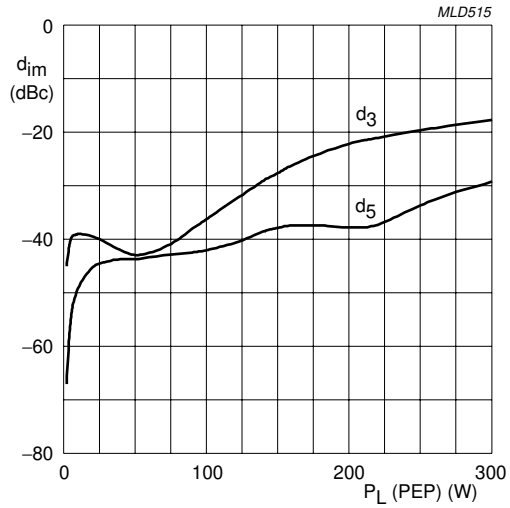
CW, class-AB operation; V_{DS} = 32 V; I_{DQ} = 1 A; P_L = 170 W (total device); T_h = 25 °C.

Fig.4 Load impedance as a function of frequency (series components); typical push-pull values.



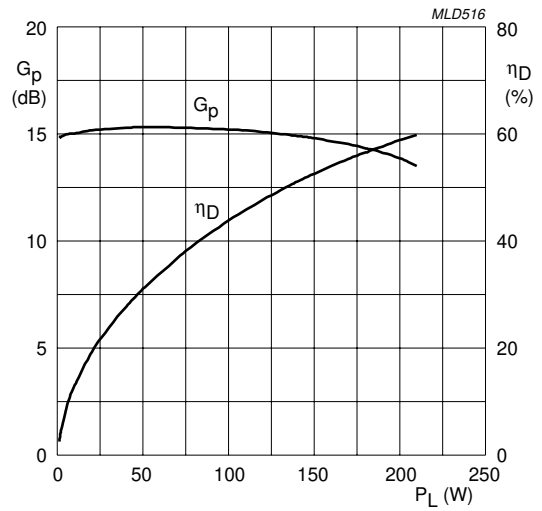
T_h = 25 °C; V_{DS} = 32 V; I_{DQ} = 1 A.
2-tone: f_1 = 860 MHz (–6 dB); f_2 = 860.1 MHz (–6 dB)
measured in an 860 MHz test circuit.

Fig.5 Power gain and drain efficiency as functions of peak envelope load power; typical values.



T_h = 25 °C; V_{DS} = 32 V; I_{DQ} = 1 A.
2-tone: f_1 = 860 MHz (–6 dB); f_2 = 860.1 MHz (–6 dB)
measured in an 860 MHz test circuit.

Fig.6 Intermodulation distortion as a function of peak envelope output power; typical values.



T_h = 25 °C; V_{DS} = 32 V; I_{DQ} = 1 A; CW, class-AB; f = 860 MHz;
measured in an 860 MHz test circuit.

Fig.7 Power gain and drain efficiency as functions of load power; typical values.

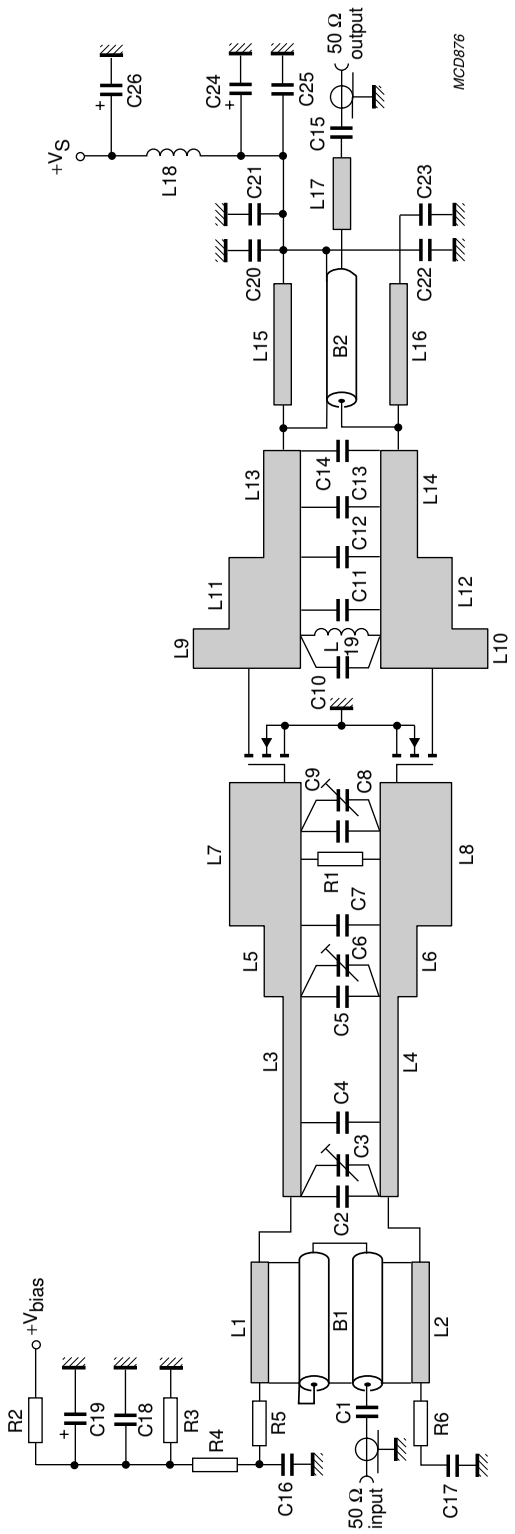


Fig.8 Class-AB common source broadband test circuit.

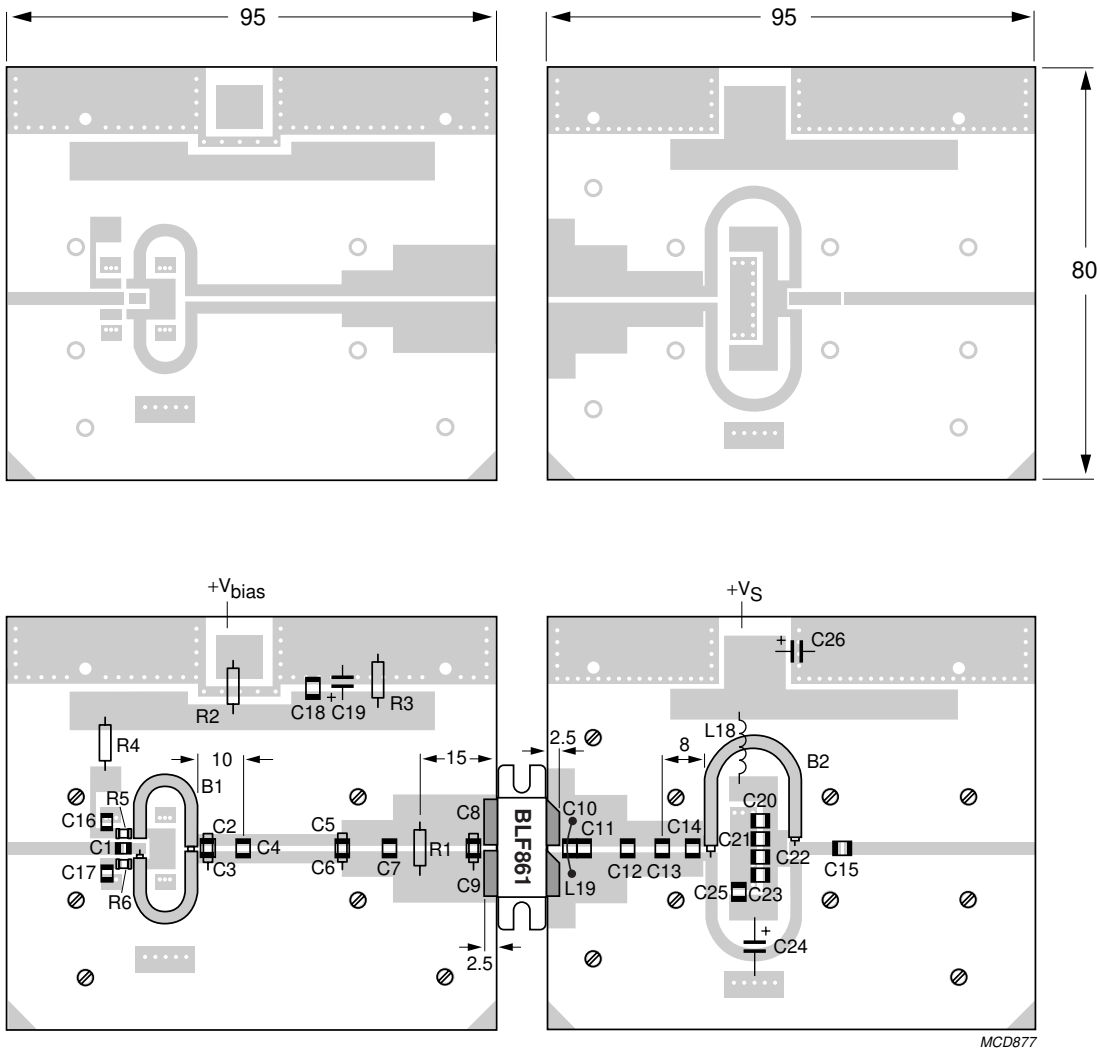
List of components class-AB broadband test circuit (see Figs 8 and 9)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1	multilayer ceramic chip capacitor; note 1	20 pF		
C2	multilayer ceramic chip capacitor; note 1	4.3 pF		
C3, C6, C9	tekelec trimmer	0.6 to 4.5 pF		
C4	multilayer ceramic chip capacitor; note 1	9.1 pF		
C5	multilayer ceramic chip capacitor; note 1	10 pF		
C7	multilayer ceramic chip capacitor; note 1	5.1 pF		
C8	multilayer ceramic chip capacitor; note 1	13 pF		
C10, C11	multilayer ceramic chip capacitor; note 2	8.2 pF		
C12, C13	multilayer ceramic chip capacitor; note 2	6.8 pF		
C14	multilayer ceramic chip capacitor; note 3	1 pF		
C15	multilayer ceramic chip capacitor; note 3	20 pF		
C16, C17	multilayer ceramic chip capacitor	1 nF		
C18	multilayer ceramic chip capacitor	100 nF		
C19, C26	multilayer ceramic chip capacitor	100 μF		
C20, C21, C22, C23	multilayer ceramic chip capacitor; note 2	100 pF		
C24	electrolytic capacitor	1000 μF		
C25	multilayer ceramic chip capacitor	1 μF		2222 595 16754
L1, L2	stripline; note 4		30.6 × 2.4 mm	
L3, L4	stripline; note 4		28 × 2.4 mm	
L5, L6	stripline; note 4		10 × 5 mm	
L7, L8	stripline; note 4		20 × 10 mm	
L9, L10	stripline; note 4		5.5 × 15 mm	
L11, L12	stripline; note 4		10 × 10 mm	
L13, L14	stripline; note 4		15 × 5 mm	
L15, L16	stripline; note 4		48.5 × 2.4 mm	
L17	stripline; note 4		10 × 2.4 mm	
L18	ferrite			
L19	wire inductor (hairpin)		length = 17 mm	
B1	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	70 mm	
B2	semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	48.5 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
R1	resistor	33 Ω		
R2	resistor	1 kΩ		
R3	resistor	100 kΩ		
R4	resistor	100 Ω		
R5, R6	SMD resistor	3.9 Ω		

Notes

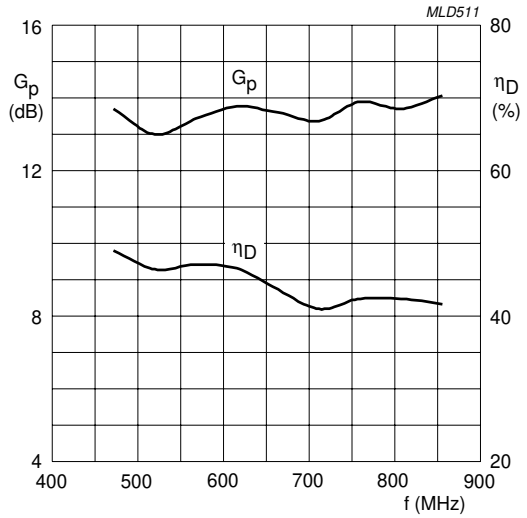
1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 180R or capacitor of same quality.
3. American Technical Ceramics type 100B or capacitor of same quality.
4. The striplines are on a double copper-clad printed-circuit board: Rogers 5880 (ε_r = 2.2); thickness 0.79 mm.



Dimensions in mm.

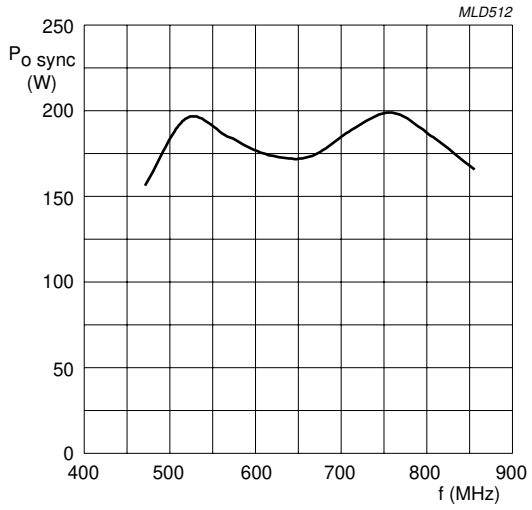
The components are situated on one side of the Rogers 5880 printed-circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through-metallization.

Fig.9 Printed-circuit board and component layout for class-AB broadband test circuit.



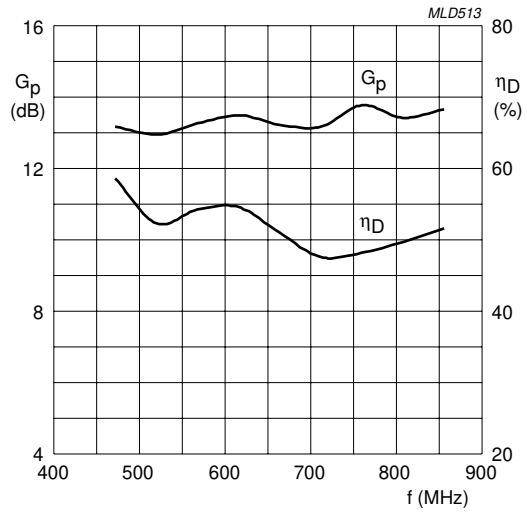
T_h = 25 °C; V_{CE} = 32 V; I_{DQ} = 1 A; PAL BG signal (TV);
sync compression: input 33%, output 27%;
measured in broadband test circuit.

Fig.10 Power gain and drain efficiency as functions of frequency; typical values.



T_h = 25 °C; V_{CE} = 32 V; I_{DQ} = 1 A; PAL BG signal (TV);
sync compression: input 33%, output 27%;
measured in broadband test circuit.

Fig.11 Peak envelope sync power as a function of frequency; typical values.

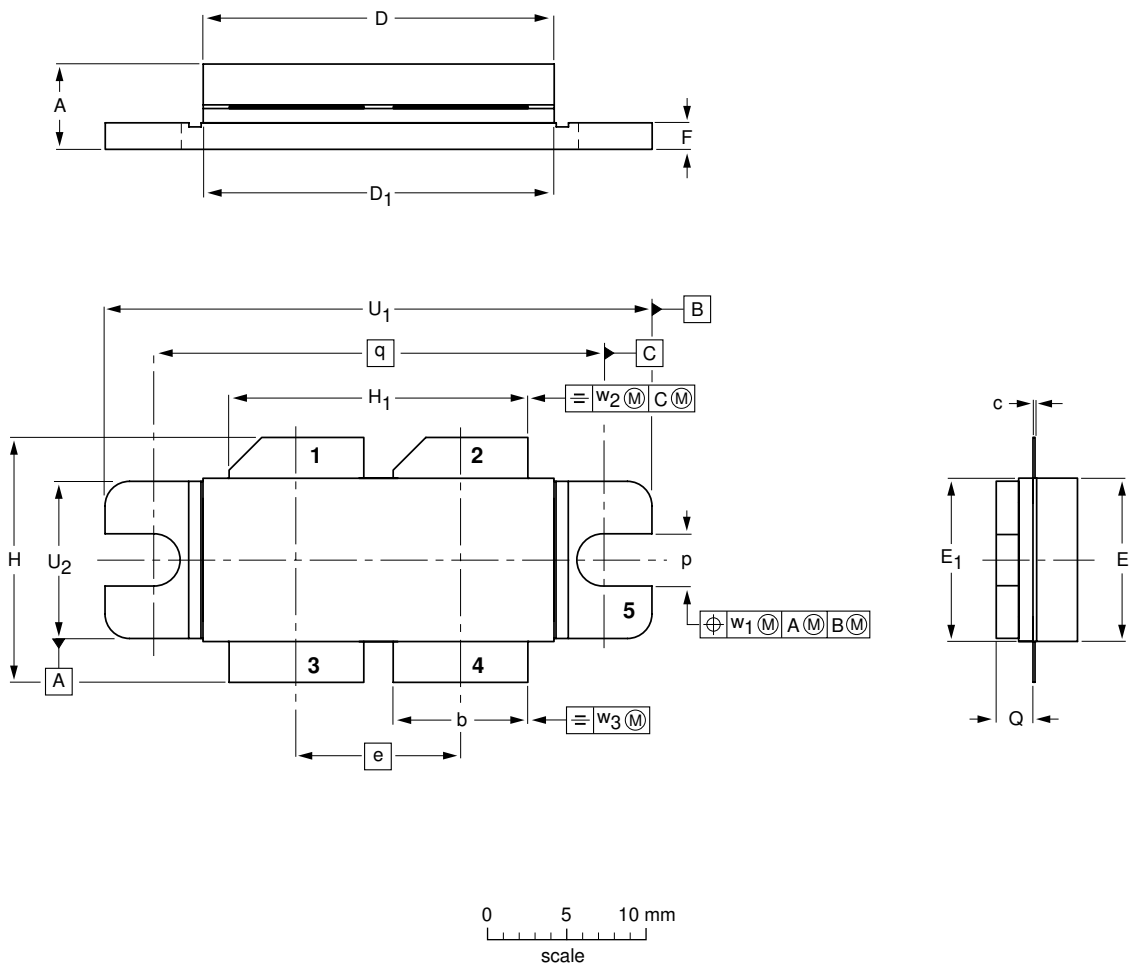


T_h = 25 °C; V_{DS} = 32 V; I_{DQ} = 1 A; CW, class-AB operation;
P_L = 150 W; measured in broadband test circuit.

Fig.12 Power gain and drain efficiency as functions of frequency; typical values.

PACKAGE OUTLINE

Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads **SOT540A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.77 5.00	8.51 8.26	0.15 0.10	22.05 21.64	22.05 21.64	10.21	10.26 10.06	10.31 10.01	1.78 1.52	15.75 14.73	18.72 18.47	3.38 3.12	2.72 2.46	27.94	34.16 33.91	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.335 0.325	0.006 0.004	0.868 0.852	0.868 0.852	0.402	0.404 0.396	0.406 0.394	0.070 0.060	0.620 0.580	0.737 0.727	0.133 0.123	0.107 0.097	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT540A						~~99-08-27~~ 99-12-28

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Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

NOTES

NOTES

NOTES

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