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# BLF8G20LS-140V; BLF8G20LS-140GV Power LDMOS transistor Rev. 3 – 1 September 2015

AMPLEON Product data sheet

#### **Product profile** 1.

### 1.1 General description

140 W LDMOS power transistor for base station applications at frequencies from 1805 MHz to 1990 MHz.

#### **Typical performance** Table 1.

Typical RF performance at  $T_{case} = 25 \ ^{\circ}C$  in a common source class-AB production test circuit.

Test signal	f	l <sub>Dq</sub>	V <sub>DS</sub>	P <sub>L(AV)</sub>	Gp	η <sub>D</sub>	ACPR <sub>5M</sub>
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	1805 to 1880	900	28	35	18.5	32	-30 <u>[1]</u>

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF per carrier; 5 MHz carrier spacing.

### 1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Decoupling leads to enable improved video bandwidth (150 MHz typical)
- Designed for broadband operation (1805 MHz to 1990 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1990 MHz frequency range

**Power LDMOS transistor** 

### 2. Pinning information

Table 2.	Pinning		
Pin	Description	Simplified outline	Graphic symbol
BLF8G20	LS-140V (SOT1244B)		
1	drain		
2	gate		6 7 → 1 → 4,5
3	source [1]		
4	decoupling lead	3	2
5	decoupling lead		aaa-003619
6	n.c.		
7	n.c.	6 2 7	
BLF8G20	LS-140GV (SOT1244C)		
1	drain		
2	gate		6 7 → 1 → 4.5
3	source [1]		
4	decoupling lead		2 3
5	decoupling lead		aaa-003619
6	n.c.	6 2 7 3	
7	n.c.		

[1] Connected to flange.

### 3. Ordering information

#### Table 3. Ordering information

Type number	Packag	Package		
	Name	Name Description V		
BLF8G20LS-140V	-	earless flanged ceramic package; 6 leads	SOT1244B	
BLF8G20LS-140GV	-	earless flanged ceramic package; 6 leads	SOT1244C	

## 4. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage		-	65	V
V <sub>GS</sub>	gate-source voltage		-0.5	+13	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

# 5. Thermal characteristics

Table 5.	Thermal characteristics			
Symbol	Parameter	Conditions	Тур	Unit
R <sub>th(j-c)</sub>	thermal resistance from junction to case	T <sub>case</sub> = 80 °C; P <sub>L</sub> = 35 W	0.4	K/W

### 6. Characteristics

#### Table 6. DC characteristics

 $T_i = 25 \ ^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 1.8 mA	65	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 180 mA	1.5	1.8	2.3	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 28 V; I <sub>D</sub> = 900 mA	1.6	2	2.4	V
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 28 V	-	-	2.8	μA
I <sub>DSX</sub>	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	33	-	A
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	280	nA
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 9 A	-	13.35	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ I <sub>D</sub> = 6.3 A	-	0.08	-	Ω

### Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; 3GPP test model 1 with 64 DPCH; PAR = 8.4 dB at 0.01 % probability on the CCDF;  $f_1 = 1807.5$  MHz;  $f_2 = 1812.5$  MHz;  $f_3 = 1872.5$  MHz;  $f_4 = 1877.5$  MHz; RF performance at  $V_{DS} = 28$  V;  $I_{Dq} = 900$  mA;  $T_{case} = 25$  °C; unless otherwise specified; in a water cooled AB test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G <sub>p</sub>	power gain	P <sub>L(AV)</sub> = 35 W	17.3	18.5	-	dB
$\eta_D$	drain efficiency	P <sub>L(AV)</sub> = 35 W	28	32	-	%
RL <sub>in</sub>	input return loss	P <sub>L(AV)</sub> = 35 W	-	-17	–10	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	P <sub>L(AV)</sub> = 35 W	-	-30	-25	dBc

### 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLF8G20LS-140V and BLF8G20LS-140GV are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS}$  = 28 V;  $I_{Dq}$  = 900 mA;  $P_L$  = 140 W (CW); f = 1800 MHz.

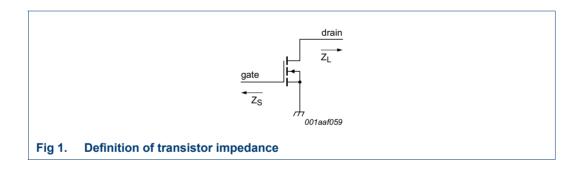
### 7.2 Impedance information

### Table 8. Typical impedance

Measured load-pull data;  $I_{Dq} = 900 \text{ mA}$ ;  $V_{DS} = 28 \text{ V}$ .

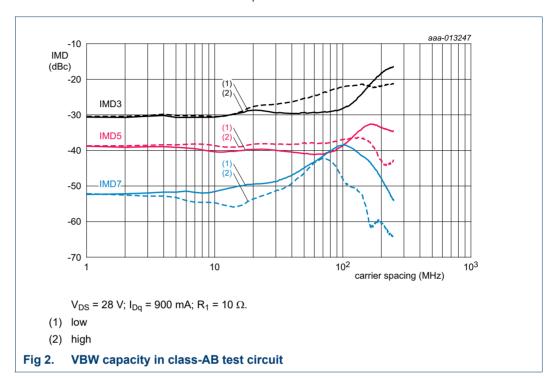
f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]
(MHz)	(Ω)	(Ω)
BLF8G20LS-140V		
1805	1.71 – 3.75j	1.5 – 3.7j
1840	2.01 – 4.01j	1.4 – 3.8j
1880	2.35 – 4.08j	1.5 – 3.8j
1930	2.62 – 4.45j	1.6 – 3.9j
1960	3.13 – 4.87j	1.4 – 3.8j
1990	3.93 – 4.54j	1.3 – 3.9j
BLF8G20LS-140GV		
1805	1.71 – 5.75j	1.5 – 5.7j
1840	2.01 – 6.01j	1.4 – 5.8j
1880	2.35 – 6.08j	1.5 – 5.8j
1930	1.62 – 6.45j	1.6 – 5.9j
1960	3.13 – 6.87j	1.4 – 5.8j
1990	3.93 – 6.54j	1.3 – 5.9j

[1]  $Z_{S}$  and  $Z_{L}$  defined in Figure 1.



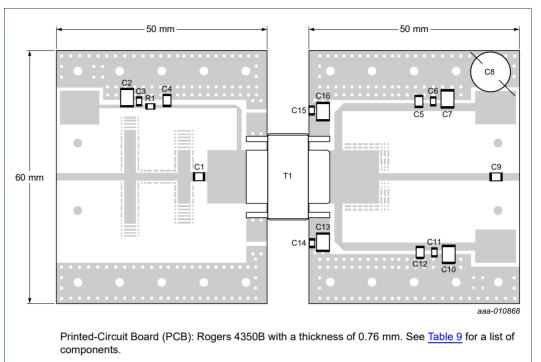
### 7.3 VBW in a class-AB operation

The BLF8G20LS-140V and BLF8G20LS-140GV show 150 MHz (typical) video bandwidth (IMD third-order intermodulation inflection point) in a class-AB test circuit in the 1805 MHz to 1880 MHz band at  $V_{DS}$  = 28 V and  $I_{Dg}$  = 900 mA.



**Power LDMOS transistor** 

### 7.4 Test circuit



#### Fig 3. Component layout

#### Table 9. List of components

See Figure 3 for component layout.

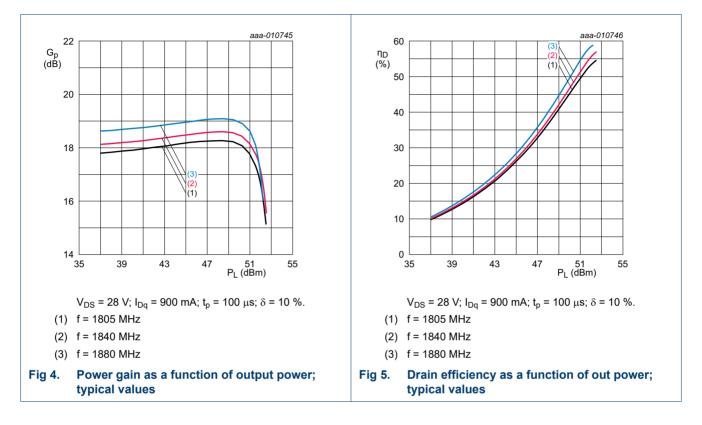
Component	Description	Value		Remarks
C1	multilayer ceramic chip capacitor	1.2 pF	[1]	ATC 800B
C2	multilayer ceramic chip capacitor	1 μF	[2]	Murata
C3	multilayer ceramic chip capacitor	100 nF	[2]	Murata
C4, C9	multilayer ceramic chip capacitor	12 pF	[1]	ATC 800B
C5, C12	multilayer ceramic chip capacitor	20 pF	[1]	ATC 800B
C6, C11	multilayer ceramic chip capacitor	220 nF	[2]	Murata
C7, C10, C13, C16	multilayer ceramic chip capacitor	4.7 μF, 50 V	[2]	Murata
C8	electrolytic capacitor	> 470 μF, 63 V		
C14, C15	multilayer ceramic chip capacitor	-		not mounted
R1	chip resistor	4.7 Ω, 1 % tolerance		SMD 0805
T1	transistor	-		Ampleon BLF8G20LS-140V

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] Murata or capacitor of same quality.

7.5 Graphical data

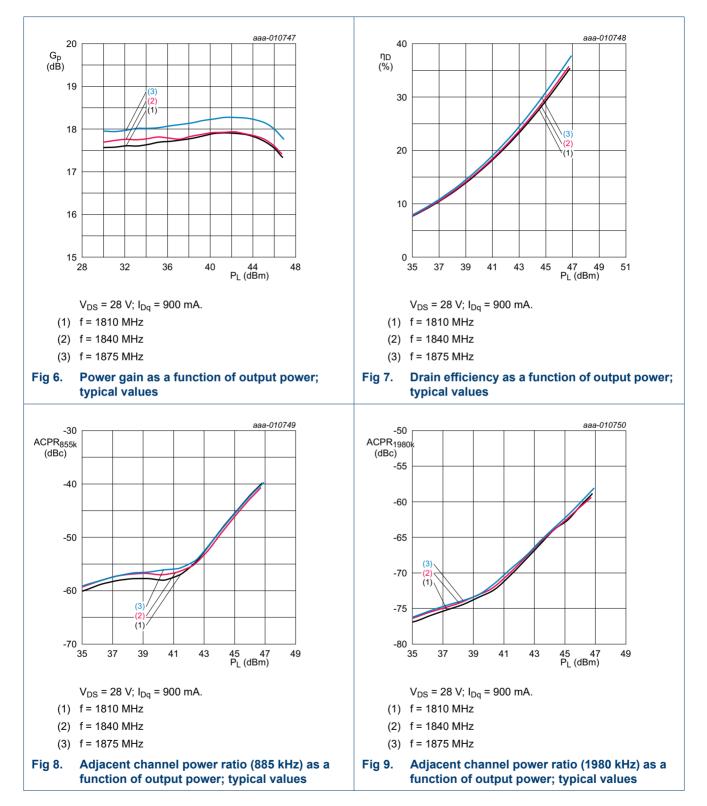
7.5.1 Pulsed CW



# BLF8G20LS-140(G)V

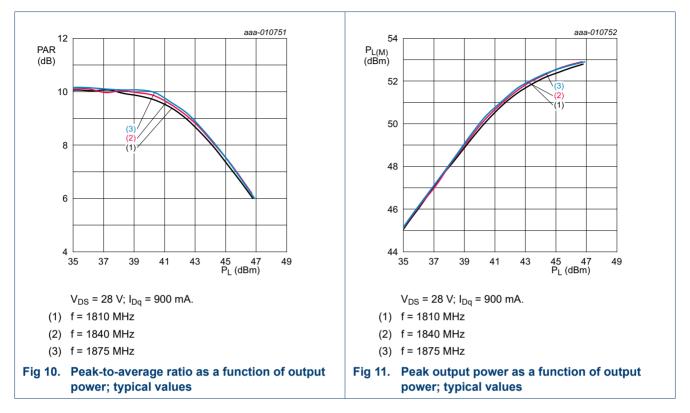
**Power LDMOS transistor** 

7.5.2 IS-95

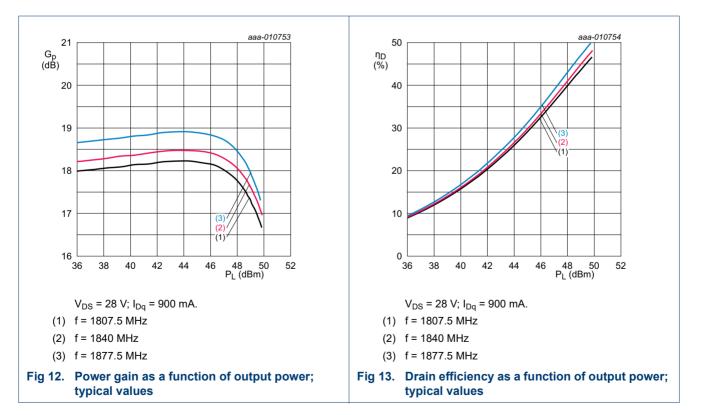


# BLF8G20LS-140(G)V

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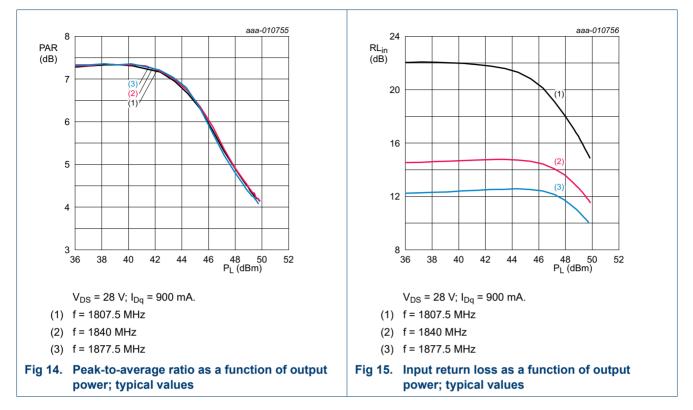
7.5.3 1-Carrier W-CDMA



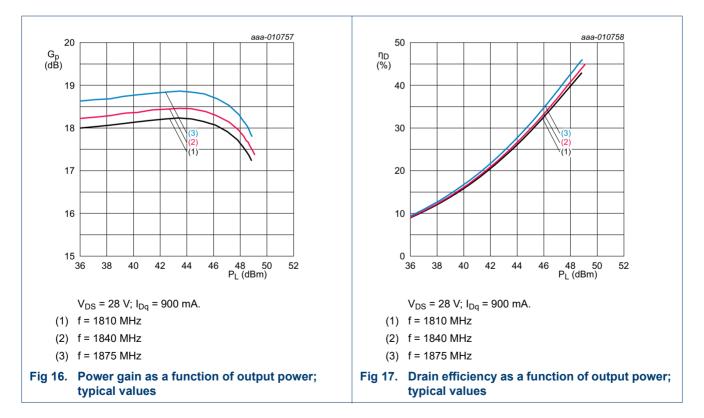
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# BLF8G20LS-140(G)V

**Power LDMOS transistor** 



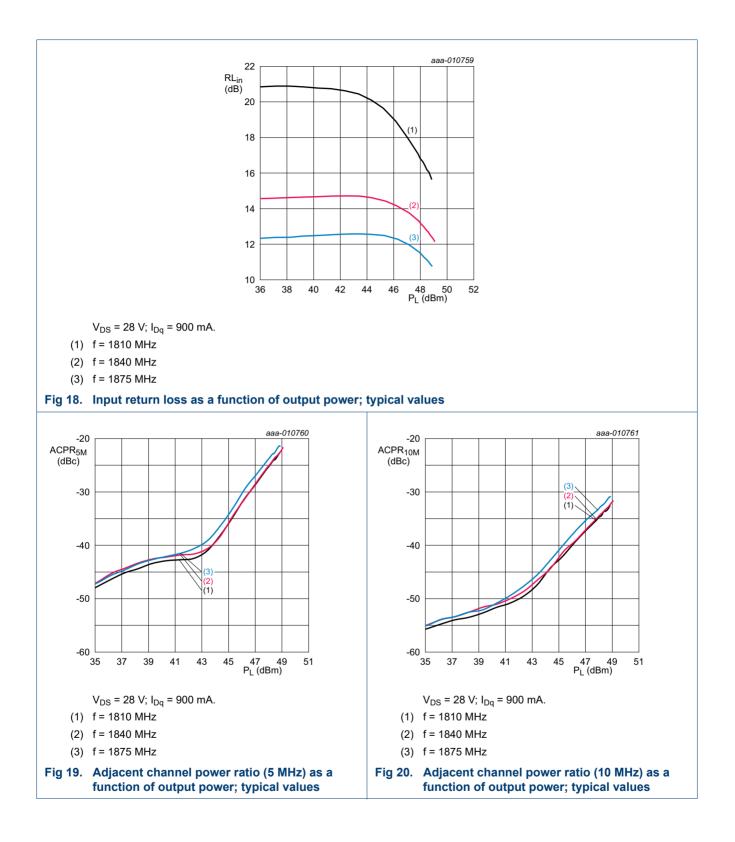
7.5.4 2-Carrier W-CDMA



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# BLF8G20LS-140(G)V

**Power LDMOS transistor** 



BLF8G20LS-140(G)V

**Power LDMOS transistor** 

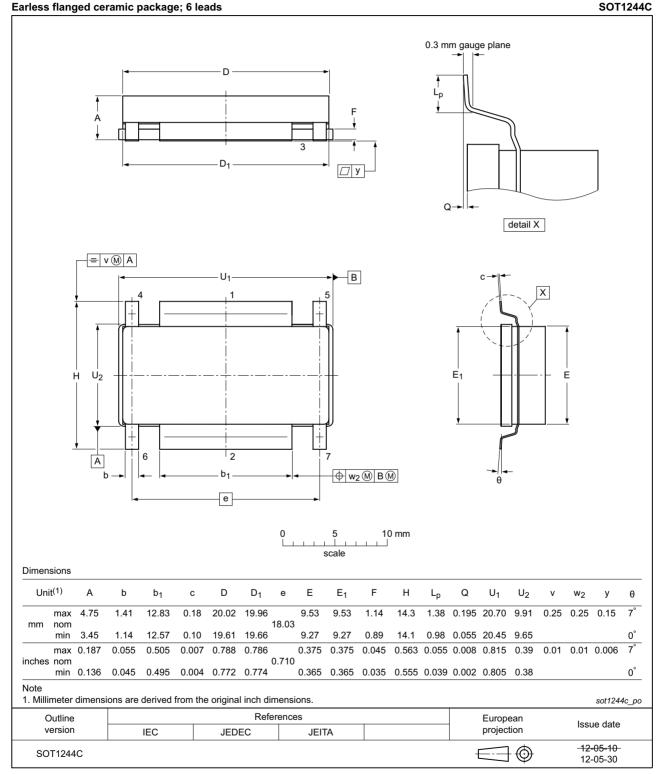
### 8. Package outline

#### Earless flanged ceramic package; 6 leads SOT1244B D A 3 D1 С В U, е С 2 5 1 🛛 У н E<sub>1</sub> Е $U_2$ A 6 2 7 Q .b<sub>1</sub> $\oplus$ w<sub>2</sub> $\otimes$ B $\otimes$ b 5 10 mm 0 scale Dimensions Unit<sup>(1)</sup> А b D $D_1$ Е E1 F н Q(2) U<sub>1</sub> b<sub>1</sub> с е $U_2$ ٧ W<sub>2</sub> у max 4.75 1.41 12.83 0.18 20.02 19.96 9.53 9.53 1.14 19.94 1.70 20.70 9.91 0.25 0.25 0.25 nom 18.03 mm 3.45 1.14 12.57 0.10 19.61 19.66 9.27 9.27 0.89 18.92 1.45 20.45 9.65 min 0.375 0.375 0.045 0.785 0.067 0.815 0.39 max 0.187 0.055 0.505 0.007 0.788 0.786 0.01 0.01 0.01 0.710 inches nom 0.365 0.365 0.035 0.745 0.057 0.805 0.38 0.004 0.772 0.774 min 0.136 0.045 0.495 Note 1. Millimeter dimensions are derived from the original inch dimensions. 2. Dimension is measured 0.030 inch (0.76 mm) from body. sot1244b\_po References Outline European Issue date version projection IEC JEDEC JEITA 12-04-18 $\bigcirc$ SOT1244B 12-05-07

### Fig 21. Package outline SOT1244B

BLF8G20LS-140(G)V

**Power LDMOS transistor** 



### Fig 22. Package outline SOT1244C

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# 9. Handling information

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

## **10. Abbreviations**

Table 10. Abbreviations			
Acronym	Description		
3GPP	3rd Generation Partnership Project		
CCDF	Complementary Cumulative Distribution Function		
CW	Continuous Wave		
DPCH Dedicated Physical CHannel			
ESD	ElectroStatic Discharge		
LDMOS	Laterally Diffused Metal Oxide Semiconductor		
MTF	Median Time to Failure		
PAR	Peak-to-Average Ratio		
SMD	Surface Mounted Device		
VBW	Video BandWidth		
VSWR	Voltage Standing Wave Ratio		
W-CDMA	Wideband Code Division Multiple Access		

# 11. Revision history

Table 11.   Revision history					
Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLF8G20LS-140V_20LS-140GV#3	20150901	Product data sheet		BLF8G20LS-140V _20LS-140GV v.2	
Modifications:	<ul> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>				
BLF8G20LS-140V_20LS-140GV v.2		Product data sheet	-	BLF8G20LS-140V _20LS-140GV v.1	
BLF8G20LS-140V_20LS-140GV v.1	20140207	Objective data sheet	-	-	

# 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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