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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

BLL8H0514L-130; BLL8H0514LS-130

LDMOS driver transistor

AMPLEON

Rev. 3 — 1 September 2015

Product data sheet

1. Product profile

1.1 General description

130 W LDMOS transistor intended for pulsed applications in the 0.5 GHz to 1.4 GHz range.

Table 1. Application information

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 50 mA; in a class-AB application circuit.

Test signal	f	t_p	δ	V_{DS}	P_L	G_p	RL_{in}	η_D	$P_{droop(pulse)}$	t_r	t_f
	(MHz)	(µs)	(%)	(V)	(W)	(dB)	(dB)	(%)	(dB)	(ns)	(ns)
pulsed RF	960 to 1215	128	10	50	130	19	10	54	0	15	8
	1200 to 1400	300	10	50	130	17	10	50	0	15	8

1.2 Features and benefits

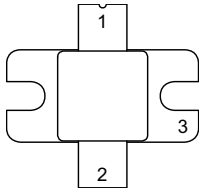
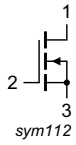
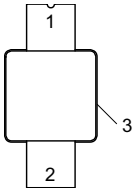
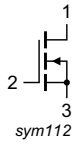
- Easy power control
- Integrated dual side ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (0.5 GHz to 1.4 GHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Amplifiers for pulsed applications in the 0.5 GHz to 1.4 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLL8H0514L-130 (SOT1135A)			
1	drain		
2	gate		
3	source [1]		
BLL8H0514LS-130 (SOT1135B)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL8H0514L-130	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT1135A
BLL8H0514LS-130	-	earless flanged ceramic package; 2 leads	SOT1135B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 130 W		
		t_p = 100 μs; δ = 10 %	0.17	K/W
		t_p = 200 μs; δ = 10 %	0.22	K/W
		t_p = 300 μs; δ = 10 %	0.25	K/W
		t_p = 100 μs; δ = 20 %	0.23	K/W
		t_p = 1 ms; δ = 10 %	0.36	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 630 mA	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 135 mA	1.3	1.8	2.25	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	15.8	18	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 135 mA	806	-	1578	mS
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 6.25 V; I_D = 135 mA	-	200	275	mΩ

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 300 μs; δ = 10 %; RF performance at V_{DS} = 50 V; I_{Dq} = 50 mA; f = 1.2 GHz to 1.4 GHz; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	P_L = 130 W	-	-	50	V
G_p	power gain	P_L = 130 W	15	17	-	dB
RL_{in}	input return loss	P_L = 130 W	-	−10	−7	dB
η_D	drain efficiency	P_L = 130 W	45	50	-	%
$P_{droop(pulse)}$	pulse droop power	P_L = 130 W	-	0	0.3	dB
t_r	rise time	P_L = 130 W	-	20	50	ns
t_f	fall time	P_L = 130 W	-	6	50	ns

7. Application information

7.1 Ruggedness in class-AB operation

The BLL8H0514L-130 and BLL8H0514LS-130 are capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 50 mA; P_L = 130 W; f = 1.2 GHz to 1.4 GHz; t_p = 300 μs; δ = 10 %.

7.2 Impedance information

Table 8. Typical impedance

f	Z_S	Z_L
(MHz)	(Ω)	(Ω)
1200	1.21 – j3.44	2.40 – j0.63
1300	1.56 – j4.49	2.30 – j0.87
1400	2.21 – j4.86	2.00 – j1.71

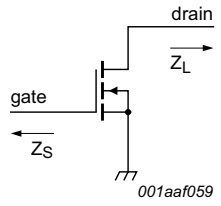
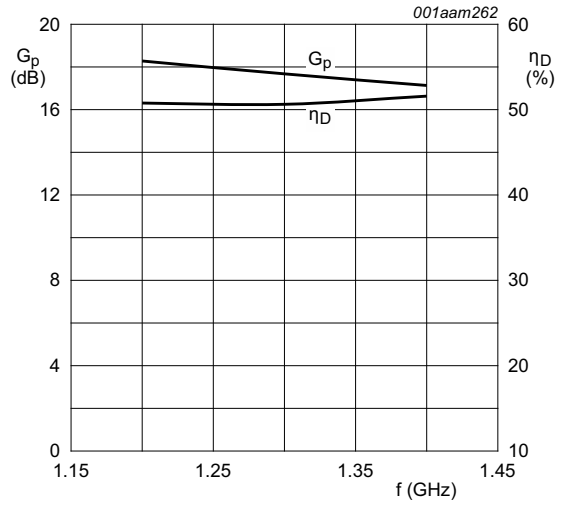


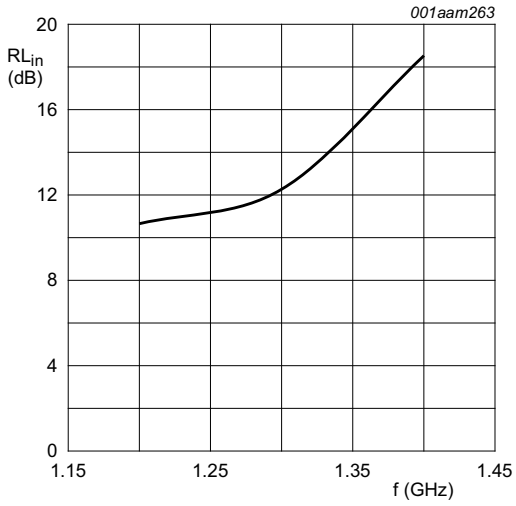
Fig 1. Definition of transistor impedance

7.3 Performance curves



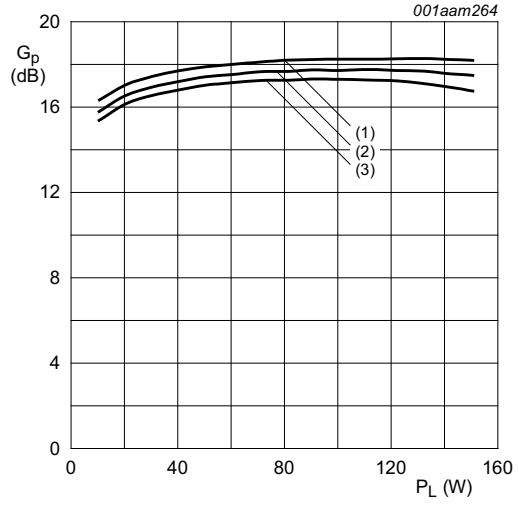
V_{DS} = 50 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

Fig 2. Power gain and drain efficiency as function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

Fig 3. Input return loss as a function of frequency; typical values



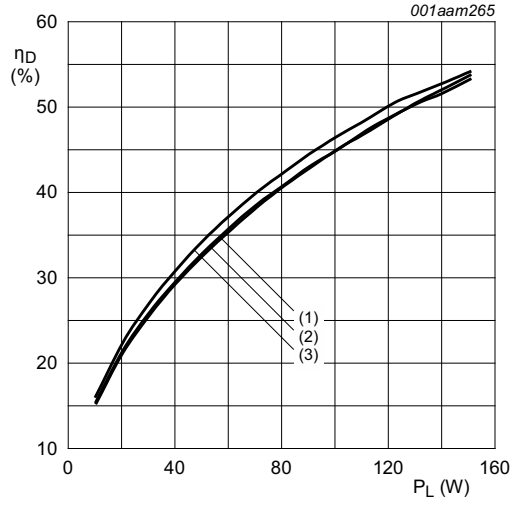
V_{DS} = 50 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

(1) f = 1.2 GHz

(2) f = 1.3 GHz

(3) f = 1.4 GHz

Fig 4. Power gain as a function of output power; typical values



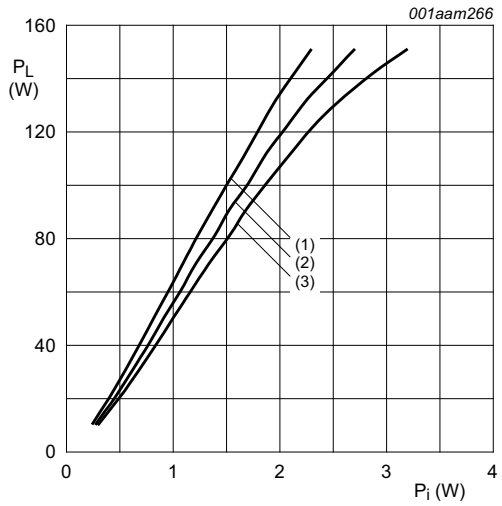
V_{DS} = 50 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

(1) f = 1.2 GHz

(2) f = 1.3 GHz

(3) f = 1.4 GHz

Fig 5. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %.

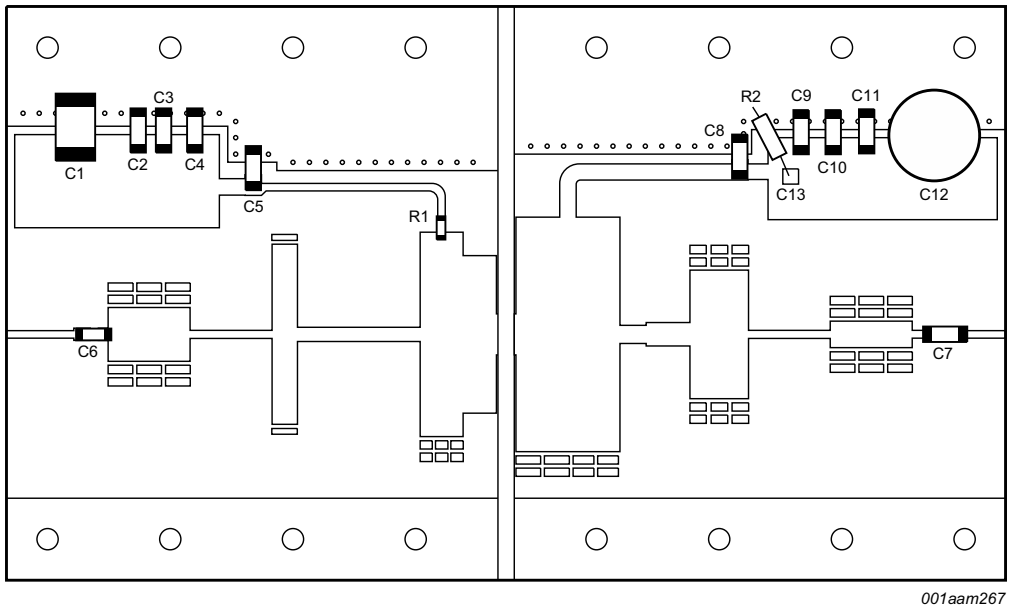
(1) f = 1.2 GHz

(2) f = 1.3 GHz

(3) f = 1.4 GHz

Fig 6. Output power as a function of input power; typical values

8. Test information



Printed-Circuit Board (PCB) material: Duroid 6006 with ε_r = 6.15 and thickness = 0.64 mm.

See Table 9 for list of components.

Fig 7. Component layout

Table 9. List of components

See Figure 7 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	10 μF, 50 V	
C2, C11	multilayer ceramic chip capacitor	1 nF [1]	
C3, C4, C6, C9, C10	multilayer ceramic chip capacitor	100 pF [2]	
C5, C7, C8	multilayer ceramic chip capacitor	43 pF [2]	
C12	electrolytic capacitor	220 μF, 63 V	
C13	multilayer ceramic chip capacitor	1 nF [3]	fitted vertically in series with R2
R1	SMD resistor	10 Ω	SMD 0603
R2	wirewound lead resistor	2.61 Ω, 0.25 W	fitted in series with C13

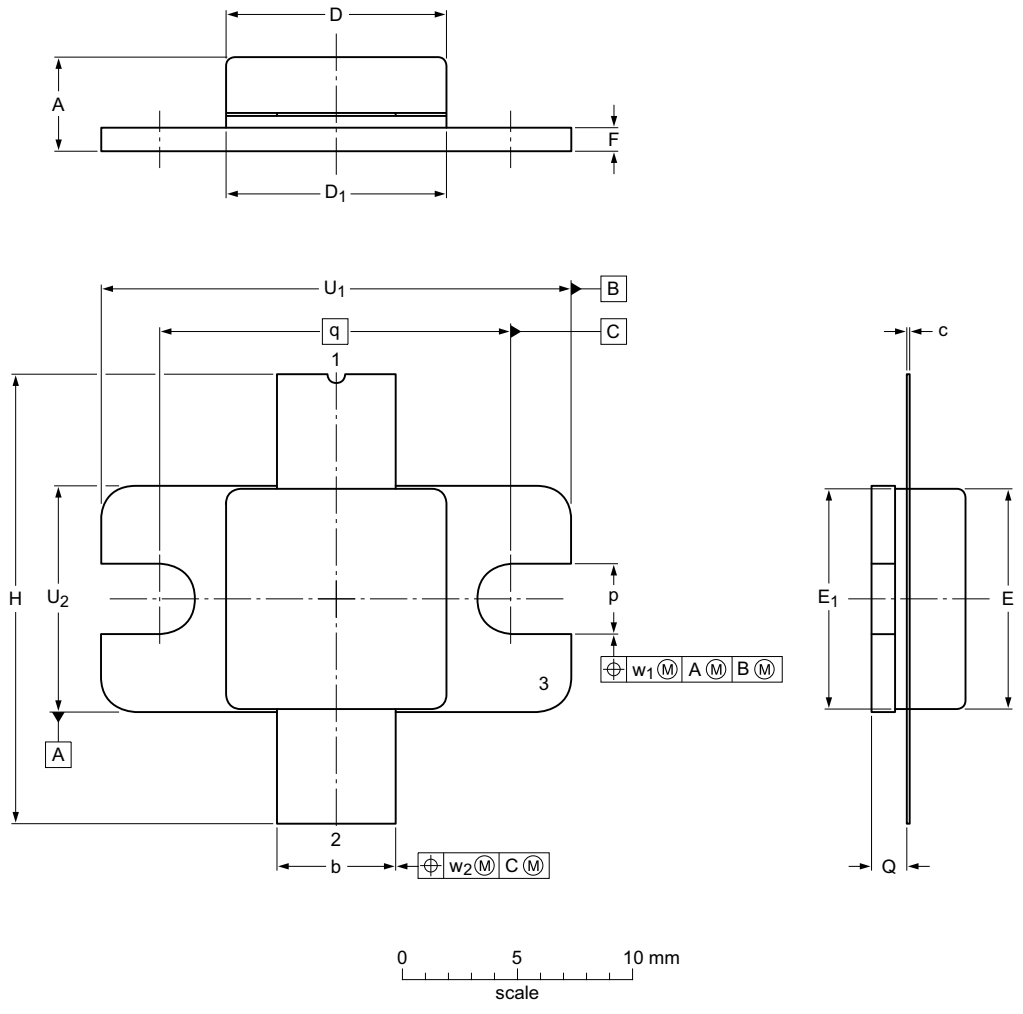
[1] American Technical Ceramics type 700A or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.

[3] American Technical Ceramics type 100B or capacitor of same quality.

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT1135A**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	max	4.65	5.26	0.18	9.65	9.65	9.65	9.65	1.14	19.94	3.30	1.70		20.45	9.91		
	nom												15.24			0.25	0.51
	min	3.76	5.00	0.10	9.40	9.40	9.40	9.40	0.89	18.92	2.92	1.45		20.19	9.65		
inches	max	0.183	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.785	0.130	0.067		0.805	0.39		
	nom												0.6			0.01	0.02
	min	0.148	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.745	0.115	0.057		0.795	0.38		

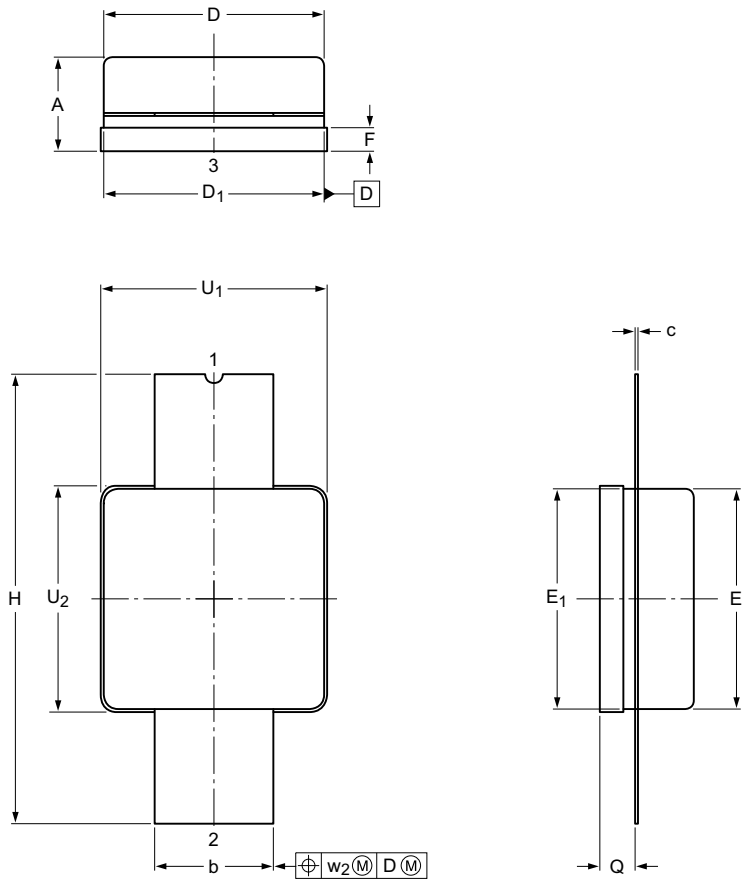
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1135a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1135A						~~09-10-12~~ 09-12-14

Fig 8. Package outline SOT1135A

Earless flanged ceramic package; 2 leads **SOT1135B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	Q	U_1	U_2	w_2
mm	max	4.65	5.26	0.18	9.65	9.65	9.65	9.65	1.14	19.94	1.70	9.91	9.91	
	nom													0.51
	min	3.76	5.00	0.10	9.40	9.40	9.40	9.40	0.89	18.92	1.45	9.65	9.65	
inches	max	0.183	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.785	0.067	0.39	0.39	
	nom													0.02
	min	0.148	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.745	0.057	0.38	0.38	

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1135b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1135B						~~09-10-12~~ 09-12-14

Fig 9. Package outline SOT1135B

10. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL8H0514L-130_0514LS-130#3	20150901	Product data sheet	-	BLL8H0514L-130_0514LS-130 #2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLL8H0514L-130_0514LS-130#2	20150209	Product data sheet	-	BLL8H0514L-130_0514LS-130 #1
BLL8H0514L-130_0514LS-130#1	20140930	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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