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BLM2425M7S60P

LDMOS 2-stage power MMIC

Rev. 3 — 9 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

60W dual path, 2-stage power MMIC transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLM2425M7S60P is designed for high power CW applications and is assembled in a high performance plastic package.

Table 1. Application performance

Per section unless otherwise specified.

Test signal	f	V _{DS}	PL	Gp	η_{D}
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	32	30	27.5	45

1.2 Features and benefits

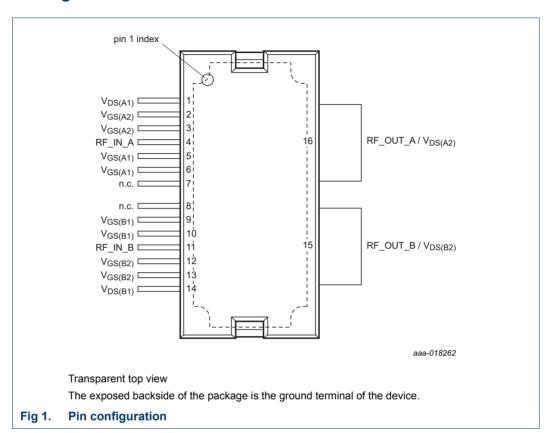
- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Biasing of individual stages is externally accessible
- On-chip matching for ease of use
- Designed for broadband operation (frequency 2400 MHz to 2500 MHz)
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

Industrial, scientific and medical applications in the frequency range 2400 MHz to $2500 \ \text{MHz}$.

2. Pinning information

2.1 Pinning



2.2 Pin description

Table 2. Pin description

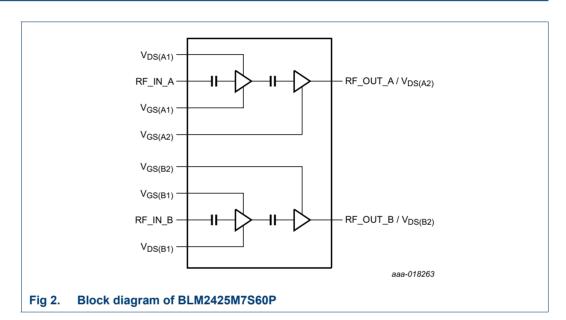
Symbol	Pin	Description	
V _{DS(A1)}	1	drain-source voltage of stage A1	
V _{GS(A2)}	2, 3	gate-source voltage of stage A2	
RF_IN_A	4	RF input path A	
V _{GS(A1)}	5, 6	gate-source voltage of stage A1	
n.c.	7	not connected	
n.c.	8	not connected	
V _{GS(B1)}	9, 10	gate-source voltage of stage B1	
RF_IN_B	11	RF input path of B	
V _{GS(B2)}	12, 13	gate-source voltage of stage B2	
V _{DS(B1)}	14	drain-source voltage of stage B1	
RF_OUT_B/V _{DS(B2)}	15	RF output path B / drain source voltage of stage B2	
RF_OUT_A/V _{DS(A2)}	16	RF output path A / drain source voltage of stage A2	
GND	flange	RF ground	

3. Ordering information

Table 3. Ordering information

Type number	Package			
	Name	Description	Version	
BLM2425M7S60P	HSOP16F	plastic, heatsink small outline package; 16 leads(flat)	SOT1211-1	

4. Block diagram



5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
V _{GS(sense)}	sense gate-source voltage		-0.5	+9	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C
T _{case}	case temperature		-	150	°C

^[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics

Measured for total device.

Symbol	Parameter	Conditions	Value	Unit
R _{th(j-c)}	thermal resistance from junction to case	final stage; T _{case} = 90 °C; P _L = 60 W	0.91	K/W

^[1] When operated with a CW signal.

7. Characteristics

Table 6. DC characteristics

 T_{case} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Final stag	ge			1		
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.422 \text{ mA}$	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 42 mA	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 253 mA	1.7	2.1	2.5	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	1.4	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	7.8	-	Α
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	140	nΑ
9 _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 1478 mA	-	2.85	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 1.48 \text{ A}$	-	350	-	mΩ
I_{Dq}	quiescent drain current	main transistor: V _{DS} = 28 V	208	233	257	mΑ
		sense transistor: $I_D = 7 \text{ mA}$; $V_{DS} = 28 \text{ V}$				
Driver sta	age					
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.116 \text{ mA}$	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 11.6 mA	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_{D} = 69.6 mA	1.7	2.1	2.5	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	1.4	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	2.2	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	140	nA
9 _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 406 mA	-	8.0	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 0.4 \text{ A}$	-	2350	-	mΩ
I _{Dq}	quiescent drain current	main transistor: V _{DS} = 28 V	67	75	83	mA
		sense transistor: $I_D = 7 \text{ mA}$; $V_{DS} = 28 \text{ V}$				

Table 7. RF Characteristics

Test signal: CW at f = 2450 MHz; RF performance at $V_{DS} = 32$ V; $I_{Dq1} = 25$ mA; $I_{Dq2} = 50$ mA; $T_{case} = 25$ °C; per section unless otherwise specified; in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	P _L = 30 W	26	27.5	-	dB
η_{D}	drain efficiency	P _L = 30 W	41.5	45	-	%
RLin	input return loss	P _L = 30 W	-	-18	-13.8	dB

8. Test information

8.1 Ruggedness

The BLM2425M7S60P is capable of withstanding a load mismatch corresponding to VSWR = 15 : 1 through all phases under the following conditions: V_{DS} = 32 V; $I_{D\alpha 1}$ = 25 mA; $I_{D\alpha 2}$ = 50 mA; f = 2450 MHz; per section unless otherwise specified.

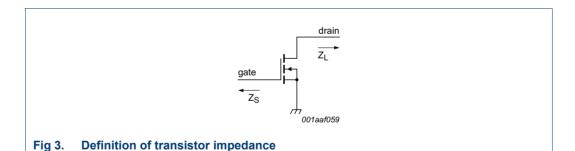
8.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values per section unless otherwise specified.

f	Z _S [1]	Z _L [1]
(MHz)	(Ω)	(Ω)
2400	19.1 + j43.2	5.3 – j2.4
2450	16.8 + j38.8	5.0 – j2.3
2500	14.4 + j33.0	4.4 – j2.4

[1] Z_S and Z_L defined in Figure 3



8.3 Test circuit

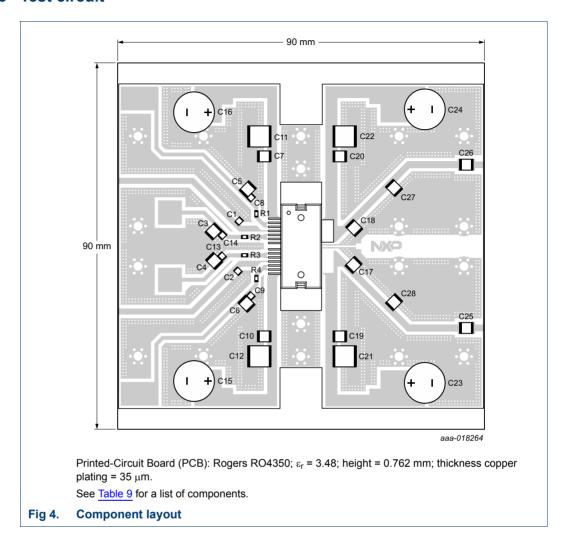


Table 9. List of components See Figure 4 for component layout.

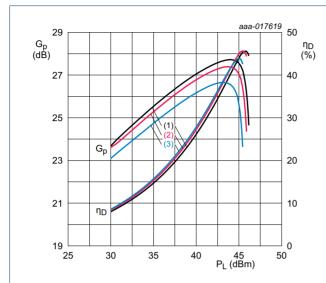
Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	1 pF [1]	
C3, C4, C5, C6	multilayer ceramic chip capacitor	1 μF, 50 V	Murata: GRM32RR71H105KA01L
C7, C10	multilayer ceramic chip capacitor	8.2 pF [2]	
C8, C9, C13, C14	multilayer ceramic chip capacitor	8.2 pF [1]	
C11, C12, C21, C22	multilayer ceramic chip capacitor	10 μF, 50 V	
C15, C16, C23, C24	electrolytic capacitor	220 μF, 63 V	
C17, C18	multilayer ceramic chip capacitor	1.6 nF [2]	
C19, C20, C25, C26	multilayer ceramic chip capacitor	8.2 pF [2]	
C27, C28	multilayer ceramic chip capacitor	0.4 pF [2]	
R1, R2, R3, R4	SMD resistor	0 Ω	SMD 0805

- [1] American Technical Ceramics type 100A or capacitor of same quality
- [2] American Technical Ceramics type 100B or capacitor of same quality

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8.4 Graphical data

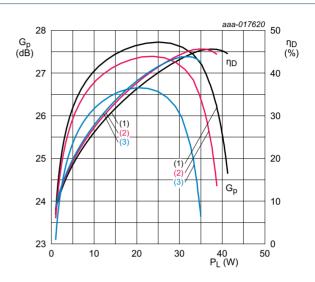
Performance curves are measured per section.



 V_{DS} = 32 V; I_{Dq1} = 25 mA; I_{Dq2} = 50 mA.

- (1) f = 2400 MHz
- (2) f = 2450 MHz
- (3) f = 2500 MHz

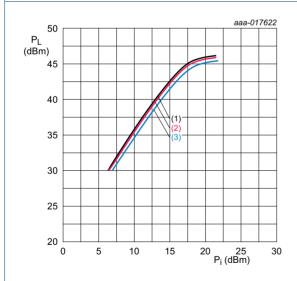
Fig 5. Power gain and drain efficiency as function of output power; typical values



 V_{DS} = 32 V; I_{Dq1} = 25 mA; I_{Dq2} = 50 mA.

- (1) f = 2400 MHz
- (2) f = 2450 MHz
- (3) f = 2500 MHz

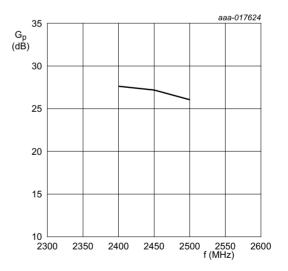
Fig 6. Power gain and drain efficiency as function of output power; typical values



 $V_{DS} = 32 \text{ V}; I_{Dq1} = 25 \text{ mA}; I_{Dq2} = 50 \text{ mA}.$

- (1) f = 2400 MHz
- (2) f = 2450 MHz
- (3) f = 2500 MHz

Fig 7. Output power as a function of input power; typical values



 V_{DS} = 32 V; I_{Dq1} = 25 mA; I_{Dq2} = 50 mA; P_{L} = 30 W.

Fig 8. Power gain as a function of frequency; typical values

9. Package outline

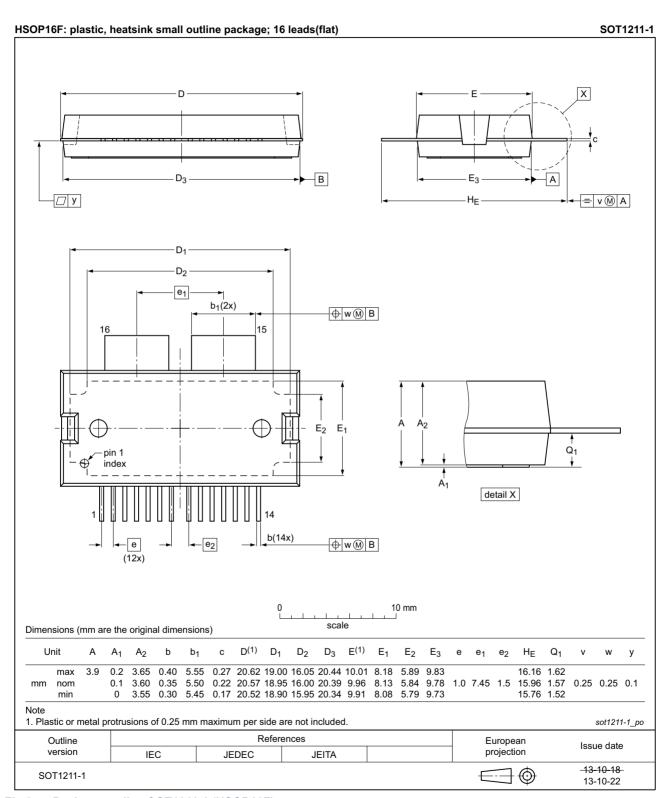


Fig 9. Package outline SOT1211-1 (HSOP16F)

10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description	
CW	Continuous Wave	
ESD	ectroStatic Discharge	
LDMOS	aterally Diffused Metal Oxide Semiconductor	
MMIC	Monolithic Microwave Integrated Circuit	
MTF	Median Time to Failure	
SMD	Surface Mounted Device	
VSWR	Voltage Standing Wave Ratio	

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLM2425M7S60P v.3	20150909	Product data sheet	-	BLM2425M7S60P#2	
Modifications:	<u>Table 7 on page 5</u> ; table updated				
BLM2425M7S60P#2	20150901	Objective	-	BLM2425M7S60P v.1	
Modifications:	The format of this document has been redesigned to comply with the new identity guidelines of Ampleon				
	Legal texts have been adapted to the new company name where appropriate				
BLM2425M7S60P v.1	20150518	Objective data sheet	-	-	

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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LDMOS 2-stage power MMIC

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LDMOS 2-stage power MMIC

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