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BLS6G2735L-30; BLS6G2735LS-30

S-band LDMOS transistor

Rev. 4 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

30 W LDMOS power transistor for S-band radar applications in the frequency range from 2.7 GHz to 3.5 GHz.

Table 1. Application information

Typical RF performance at T_{case} = 25 °C; t_p = 300 μs; δ = 10 %; I_{Dq} = 50 mA.

Test signal	f (GHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
Typical RF performance in a class-AB production test circuit in band 3.1 GHz to 3.5 GHz							
pulsed RF	3.1 to 3.5	32	30	13	50	20	10
Typical RF performance in an application circuit in small band 2.7 GHz to 3.3 GHz							
pulsed RF	2.7 to 3.3	32	35	14	50	20	10
Typical RF performance in an application circuit in small band 2.7 GHz to 3.5 GHz							
pulsed RF	2.7 to 3.5	32	30	12	47	20	10

1.2 Features and benefits

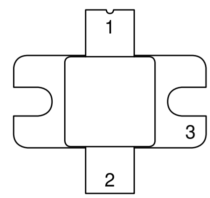
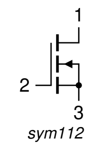
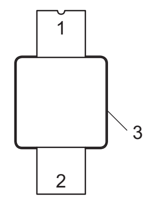
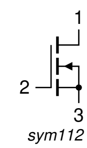
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (2.7 GHz to 3.5 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- S-band radar applications in the frequency range 2.7 GHz to 3.5 GHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLS6G2735L-30 (SOT1135A)			
1	drain		
2	gate		
3	source [1]		
BLS6G2735LS-30 (SOT1135B)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS6G2735L-30	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT1135A
BLS6G2735LS-30	-	earless flanged ceramic package; 2 leads	SOT1135B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	60	V
V_{GS}	gate-source voltage	–0.5	+13	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_h = 85 °C; $P_{L(CW)}$ = 30 W		
		t_p = 100 μs; δ = 10 %	0.507	K/W
		t_p = 200 μs; δ = 10 %	0.662	K/W
		t_p = 300 μs; δ = 10 %	0.761	K/W
		t_p = 100 μs; δ = 20 %	0.594	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 40 mA	1.4	2	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	8.2	-	A
I_{GSS}	gate leakage current	V_{GS} = 8.3 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 1.4 A	-	2.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.4 A	-	0.37	0.58	Ω

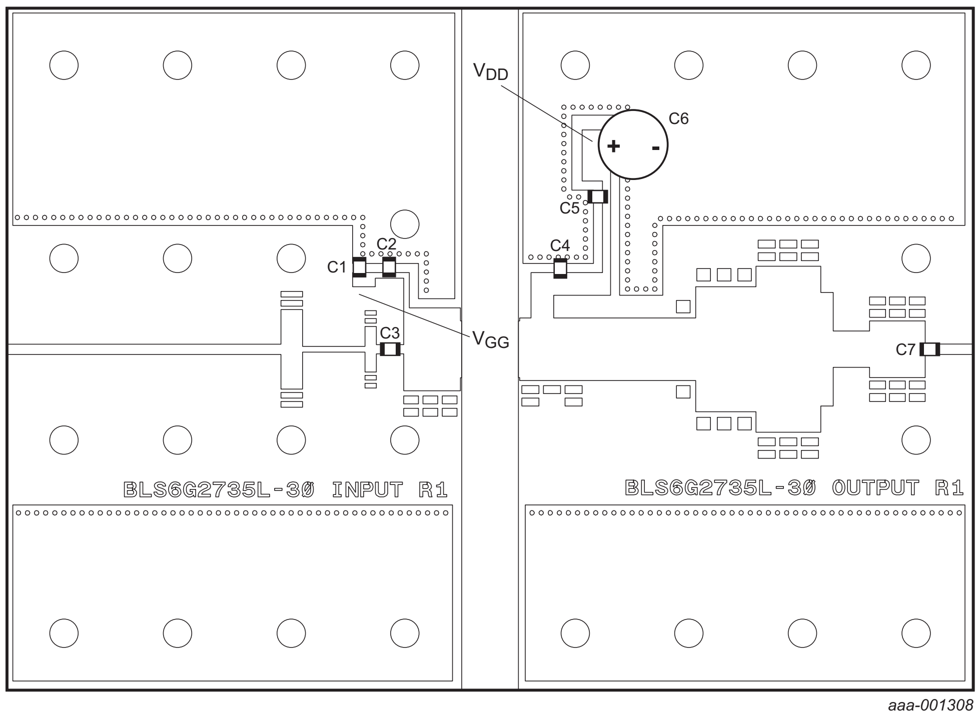
Table 7. RF characteristics

Test signal: pulsed RF; f_1 = 3100 MHz; f_2 = 3300 MHz; f_3 = 3500 MHz; t_p = 300 μs; δ = 10 %; V_{DS} = 32 V; I_{Dq} = 50 mA; T_{case} = 25 °C; unless otherwise specified, in the class-AB RF production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		-	30	-	W
G_p	power gain	P_L = 30 W	11	13	-	dB
η_D	drain efficiency	P_L = 30 W	43	50	-	%
t_r	rise time	P_L = 30 W	-	20	50	ns
t_f	fall time	P_L = 30 W	-	10	50	ns

7. Application information

7.1 Circuit information for application circuit (2.7 GHz to 3.5 GHz)



Printed-Circuit Board (PCB): Rogers 3006; ε_r = 6.15; thickness = 0.64 mm; thickness copper plating = 35 μm.

See Table 8 for a list of components.

Fig 1. Component layout for RF test circuit

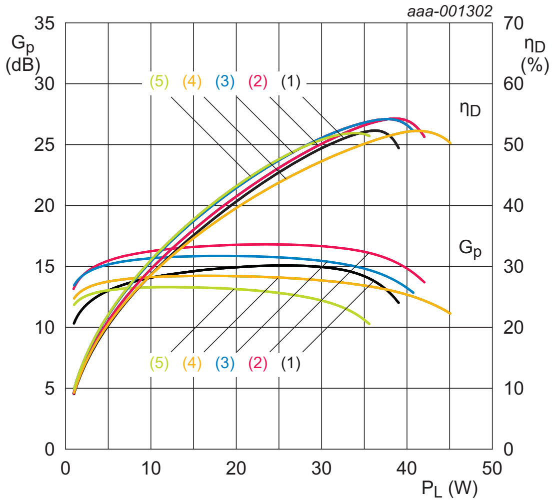
Table 8. List of components
For test circuit see Figure 1.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	2 μF, 50 V	[1]
C2	multilayer ceramic chip capacitor	100 pF	[2]
C3	multilayer ceramic chip capacitor	0.6 pF	[2]
C4, C7	multilayer ceramic chip capacitor	10 pF	[2]
C5	multilayer ceramic chip capacitor	1 μF, 50 V	[1]
C6	electrolytic capacitor	470 μF, 63 V	

[1] TDK or capacitor of same quality.

[2] American Technical Ceramics type 800A or capacitor of same quality.

7.2 Measured in application circuit from 2.7 GHz to 3.5 GHz



V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %

(1) f = 2700 MHz

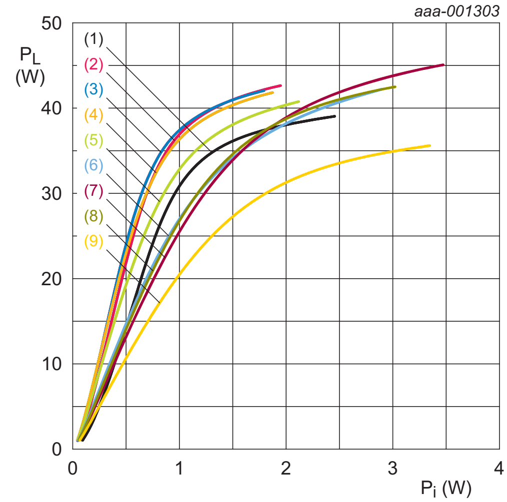
(2) f = 2900 MHz

(3) f = 3100 MHz

(4) f = 3300 MHz

(5) f = 3500 MHz

Fig 2. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %

(1) f = 2700 MHz

(2) f = 2800 MHz

(3) f = 2900 MHz

(4) f = 3000 MHz

(5) f = 3100 MHz

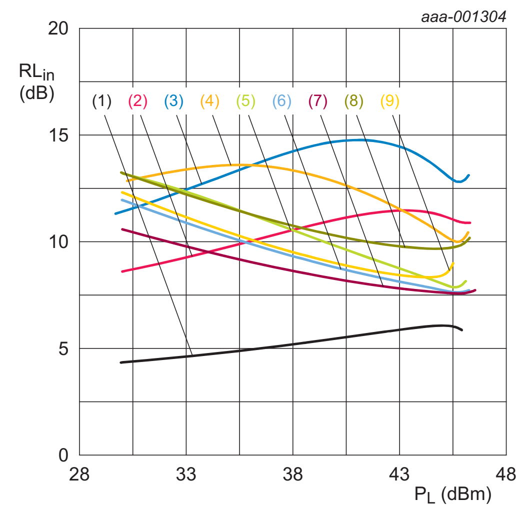
(6) f = 3200 MHz

(7) f = 3300 MHz

(8) f = 3400 MHz

(9) f = 3500 MHz

Fig 3. Output power as a function of input power; typical values



V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %

(1) f = 2700 MHz

(2) f = 2800 MHz

(3) f = 2900 MHz

(4) f = 3000 MHz

(5) f = 3100 MHz

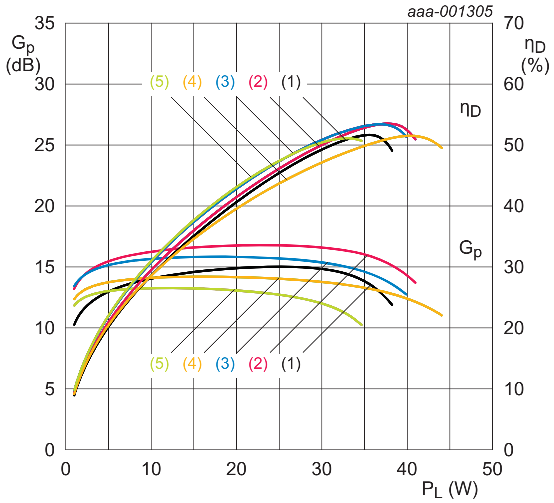
(6) f = 3200 MHz

(7) f = 3300 MHz

(8) f = 3400 MHz

(9) f = 3500 MHz

Fig 4. Input return loss as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 100 μs; δ = 20 %

(1) f = 2700 MHz

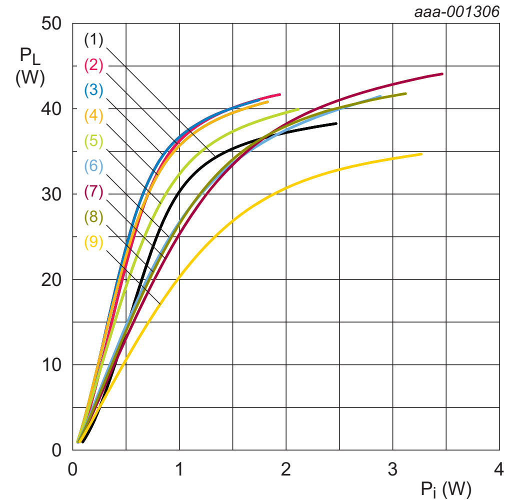
(2) f = 2900 MHz

(3) f = 3100 MHz

(4) f = 3300 MHz

(5) f = 3500 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 100 μs; δ = 20 %

(1) f = 2700 MHz

(2) f = 2800 MHz

(3) f = 2900 MHz

(4) f = 3000 MHz

(5) f = 3100 MHz

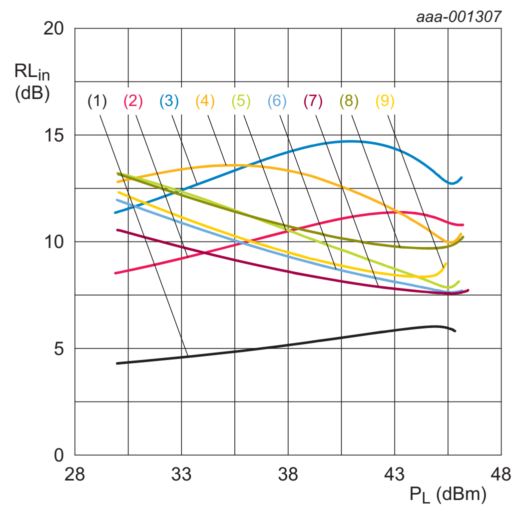
(6) f = 3200 MHz

(7) f = 3300 MHz

(8) f = 3400 MHz

(9) f = 3500 MHz

Fig 6. Output power as a function of input power; typical values



V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 100 μs; δ = 20 %

(1) f = 2700 MHz

(2) f = 2800 MHz

(3) f = 2900 MHz

(4) f = 3000 MHz

(5) f = 3100 MHz

(6) f = 3200 MHz

(7) f = 3300 MHz

(8) f = 3400 MHz

(9) f = 3500 MHz

Fig 7. Input return loss as a function of output power; typical values

8. Test information

8.1 Ruggedness in class-AB operation

The BLS6G2735L-30 and BLS6G2735LS-30 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 50 mA; P_L = 30 W; t_p = 300 μs; δ = 10 %.

8.2 Impedance information

Table 9. Typical impedance

Source and load impedances obtained in a wideband test circuit.

f GHz	Z_S Ω	Z_L Ω
2.7	3.4 – j16.0	32.7 – j3.8
2.9	4.3 – j13.0	20.3 – j4.2
3.1	5.4 – j11.6	18.3 – j3.9
3.3	5.4 – j12.0	15.0 – j7.2
3.5	3.7 – j11.7	8.4 – j6.6

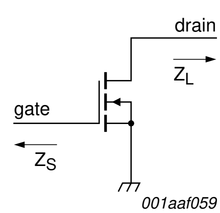
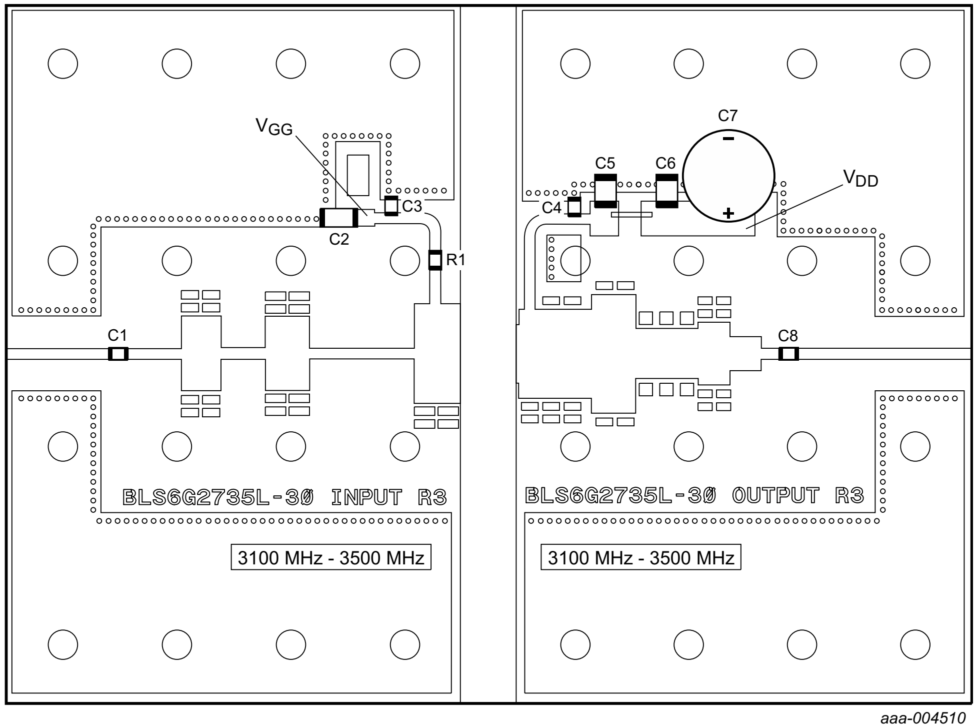


Fig 8. Definition of transistor impedance

8.3 Circuit information for production test circuit (3.1 GHz to 3.5 GHz)



Printed-Circuit Board (PCB): Rogers Duroid 6006; ε_r = 6.15; thickness = 0.64 mm; thickness copper plating = 35 μm.

See Table 10 for a list of components.

Fig 9. Component layout for RF production test circuit

Table 10. List of components

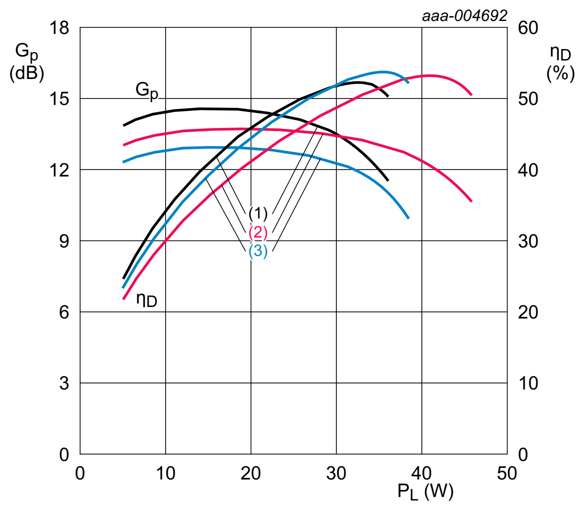
For test circuit see Figure 9.

Component	Description	Value	Remarks
C1, C3, C4, C8	multilayer ceramic chip capacitor	10 pF	[1]
C2	multilayer ceramic chip capacitor	1 μF	[2]
C5	multilayer ceramic chip capacitor	4.7 μF, 50 V	[2]
C6	multilayer ceramic chip capacitor	10 μF, 50 V	[2]
C7	electrolytic capacitor	100 μF, 63 V	
R1	SMD resistor	10 Ω	

[1] American Technical Ceramics type 800A or capacitor of same quality.

[2] TDK or capacitor of same quality.

8.4 Measured in RF production test circuit from 3.1 GHz to 3.5 GHz



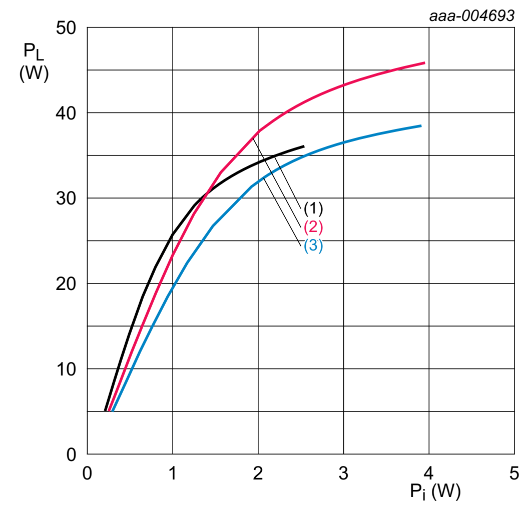
V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %

(1) f = 3100 MHz

(2) f = 3300 MHz

(3) f = 3500 MHz

Fig 10. Power gain and drain efficiency as function of output power; typical values



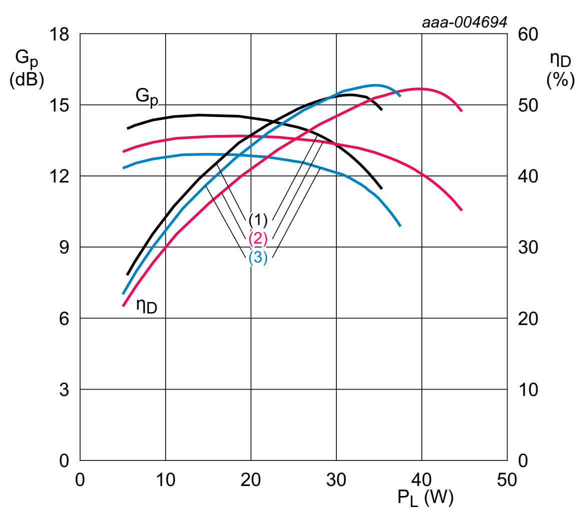
V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 300 μs; δ = 10 %

(1) f = 3100 MHz

(2) f = 3300 MHz

(3) f = 3500 MHz

Fig 11. Output power as a function of input power; typical values



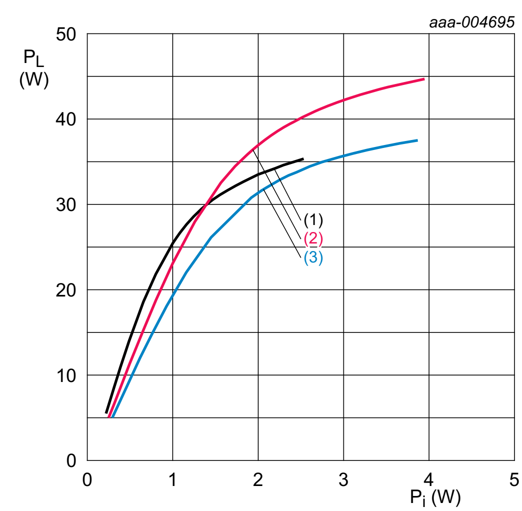
V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 100 μs; δ = 20 %

(1) f = 3100 MHz

(2) f = 3300 MHz

(3) f = 3500 MHz

Fig 12. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 50 mA; t_p = 100 μs; δ = 20 %

(1) f = 3100 MHz

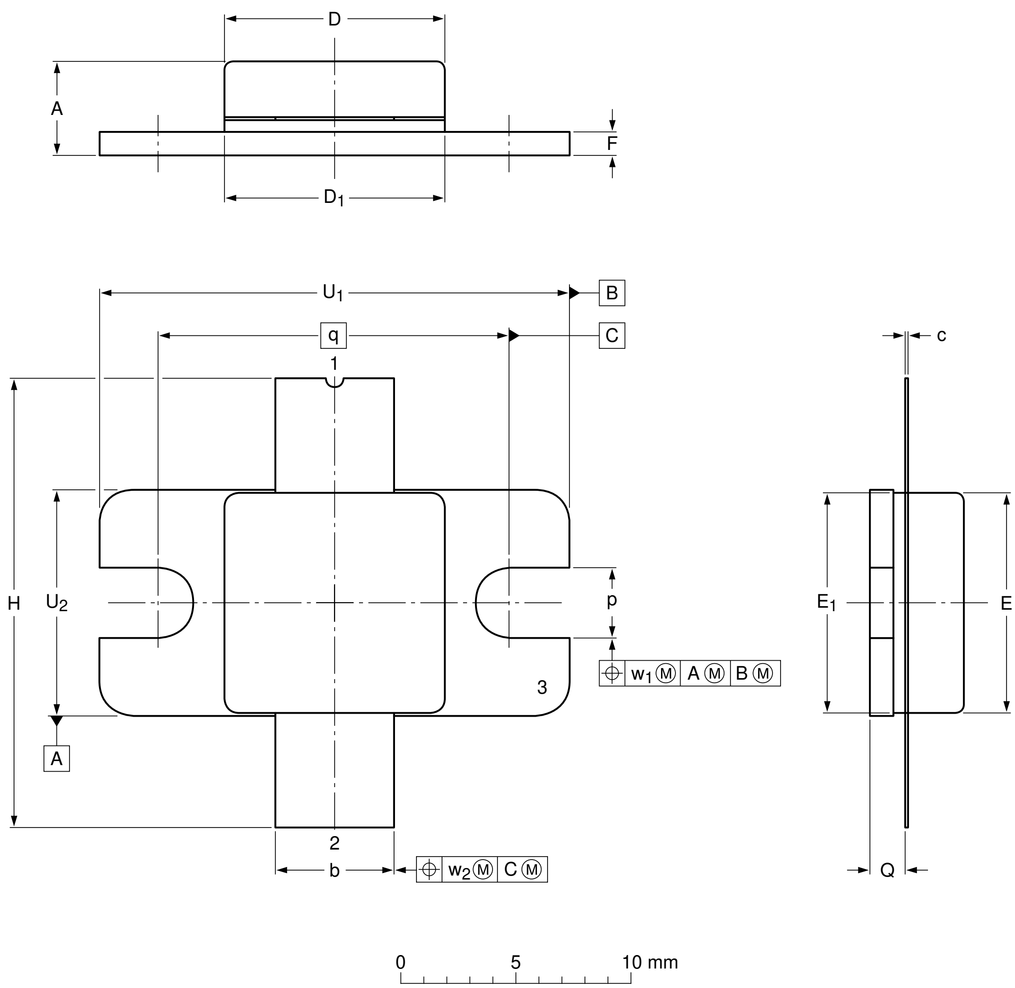
(2) f = 3300 MHz

(3) f = 3500 MHz

Fig 13. Output power as a function of input power; typical values

9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT1135A**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	max	4.65	5.26	0.18	9.65	9.65	9.65	9.65	1.14	19.94	3.30	1.70		20.45	9.91		
	nom												15.24			0.25	0.51
	min	3.76	5.00	0.10	9.40	9.40	9.40	9.40	0.89	18.92	2.92	1.45		20.19	9.65		
inches	max	0.183	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.785	0.130	0.067		0.805	0.39		
	nom												0.6			0.01	0.02
	min	0.148	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.745	0.115	0.057		0.795	0.38		

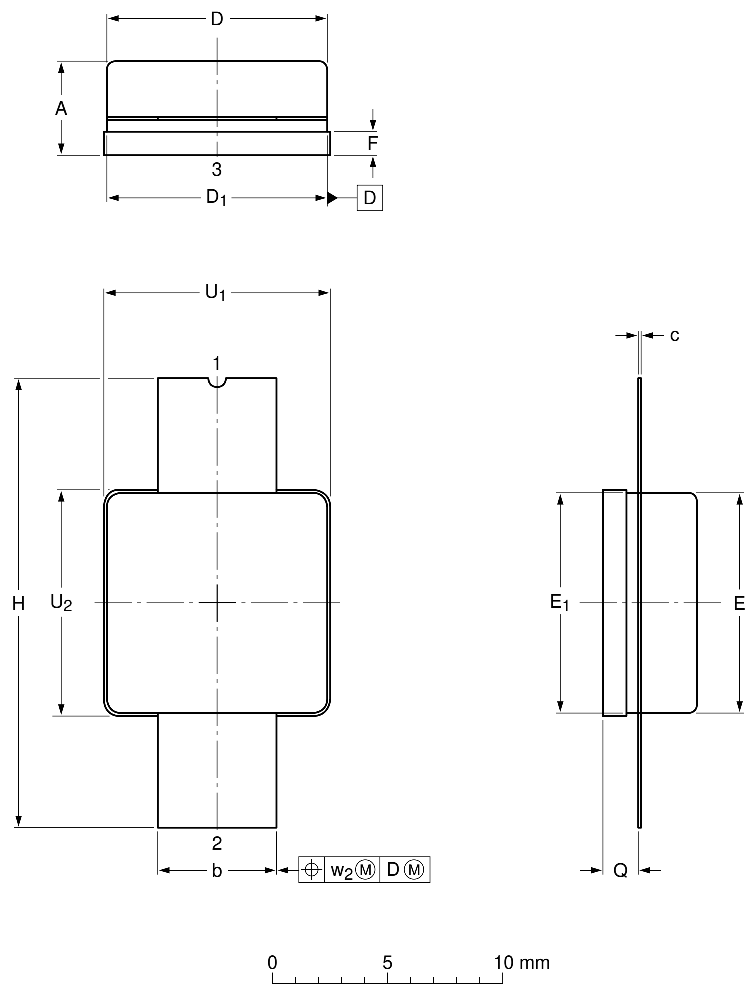
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1135a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1135A						~~09-10-12~~ 09-12-14

Fig 14. Package outline SOT1135A

Earless flanged ceramic package; 2 leads **SOT1135B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	F	H	Q	U_1	U_2	w_2
mm	max	4.65	5.26	0.18	9.65	9.65	9.65	9.65	1.14	19.94	1.70	9.91	9.91	
	nom													0.51
	min	3.76	5.00	0.10	9.40	9.40	9.40	9.40	0.89	18.92	1.45	9.65	9.65	
inches	max	0.183	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.785	0.067	0.39	0.39	
	nom													0.02
	min	0.148	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.745	0.057	0.38	0.38	

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1135b_po

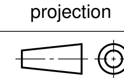
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1135B						~~09-10-12~~ 09-12-14

Fig 15. Package outline SOT1135B

10. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 11. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
S-band	Short wave Band
VSWR	Voltage Standing-Wave Ratio

12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS6G2735L-30_6G2735LS-30#4	20150901	Product data sheet		BLS6G2735L-30_6G2735LS-30 v.3
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLS6G2735L-30_6G2735LS-30 v.3	20120924	Product data sheet	-	BLS6G2735L-30_ 6G2735LS-30 v.2
BLS6G2735L-30_6G2735LS-30 v.2	20120904	Preliminary data sheet	-	BLS6G2735L-30_ 6G2735LS-30 v.1
BLS6G2735L-30_6G2735LS-30 v.1	20111011	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contact information

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